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FM482

User Manual

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 4DSP Inc. 2007

Revision History

Date	Revision	Version
02-01-07	First release	1.0
02-23-07	Updated Pn4 pin allocation table	1.1
03-14-07	Updated clock tree diagram	1.2
04-26-07	Corrected typos	1.3
05-15-09	- Added the technical support chapter and the external power warning. - Added external power warning paragraph	1.4

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1 Acronyms and related documents

1.1 Acronyms

ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
DCI	Digitally Controlled Impedance
DDR	Double Data Rate
DSP	Digital Signal Processing
EPROM	Erasable Programmable Read-Only Memory
FBGA	Fineline Ball Grid Array
FPDP	Front Panel Data Port
FPGA	Field Programmable Gate Array
JTAG	Join Test Action Group
LED	Light Emitting Diode
LVTTL	Low Voltage Transistor Logic level
LVDS	Low Differential Data Signaling
LSB	Least Significant Bit(s)
LVDS	Low Voltage Differential Signaling
MGT	Multi-Gigabit Transceiver
MSB	Most Significant Bit(s)
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCI-e	PCI Express
PLL	Phase Locked Loop
PMC	PCI Mezzanine Card
QDR	Quadruple Data rate
SDRAM	Synchronous Dynamic Random Access memory
SRAM	Synchronous Random Access memory

Table 1: Glossary

1.2 Related Documents

- IEEE Std 1386.1-2001 : IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC).
- ANSI/VITA 39-2003 : PCI-X for PMC and Processor PMC.
- ANSI/VITA 20-2001 : Conduction Cooled PMC.
- ANSI/VITA 42.0-2005 : XMC Switched Mezzanine Card Auxiliary Standard.
- IEEE Std 1386-2001 : IEEE Standard for a Common Mezzanine Card (CMC) Family.
- Xilinx Virtex-4 user guide
- Xilinx PCI-X core datasheet
- Xilinx Virtex-4 Rocket I/O guide

1.3 General description

The FM482 is a high performance PMC/XMC dedicated to digital signal processing applications with high bandwidth and complex algorithms requirements. The FM482 can interface to a PCI-e, PCI-X and/or PCI bus. It offers various interfaces, fast on-board memory resources and two Virtex-4 FPGA devices. It can be utilized, for example, to accelerate frequency-domain algorithms with off-the-shelf Intellectual Property cores for applications that require the highest level of performances. The FM482 is mechanically and electrically compliant to the standard and specifications listed in section 1.2 of this document.

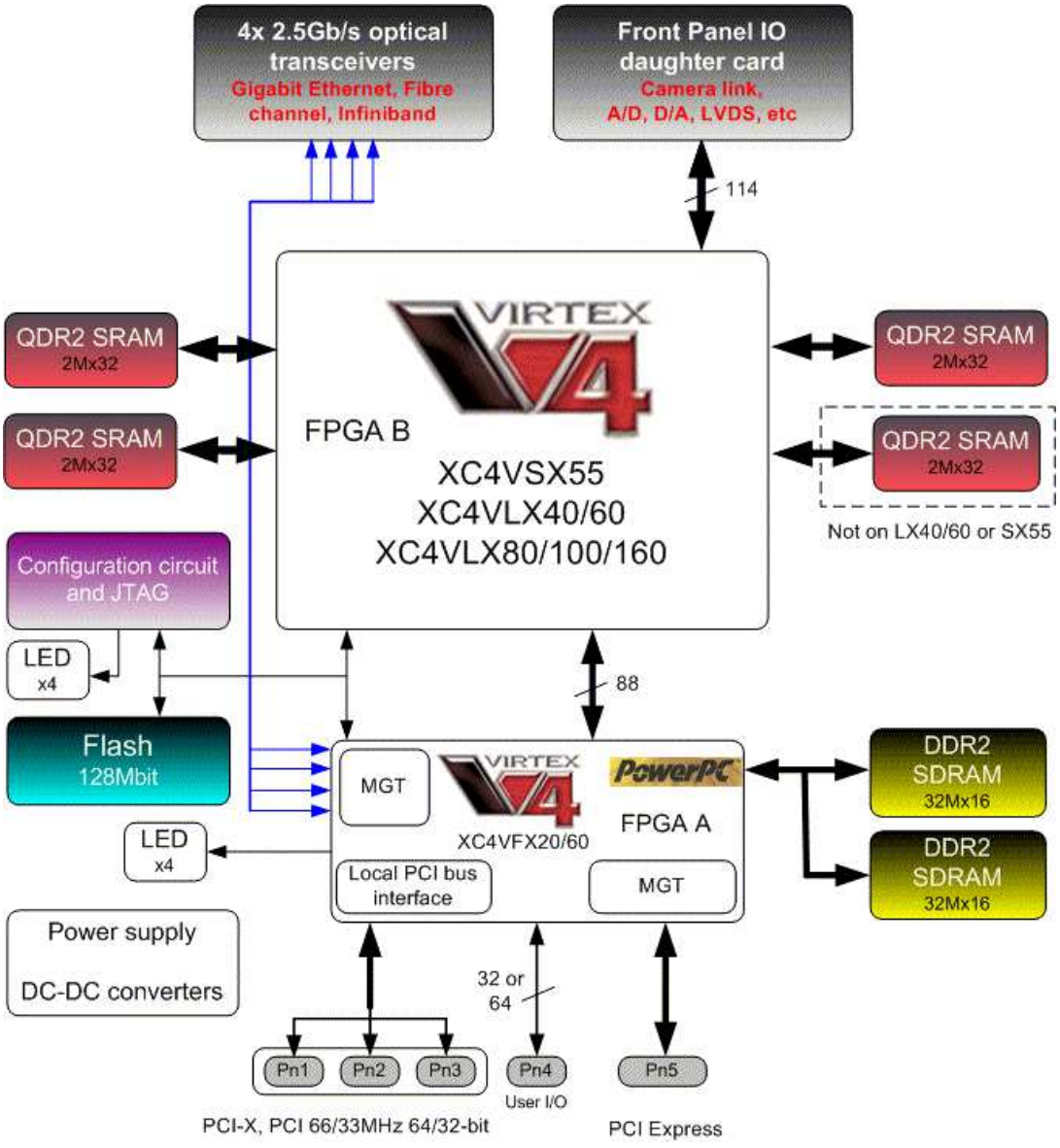


Figure 1: FM482 block diagram

2 Installation

2.1 Requirements and handling instructions

- The FM482 must be installed on a motherboard compliant to the IEEE Std 1386-2001 standard for 3.3V PMC or on a motherboard compliant to the XMC Switched Mezzanine Card Auxiliary Standard
- Do not flex the board
- Observe SSD precautions when handling the board to prevent electrostatic discharges.
- Do not install the FM482 while the motherboard is powered up.

2.2 Firmware and software

Drivers, API libraries and a program example working in combination with a pre-programmed firmware for both FPGAs are provided. The FM482 is delivered with an interface to the Xilinx PCI core in the Virtex-4 device A and an example VHDL design in the Virtex-4 device B so users can start performing high bandwidth data transfers over the PCI bus right out of the box. For more information about software installation and FPGA firmware, please refer the FM482 Get Started Guide.

3 Design

3.1 FPGA devices

The Virtex-4 FPGA devices interface to the various resources on the FM482 as shown on Figure 1. They also interconnect to each other via 86 general purpose pins and 2 clock pins.

3.1.1 Virtex-4 device A

3.1.1.1 Virtex-4 device A family and package

The Virtex-4 device A is from the Virtex-4 FX family. It can be either an XC4VFX20 or XC4VFX60 in a Fineline Ball Grid array with 672 balls (FF672).

3.1.1.2 Power PC embedded processor

Up to two IBM PowerPC RISC processor cores are available in the Virtex-4 device A. This core can be used to execute C based algorithms and control the logic resources implemented in the FPGA.

3.1.1.3 Virtex-4 device A external memory interfaces

The Virtex-4 device A is connected to a 128Mbytes SDRAM bank with a 32-bit data bus width. This memory resource can be used by the PowerPC core or can serve as data buffer.

3.1.1.4 PCI interface

The Virtex-4 device A interfaces directly to the PCI bus via the PMC Pn1, Pn2 and Pn3 connectors or to the PCI-e bus via the Pn5. An embedded PCI core from Xilinx is used to communicate over the PCI bus with the host system on the motherboard. PCI-e 4 lanes, PCI-X 64-bit 66MHz/133MHz, PCI 64-bit 66MHz and PCI 32-bit 33MHz are supported on the FM482. The bus type must be communicated at the time of the order so the right Virtex-4 device A firmware can be loaded into the flash prior to delivery.

The following performances have been recorded with the FM482 transferring data on the bus:

- PCI-X 64-bit 133MHz: 750Mbytes/s sustained
- PCI-X 64-bit 66MHz: 450Mbytes/s sustained
- PCI 32-bit 33MHz: 120Mbytes/s sustained

The PCI-express is using the MGT I/Os on the Virtex-4 device A. Power filtering, low jitter clock and special routing are used to achieve the performances required by this standard. Please refer to the Front Panel Optical transceivers section of this document for more details (3.6).

3.1.1.5 LED

Four LEDs are connected to the Virtex-4 device A. In the default FPGA firmware, the LEDs are driven by the Virtex-4 device B via the Virtex-4 device A/ Virtex-4 device B interface.

The LEDs are located on side 2 of the PCB in the front panel area.

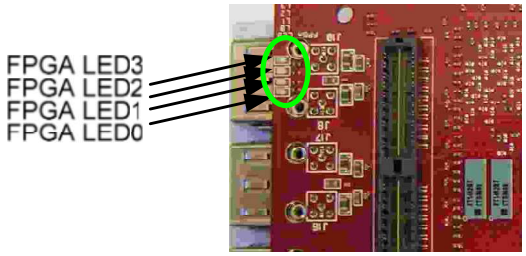


Figure 2: FPGA LED locations

3.1.1.6 Pn4 user I/O connector

The Pn4 connector is wired to the Virtex-4 device A. The 32 lower bits are available only if an XC4VFX60 device is mounted on board. The 32 higher bits are available only if PCI 32-bit is used and only if specified at the time of order.

All signals are user-defined 3.3V LVTLL./LVCMOS.

Connector pin	Signal name	FPGA pin		FPGA pin	Signal name	Connector pin
1	Pn4_IO0	M9		M10	Pn4_IO1	2
3	Pn4_IO2	N11		M11	Pn4_IO3	4
5	Pn4_IO4	N7		N8	Pn4_IO5	6
7	Pn4_IO6	N6		P6	Pn4_IO7	8
9	Pn4_IO8	P10		P11	Pn4_IO9	10
11	Pn4_IO10	P9		N9	Pn4_IO11	12
13	Pn4_IO12	R8		P8	Pn4_IO13	14
15	Pn4_IO14	R6		R7	Pn4_IO15	16
17	Pn4_IO16	N21		M21	Pn4_IO17	18
19	Pn4_IO18	M20		M19	Pn4_IO19	20
21	Pn4_IO20	P19		N19	Pn4_IO21	22
23	Pn4_IO22	N18		N17	Pn4_IO23	24
25	Pn4_IO24	P16		N16	Pn4_IO25	26
27	Pn4_IO26	R18		P18	Pn4_IO27	28
29	Pn4_IO28	P21		P20	Pn4_IO29	30
31	Pn4_IO30	R17		R16	Pn4_IO31	32
33	Pn4_IO32	L9		M5	Pn4_IO33	34
35	Pn4_IO34	L5		AD11	Pn4_IO35	36
37	Pn4_IO36	AD10		L4	Pn4_IO37	38
39	Pn4_IO38	L3		AB11	Pn4_IO39	40
41	Pn4_IO40	AC11		M4	Pn4_IO41	42
43	Pn4_IO42	N4		T9	Pn4_IO43	44
45	Pn4_IO44	T8		P5	Pn4_IO45	46
47	Pn4_IO46	R5		AA10	Pn4_IO47	48
49	Pn4_IO48	AB10		P4	Pn4_IO49	50
51	Pn4_IO50	R3		W10	Pn4_IO51	52
53	Pn4_IO52	Y10		N3	Pn4_IO53	54
55	Pn4_IO54	P3		U6	Pn4_IO55	56
57	Pn4_IO56	U5		T4	Pn4_IO57	58
59	Pn4_IO58	T3		U7	Pn4_IO59	60
61	Pn4_IO60	V6		U4	Pn4_IO61	62
63	Pn4_IO62	V4		U9	Pn4_IO63	64

Table 2 : Pn4 pin assignment

3.1.2 Virtex-4 device B

3.1.2.1 Virtex-4 device B family and package

The Virtex-4 device B is dedicated to Digital Signal Processing applications and can be chosen from the SX or LX family devices. Its package is based on Fineline Ball Grid array with 1148 balls. In terms of logic and dedicated DSP resources, the FPGA B can be chosen from the following types: SX55, LX40, LX60, LX80, LX100 and LX160.

3.1.2.2 Virtex-4 device B external memory interfaces

The Virtex-4 device B interfaces to four 8Mbytes QDR2 SRAM devices with 32-bit data bus, Please note that the four QDR2 SRAM devices are only available with the LX80, LX100 and LX160 devices. For smaller Virtex-4 FPGAs (LX40, LX60 and SX55) only three QDR2 SRAM devices are connected to the FPGA.

3.1.2.3 Virtex-4 device B interface to Front Panel daughter card

The Virtex-4 device B interfaces to the front panel daughter card on the FM482 via a high speed connector. 114 I/Os are available from the FPGA to/from the daughter card.

Refer to the Front Panel I/O section of this document for more details about the daughter card connector electrical characteristics.

3.2 FPGA devices configuration

3.2.1 Flash storage

The FPGA firmware is stored on board in a flash device. The 128Mbit device is partly used to store the configuration for both FPGAs. In the default CPLD firmware configuration, the Virtex-4 devices A and B are directly configured from flash if a valid bitstream is stored in the flash for each FPGA. The flash is pre-programmed in factory with the default firmware example for both FPGAs.

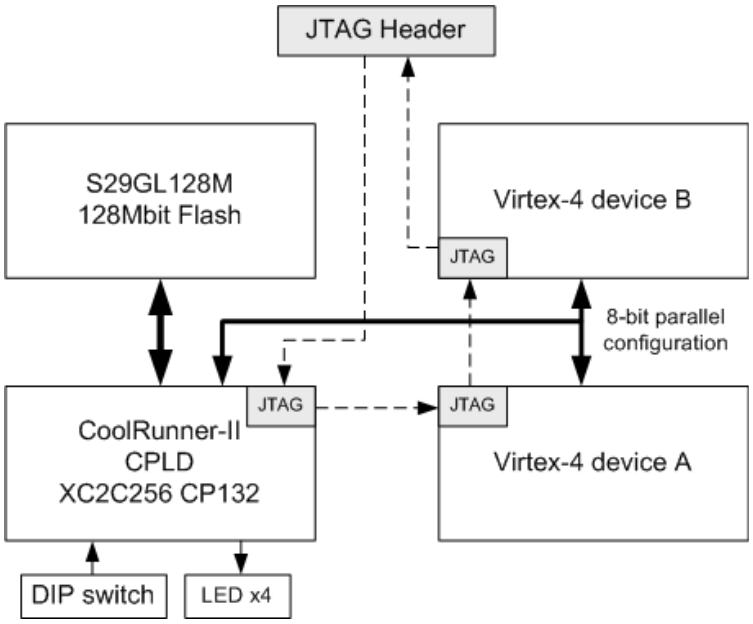


Figure 3 : Configuration circuit

3.2.2 CPLD device

As shown on Figure 2, a CPLD is present on board to interface between the flash device and the FPGA devices. It is of type CoolRunner-II. The CPLD is used to program and read the flash. The data stored in the flash are transferred from the host motherboard via the PCI bus to the Virtex-4 device A and then to the CPLD that writes the required bit stream to the storage device. A 31.25 MHz clock connects to the CPLD and is used to generate the configuration clock sent to the FPGA devices. At power up, if the CPLD detects that an FPGA configuration bitstream is stored in the flash for both FPGA devices, it will start reading programming the devices in SelecMap mode.

Do NOT reprogram the CPLD without 4DSP approval

The CPLD configuration is achieved by loading with a Xilinx download cable a bitstream from a host computer via the JTAG connector. The FPGA devices configuration can also be performed using the JTAG.

3.2.2.1 DIP Switch

A switch (J1) is located next to the JTAG programming connector (J6) see Figure 4. The switch positions are defined as follows:

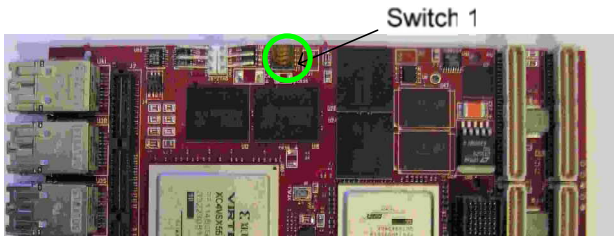


Figure 4: switch (J1) location

Sw1	OFF	Default setting. The Virtex-4 device A configuration is loaded from the flash at power up.
	ON	Virtex-4 device A safety configuration loaded from the flash at power up. To be used only if the Virtex-4 device A cannot be configured or does not perform properly with the switch in the OFF position.
Sw2		Reserved
Sw3		Reserved
Sw4		Reserved

Table 3: Switch description

3.2.2.2 LED and board status

Four LEDs connect to the CPLD and give information about the board status.

LED 0	Flashing	FPGA A or B bitstream or user_ROM_register is currently being written to the flash
	ON	FPGA A not configured
	OFF	FPGA A configured
LED 1	Flashing	FPGA A or B bitstream or user_ROM_register is currently being written to the flash
	ON	FPGA B not configured
	OFF	FPGA B configured
LED 2	Flashing	The Virtex-4 device A has been configured with the safety configuration bitstream programmed in the flash at factory. Please write a valid Virtex-4 device A bitstream to the flash.
	ON	Flash is busy writing or erasing
	OFF	Flash device is not busy
LED 3 LED 3	ON	CRC error. Presumably a wrong or corrupted FPGA bitstream has been written to the flash. Once on this LED remains on
	OFF	No CRC error detected

Table 4: LED board status

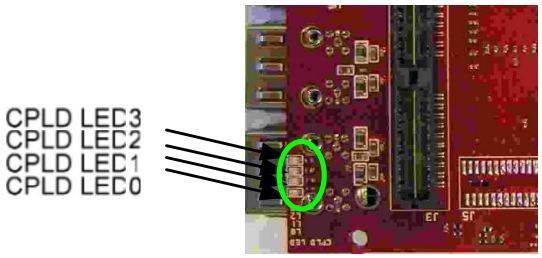


Figure 5: CPLD LED locations

3.2.3 JTAG

A JTAG connector is available on the FM482 for configuration purposes. The JTAG can also be used to debug the FPGA design with the Xilinx Chipscope.

The JTAG connector is located on side 1 of the PCB (see Figure 6).

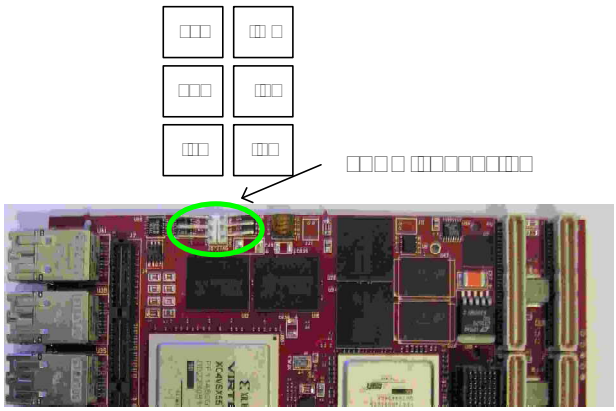


Figure 6: JTAG connector (J6) location

The JTAG connector pinout is as follows:

Pin #	Signal	Signal	Pin #
1	1.8V	TMS	4
2	GND	TDI	5
3	TCK	TDO	6

Table 5 : JTAG pin assignment

3.3 Clock tree

The FM482 clock architecture offers an efficient distribution of low jitter clocks. In addition to the PCI Express bus, the MGT reference clocks of 106.25MHz and 125MHz (Epson EG2121CA) make it possible to implement several standards over the MGT I/Os connected to the optical transceivers.

Both FPGAs receive a low jitter 125MHz clock. A low jitter programmable clock able to generate frequencies from 62.5MHz to 255.5MHz in steps of 0.5MHz is also available. This clock management approach ensures maximum flexibility to efficiently implement multi-clock

domains algorithms and use the memory devices at different frequencies. Both clock buffer devices (CDM1804) and the frequency synthesizer (ICS8430-61) are controlled by the Virtex-4 device A.

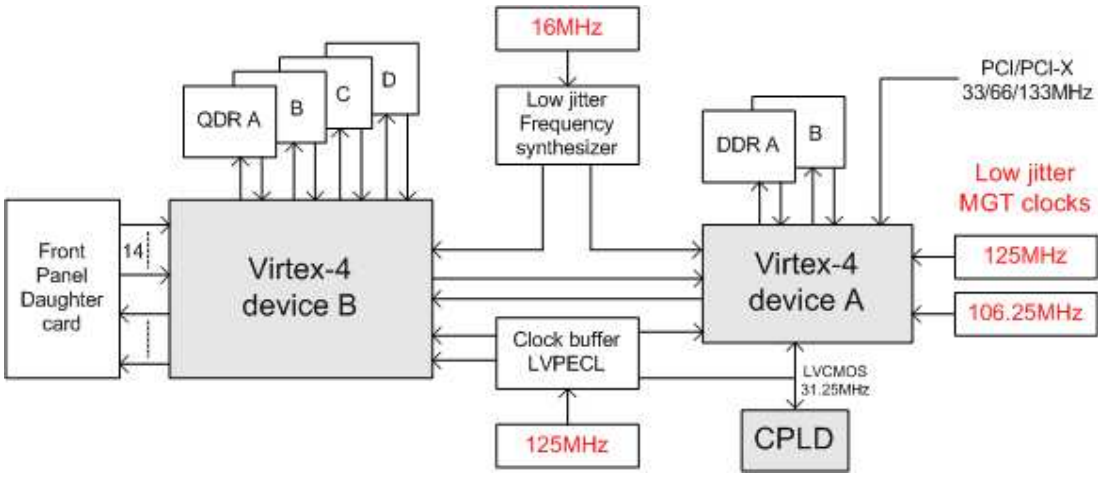


Figure 7 : Clock tree

3.4 Memory resources

3.4.1 QDR2 SRAM

Four independent QDR2 SRAM devices are connected to the Virtex-4 device B. The QDR2 SRAM devices available on the FM482 are 2M words deep (8Mbytes per memory device).

Please note that only three QDR SRAM devices are available to the user if the XC4VLX40, XC4VLX60 or XC4VSX55 FPGA device is mounted on board.

3.4.2 DDR2 SDRAM

Two 16-bit DDR2 SDRAM devices of 128MBytes each are connected to Virtex-4 device A. The two memories share the same address and control bus and have their own data bus. This memory resource can be accessed by the PowerPC processor in the Virtex-4 device A or can be used as a data buffer for custom user logic.

3.5 Front Panel IO daughter card

3.5.1 Virtex-4 device B to I/O front Panel daughter card

(only available with daughter card purchase)

The Virtex-4 device B interfaces to a 120-pin connector placed in the Front panel I/O area (on both side 1 and side 2 of the PCB). It serves as a base for a daughter card and offers I/O diversity to the FM482 PMC. On side 2 of the PCB, the connectors and mounting holes placement complies with the SLB standard except for the 1.5V mounting hole that is not present on this module.

The FPGA I/O banks are powered either by 1.8V, 2.5V or 3.3V via a large 0 ohms resistor (3.3V is the default if not specified otherwise at the time of order). Using the Xilinx DCI termination options to match the signals impedance allows many electrical standards to be supported by this interface. All signals are routed as 100-ohm LVDS pairs. The VRP and VRN pins on the I/O banks connected to the daughter card connector are respectively pulled up and pulled down with 50-ohm resistors in order to ensure optimal performances when using the Xilinx DCI options. The VREF pins are connected to 0.9V for DDR2 DCI terminations. Please, contact 4DSP Inc. for more information about the daughter card types available.

The 120-pin Samtec connector pin assignment is as follows. All signals are shown as LVDS pairs in the table but they can be used for any standard that does not breach the electrical rules of the Xilinx I/O pad.

Connector pin	Signal Name	FPGA pin		FPGA pin	Signal name	Connector pin
1	FP_P0	W24		AA23	FP_P1	2
3	FP_N0	Y24		AA24	FP_N1	4
5	FP_P2[2]	AA25		AA28	FP_P3	6
7	FP_N2[2]	AA26		AA29	FP_N3	8
9	FP_P4	AB30		AC28	FP_P5	10
11	FP_N4	AA30		AB28	FP_N5	12
13	FP_P6	AB22		AD27	FP_P7	14
15	FP_N6	AB23		AC27	FP_N7	16
17	FP_P8	AC29		AC32	FP_P9	18
19	FP_N8	AC30		AC33	FP_N9	20
21	FP_P10[2]	AD34		AE32	FP_P11	22
23	FP_N10[2]	AC34		AD32	FP_N11	24
25	FP_P12	AE29		AF31	FP_P13	26
27	FP_N12	AD29		AE31	FP_N13	28
29	FP_P14	AE33		AF33	FP_P15	30
31	FP_N14	AE34		AF34	FP_N15	32
33	FP_P16[2]	AF29		AH19	FP_P17[1]	34
35	FP_N16[2]	AF30		AH18	FP_N17[1]	36
37	FP_P18[1]	AG18		AG30	FP_P19	38
39	FP_N18[1]	AG17		AG31	FP_N19	40

Table 6 : Front Panel IO daughter card pin assignment Bank A

[1] Connected to a global clock pin on the FPGA. LVDS output not supported.

[2] Connected to a regional clock pin on the FPGA. LVDS output not supported.

Connector pin	Differential	FPGA pin		FPGA pin	Differential	Connector pin
41	FP_P20	AG32		AJ34	FP_P21	42
43	FP_N20	AG33		AH34	FP_N21	44
45	FP_P22	AH32		AJ30	FP_P23	46
47	FP_N22	AH33		AH30	FP_N23	48
49	FP_P24(2)	AK31		AK33	FP_P25	50
51	FP_N24(2)	AK32		AK34	FP_N25	52
53	FP_P26	AL33		AM31	FP_P27	54
55	FP_N26	AL34		AL31	FP_N27	56
57	FP_P28	AM32		AP30	FP_P29	58
59	FP_N28	AM33		AN30	FP_N29	60
61	FP_P30	AM30		AH28	FP_P31	62
63	FP_N30	AL30		AH29	FP_N31	64
65	FP_P32	AK29		AL28	FP_P33	66
67	FP_N32	AJ29		AL29	FP_N33	68
69	FP_P34	AP29		AN28	FP_P35(2)	70
71	FP_N34	AN29		AM28	FP_N35(2)	72
73	FP_P36(2)	AG27		AG28	FP_N36(2)	74
75	3.3V/2.5V/1.8V				Vbatt (3)	76
77	3.3V/2.5V/1.8V				0.9V	78
79	3.3V/2.5V/1.8V				3.3V/2.5V/1.8V	80
81	FP_P37	AF28		AJ27	FP_P38	82
83	FP_N37	AE27		AH27	FP_N38	84
85	FP_P39	AM26		AP27	FP_P40	86
87	FP_N39	AM27		AN27	FP_N40	88
89	FP_P41	AP25		AL26	FP_P42	90
91	FP_N41	AP26		AK26	FP_N42	92
93	FP_P43	AG25		AF26	FP_P44	94
95	FP_N43	AG26		AE26	FP_N44	96
97	FP_P45(1)	AJ17		AN25	FP_P46	98
99	FP_N45(1)	AH17		AM25	FP_N46	100
101	FP_P47	AP24		AK24	FP_P48	102
103	FP_N47	AN24		AJ24	FP_N48	104
105	FP_P49	AG23		AK22	FP_P50	106
107	FP_N49	AF24		AK23	FP_N50	108
109	FP_P51	AL23		AN22	FP_P52	110
111	FP_N51	AM23		AN23	FP_N52	112
113	FP_P53(2)	AL24		AP21	FP_P54	114
115	FP_N53(2)	AL25		AP22	FP_N54	116
117	FP_P55(1)	AE17		AK21	FP_P56	118
119	FP_N55(1)	AE16		AL21	FP_N56	120

Table 7 : Front Panel IO daughter card pin assignment Bank B and C

(1) Connected to a global clock pin on the FPGA. LVDS output not supported.

(2) Connected to a regional clock pin on the FPGA. LVDS output not supported.

(3) Vbatt is connected to both Virtex-4 devices Vbatt pin.

3.5.2 Power connection to the front panel I/O daughter card

The Front Panel I/O daughter card on side 1 of the PCB is powered via a 7-pin connector of type BKS (Samtec). Each pin can carry up to 1.5A. The power connector's pin assignment is as follows.

Pin #	Signal	Signal	Pin #
1	+3.3V	+3.3V	2
3	+5V	GND	4
5	+12V	GND	6
7	-12V		

Table 8: Daughter card power connector pin assignment on PMC side 1

On side 2 of the PCB, the daughter card is powered via a 33-pin connector of type BKS (Samtec). Each pin can carry up to 1.5A. The power connector's pin assignment is as follows.

Pin #	Signal	Signal	Pin #
1	+3.3V	GND	2
3	+3.3V	GND	4
5	+3.3V	GND	6
7	+3.3V	GND	8
9	+5V	GND	10
11	+5V	GND	12
13	+5V	GND	14
15	+5V	GND	16
17	+12V	GND	18
19	+12V	GND	20
21	-12V	GND	22
23	-12V	GND	24
25	GND	reserved	26
27	reserved	reserved	28
29	reserved	reserved	30
31	reserved	reserved	32
33	GND		

Table 9: Daughter card power connector pin assignment on PMC side 2

3.6 Front Panel optical transceivers

Four 2.5Gb/s optical transceivers (LTP-ST11M) are available on the FM482 in the front panel area. They are connected to the MGT I/Os of the Virtex-4 device A. Infiniband protocols as well as Gigabit Ethernet and Fibre channel (sFPDP) can be implemented over the transceivers. Lower rate optical transceivers (2.125Gb/s and 1.0625Gb/s) are available in the same form factor.

Two low jitter clocks (106.25MHz and 125MHz) are directly connected to the MGT clock inputs so multi-rate applications can be implemented on the FM482.

The MGT banks have power supplies independent from the digital supply provided to the FPGAs in order to insure low noise and data integrity. The LT1963 device will be used to generate the 1.2V, 1.5V and 2.5V necessary for the MGT to operate. The power filtering network includes a 220nF decoupling capacitor and ferrite bead (MP21608S221A) per power pin.

The signal differential pairs are routed on a specific inner layer with one reference GND plane on each side of the layer stack up.

Please note that the optical transceivers are not available if the FM482 is Conduction Cooled.

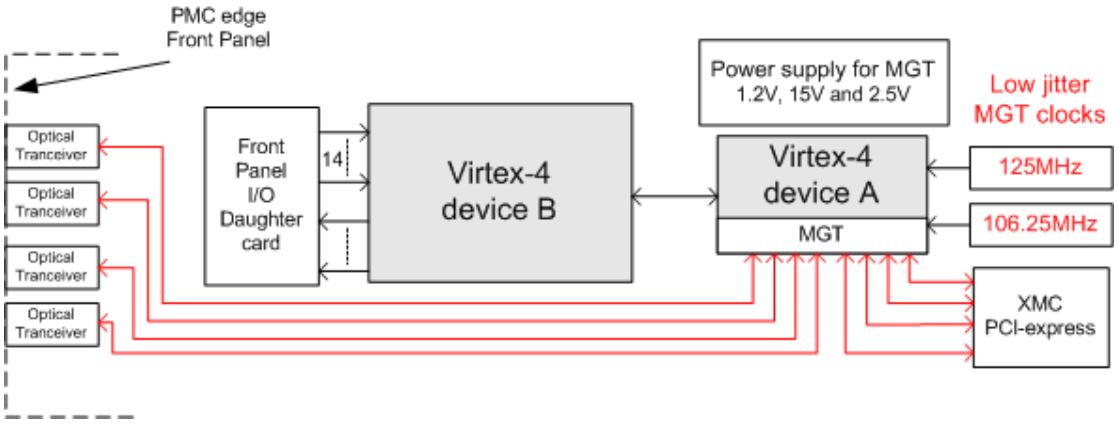


Figure 8: Optical transceivers

4 Power requirements

The Power is supplied to the FM482 via the PMC and/or XMC connectors. Several DC-DC converters generate the appropriate voltage rails for the different devices and interfaces present on board.

The FM482 power consumption depends mainly on the FPGA devices work load. By using high efficiency power converters, all care has been taken to ensure that power consumption will remain as low as possible for any given algorithm.

After power up the FM482 typically consumes 2W of power. For precise power measurements it is recommended to use the Xilinx power estimation tools for both FPGA A and B. The maximum current rating given in the table below is the maximum current that can be drawn from each voltage rail in the case resources are used to their maximum level.

Device/Interface	Voltage	Maximum current rating
DCI and memory reference voltage	0.9V	5 A
Virtex-4 device A & B core	1.2V	12A
QDR2, DDR2 SDRAM core and I/O banks, Virtex-4 devices I/O banks	1.8V	10A
Virtex-4 device B I/O bank connected to the front panel daughter card	1.8V/2.5/3.3V	1.5A
Virtex-4 device A I/O bank connected to the PCI bus, Flash, CPLD, front Panel I/O daughter card	3.3V	2A
Front Panel IO daughter card	5V	1A
Front Panel IO daughter card	12V	0.5A
Front Panel IO daughter card	-12V	0.5A
MGT power supply	1.2V, 1.5V, 2.5V	1.7A, 0.5A, 0.01A respectively

Table 10 : Power supply

Optionally, the FM482 can be used as a stand alone module and is powered via the external power connector.

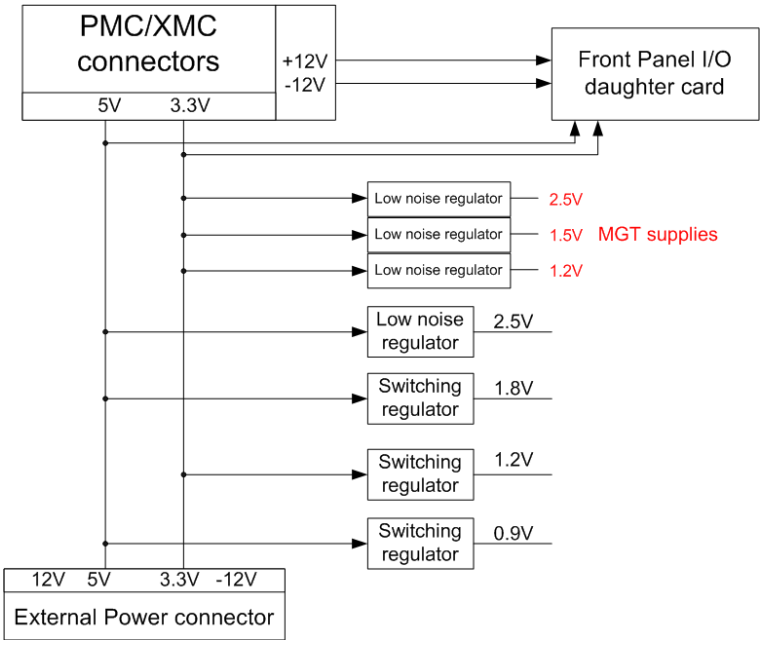


Figure 9 : Power supply

An ADT7411 device is used to monitor the power on the different voltage rails as well as the temperature. The ADT7411 data are constantly passed to the Virtex-4 device A. Measurements can be accessed from the host computer via the PCI bus. A software utility delivered with the board allows the monitoring of the voltage on the 2.5V, 1.8V, 1.2V and 0.9V rails. It also displays the Virtex-4 device B junction temperature.

4.1 External power connector for stand alone mode

An external power connector (J2) is available on side 2 of the PMC, next to the PMC connectors. It is used to power the board when it is in stand alone mode. This is a right angled connector and it will be mounted on board only if the card is ordered in its stand alone version (FM482-SA). The height and placement of this connector on the PCB breaches the PMC specifications and the module should not be used in an enclosed chassis compliant to PMC specifications if the external power connector is present on board.

Do not connect an external power source to J2 if the board is powered via the PMC connectors. Doing so will result in damaging the board.

The external power connector is of type Molex 43045-1021. Each circuit can carry a maximum current of 5A. The connector pin assignment is as follows:

Pin #	Signal	Signal	Pin #
1	3.3V	3.3V	2
3	5V	5V	4
5	GND	GND	6
7	GND	GND	8
9	-12V	12V	10

Table 11 : External power connector pin assignment

WARNING

UNREGULATED UNPROTECTED EXTERNAL POWER SUPPLY CONNECTION

This board is designed with an UNSUPPORTED feature for an external power connector labeled as J2. Mounting a connector on the PCB breaches the PMC electrical and mechanical specifications of the PMC standard. This is a FACTORY ONLY feature that is used in the manufacturing process when powering the board is required in an UN-MOUNTED PCI bus mode, thus in stand alone mode. DO NOT connect an external power source to J2, doing so may result in damaging the board and will automatically VOID WARRANTY. Consult factory for further information.

5 Environment

5.1 Temperature

Operating temperature

- 0°C to +60°C (Commercial)
- -40°C to +85°C (Industrial)

Storage temperature:

- -40°C to +120°C

5.2 Convection cooling

600LFM minimum

5.3 Conduction cooling

The FM482 can optionally be delivered as conduction cooled PMC. The FM482 is compliant to ANSI/VITA 20-2001 standard for conduction cooled PMC.

6 Safety

This module presents no hazard to the user.

7 EMC

This module is designed to operate from within an enclosed host system, which is build to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system. This module is protected from damage by fast voltage transients originating from outside the host system which may be introduced through the system.

8 Warranty

	Hardware	Software/Firmware
[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]

9 FM482 picture

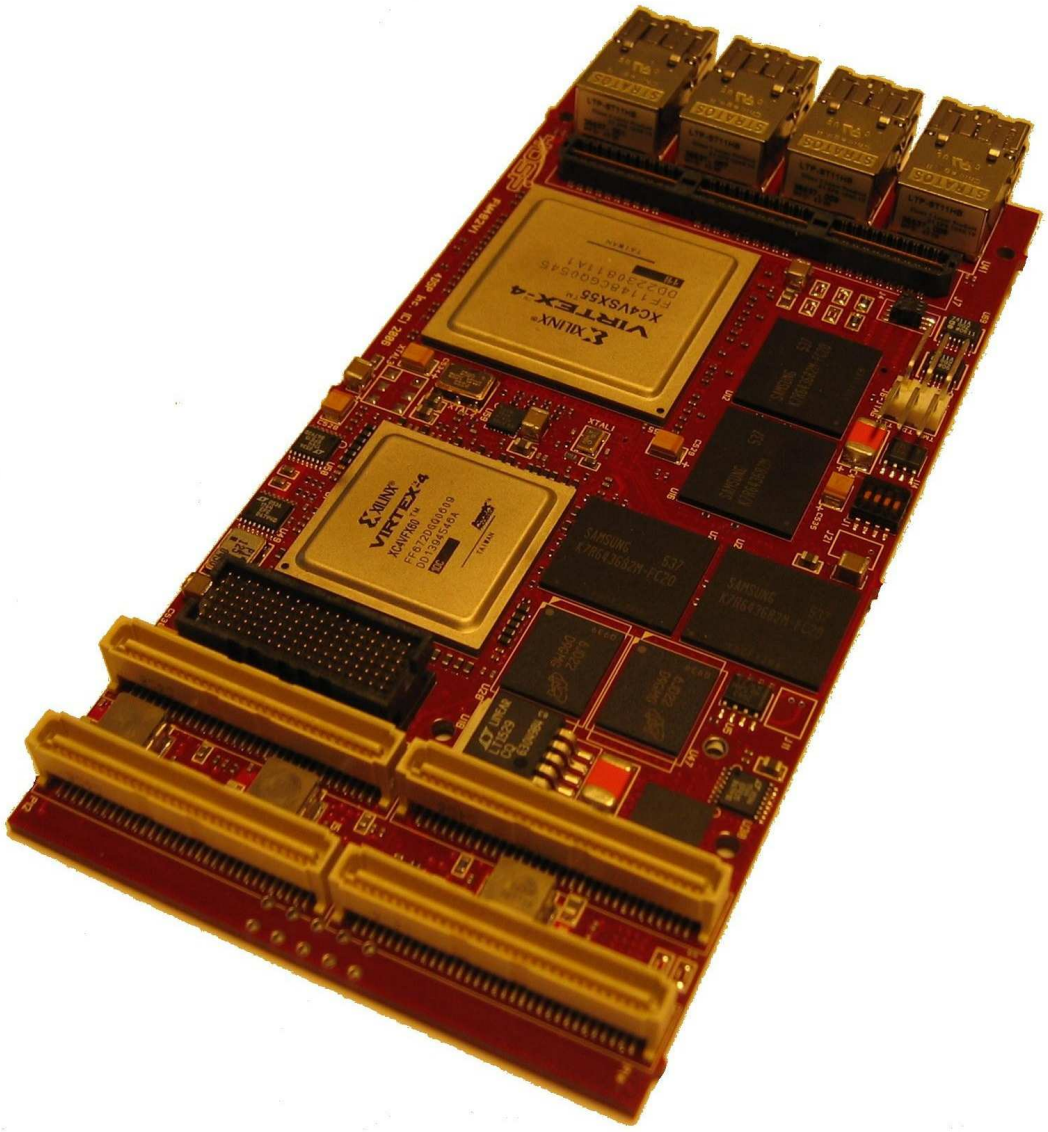


Figure 10: FM482

10 Technical support

Technical support for all 4DSP Product, hardware, software and firmware is available under 4DSP Terms and Conditions of Sales ONLY in its original condition AS-SHIPPED unless agreed to by 4DSP and documented in writing, prior to any modifications.

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Technical support requests should be sent to support@4dsp.com

Any electrical connections made to the board or other components shall be made only with approved connectors as specifically identified in the products official documentation.

Any modification to hardware including but not limited to removing of components, soldering or other material changes to in part or in whole to the PCM and/or its components will immediately invalidate and make void any warranty or extended support if any.

Further, and changes or modifications to software and/or firmware supplied with the Product, unless provided for in the Products official documentation, shall immediately invalidate and make void any warranty or extended support if any.

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