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SYS68K/CPU-30 R4
Installation Guide

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1 Safety Notes

This section provides safety precautions to follow when installing, operating, and maintaining the SYS68K/CPU-30 R4. For your protection, follow all warnings and instructions found in the following text.

General

This *Installation Guide* provides the necessary information to install and handle the SYS68K/CPU-30 R4. As the product is complex and its usage manifold, we do not guarantee that the given information is complete. In case you need additional information, ask your Force Computers representative.

The SYS68K/CPU-30 R4 has been designed to meet the standard industrial safety requirements. It must not be used except in its specific area of office telecommunication industry and industrial control.

Only personnel trained by Force Computers or qualified persons in electronics or electrical engineering are authorized to install, uninstall or maintain the SYS68K/CPU-30 R4. The information given in this manual is meant to complete the knowledge of a specialist and must not be taken as replacement for qualified personnel.

Make sure that contacts and cables of the board cannot be touched while the board is operating.

Installation

Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their life. Therefore:

- **Before touching integrated circuits, ensure that you are working in an electrostatic-free environment.**
- **When plugging the board in or removing it, do not press on the front panel but use the handles.**
- **Before installing or uninstalling the board, read section 2 “Installation” on page 3.**
- **Before installing or uninstalling an additional device or module, read the respective documentation.**
- **Ensure that the board is connected to the VMEbus via both connectors, the P1 and the P2 and that power is available on both..**

Power up

Before powering up check that the default switch settings are correct as outlined in section 2.2 “Default Switch Settings” on page 6.

Operation

When operating the board in areas of strong electromagnetic radiation ensure that the board is bolted on the VME rack and shielded by closed housing.

EMC

If boards are integrated into open systems, always cover empty slots.

Expanding

- **Check the total power consumption of all components installed (see the technical specification of the respective components).**
- **Ensure that any individual output current of any source stays within its acceptable limits (see the technical specification of the respective source).**
- **Only replace components or system parts with those recommended by Force Computers. In case you use components other than those recommended by Force Computers, you are fully responsible for the impact on EMI and the eventually changed functionality of the product.**

Battery Change

If a Lithium battery on the board has to be exchanged, observe the following safety notes:

- **Incorrect exchange of Lithium batteries can result in a hazardous explosion.**
- **Always use the same type of Lithium battery as is already installed.**

Protect your Environment

Always dispose used batteries and/or old boards according to your country's legislation.

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2 Installation

The installation of the board is easy, requiring only a power supply and a VMEbus backplane. The power supply must meet the specifications described in Table 1, “Specifications for the CPU-30 R4 Board,” on page 7. The processor board requires +5 V supply voltage; ±12 V are needed for the RS-232 serial interface and the Ethernet Interface.

For the initial power up, a terminal can be connected to the 9-pin D-Sub microconnector of serial port 1, which is located on the front panel. The serial port provides RS-232 interface signal level.

Caution

Before powering up check that the default switch settings are correct as outlined in Section 2.2 ‘Default Switch Settings’**.**

2.1 Location Diagrams of the SYS68K/CPU-30 R4

The following two location diagrams show the important components on the top side and the bottom side of the CPU-30 R4. Both of these diagrams only show the components on the board which are of interest to the user.

Figure 1 **Diagram of the CPU-30 R4 (Top View)**

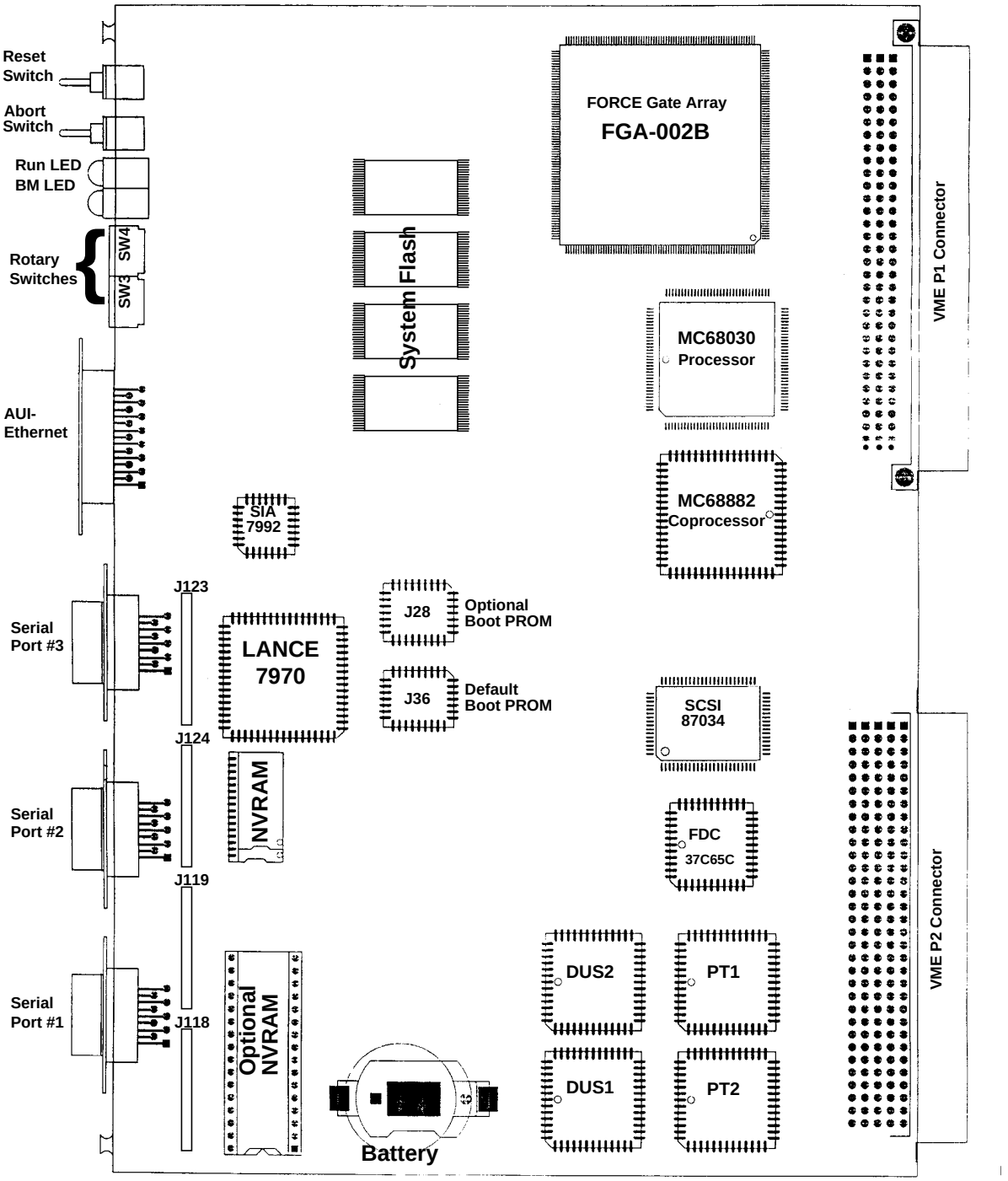

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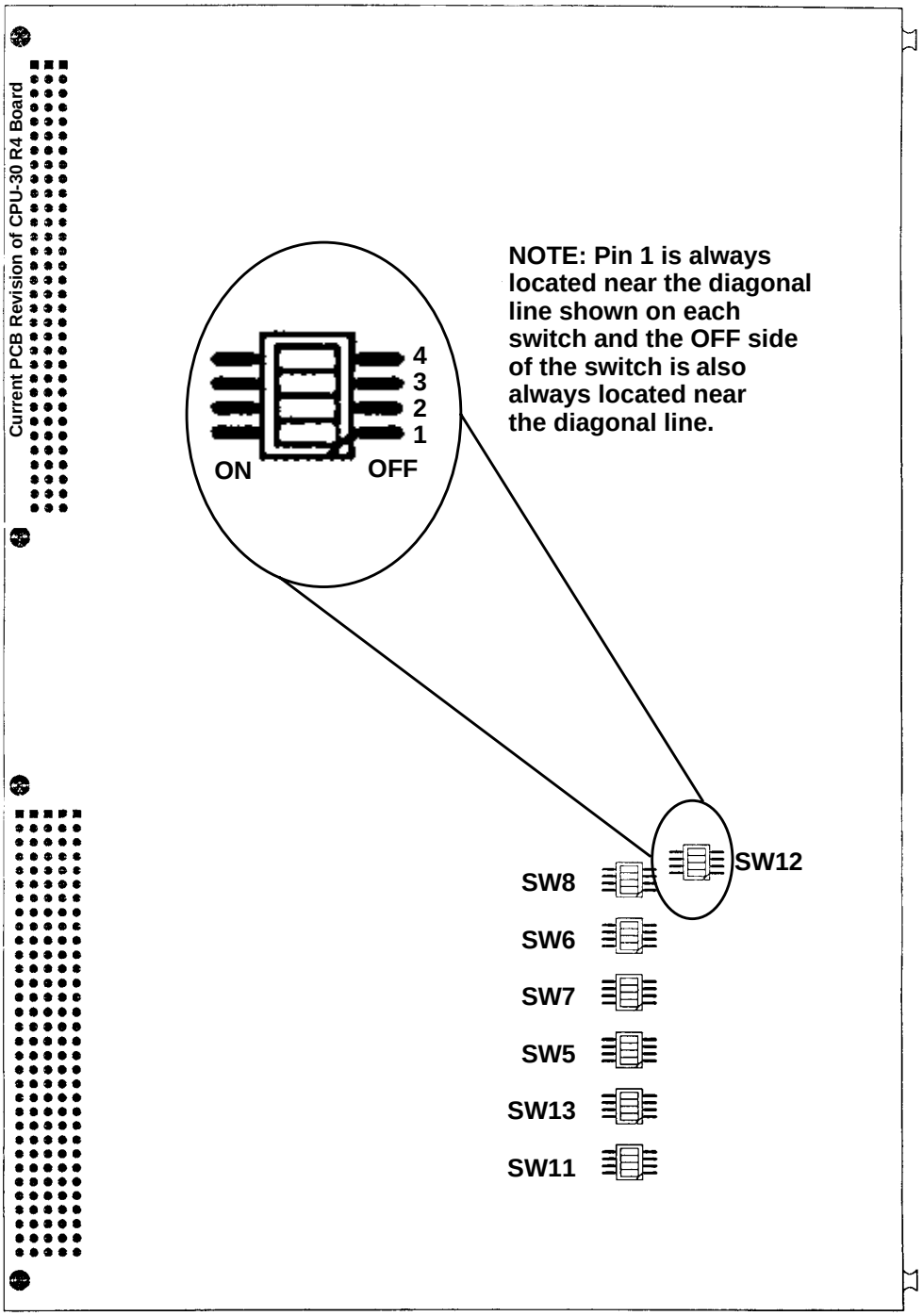
Figure 2 **Diagram of the CPU-30 R4 (Bottom View)**



2.2 Default Switch Settings

The following table shows the default settings for all the switches on the board.For the position of the switches on your CPU-30 R4 board see Figure 2, “Diagram of the CPU-30 R4 (Bottom View),” on page 5.

Note: **The battery backup for SRAM and RTC is disabled with the default switch setting. Stored data will be lost.**

Table 1 Default Switch Settings

Diagram of Switch with Default Setting	Switches	Default Setting	Function
SWITCH 5			
	SW5-1	OFF	OFF=Boot PROM access to default Boot PROM and optional Boot PROM ON=Boot PROM access to optional Boot PROM only (Access to default Boot PROM is disabled)
	SW5-2	OFF	OFF=Optional Boot PROM Pinout for Flash PROM ON=Optional Boot PROM Pinout for EPROM
	SW5-3	OFF	OFF=Write to Boot PROM enabled ON=Write to Boot PROM disabled
	SW5-4	OFF	OFF=Write to System Flash Memory enabled ON=Write to System Flash Memory disabled
SWITCH 6			

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Table 1 Default Switch Settings (Continued)

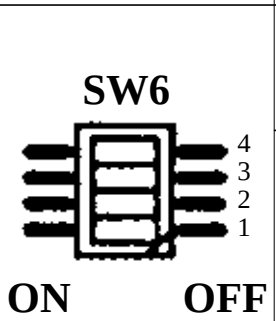
Diagram of Switch with Default Setting	Switches	Default Setting	Function
	SW6-1	OFF	**BUSTIMER (1:0)** **SW6-1 SW6-2 Time** SW6-1 OFF=VME Bustimer bit 1=1OFF OFF83.53ms SW6-1 ON=VME Bustimer bit 1=0OFF ON 1.30 ms ON OFF 81.6 µs ON ON 10.2 µs SW6-2 OFF=VME Bustimer bit 0=1 SW6-2 ON=VME Bustimer bit 0=0
	SW6-2	OFF	
	SW6-3	OFF	**SLOT, BRSEL (1:0) : VME BR** SLOT-x detected, 11 : 3 SW6-3 OFF=VME BRSEL bit 1=1 SLOT-x detected, 10 : 2 SW6-3 ON=VME BRSEL bit 1=0SLOT-x detected, 01 : 1 SLOT-x detected, 00 : 0 SW6-4 OFF=VME BRSEL bit 0=1SLOT-1 detected, -- : 3 SW6-4 ON=VME BRSEL bit 0=0
	SW6-4	OFF	

Table 1 Default Switch Settings (Continued)

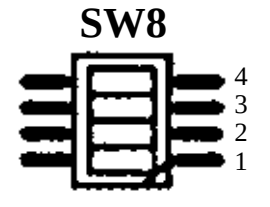
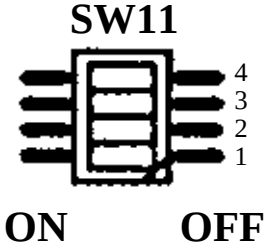
Diagram of Switch with Default Setting	Switches	Default Setting	Function
SWITCH 7			
	SW7-1	OFF	OFF=RESET Switch enabled ON=RESET Switch disabled
	SW7-2	OFF	OFF=ABORT Switch enabled ON=ABORT Switch disabled
	SW7-3	OFF	OFF=SCSI active termination enabled ON=SCSI active termination disabled
	SW7-4	OFF	OFF=additional VME Bustimer enabled if VME slot-1 function detected (otherwise disabled) ON=VME Bustimer disabled
SWITCH 8			
	SW8-1	OFF	OFF=VME slot-1 auto-detection enabled ON=VME slot-1 function disabled
	SW8-2	OFF	OFF=VME_SYSFAIL output enabled ON=VME_SYSFAIL output disabled
	SW8-3	OFF	OFF=VME_SYSRESET output enabled ON=VME_SYSRESET output disabled
	SW8-4	OFF	OFF=VME_SYSRESET input enabled ON=VME_SYSRESET input disabled
SWITCH 11			
	SW11-1	OFF	OFF=Power backup from battery disabled ON=Power backup from battery enabled
	SW11-2	OFF	OFF=Power Backup from VME STBY disabled ON=Power Backup from VME STBY enabled
	SW11-3	OFF	OFF=NVRAM supplied by Power Backup disabled ON=NVRAM supplied by Power Backup enabled
	SW11-4	OFF	OFF=Default NVRAM access only ON=Optional and default NVRAM access

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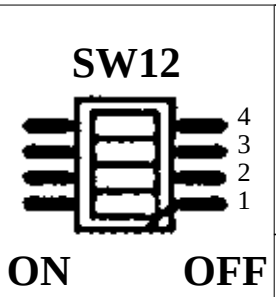
Table 1 Default Switch Settings (Continued)

Diagram of Switch with Default Setting	Switches	Default Setting	Function
SWITCH 12			
	SW12-1	OFF	OFF=Serial port 1 for RS-232, Hybrid FH-002 on J119 ON=Serial port 1 for RS-422, Hybrid FH-003 or FH-422T on J119 Serial port 1 for RS-485, Hybrid FH-007 on J119
	SW12-2	OFF	OFF=Serial port 2 for RS-232, Hybrid FH-002 on J124 ON=Serial port 2 for RS-422, Hybrid FH-003 or FH-422T on J124 Serial port 2 for RS-485, Hybrid FH-007 on J124
	SW12-3	OFF	OFF=Serial port 3 for RS-232, Hybrid FH-002 on J123 ON=Serial port 3 for RS-422, Hybrid FH-003 or FH-422T on J123 Serial port 3 for RS-485, Hybrid FH-007 on J123
	SW12-4	OFF	OFF=Serial port 4 for RS-232, Hybrid FH-002 on J118 ON=Serial port 4 for RS-422, Hybrid FH-003 or FH-422T on J118 Serial port 4 for RS-485, Hybrid FH-007 on J118
SWITCH 13			
	SW13-1	OFF	OFF=Timer IRQ enabled ON=Timer IRQ disabled
	SW13-2	OFF	OFF=Watchdog reset disabled ON=Watchdog reset enabled
	SW13-3	OFF	Reserved (must be OFF)
	SW13-4	OFF	Reserved (must be OFF)

2.3 Front Panel

The table below outlines the layout on the front panel. Additionally, there is a drawing of the front panel on page 11. The front panel devices are briefly described on the pages following the drawing.

Table 2 Front Panel Layout

Device	Function	Name
Switch	Reset	RESET
Switch	Abort	ABORT
LED	RUN/HALT	RUN
LED	VME BM	BM
Rotary Switch	4-bit Input	2
Rotary Switch	4-bit Input	1
15-pin D-Sub connector	AUI-Ethernet Interface	L
9-pin D-Sub connector	Serial Interface	3
9-pin D-Sub connector	Serial Interface	2
9-pin D-Sub connector	Serial Interface	1

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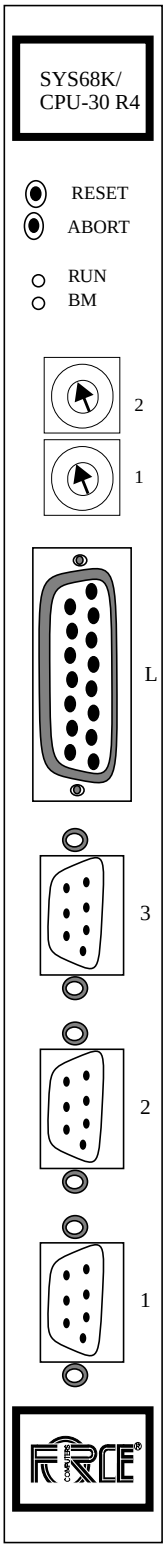
Figure 3 **Front Panel**



RESET and ABORT Keys

Status LEDs

Rotary Switches

15-pin D-Sub Connector

9-pin D-Sub Connector

9-pin D-Sub Connector

9-pin D-Sub Connector

2.3.1 RESET and ABORT Keys

The RESET key generates an on-board reset. The ABORT key generates an IRQ on a programmable level. Both keys can be disabled via the switches described below:

SW7-1	Description
OFF (default)	RESET key enabled
ON	RESET key disabled

SW7-2	Description
OFF (default)	ABORT key enabled
ON	ABORT key disabled

2.3.2 Status LEDs

The CPU-30 R4 includes two front panel LEDs: RUN/HALT LED and BM LED.
The RUN/HALT LED displays the condition that the processor is halted or reset is active and, in this case, the LED turns red. The RUN/HALT LED turns green on normal operation.
The bus master BM LED is used to indicate VMEbus mastership of the CPU-30 R4 and, in this case, the LED turns green.

2.3.3 Voltage Sensor

The voltage sensor generates a power-up reset if the voltage level is below 4.75 V.

2.3.4 Watchdog Timer

This timer can be enabled by software and will generate an NMI followed by a power-up reset, when it is not retriggered

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.

SW13-2	Description
OFF (default)	Watchdog reset disabled
ON	Watchdog reset enabled

2.3.5 Two Rotary Switches

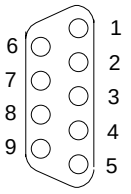
Two software readable four-bit rotary switches are installed on the board and are accessible via the front panel.

2.4 Serial I/O Channels

The CPU-30 R4 has three serial I/O channels available via 9-pin D-Sub connectors on the front panel. All channels will support RS-232, RS-422 and RS-485 interfaces via the FORCE hybrids FH-xxx. The default configuration is RS-232.
The following table shows the pinout of the serial I/O channels for RS-232.

Table 3 9-pin D-Sub Connector Pinout[1)] (RS-232)

Pin	Signal	Direction	Description
1	DCD	in	Data Channel Detector
2	RxD	in	Receive Data
3	TxD	out	Transmit Data
4	DTR	out	Data Terminal Ready
5	GND	-	Signal Ground
6	DSR	in	Data Set Ready
7	RTS	out	Request to Send
8	CTS	in	Clear to Send
9	GND *	-	Signal Ground



1. Default terminal port setup: 9600 Baud, 8 data bits, 1 stop bit, no parity.

Note: ***With FH-002, this signal is provided by the hybrid being used. The signal DTR is always driven active and the signal DSR is always read active by software. The RS-232 interface on your current CPU-30 revision 4.x board is fully compatible to the RS-232 interface on the earlier CPU-30 revision 3.2 board. However, the default jumper settings prescribed for the earlier board must be used to obtain this functionality.**

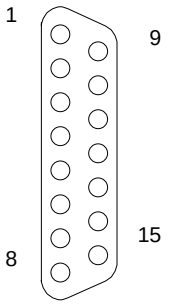
2.5 AUI-Ethernet

The AUI-Ethernet Interface is available on the front panel via a 15-pin D-Sub connector.
The unique Ethernet address is displayed by the banner when entering the FGA Boot debugger. FGA Boot also provides a utility function to get the CPU board's Ethernet address: "#40 (0x28) Get Ethernet Number".
The following table shows the pinout of the AUI-Ethernet connector

.

Table 4 15-pin AUI-Ethernet Connector

Pin	Description
1	GND
2	Collision Detect+
3	Transmit Data+
4	GND
5	Receive Data+
6	GND
7	Not connected
8	GND
9	Collision Detect-
10	Transmit Data-
11	GND
12	Receive Data-
13	+12V
14	GND
15	Not connected



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2.6 SCSI

The MB87033/34 provides an 8-bit single-ended SCSI interface. It is routed to the VMEbus P2 connector.
The termination is switch selectable and "TERMPWR" is supported. The following switches control the SCSI termination.

SW7-3	Description
OFF (default)	SCSI active termination enabled
ON	SCSI active termination disabled

Note: **TERMPWR is always supplied; if termination power is supplied externally by a source other than the VME connector, the active termination is still maintained, although the VME may not be powered.**

2.7 Parallel I/O (Option)

The parallel I/O signals are only available with the optional 5-row VMEbus P2 connector.

2.8 Connector Pinout for VMEbus P2

Table 5 Signal Assignment of the VME P2 Connector

PIN	Row Z (factory option)	Row A	Row C	Row D (factory option)
1	PIT2 A0	SCSI Data 0	FDC RPM (TxD Port 2)	NC
2	GND	SCSI Data 1	FDC HLO-AD (FDC EJECT) (RxD Port 2)	NC
3	PIT2 A1	SCSI Data 2	FDC DSEL2	TxD Port 1
4	GND	SCSI Data 3	FDC INDEX	RxD Port 1
5	PIT2 A2	SCSI Data 4	FDC DSEL1	RTS Port 1
6	GND	SCSI Data 5	FDC DSEL2	CTS Port 1
7	PIT2 A3	SCSI Data 6	FDC DSEL1	DTR Port 1
8	GND	SCSI Data 7	FDC MO-TOR	DCD Port 1
9	PIT2 A4	SCSI DP	FDC DIREC	GND Port 1
10	GND	GND	FDC STEPX	TxD Port 2
11	PIT2 A5	GND	FDC WDA-TA	RxD Port 2
12	GND	GND	FDC WGATE	RTS Port 2
13	PIT2 A6	TERMPWR	FDC TRK00	CTS Port 2
14	GND	GND	FDC WPROT	DTR Port 2
15	PIT2 A7	GND	FDC RDA-TA	DCD Port 2
16	GND	SCSI ATN	FDC SDSEL	GND Port 2
17	PIT2 H1	GND	FDC RDY	TxD Port 3
18	GND	SCSI BSY	(RTS Port 2)	RxD Port 3

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Table 5 Signal Assignment of the VME P2 Connector (Continued)

PIN	Row Z (factory option)	Row A	Row C	Row D (factory option)
19	PIT2 H2	SCSI ACK	GND	RTS Port 3
20	GND	SCSI RST	GND	CTS Port 3
21	PIT2 H3	SCSI MSG	(CTS Port 2)	DTR Port 3
22	GND	SCSI SEL	GND	DCD Port 3
23	PIT2 H4	SCSI CD	GND	GND Port 3
24	GND	SCSI REQ	(TxD Port 3)	DSR Port 1
25	PIT1 H1	SCSI IO	(RxD Port 3)	DSR Port 2
26	GND	(RTS Port 1)	(RTS Port 3)	DSR Port 3
27	PIT1 H2	GND	(CTS Port 3)	PIT1 C0
28	GND	(CTS Port 1)	(TxD Port 1)	PIT1 C1
29	PIT1 H3	DSR Port 4	DCD Port 4 (RxD Port 1)	PIT1 C4
30	GND	RTS Port 4	RxD Port 4	PIT1 C7
31	PIT1 H4	CTS Port 4	TxD Port 4	NC
32	GND	GND Port 4	DTR Port 4	NC

Note: **The signals marked in parenthesis are only available with the use of FH-002 hybrids, which are available at Force Computers.**

2.9 Introduction to VMEPROM Firmware

The VMEPROM firmware is a full multitasking multiuser real-time system. It is stored in the on-board System Flash Memory and provides the following functionality:

- Configuration of the board
- Starting an application
- Application hooks
- Shell with over 80 commands
- Programming of Boot Flash devices

2.9.1 Booting up VMEPROM

To start VMEPROM, the rotary switches must both be set to ‘F.

Table 6 Rotary Switches

MODE 1	F
MODE 2	F

The different functions of the rotary switches are described in detail in the VMEPROM section of the *SYS68K/CPU-30 R4 Technical Reference Manual.*

Correct Operation
To test the correct operation of the CPU board, the following command must be typed in:

```
# SELFTEST <CR>
```

The selftest command tests some I/O devices, the main memory and the system timer tick interrupt. Depending on the size of the main memory, it may last a different amount of time (count about one minute per megabyte).
After all tests are done, the following message will appear on the terminal screen:

```
VMEPROM Hardware Selftest
-------------------------
I/O test ........ passed
Memory test ..... passed
Clock test ...... passed
```

2.10 The SYS68K/IOBP-1

Force Computers offers an IOBP-1 back panel for easy connection of I/O signals through the VMEbus P2 connector. This board can be plugged into the VMEbus P2 connector of a VMEbus board which carries the SCSI, FDC, and serial I/O signals on the VMEbus P2. It contains a SCSIbus connector (P2), a floppy disk interface connector (P3), and a serial I/O connector (P5). All VMEbus P2 connector row A and C pins are routed

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to the 64-pin male connector (P4). The pinout of these connectors is shown in the following table.

Table 7 SYS68K/IOBP-1 Pin Assignment

PIN No. IOBP-1 P1	**PIN No. VME bus P2**	**Row A Signal Mnemonic**		**Row B Signal Mnemonic**	**Row C Signal Mnemonic**	
32	1	DB 0	SCSI	-		
31	2	DB 1	SCSI	GND		
30	3	DB 2	SCSI	-	Drive Select 4 (2)	FDC
29	4	DB 3	SCSI	-	Index	FDC
28	5	DB 4	SCSI	-	Drive Select 1	FDC
27	6	DB 5	SCSI	-	Drive Select 2	FDC
26	7	DB 6	SCSI	-	Drive Select 3 (1)	FDC
25	8	DB 7	SCSI	-	Motor On	FDC
24	9	DB P	SCSI	-	Direction In	FDC
23	10	GND		-	Step	FDC
22	11	GND		-	Write Data	FDC
21	12	GND		GND	Write Gate	FDC
20	13	TERMP-WR	SCSI	-	Track 000	FDC
19	14	GND		-	Write Protect	FDC
18	15	GND		-	Read Data	FDC

Table 7 SYS68K/IOBP-1 Pin Assignment (Continued)

PIN No. IOBP-1 P1	PIN No. VME bus P2	Row A Signal Mnemonic		Row B Signal Mnemonic	Row C Signal Mnemonic	
17	16	ATN	SCSI	-	Side Select	FDC
16	17	GND		-	FDC READY	FDC
15	18	BSY	SCSI	-		
14	19	ACK	SCSI	-	GND	
13	20	RST	SCSI	-	GND	
12	21	MSG	SCSI	-		
11	22	SEL	SCSI	GND	GND	
10	23	C/D	SCSI	-	GND	
9	24	REQ	SCSI	-		
8	25	I/O	SCSI	-		
7	26			-		
6	27	GND		-	Reserved	
5	28			-	Reserved	
4	29	DSR	SER	-	DCD	SER
3	30	RTS	SER	-	RXD	SER
2	31	CTS	SER	GND	TXD	SER
1	32	GND	SER	-	DTR	SER

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3 History of Manual Publication

Below is a description of the publication history of this *SYS68K/CPU-30 R4 Installation Guide.*

Table 8 History of Manual

Edition No.	Description	Date
1	First Print	February 1996
2	Description of switch SW11-3 in table 1 has been corrected	May 1996
3	Revised safety note	October 1996
4	“AUI-Ethernet” has been changed.	January 1997
5	Configuration of serial ports 1-4 for RS-232, 422 and 485 completed, location diagram and switch settings of SW12 in table 1 updated	January 1998
6.0	Section “Safety Notes” included	September 1999
7.0	Editorial changes	November 1999

Product Error Report

PRODUCT:	SERIAL NO.:
DATE OF PURCHASE:	ORIGINATOR:
COMPANY:	POINT OF CONTACT:
TEL.:	EXT.:
ADDRESS: _____ _____ _____	
PRESENT DATE:	
AFFECTED PRODUCT: ❑ HARDWARE ❑ SOFTWARE ❑ SYSTEMS	AFFECTED DOCUMENTATION: ❑ HARDWARE ❑ SOFTWARE ❑ SYSTEMS
ERROR DESCRIPTION: _____ _____ _____ _____ _____ _____ _____ _____ _____ _____	

THIS AREA TO BE COMPLETED BY FORCE COMPUTERS:

DATE:

PR#:

RESPONSIBLE DEPT.: ❑ MARKETING ❑ PRODUCTION

ENGINEERING ➠ ❑ BOARD ❑ SYSTEMS

✉ Send this report to the nearest Force Computers headquarter listed on the back of the title page.