Document Number: 814256
Version: 2
Date: February 2006

COMPACT CHAMP-AV IV QUAD POWERPC™

(SCP-424)

USER'S MANUAL

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REVISION HISTORY

Rev	By	Date	Description
1	JP	August 2005	First release.
2	BC	February 2006	Removed warning label from Chapter 2 page 5.

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TRADEMARKS

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PREFACE

PURPOSE

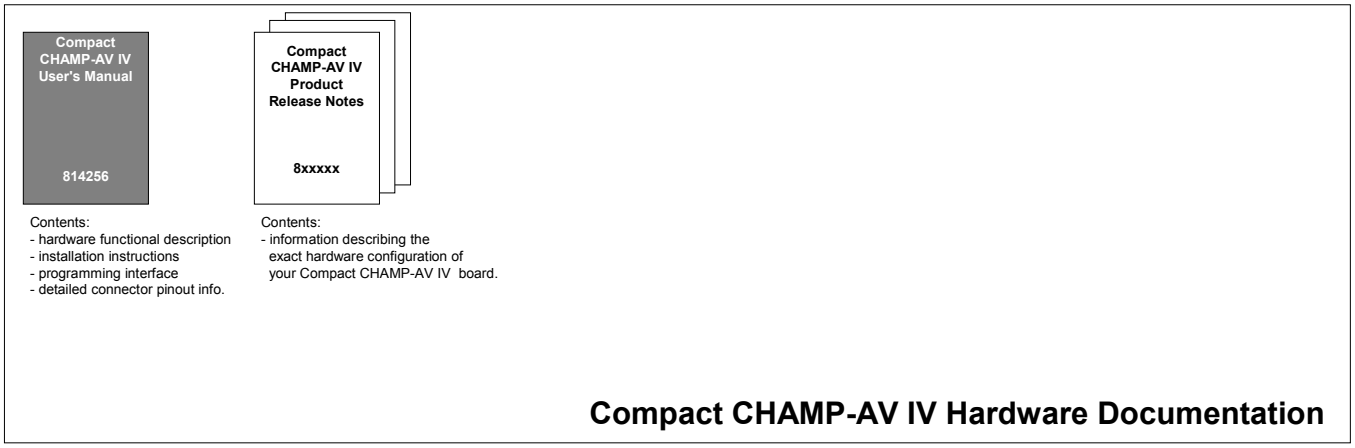
This manual describes the cPCI based Compact CHAMP-AV IV. After explaining the capabilities of the Compact CHAMP-AV IV, the manual provides the procedure for correctly installing it and checking its operation.

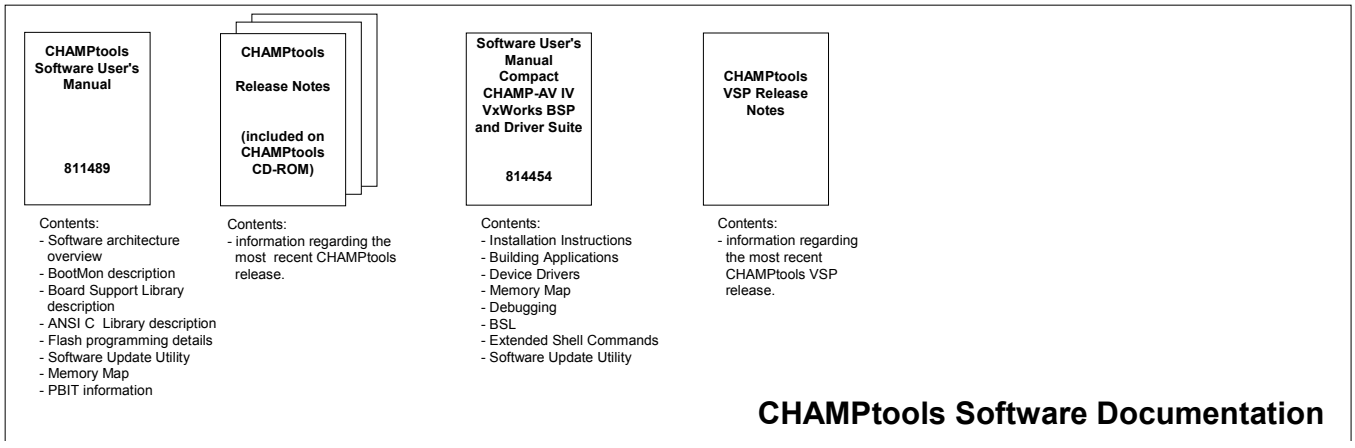
AUDIENCE

This document is aimed at readers with a technical understanding of hardware engineering fundamentals, as well as a basic understanding of the cPCI, PCI, and digital signal processing hardware and software.

DOCUMENTATION ROADMAP

The figure below will help you understand what documentation is available for the Compact CHAMP-AV IV. These documents are delivered in Adobe Acrobat.pdf format on CD-ROM, or may be obtained via our TechNet web site at http://www.technet.dy4.com/.





SCOPE

This manual contains the following chapters:

Chapter 1 - Product Overview. This chapter provides an overview of the features and functions of the Compact CHAMP-AV IV. This includes a technical description of the block diagram.

Chapter 2 - Pre-Installation Tasks. This chapter discusses tasks that must be performed before installing the Compact CHAMP-AV IV in a system, including checking power requirements.

Chapter 3 - Hardware Installation. This chapter explains how to install the Compact CHAMP-AV IV into a cPCI chassis and verify that it is operating correctly.

Chapter 4 - Programming Interface. Describes the memory maps for the Compact CHAMP-AV IV.

Appendix A - Connector Pin Assignments. This appendix lists the interface connector pinouts for the Compact CHAMP-AV IV.

RELATED SOFTWARE DOCUMENTS

For information on installing the Compact CHAMP-AV IV software, refer to the CHAMPtools Software User's Manual (document number 811489).

Wind River Systems Doumentation

Information describing the operation of the version 1.2 WIND POWER *ICE* and visionPROBE II emulators is provided in the following Wind River Systems publications:

- WIND POWER *ICE* for WIND POWER *IDE* User's Guide, part # DOC-15149-NN-00
- WIND POWER *IDE* Getting Started, part # DOC-15146-ZD-00
- WIND POWER *IDE* Release Notes
- visionPROBE II for WIND POWER *IDE* User's Guide, part # DOC-15145-ND-00

CONVENTIONS USED IN THIS MANUAL

This document and the accompanying documents in the documentation package use various icon conventions and abbreviations to make the documents clearer and easier to read. These conventions cover typography for such elements as sample software code and keystrokes, signal meanings, and graphical elements for important information such as warnings or cautions.

Company Name

The abbreviation "CWCEC" seen in this document is used to represent the company name "Curtiss-Wright Controls Embedded Computing", which is a division of Curtiss-Wright Controls, Inc.

Product Naming Conventions

The generic product name "Compact CHAMP-AV IV" is used throughout this manual to represent the SCP-424 (commercial version of the Compact CHAMP-AV IV)

Typographic Conventions

Table 1 lists the typographical conventions used in this documentation package.

TABLE 1: Typographic Conventions

Item	Convention	Example
Keystrokes	Keys are listed as they appear on most keyboards, surrounded by < > marks. Combinations of key-strokes appear within a single set of < > brackets.	Type < Ctrl-Alt-C > to return to the previous menu. Type < Esc > to exit.
File Names	File names are set in italics.	Copy the file named *bootA.exe*.
Directory Names	Directory names show the full directory path. The last directory in the path does not have a trailing slash following it.	Go to the *c:\windows\temp\backup* directory.
Monitor Displays	Prompts and other text appearing on monitors is set in bold monospace type.	**`BootMon>`**
Firmware Code	Firmware code, and any informtion you need to type in response to a prompt, is set in monospace type.	`bootMon2.exe`

Signal Conventions

Table 2 lists symbols that can follow a signal name. For example, the Hash (#) is used with a PCI or cPCI signal name, such as FRAME#.

TABLE 2: Signal Conventions

Symbol	Description
#	The signal is active LOW.
[no symbol]	The signal is active HIGH.

Abbreviations

Table 3 lists the abbreviations used to describe the size of a memory device or a range of addresses.

TABLE 3: Abbreviations

Abbreviation	Convention
1 Kbyte	1,024 bytes
1 Mbyte	1,024 Kbytes
1 Gbyte	1,024 Mbytes

Memory Addresses

Unless otherwise stated, all memory addresses are shown in hexadecimal notation.

Icons

The following icons are used throughout the documentation package:

Cross Reference

Cross references to other documents are used when a subject being discussed is addressed in depth by another, more authoritative document. Cross references are also used for document chapters and sections.

Warning

The warning icon indicates procedures in the manual that, if not carried out, or if carried out incorrectly, could cause physical injury, electrical damage to equipment, or a non-recoverable corruption of data. Warnings include instructions for preventing such damage. Please observe warning icons and read the accompanying text completely before carrying out the procedure.

Caution

The caution icon indicates non-catastrophic incidents, complex practices, or procedures which, if not observed, could result in damage to the hardware. Cautions include specific instructions for avoiding or minimizing these incidents.

Note

The note icon highlights exceptions and special information.

Tip

Tips provide extra information on the subject matter. This could include hints about how to use your current CWCEC card to its maximum potential.

REFERENCE DOCUMENTATION

Refer to the following standards for information about the specifications the Compact CHAMP-AV IV is designed for compliance with:

- IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC), IEEE Std 1386.1-2001, June 14, 2001
- IEEE Standard for a Common Mezzanine Card (CMC) Family, IEEE Std 1386-2001, June 14, 2001
- PCI Local Bus Specification, PCI-SIG, Revision 2.3, March 29, 2002
- PCI-X Electrical and Mechanical Addendum to the PCI Local Bus Specifications, PCI_SIG, Rev. 2.0, Nov. 4, 2002
- PCI-X Protocol Addendum to the PCI Local Bus Specification, PCI-SIG, Rev. 2.0, July 29, 2002
- Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange, ANSI/TIA/EIA-232-F-1997, September 30, 1997
- MPC7447/A RISC Microprocessor User's Manual, Rev. 0, 8/2003
- PowerPC™ Microprocessor Family: The Programming Environments for 32-Bit Microprocessors, Motorola
- MV64460, MV64461, MV64462 System Controller for PowerPC Processors, Part 1 of 2 Hardware Specification, Doc. Number: MV-S101286-01, Revision B, Marvell, July 22, 2004
- MV64460, MV64461, MV64462 System Controller for PowerPC Processors, Part 2 of 2 User Manual, Doc. Number: MV-S101286-00, Revision B, Marvell, July 22, 2004
- Double Data Rate (DDR) SDRAM Spec, JEDEC Standard No. 79, Release 2, Feb. 2002
- Stub Series Terminated Logic for 2.5V (SSTL_2), JESD8-9A, Dec. 2000
- MPC8540 Integrated Processor Hardware Specification, Rev 3.1, 12/2004
- MPC8540 PowerQUICC III Integrated Host Processor Reference Manual, Rev 1, 7/2004
- PICMG 2.0 R 3.0 CompactPCI Specification, October 1, 1999
- PICMG 2.1 R2.0 CompactPCI Hot Swap Specification, January 17, 2001
- PCIMG 2.16 R1.0 CompactPCI Packet Switching Backplane (PSB) Specification, September 5, 2001

Please refer to DPK-TechDoc-CD for additional reference information, supplied in Portable Document Format (PDF) files readable by Adobe® Acrobat® Reader software. This Technical Documentation CD-ROM includes useful weblinks, an I/O pinout configurator utility, and a helpful guide to the VMEbus, among other things. You'll also find copies of the relevant cable assembly drawings on the CD.

Note

The DPK-TechDoc-CD CD-ROM also provides a copy of the Adobe Acrobat Reader software, version 4.0, including the Acrobat Search plug-in, to enable you to get the most out of your CD-ROM by enabling full-text searches of the information.

1 PRODUCT OVERVIEW

IN THIS CHAPTER...

This chapter discusses the high-level features of the Compact CHAMP-AV IV product. The following topics are discussed:

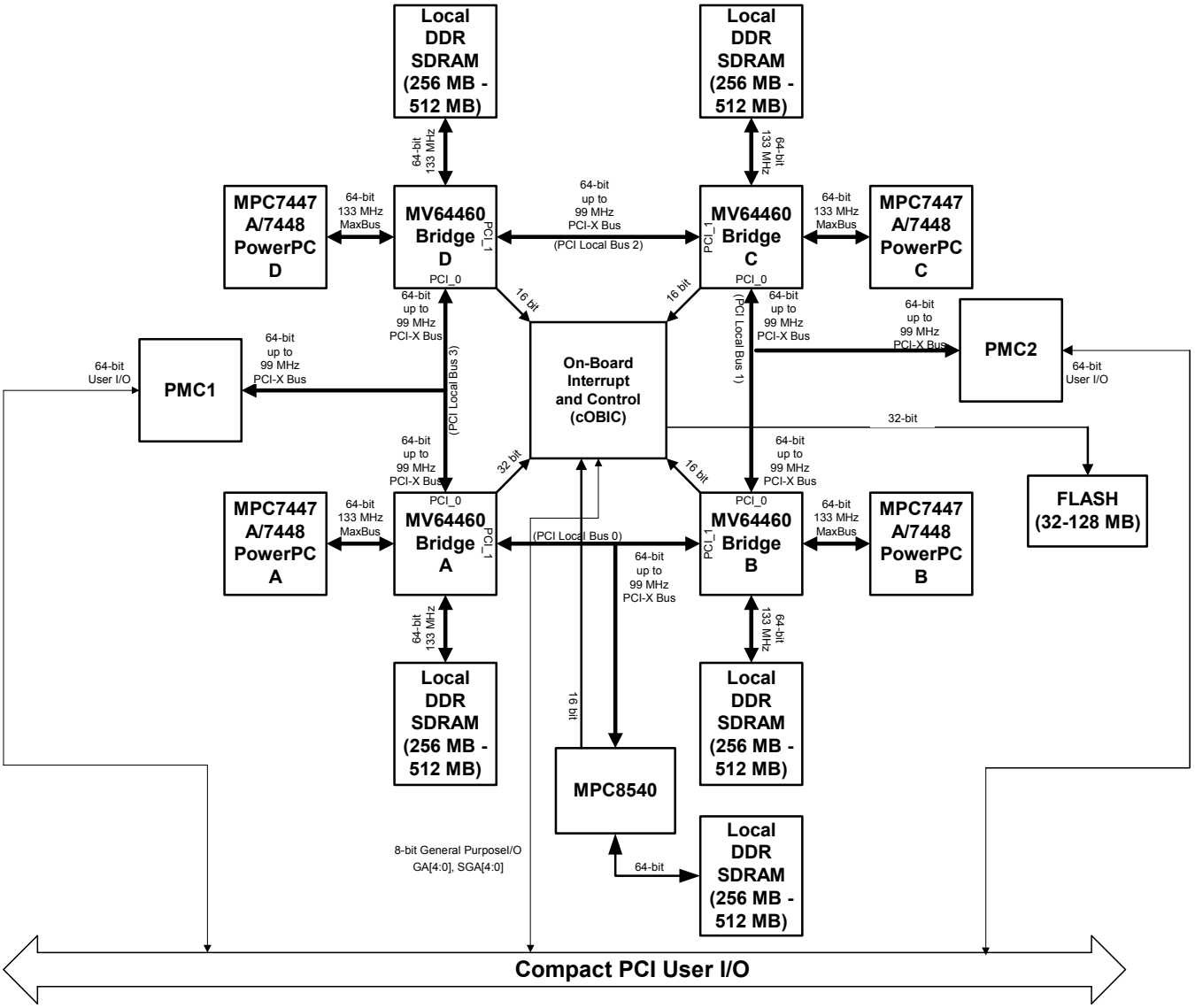
GENERAL DESCRIPTION

The Compact CHAMP-AV IV is a cPCI variant of our fourth generation VME-based quad PowerPC™ AltiVec DSP board. The Compact CHAMP-AV IV introduces an architecture based on the latest PowerPC™ and PCI-X bridge devices, to provide a very high bandwidth platform that maximizes the processing potential of four Freescale PowerPC™ MPC7448 or 7447A processors. The Compact CHAMP-AV IV also has a powerful fifth processor, the Freescale MPC8540 PowerQUICC III.

The Compact CHAMP-AV IV is particularly well suited to large, multi-slot systems. This is by virtue of its four 800 MB/sec (peak) PCI buses and its five Gigabit Ethernet connections (one per processor), which together provide very high I/O throughput and switching bandwidth. This together with its four altivec-enabled 7447A processors and fifth PowerPC processor allow the computing power and data movement to be well matched. The Compact CHAMP-AV IV has a rich set of features designed to accelerate multi-processing application performance and speed the software development process. A diverse offering of peripherals enable the Compact CHAMP-AV IV to be readily integrated into many types of systems such as benign military, signal intelligence, command, control and communications, as well as telecommunications systems.

The architecture of the Compact CHAMP-AV IV is illustrated in Figure 1.1 on page 1-3.

FIGURE 1.1: Compact CHAMP-AV IV Functional Block Diagram



FEATURE SUMMARY

- PICMG® 2.16 multi-processor card, CompactPCI form-factor (no cPCI interface)
- Four PowerPC™ 7448/7447A (AltiVec Technology™-enhanced) CPUs operating at up to 1.0 GHz (7447A) or 1.5 GHz (7448)
  - 64 Kbyte L1 and 1 Mbyte (7448)/512 Kbyte (7447A) L2 internal caches operating at core processor speed
  - 32 GFLOPs, 176 SPECint95, 132 SPECfp95 peak computational power (7447A)
  - 48 GFLOPs, 264 SPECint95, 198 SPECfp95 peak computational power (7448)
- Up to 512 Mbytes DDR-266 SDRAM per processor (2 Gbyte total)
- PowerPC™ 8540 at 500-800 MHz for control functions
  - 256 or 512 Mbytes DDR SDRAM
- QuadFlow architecture with up to 3.2 GB/s peak on-board throughput
- Five Gigabit Ethernet (GbE) ports, one per processor
- PICMG 2.16 compliance
- Support for two 64-bit, 100 MHz PCI-X mezzanine modules (PMC-X)
- Two EIA-232 serial ports
- Support for switch fabric PMC modules with differential routing to backplane
- VxWorks® Board Support Package
- IXLibs-AV optimized AltiVec DSP function library
- Verari VSI/Pro® Image VSIPL DSP library
- air-cooled level 0 ruggedization

TECHNICAL DESCRIPTION

The operation of the Compact CHAMP-AV IV is described in the following sections, with reference to the high level block diagram illustrated in Figure 1.1.

QUADFLOW ARCHITECTURE

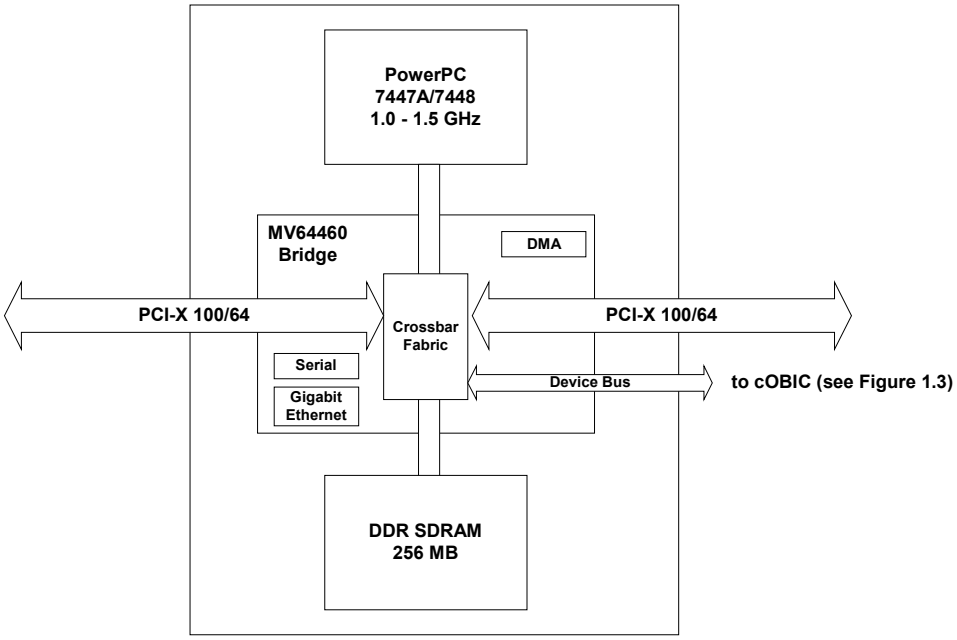
The Compact CHAMP-AV IV architecture is suited to DSP applications that place a high premium on processor to memory, processor to processor, and PMC I/O to memory bandwidth. The data flow capabilities of the Compact CHAMP-AV IV ensure that applications can extract the most from the raw computing performance of the four AltiVec engines. The Compact CHAMP-AV IV architecture encompasses three key attributes that contribute to maximizing DSP performance:

- The performance of the processor, I/O and memory subsystems.
- High-bandwidth, low-latency connections between processor nodes.
- A non-blocking bridge architecture with added data paths for simultaneous data transfers.

PROCESSOR NODES

The Compact CHAMP-AV IV provides four high performance processing nodes connected in a ring via high speed PCI-X buses. Each node consists of a 1 GHz PowerPC™ 7448/7447A processor with 1 Mbyte (7448)/512 Kbytes (7447A) of internal L2 cache and its own dedicated bank of DDR-266 SDRAM. Each processor node incorporates a Marvell MV64460 Discovery™ III bridge which acts as a non-blocking crossbar interface between the MPC7448/7447A processor, the DDR SDRAM, two 64-bit, 100 MHz PCI-X buses, and Gigabit Ethernet. See Figure 1.2 for additional details.

FIGURE 1.2: Processor Node Block Diagram



In multi-processing applications, problems are either addressed by spreading the data set across many processors or by utilizing the processors in a pipeline, with each processor performing a stage of the algorithm. In either case, the application requires the transfer of data between processors. The data movement is often the limiting feature of board performance rather than raw computing power. The QuadFlow architecture solves the processing and data flow requirements of high performance embedded systems.

Each node connects to two adjacent nodes via a pair of PCI-X interfaces and provides an off-board high-bandwidth Gigabit Ethernet connection. Each node has a separate 16-bit port into the On-Board Interrupt and Control c(OBIC) FPGA, except for Node A, which has a 32-bit port (see "On-Board Interrupt and Control (cOBIC)" on page 1-8 for details). With each PowerPC having a dedicated bus to its own memory, application performance does not degrade as it does in shared memory designs.

The processor bus between the MPC7448/MPC7447A and the Discovery III bridge operates at a bus speed of 133 MHz and utilizes the PowerPC MPX mode of operation, providing higher memory bus performance compared with the 60x bus.

Each processing node has two independent 64-bit, 100 MHz PCI-X connections, one to each of the adjacent nodes. Separate, simultaneous transfers can occur on all four (QuadFlow) of the PCI-X segments, resulting in a peak aggregate bandwidth of 3.2 GB/s. The peak PCI bandwidth into any one node is 1600 MB/sec. High throughput translates to lower latencies in application performance. Another advantage of the dual PCI-X connections at each node is that transfers between adjacent nodes do not traverse a PCI-PCI bridge, and thus only one PCI segment is used. This requires only a single PCI arbitration cycle, once again providing minimum latency for data transfers. The Discovery™ III bridge features a highly programmable arbitration controller which allows priority allocation between the processor, PCI, and DMA engines for access to the DDR SDRAM memory. Users can fine tune the priority of these devices to suit the needs of their application and achieve the best possible efficiency of the memory subsystem.

Each Discovery™ III bridge provides four DMA controller engines which are capable of transfering data between any of the bridges' interfaces. The DMA capability is particularly useful for managing transfers between processor node memory banks and transfers to and from PMC devices. In addition, the Discovery III bridge provides two XOR DMA controller engines that can read from up to eight sources, perform bitwise XOR between the eight sources, and write the result to a destination.

These architectural advantages of the Compact CHAMP-AV IV will simplify and speed the process of application development. Developers can focus on the problem, rather than optimizing for board architectures that restrict data flow to one or two simultaneous transactions. The memory map of the Compact CHAMP-AV IV allows any processor to access the memory of any other processor and both PMC sites. Any PMC module can access any of the processor node memories.

NODE E PROCESSOR

The Compact CHAMP-AV IV includes a fifth processor, called Node E. This processor, an MPC8540, is a highly integrated device that contains a DDR SDRAM controller, PCI-X interface, local bus (similar to Disco III device bus), Gigabit Ethernet MAC and UART on chip. The 8540 can be used in a wide variety of applications as a control and management interface, traffic manager, or other function. This capability allows the other nodes to focus on more processing-intensive applications.

The 8540 can access all the memory of the other nodes and both PMCs over the PCI-X bus. It also has its own interface into the cOBIC so that all the features of the cOBIC are available to this device as well.

DOUBLE DATA RATE SDRAM

Each 7448/7447A processor node on the Compact CHAMP-AV IV consists of either 256 or 512 Mbytes of Double Data Rate (DDR) SDRAM. The instantaneous peak data transfer rate to the DDR-266 SDRAM is over 2.0 GB/s at 133 MHz. The DDR SDRAM is accessible from the processor and from both PCI buses.

Processor Node E has either 256 or 512 Mbytes of DDR SDRAM. This memory operates at DDR 200, which gives an instantaneous peak data transfer rate of 1.6 GB/s at 100 MHz. Processor E memory is accessible from the processor and from the PCI bus.

FLASH MEMORY

The Compact CHAMP-AV IV provides 32, 64, 128 or 256 MBytes of 32-bit Flash memory on node A. The Flash devices are specified for 100,000 erase cycles per sector (typical) and a data retention time of 20 years (typical).

For security against inadvertent Flash programming, set Switches S2[3] and S2[4] both to the "ON"position. (Note: switch is "ON" when the slide bar is moved towards the card edge).

HIGH SPEED SRAM

Incorporated into the Discovery™ III system controller, the Compact CHAMP-AV IV provides 256 Kbytes of high-speed SRAM per processor node. While useful as a general purpose high-performance memory area that offloads traffic to SDRAM, the SRAM is particularly beneficial for holding descriptors for Discovery™ III peripheral devices, allowing DMA units to simultaneously access data from SDRAM while descriptors are accessed from the SRAM.

PMC-X SITES

The Compact CHAMP-AV IV is equipped with two mezzanine sites compatible with the PCI (PMC) and PCI-X (PMC-X) standards. The PMC-X interfaces support 64-bit, PCI-X100 transfers (100 MHz PCI-X) with a resulting peak rate of 800 MB/s. The board is backward compatible with PCI-X66 (66 MHz PCI-X), PCI-66 (66 MHz conventional PCI) and PCI-33 (33 MHz conventional PCI). The interfaces are mapped to all five processor nodes allowing transfers between any node and any interface. All four PMC interrupt signals may be routed under software control to any of the processors, allowing the developer the choice of which processor hosts the PMC control software.

PMC I/O is supported on both the front panel as well as the P3 and P5 backplane connectors. The routing of I/O signals from PMC to P3 and P5 is arranged in differential pairs with careful impedance control and matching of trace lengths. This technique supports the latest generation of high performance digital interfaces included on some PMCs, such as the StarLink switch fabric PMC, the PMC-643 Fibre Channel and the PMC-706 and PMC-708 Graphics PMCs. With a pair of StarLink PMCs, the Compact CHAMP-AV IV can act as a combined StarFabric node and switch, with a massive 3.2 GB/sec of I/O (including switching throughput) between the PMCs and the I/O connectors.

PCI LOCAL BUS

The Compact CHAMP-AV IV contains four local PCI buses. The four buses are interconnected through the PCI-X to PCI-X bridging capability of the Discovery III bridges. The PCI buses connect Nodes A, B, C and D in a ring architecture and operate at a maximum rate of 100 MHz, 64 bits (800 MBytes/s). Each node connects into the ring via two PCI/PCI-X buses. This feature provides maximum data throughput on the board since each processor can access both sides of the ring simultaneously. Node E is connected to the PCI/PCI-X segment between Nodes A & B.

On reset, the Compact CHAMP-AV IV startup code automatically scans the PCI/PCI-X devices and assigns bus numbers to these segments. Since the bus numbers are dynamically allocated after board reset, the bus numbers may differ between power-on cycles if different PMCs are installed between these events. For instance if a PMC-X/PMC site is populated with a device that further segments the PCI/PCI-X bus, the bus numbers assigned will differ compared to those that would be assigned for a device that did not contain the additional buses.

The PCI-X bus between Nodes A and B and between Nodes C and D will always operate in PCI-X100 mode (PCI-X mode at 100 MHz/64 bit). However, the speed of PCI/PCI-X buses between Nodes B and C and between Nodes A and D will depend upon the PMC-X/PMC that is installed on those buses. A 33 or 66 MHz PMC will drop the speed of the bus on which it is installed to PCI33 or PCI66 (PCI mode at 33 or 66 MHz), respectively. A signalling voltage of 5 volts (VIO) will also drop the speed of the PCI bus to PCI33.

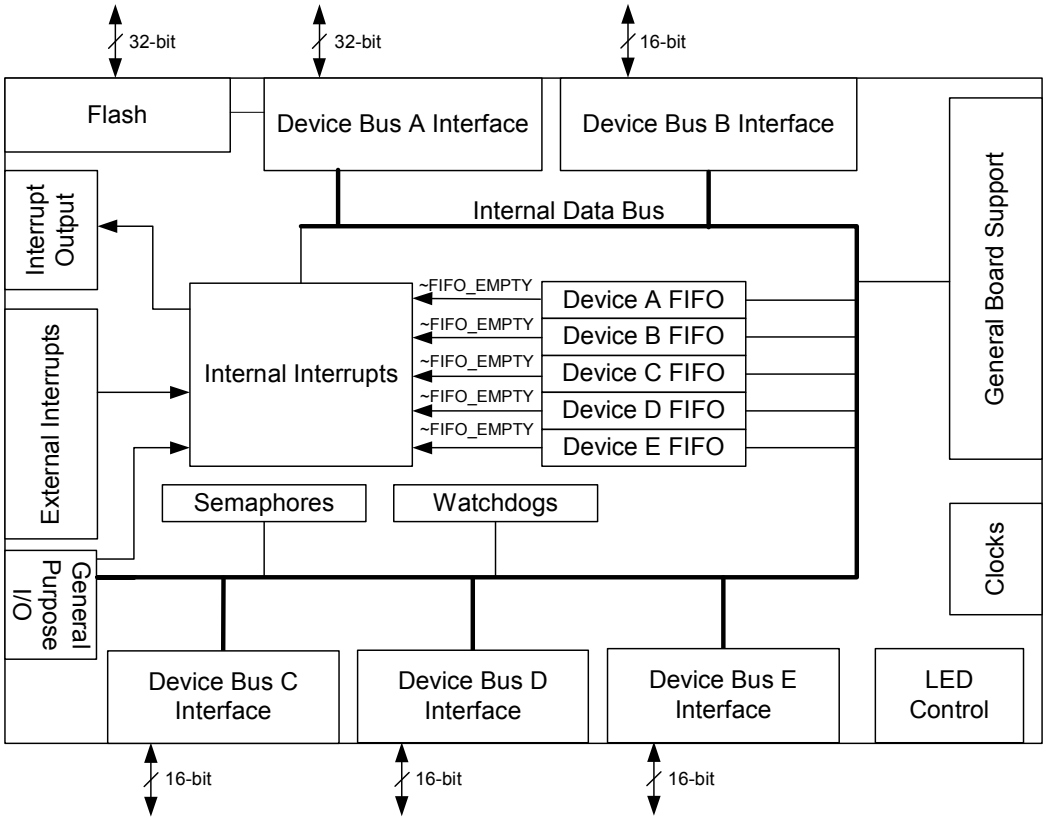
ON-BOARD INTERRUPT AND CONTROL (CCOBIC)

The Compact CHAMP-AV IV has special purpose hardware to accelerate inter-processor messaging and control, as well as to provide other important board capabilities (such as watchdog timers, semaphores and LED control). Each node has a unique connection into the cOBIC through the Device Interface on the Discovery controller, except the 8540 which has a connection through its local bus interface. This allows the user to access the feature set of the cOBIC without having to use a PCI bus. The board support library in CHAMPtools contains functions to support the cOBIC features. Because these functions are provided, detailed information regarding the cOBIC registers and bit format is not provided in this manual. If the user desires to write low-level code to control the cOBIC, please contact Customer Support for additional cOBIC information.

A customer upgradeable serial PROM is used to configure the cOBIC. On power up the cOBIC automatically loads its configuration from this PROM.

The Compact CHAMP-AV IV also contains an alternate serial PROM which can be used to configure the cOBIC in the event that there is a problem with the main PROM. This PROM is not upgradeable by the customer and puts the cOBIC into a known working state. Switch SW4 is used to select the main PROM and the alternate PROM (see "Configuring Switches" on page 2-8). A block diagram of the cOBIC is shown below in Figure 1.3.

FIGURE 1.3: cOBIC Block Diagram



cOBIC Feature Summary

As seen in Figure 1.3 above, the cOBIC incorporates the following features:

An Internal Interrupt Module

- Twenty-One internal interrupts
- Interrupt detection and steering
- Interrupt masking

An External Interrupt Module

- Twenty-Four external interrupts supplied to the cOBIC
- Interrupt detection and steering
- Interrupt masking

An Inter-Processor Module

- Mailbox Interrupts supported by five FIFOs, one per processor. Only the processor that "owns" a FIFO can read it while all processors can write it.
- Dedicated inter-processor interrupts
- Sixteen semaphore registers
- Five Watchdog timers, one per processor.

General Purpose I/O

- Eight general purpose I/O signals to rear panel J4 connector (GPIO_0 through GPIO_7)
- Two may be used for interrupts or GPIO (GPIO_1 and GPIO_2)

General Board Support Module

- Provides the hardware for the control of miscellaneous board resources.

Internal and External Interrupt Modules

Figure 1.4 on page 1-10 provides an overview of the interrupt routing on the board while Table 1.1 and Table 1.2 list the internal and external interrupt sources respectively. Figure 1.5 notes how these interrupts are routed to the interrupt outputs connected to each processor.

Interrupt Routing

As can be seen from Figure 1.4 and Figure 1.5, the cOBIC provides an interrupt routing function. In a single processor system, it is obvious where all interrupt processing tasks are handled. In a multi-processor system, a fixed mapping of hardware interrupts to specific processors is likely to be less then optimum. The Compact CHAMP-AV IV allows the hardware to adapt to the needs of the software. All of the internal and external interrupt sources (PMC modules, GPIO, PCI, etc.) are routed into a software-configurable multiplexer that allows any processor to receive interrupts from any device. This feature speeds interrupt response time by routing the interrupt directly to the intended processor. Since the interrupt status registers are within the accelerator, the application avoids using the PCI bus during the interrupt service routine, thus reducing the incurred latency.

FIGURE 1.4: Interrupt Routing

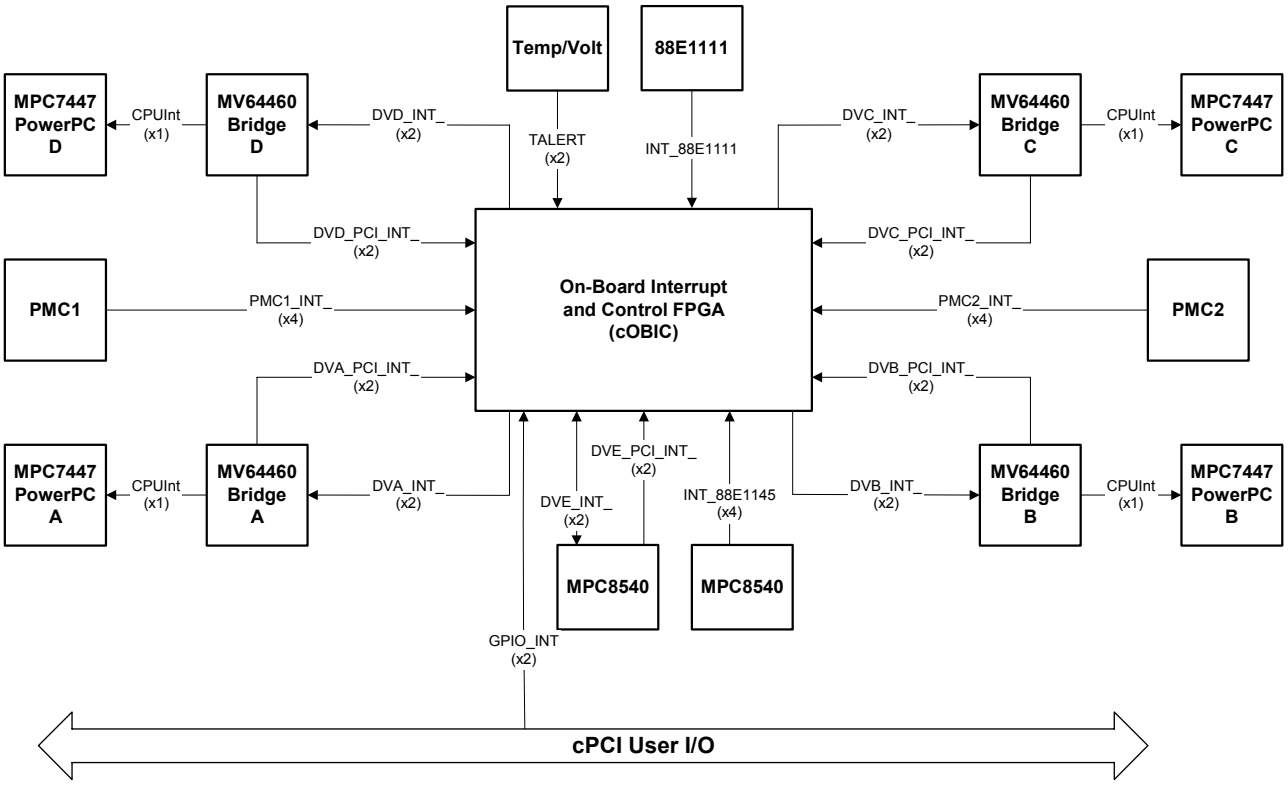
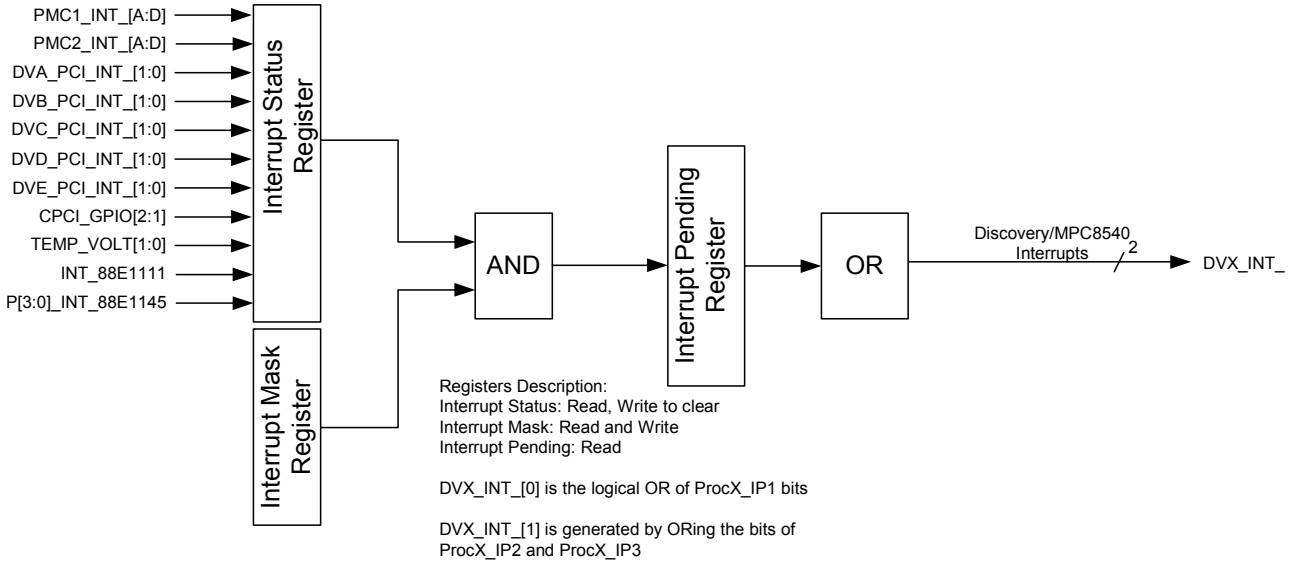


TABLE 1.1: Internal Interrupt Sources

Interrupt Input	Detection Mode	Location for Clearing	Description
FIFO Not Empty [A:E]	N/A	cOBIC	There is a 16-bit, 32 Deep FIFO associated with each processor. When one of these FIFO's receives data, it produces an interrupt.
Watchdog[A:E]	N/A	cOBIC	An Avionics style watchdog timer is associated with each node. If the watchdog is kicked too soon or too late, an interrupt is generated.
Inter-Processor Int[7:0]	N/A	cOBIC	Each processor can generate up to 8 interrupts to another processor.

FIGURE 1.5: Interrupt Structure



More information describing the operation of the various external interrupts seen in Figure 1.5 is provided below in Table 1.2.

TABLE 1.2: External Interrupt Sources

Interrupt Input	Detection Mode	Location for Clearing	Description
PMC1[D, C, B, A]	Active low	Source	Interrupts A - D from PMC in Site 1
PMC2[D, C, B, A]	Active low	Source	Interrupts A - D from PMC in Site 2
DVA_PCI_INT[1:0]	Active low	Source	PCI Interrupts from MV64460, Node A
DVB_PCI_INT[1:0]	Active low	Source	PCI Interrupts from MV64460, Node B
DVC_PCI_INT[1:0]	Active low	Source	PCI Interrupts from MV64460, Node C
DVD_PCI_INT[1:0]	Active low	Source	PCI Interrupts from MV64460, Node D
DVE_PCI_INT[1:0]	Active low	Source	PCI Interrupts from MPC8540, Node E

TABLE 1.2: External Interrupt Sources (Continued)

Interrupt Input	Detection Mode	Location for Clearing	Description
GPIO[2:1]	Edge (Rising or Falling) or Level (Active Low or High)	Source	User Interrupts from cPCI connector J4, pins B25 and D25.
TALERAD	Active low	cOBIC	Overtemperature alarm from Nodes AD sensor (not currently implemented)
TALERBC	Active low	cOBIC	Overtemperature alarm from Nodes BC sensor (not currently implemented)
INT_88E1111			Ethernet interrupt from node E Phy (not currently implemented)
P[3:0]_INT_88E1145			Ethernet interrupts from nodes A-D Phy (not currently implemented)

The DVx_PCI_INT[1:0] interrupts from each node are actually the PCI interrupts from the Discovery part. Through interrupt steering registers in the Discovery, interrupts from various MV64460 resources (DMA, Timers, etc.) can be mapped to these outputs.

TALERAD and TALERBC provide over temperature alarm information to the cOBIC. The sensors that generate these alarms are located at U225 and U229. TALERBC originates from U229 while TALERAD originates from U225 (see Figure 1.9 on page 1-22).

Each temperature sensor monitors three separate temperatures. TALERBC monitors the temperature of processor B, processor C, and the temperature of the board at the location of U23 (location of itself). TALERAD monitors the temperature of processor A, processor D, and the temperature of the board at the location of U19 (location of itself).

Inter-Processor Module

In multi-processor applications, software designers implement message passing schemes between the various processors in the system. The most common implementation is for the transmitting processor to cause an interrupt to occur on the receiving processor, with a pre-agreed protocol between the pair to define the location and content of the message.

The problem with this mechanism is that many board architectures suffer latencies and other slowdowns because the same PCI bus that is used for inter-processor data transfers is also used for passing these interrupts. The Compact CHAMP-AV IV has special purpose hardware to accelerate inter-processor messaging. This hardware is contained in the inter-processor module and consists of processor to processor mailbox interrupts and hardware-controlled interrupt routing facilities.

The inter-processor module consists of five FIFOs for support of mailbox interrupts, five inter-processor interrupt registers, sixteen semaphore registers, five watchdog timers and a multi-board synchronous timer. These features are described below:

Mailbox Interrupts

The cOBIC provides mailbox interrupts, whereby a processor can interrupt another processor and deliver a 16-bit value. Each processor has a 16-bit, 32-deep FIFO. Any processor can write to the FIFO of any other processor. An entry in the FIFO causes an interrupt to the associated processor, if enabled. The software can use the 16-bit value to include a message with the interrupt. The combination of a separate data path and the inclusion of a 16-bit message can significantly reduce the latency of using interrupts to send messages between processors.

Inter-processor Interrupts

The Inter-Processor Module also contains the Inter-Processor Interrupt generation registers. Typically the external interrupts are not latched in cOBIC since they are latched at the source. However, the interrupts generated from Inter-Processor Interrupt generation registers (IPI) are latched. The IPI generation register has two primary fields to consider (see Table 1.3). A three-bit Processor ID field defines the processor to be interrupted and a three-bit field that defines the Processor Interrupt Identification value. To use the register,

a six-bit value is written to the IPI register. This causes the Inter-Processor Interrupt Status register to be updated for the target processor. The Inter-Processor Interrupt Status register for the target processor reflects the decoded Processor Identification value. For instance, processor A writing a binary 0001_0011 to its IPI register causes Processor Identification bit 3 to be set in Processor B Interrupt Status register. Note that the processor that originated the interrupt is not evident by the value in the Inter-Processor Interrupt Status Register.

Since the Inter-Processor interrupts are latched, the target processor application must clear these interrupts by writing to the appropriate Inter-Processor Interrupt Status (IPIS) register. For the example described above, processor B receives an interrupt from processor A, with a status value reflecting INT3 asserted in the Inter-Processor Interrupt Status register. The user must write a one to this bit to clear the interrupt.

TABLE 1.3: Inter-Processor Interrupt Generation Register

		Processor Identification Bits			Interrupt Identification Bits		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Not Used	Not Used						

Processor Identification Bits (5:3)	Definition
000	Reserved
001	Interrupt Processor A
010	Interrupt Processor B
011	Interrupt Processor C
100	Interrupt Processor D
101	Interrupt Processor E
110	Reserved
111	Interrupt Processors A, B, C, D, E
Interrupt Identification Bits (2:0)	**Definition**
000	Interrupt # 0 (INT0) is passed to the target processor
001	Interrupt # 1 (INT1) is passed to the target processor
010	Interrupt # 2 (INT2) is passed to the target processor
011	Interrupt # 3 (INT3) is passed to the target processor
100	Interrupt # 4 (INT4) is passed to the target processor
101	Interrupt # 5 (INT5) is passed to the target processor
110	Interrupt # 6 (INT6) is passed to the target processor
111	Interrupt # 7 (INT7) is passed to the target processor

Semaphore Registers

Note

Register information is provided for reference only. Use the BSL functions to manipulate the semaphore registers.

There are sixteen 16-bit semaphore registers in the cOBIC. Any of the five processors may clear the semaphore by writing 0x0000. Any of the five processors may claim the semaphore by writing a non-zero value. However, the write will be ignored unless the semaphore value is 0x0000 prior to the write. Thus, once a processor has written a non-zero value, no other writes are allowed except a write of 0x0000. This functionality ensures that only one device will own the semaphore at a time and that any device is able to clear the semaphore.

This scheme is backwards compatible with earlier software which writes a zero to bit 7 to clear the register and cannot write to the register unless bit 7 of the register is a zero, and the present write has bit 7 = 1.

These semaphore registers are typically used to coordinate the sharing of hardware resources between multiple tasks. The hardware solution provides a faster alternative to traditional software/memory techniques and avoids the use of shared memory and PCI buses to access the semaphores.

TABLE 1.4: Semaphore Register Format

15	14	13	12	11	10	9	8
Semaphore owned tag	Semaphore owned tag	Semaphore owned tag	Semaphore owned tag	Semaphore owned tag	Semaphore owned tag	Semaphore owned tag	Semaphore owned tag

7	6	5	4	3	2	1	0
Semaphore owned tag	Semaphore owned tag	Semaphore owned tag	Semaphore owned tag	Semaphore owned tag	Semaphore owned tag	Semaphore owned tag	Semaphore owned tag

Avionics Style Watchdog Timer

The Compact CHAMP-AV IV provides five watchdog timers, one for each processor. Each watchdog timer is a presettable up counter with a resolution of approximately 970 ns. Time-out periods from 1 µs to 16 seconds can be programmed. Initialization software can select whether a watchdog exception event causes an interrupt, a local processor reset, or a card reset. The watchdog can be locked so that once enabled to cause a reset, the watchdog cannot be disabled.

The watchdog timer can be used in two ways. As a standard watchdog timer, a single time period is programmed which defines a maximum interval between writes to the watchdog register. For increased system integrity, the watchdog can optionally be configured to operate in "Avionics" mode whereby a minimum interval between writes to the watchdog register is also enforced. In other words, writing to the watchdog register too soon or too late causes an exception event. If a fault occurs the timer is stopped.

The following resources are provided for each Watchdog Timer:

- 24-bit Minimum timer
- 24-bit Maximum timer
- Watchdog Enable bit
- Watchdog "Kick" register

Each timer has a 24-bit minimum and a 24-bit maximum read/write register (see the CHAMPtools Software User's Manual). If the watchdog is kicked (by writing to the Watchdog Kick Register) before the minimum timer expires, or if it is not kicked before the maximum timer expires, a fault is generated. A fault can be selected to cause a reset of the processor associated with that watchdog, a board reset, or an interrupt to any of the four processors. Each watchdog timer is enabled by setting the WDT_EN bit in its associated control register (see the CHAMPtools Software User's Manual). If a fault occurs, the watchdog timer is halted. Also, the minimum and maximum registers may be locked by setting the WDT_LOCK bit in the associated control register.

A reset of the associated processor will generate an active LOW pulse (3.84us wide) on CPX_RESET_, where X = A, B, C, D, or E. It will also reset the minimum and maximum registers to their default values. A board reset will hold BB_RESET_ in a LOW state until FPGA_RST_ is received or the watchdog timer is disabled by clearing WDT_EN. An interrupt will be held until WDT_EN is cleared.

As an example, let's say you wanted to set up the watchdog timer so that the software could kick it between 5ms and 12ms without generating a fault. Thus, a fault would be generated if software kicked it less than 5ms or more than 12ms following the previous kick or from the original start. When a fault occurs, you want the processor associated with that watchdog timer to be reset.

To set-up this scenario, first clear the WDT_EN bit in the Watchdog Control Register. This disables the watchdog timer. Then set the WDT_RST_EN bit in the Watchdog Control Register to allow a reset of the processor if a fault occurs. Then write 0x0000_3053 to the Watchdog Maximum Register and 0x0000_1423 to the Watchdog Minimum Register. To enable the watchdog timer, set the WDT_EN bit.

As another example, suppose you wanted an interrupt generated on a fault instead of a reset. This is accomplished by setting the associated bit in the Mask3 register. A watchdog timer fault will then generate an interrupt. At this point, the watchdog timer will halt. To clear the interrupt, clear the WDT_EN bit.

General Purpose I/O and Interrupt Inputs

The Compact CHAMP-AV IV provides eight additional general purpose LVTTL I/O lines which are accessible at the J4 connector. The GPIO signals may be configured individually to be inputs or outputs. Outputs may be configured to be open drain or LVTTL. Each signal is pulled up to 3.3V through a 4.7 K. pull-up resistor. Note that 3.3V LVTTL is interoperable with 5V TTL logic.

Two of the GPIO lines may be configured to act as interrupt inputs, either edge or level sensitive. This flexibility can save a user from building custom logic to condition signals to be used as interrupt sources.

Note

At the present time there is no support in the Board Support Library for these General Purpose I/O and Interrupt inputs.

General Board Support

The General Board Support module provides the features below:

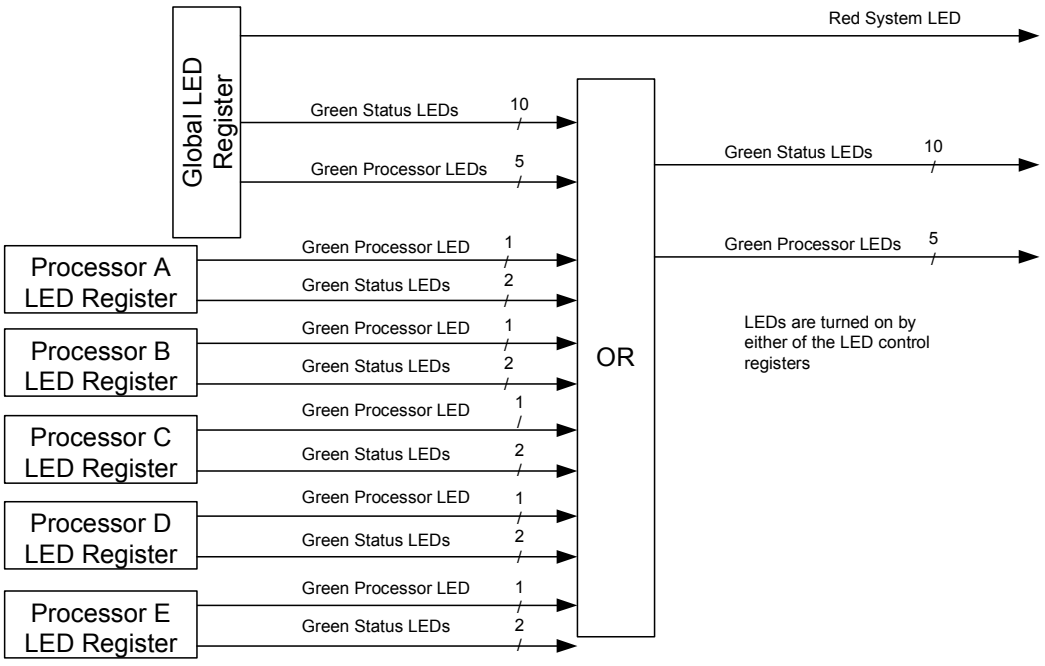
- Readable and writable test registers to facilitate Discovery device interface testing
- Processor ID information associated with each Discovery device interface
- cOBIC Device Revision Register
- Global LED control registers
- Local LED control registers
- Jumper status information read from eight input pins
- Software controlled independent processor resets included with a standard board reset

Indicator LEDs

The Compact CHAMP-AV IV provides fifteen user-controllable LEDs. Five of these are the green processor status LEDs, which are visible on the front panel of the air-cooled version, and ten more are surface mount LEDs located on the back of the board (see Figure 1.9 on page 1-22). All of the Compact CHAMP-AV IV surface mount LEDs can be controlled by any of the processors writing to the Global LED register. Further, each of the processors has a processor LED register that controls the green processor status LED and two of the surface mount status LEDs. See Figure 1.6 on page 1-16 for additional information.

There is an additional red LED on the front panel used to indicate a failure determined by the on-board diagnostic firmware.

FIGURE 1.6: LED Control



COMPACT PCI INTERFACE

The Compact CHAMP-AV IV does not have an interface to the Compact PCI backplane. The only signals on J1 and J2 that are used are reset, BDSEL, HEALTHY# and geographical addressing.

SERIAL PORTS

The Compact CHAMP-AV IV provides two EIA-232 asynchronous serial ports, one on Node A and the other on Node E. The serial port for Node A is implemented using the Discovery III Multi Protocol Serial Controller (MPSC), while the serial port for Node E is implemented in the 8540. On-board EIA-232 transceivers are used to convert the electrical signals between EIA-232 and LVTTL levels.

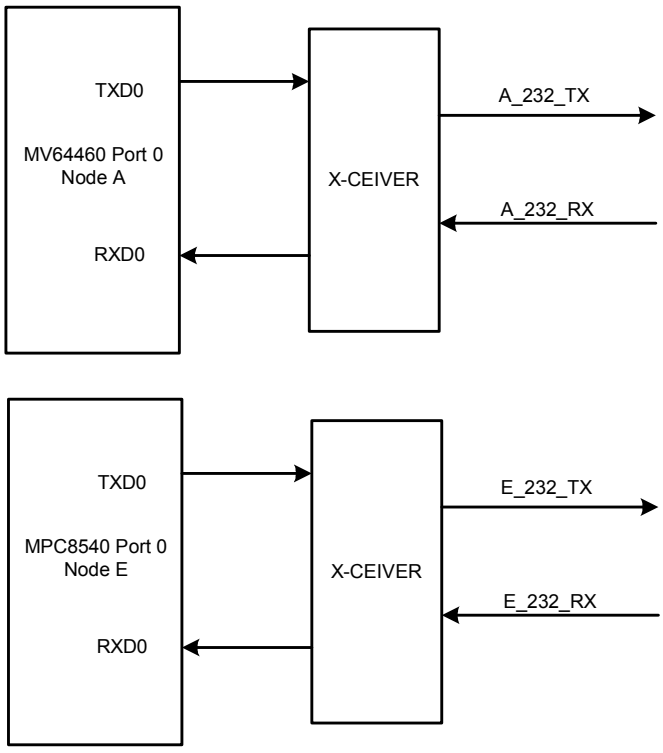
TABLE 1.5: Serial Port Summary

PORT	SIGNAL NAME	FUNCTION
Node A, Serial Port 0	A_232_TX	Transmit Data
	A_232_RX	Receive Data
Node E, Serial Port 0	E_232_TX	Transmit Data
	E_232_RX	Receive Data

Nodes A and E, Serial Port 0 (EIA-232 Asynchronous Mode)

Figure 1.7 illustrates the signal names and direction (input or output) associated with Serial Port 0 on Nodes A and E.

FIGURE 1.7: Nodes A and E, Serial Port 0 (EIA-232 Asynchronous Mode)



ETHERNET INTERFACES

The Compact CHAMP-AV IV has five Gigabit Ethernet interfaces, one per processor.

Processors A-D (MPC7447A/7448) use the Gigabit Ethernet MAC located in their associated MV64660 (Discovery III) bridge. There are two Ethernet interfaces per Discovery III, Ethernet 0 and Ethernet 1. Only Ethernet 0 is used. The Discovery III bridge implements a number of features that are designed to minimize processor loading due to Ethernet traffic. These include dedicated DMA engines, support for Jumbo packets up to 9 Kbytes, automatic retransmission following a collision, efficient buffer management schemes and checksum calculations for TCP, IP and UDP.

The Gig-E interface for each processor is physically connected to a Marvell MV88E1145 Quad Gigabit Ethernet Physical layer device (Quad-PHY). Each processor also has a management interface to the Quad-PHY to control the device and read status. The MV88E1145 has a number of useful features such as auto-negotiation, MDI/MDIX crossover and polarity reversal. Auto-negotiation enables the Ethernet interface to negotiate to highest speed (10/100/1000 Mbps) supported by all devices on an Ethernet segment. The Quad-PHY can automatically determine whether or not it needs to cross over between pairs so that an external crossover cable is not required. The Quad-PHY also detects and corrects for polarity reversal on receive pairs in 1000Base-T and 10Base-T modes, in 100Base-T polarity reversal does not matter. Each Discovery III uses an RGMII (Reduced Gigabit Media Independent Interface) to transfer data between itself and the Quad-PHY.

Processor E (MPC8540) uses its internal Gigabit Ethernet MAC interface. The 8540 Ethernet controller also implements a number of features that are designed to minimize processor loading due to Ethernet traffic. These include dedicated DMA engines, automatic retransmission following a collision, efficient buffer management schemes and checksum calculations for TCP, IP and UDP.

The MPC8540 Gig-E interface is physically connected to a Marvell MV88E1111 Gigabit Ethernet Physical layer device (PHY). The 8540 also has a management interface to the PHY to control the device and read status. The MV88E1111 is a one channel version of the MV88E1145 and has similar features. The MPC8540 uses a GMII (Gigabit Media Independent Interface) to transfer data between itself and the PHY.

POWER

The Compact CHAMP-AV IV has the following power distribution/monitoring capabilities:

- Power monitoring of backplane 3.3 and 5 Volts: If a low voltage condition is detected on either of the backplane voltages, then the on-board power planes will be disabled. The cPCI interface power is not disabled.
- Power sequencing: 5V, 3.3V and all on-board power supply outputs are sequenced to protect components. They power up at the same time as the backplane power.
- The Compact CHAMP-AV IV includes monitoring circuitry that activates board reset upon the following conditions:
  - Low voltage condition (all on-board power rails are monitored)
  - Power up
  - Front panel reset
  - Software generated reset
  - cPCI system reset

RESET

The Compact CHAMP-AV IV has the following reset capabilities:

- front panel reset button
- capability to be reset via software (front panel reset emulation)
- J4 reset pin (PBRST on J4 Row D pin 1). Grounding this pin is equivalent to activating the front panel reset.
- Individual processor reset through the Boot Monitor.
- cPCI system reset

TIMERS

The Compact CHAMP-AV IV board provides a large number of timing resources to facilitate precise timing and control of system events. A list of available timers is given in Table 1.5 below.

TABLE 1.6: Timing Resources

Timer Facility	Implementation	Type	Size	Tick Rate / Period	Maximum Duration
PowerPC	CPU	Free-running counter	64 bit	33.25 MHz / 30 ns (at 133 MHz Bus Speed)	17,548 years
Time Base Register	**Implementation**	**Type**	**Size**	**Tick Rate / Period**	**Maximum Duration**
PowerPC	CPU	Presettable, readable (counts up)	32 bit	33.25 MHz / 30 ns	128.8 seconds
Decrementers	**Implementation**	**Type**	**Size**	**Tick Rate / Period**	**Maximum Duration**
General Purpose # 0-3	Discovery III	Presettable, readable (counts down)	32 bit	125.0 MHz / 8 ns	34.3 seconds
Watchdog Timers (one per CPU)	cOBIC (FPGA)	Presettable, readable (counts down)	24 bit	1 MHz / 1 µS	16.7 seconds

TEMPERATURE/VOLTAGE SENSORS

The Compact CHAMP-AV IV provides sensors to monitor board temperatures and voltage levels. The sensors allow six temperatures and six voltages to be measured. The sensors can generate an interrupt based on programmable high and low voltage and temperature thresholds. The Board Support Library functions will allow the user to read the sensors at any time and to program the sensor's threshold values.

The Compact CHAMP-AV IV has two temperature/voltage sensor Integrated Circuits (ICs) installed on the back of the board (Maxim MAX6656). The ICs are located at locations U225 and U229 (see Figure 1.9 on page 1-22). In revision A of the Compact AV-IV baseboard, the sensors are connected to Node A of the Discovery III bridge. In revision B (and later) of the Compact AV-IV baseboard, the sensors are connected to both Node A of the Discovery III bridge, as well as to the MPC8540. Each sensor IC is capable of measuring three temperatures, one local temperature and two remote temperatures. The local temperature is the temperature of the card at the IC's location. The remote temperatures are the die temperatures of the 7448/7447A PowerPC processors. Sensor U225 can measure its own temperature and the die temperature of processors A and D. Sensor U229 can measure its own temperature and the die temperature of processors B and C. The local and remote

temperature sensors can measure temperatures in the range of -55 °C to 125 °C and have an accuracy of approximately ±3 °C over the temperature range of 0 °C to 100 °C. The temperatures are digitized with 11-bit resolution providing a resolution of 0.125 °C. The conversion time for a single measurement is 125 ms typical and 155 ms max.

Each sensor can measure three voltages. Sensor U229 measures the following voltages: 5 V (voltage supplied to PMC1), 3.3 V, and 2.5 V. Sensor U225 measures the following voltages: 5 V (voltage supplied to PMC2), 3.3 V, and 1.8 V. The voltage accuracy is 1.5% over the range of 30% to 120% of its nominal value. The voltage is digitized with 8-bit resolution. The conversion time for a single measurement is 62.5 ms typical.

Each sensor has an open-drain SMBus ALERT output that is connected to the cOBIC (see Figure 1.4 on page 1-10). The cOBIC treats these signals as interrupt sources. The ALERT interrupts are generated in response to one or more of the following conditions: High or Low Temperature or High or Low Voltage. Once the ALERT interrupt is asserted, it remains asserted (latched) until it is cleared through software. Each sensor has twelve programmable ALERT thresholds consisting of a high and low threshold for each temperature sensor and each voltage sensor.

Each sensor has an open-drain over-temperature OVERT output. The OVERT output from both sensors are wire-ored together and connected to the on-board power control circuitry. If either sensor's OVERT output is asserted, the on-board power control circuitry will turn off the on-board power and the power will remain off until the backplane power is cycled. The OVERT signal is only asserted in response to a High Temperature condition. Each sensor has three programmable OVERT thresholds consisting of a high temperature threshold for each sensor. The default threshold temperature is 127 °C. The OVERT feature is designed to help prevent or minimize board damage in the event of a catastrophic over temperature condition. During normal operation, the board temperatures will never approach 127° C.

COP INTERFACE

The Compact CHAMP-AV IV COP signals utilize 3.3 V signaling and are available on the J4 connector. When connecting an emulator to these signals, the emulator must be configured for 3.3 V signaling. The COP interface is accessible via the:

Warning

Improper connection of the emulator can damage the Compact CHAMP-AV IV board and/or the emulator. Observe orientation indicators on the emulator header. Only 3.3V signaling is supported.

PHYSICAL CHARACTERISTICS

Figure 1.8 shows the location of the major components and the mating connectors on the top side of the Compact CHAMP-AV IV.

All ruggedization levels of the board have a thermal shunt that covers some of the components.

FIGURE 1.8: Compact CHAMP-AV IV Board Layout

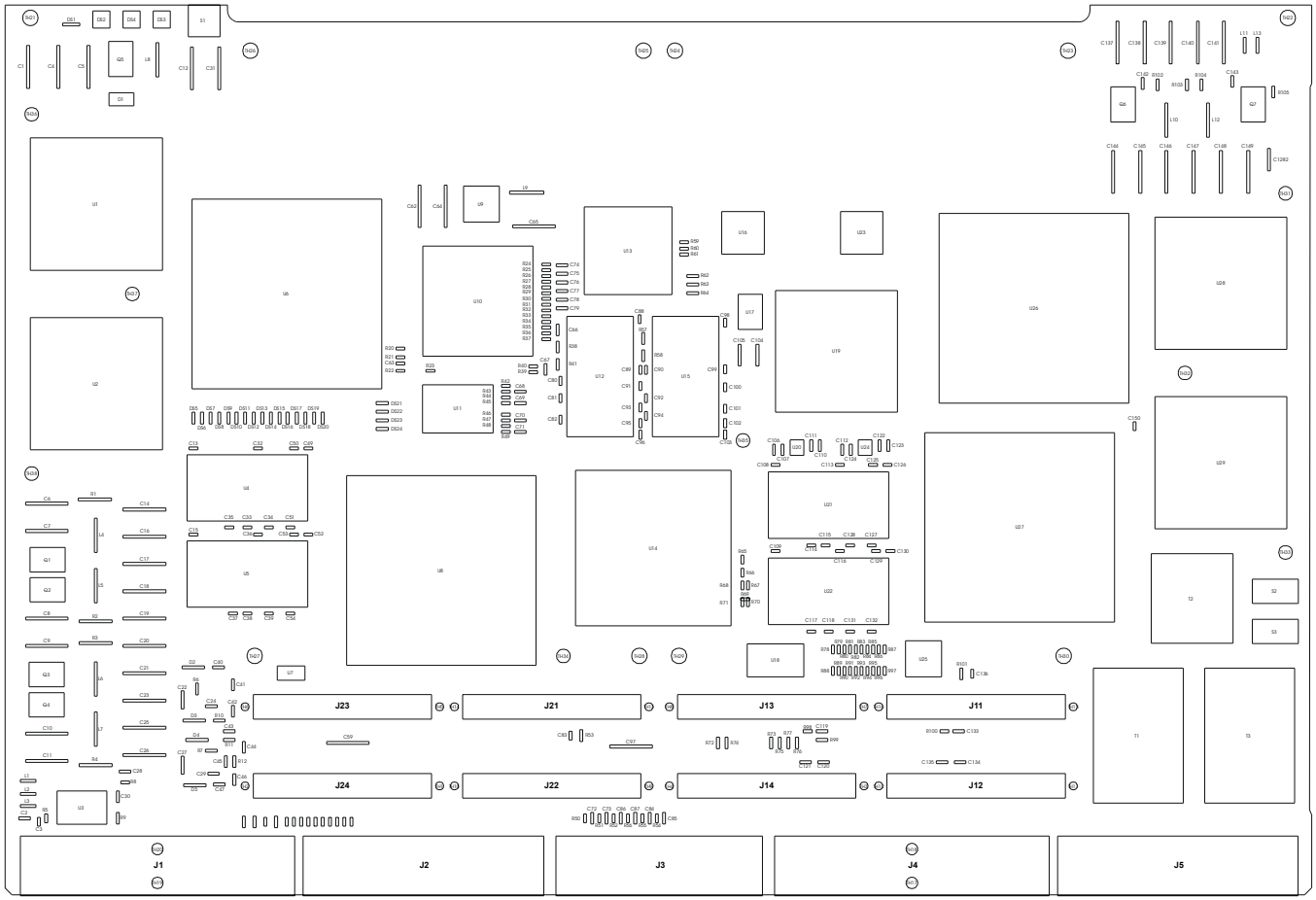
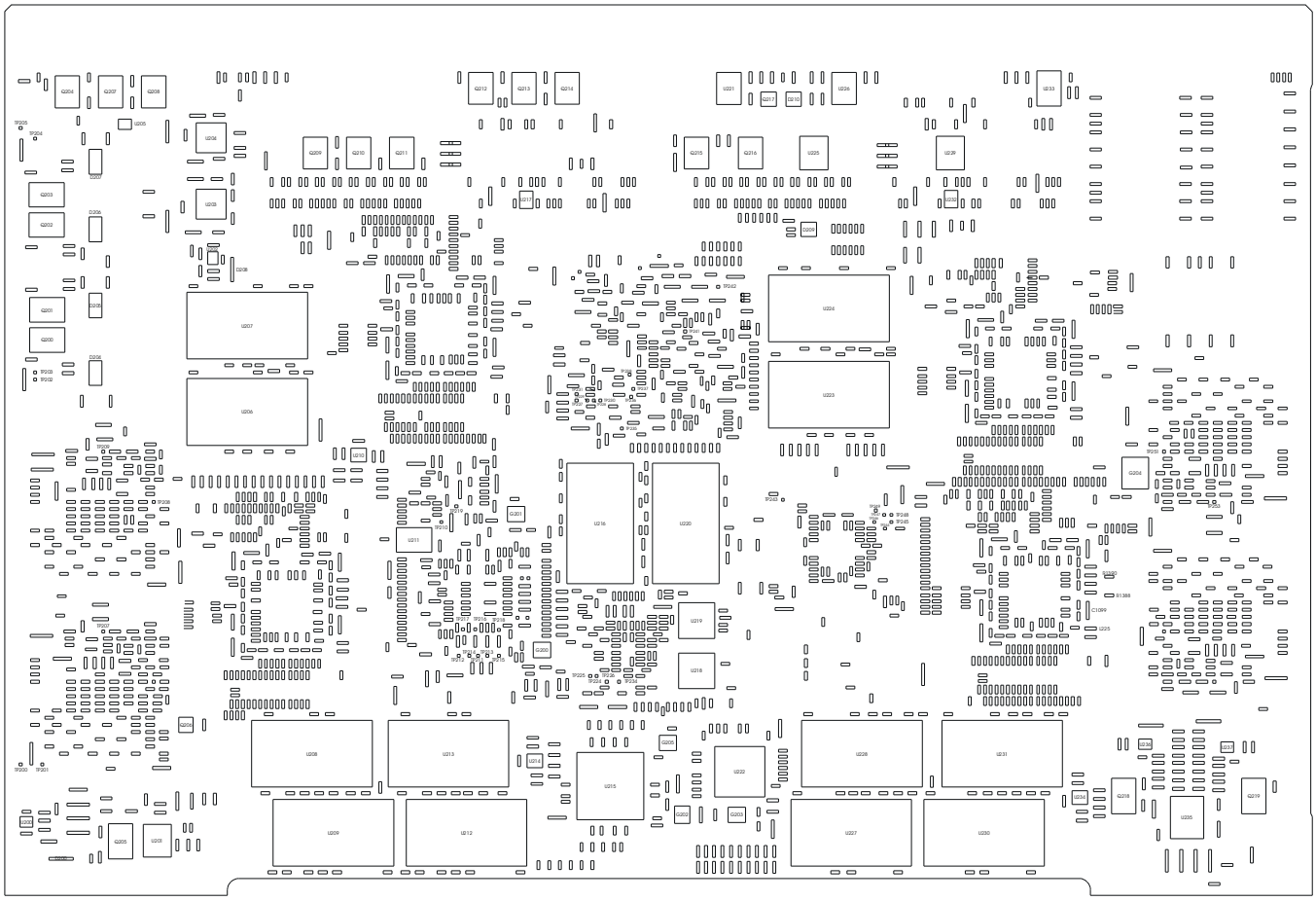
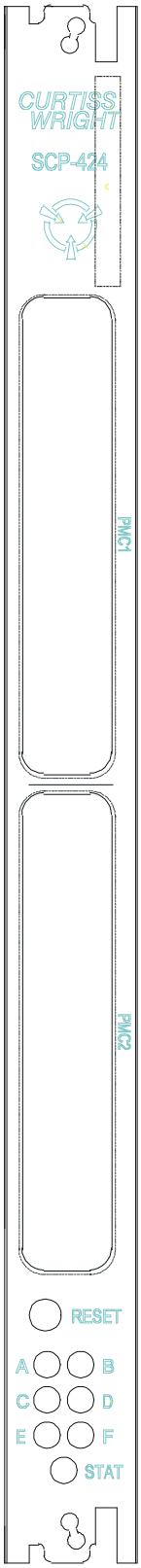


FIGURE 1.9: Bottom View of Compact CHAMP-AV IV PWB



SCP-424 Front Panel

An illustration showing the front panel that is mounted on the Compact CHAMP-AV IV (also known as the SCP-424) is provided below, along with a brief description of the indicators and connectors it provides.



PMC Slots: Two openings are provided on the SCP-424 front panel to provide access to connectors that may be incorporated on optional PMC modules that may be installed on the basecard PWB. If there are no PMC modules mounted, the openings are filled with bezels.

Reset Pushbutton: This button can be used to initiate a card reset.

Processor Status LEDs A, B, C, D, E: Each of the processors has a processor LED register that controls the green processor status LEDs seen opposite and two of the surface mount status LEDs on the PWB.

F LED: The F LED is the red Fail LED, used to indicate a failure determined by the on-board diagnostic firmware.

STAT LED: The STAT LED on the front panel is the blue "hot swap event LED".

MATING CONNECTORS

Table 1.7 summarizes these connectors, providing a brief description and an indication of what functions/interfaces are supported by each.

TABLE 1.7: Summary of Compact CHAMP-AV IV Connectors, Functions Supported

Connector Designation	Description	Supported I/O Configurations
J11, J12, J13, J14	connectors for PMC module site 1, compliant with IEEE P1386.	Connectors used for interconnection with optional 32-bit or 64-bit PMC module. All 64 PMC module site 1 I/O signals are accessible via the basecard P0 connector.
J21, J22, J23, J24	connectors for PMC module site 2, compliant with IEEE P1386.	Connectors used for interconnection with optional 32-bit or 64-bit PMC module. All 64 PMC module site 2 I/O signals are accessible via the basecard P2 connector, rows A and C.
J3	95 pin, 5 x 19 2mm connector.	PMC Site 2 I/O signals, Gigabit Ethernet interfaces forn processors A and B.
J4	125 pin, 5 x 25, 2mm connector.	Gigabit Ethernet interfaces for processors C, D, and E; GPIO signals, PowerPC COP emulator interface signals.
J5	110 pin, 5 x 22, 2mm connector.	PMC Site 1 I/O signals, EIA-232 serial ports for Nodes A and E.

Cross Reference

For complete descriptions of all the basecard mating connectors, including detailed pinout listings and electrical characteristics of signals, refer to Appendix A of this manual.

Tip

The Technical Documentation CD-ROM includes a pinout configurator utility. This 32-bit Windows utility generates the P0 and P2 pinouts based on the I/O configuration of the Compact CHAMP-AV IV and the PMC modules installed on it.

DIMENSIONS

Table 1.8 lists the physical dimensions of the Compact CHAMP-AV IV.

TABLE 1.8: Compact CHAMP-AV IV Dimensions

Parameter	Dimensions
Height	233.2 mm (9.181 in.)
Depth	159.8 mm (6.293 in.)
PWB Thickness	1.63 mm (0.064 in.)

WEIGHT

Table 1.9 lists the weight of the Compact CHAMP-AV IV.

TABLE 1.9: Compact CHAMP-AV IV Weight

Card Type	Weight
Compact CHAMP-AV IV	(est. 1.3 lbs - TBD)

OVERVIEW OF AVAILABLE SOFTWARE

The following sections outline the various software components associated with the Compact CHAMP-AV IV:

BUILT IN TEST (BIT) FIRMWARE

The Compact CHAMP-AV IV hosts a firmware package that performs both board initialization as well as Power-up Built-In Test (PBIT). PBIT consists of a set of essential tests that provide confidence that the hardware is operating correctly, as well as test sequencing which is stored in Flash memory and is tailorable.

Cross Reference

For more information see the "PBIT Diagnostic Tool" section of the CHAMPtools Software User's Manual, as well as the CHAMPtools IBIT/CBIT User's Manual.

OPERATING SYSTEM SOFTWARE

The Compact CHAMP-AV IV is supported with an extensive array of software items, which cover all facets of developing application code for the board. Users have the option of choosing to develop with a variety of operating systems and development tools. The following operating systems are supported on the Compact CHAMP-AV IV:

- A VxWorks Board Support Package (BSP) is available with support for the Tornado development environment. The BSP supports the VxWorks Shared Memory Networking feature. This allows the user to share a single network connection between multiple processors. In development, users can connect to a single Ethernet port, and then make TCP/IP connections to any processor in the system. For deployed systems, the shared network is especially beneficial as only a single Ethernet port must be cabled in the chassis to support in-system upgrades of software.
- A monolithic (no operating system) runtime environment.

OPTIMIZED DSP LIBRARIES

Several DSP processing options are provided.

IXLibs-AV is a library of fully optimized DSP functions that take advantage of the AltiVec instruction unit. By using IXLibs-AV the user is spared the complexity of programming the Altivec instruction unit. For customers with AltiVec expertise, the library includes assembly language macros and an open vector data storage format to support the mixing of user and library functions in an application. See the IXLibs-AV data sheet for detailed information.

VSI/Pro (a VSIPL-compliant library) is available from Verari Systems.

Scientific Subroutine Library is an SAL (Scientific Algorithm Library)-compliant package that also features support for Standard Math (legacy) libraries.

SOFTWARE DEVELOPMENT TOOLS

An extensive array of software development tools, utilities and libraries is available to aid in software development. Some of these utilities are listed below:

Board Support Library

The Board Support Library contains C functions to access hardware features of the Compact CHAMP-AV IV, such as interrupts, semaphores, VME, Flash read/write, Watchdog Timer, Multiboard Synchronization Timer, indicator LEDs, etc..

The Board Support Library is self-contained code that be can used with or without an operating system.

Cross Reference

For additional information about the Board Support Library functions, please refer to the CHAMPtools Software User's Manual, which provides a table of all Board Support Library functions.

Software Update Utility

The Software Update Utility is a Windows program that communicates with the Compact CHAMP-AV IV board through the Ethernet port. It is used to display and modify board configuration information, upgrade board software, and load application code.

Wind River Systems Vision Probe II, Wind Power ICE Emulators

The Compact CHAMP-AV IV supports the use of the Wind Power ICE emulator (or equivalent) via COP signals which are presented on the backplane connectors.

2 PRE-INSTALLATION TASKS

IN THIS CHAPTER...

This chapter discusses the following topics:

UNPACKING THE CARD

Warning

To avoid personal injury or damage to this Circuit Card Assembly, disconnect the chassis from its power source before removing or installing any cards.

This Circuit Card Assembly uses components that are sensitive to electrostatic discharges. It must be kept sealed in its conductive package until just before you install it. Remove the card from its protective package only at a grounded workstation while wearing an approved grounding wrist strap. Avoid touching any metal contacts on the card. Static discharges can damage integrated circuits.

To unpack the card from its protective package, follow these steps:

1. Unpack the Circuit Card Assembly from the shipping carton in a suitable work area. If the shipping carton appears to be damaged, request that an agent of the shipper or carrier be present during unpacking and inspection.
2. Find the packing list. Make sure all the items on the list are present.
3. Save the packing material for storing or reshipping the card.
4. If your Compact CHAMP-AV IV was shipped with PMC modules installed, make sure they are firmly attached to the basecard.

CHECKING HARDWARE REQUIREMENTS

Make sure the various hardware requirements summarized beginning on page 2-2 have been met before you install the Compact CHAMP-AV IV.

CHASSIS REQUIREMENTS

The SCP-424 is a PCIMG 2.16 compliant card that is designed to be used in a PICMG 2.16 or standard cPCI backplane.

Cross Reference

Refer to the Ruggedization Guidelines data sheet (included on the Technical Documentation CD-ROM and also available on www.dy4.com) for more information.

POWER REQUIREMENTS

The Compact CHAMP-AV IV requires +5 V and +3.3 V power supplies in order to operate. Table 2.1 shows the power requirements for the Compact CHAMP-AV IV.

TABLE 2.1: Power Requirements

Voltage	7447A, 1.1 V core, 1064 MHz		7447A, 1.0 V core, 998 MHz		7448, 1.0 V core, 1000 MHz	
	Typical Power (see Note 1)	Maximum Power (see Note 2)	Typical Power (see Note 1)	Maximum Power	Typical Power (see Note 3)	Maximum Power (see Note 3)
Total	64.9	77.1	54.7	TBD	TBD	TBD
+5 V	34.5	52.3	24.6	TBD	TBD	TBD
+3.3 V	30.4	24.8	30.1	TBD	TBD	TBD
+12 V	(see Note 4)	(see Note 4)	(see Note 4)	(see Note 4)	(see Note 4)	(see Note 4)
-12 V	(see Note 4)	(see Note 4)	(see Note 4)	(see Note 4)	(see Note 4)	(see Note 4)

Notes:

1. Power Dissipation is dependant on the application executed by the processors. The values in this column were measured from a board running a stress test designed to emulate a typical user's application under fairly heavy load. For more information, please consult technical support. Values measured at 25°C ambient.
2. Power Dissipation is dependant on the application executed by the processors. The values in this column were measured from a board running a stress test designed to draw the maximum current. For more information, please consult technical support. Values measured at 25°C ambient.
3. Values available 1Q06.
4. The ± 12V supplies are not used by the Compact CHAMP-AV IV circuitry, however they are routed to the PMC sites on the board, therefore the current drawn from these supplies is PMC module-dependent.

The voltage tolerances and power requirements for each supply are summarized in Table 2.2. Missing or below-level voltages will cause the power detection circuitry on the board to hold the board in a powered down state. The power detection circuitry does not monitor the 12V supplies since these power rails are used only to provide +/-12V to the PMC sites (no on-board circuitry uses these voltages).

In order to ensure proper operation of the Compact CHAMP-AV IV board, the remote voltage sense lines for the 5V and 3.3V power must be connected from the power supplies to the voltage rails on the backplane. Chassis units (with built in power supplies) furnished by most vendors should already have these lines connected. However, if the chassis is powered from a user-supplied power source, these lines must be connected. Consult the power supply user manual if you have questions concerning the proper connection of these lines.

TABLE 2.2: cPCI Voltage Specifications

Power Supply	Required Tolerance
+5 V	4.75 to 5.25 V
+3.3 V	3.00 to 3.60 V
+12 V	11.4 V to 12.6 V
-12 V	-13.2 V to -11.8 V

Caution

5V and 3.3 V power must be supplied to the board through the cPCI backplane.

The cPCI chassis power supplies must be properly sized for the system and must utilize remote backplane sensing to properly regulate the backplane voltages.

FLASH CONFIGURATION PARAMETERS

The on-board Flash contains configuration parameters that are used to configure certain features of the board. These parameters are explained in the CHAMPtools Software User's Manual. As explained in the CHAMPtools manual, the Software Update Utility or Boot Monitor can be used to modify these parameters. For initial power-up of the board, there should be no need to modify these parameters.

PMC/PMC-X MODULE INSTALLATION REQUIREMENTS

The Compact CHAMP-AV IV provides two PCI/PCI-X Mezzanine Card (PMC/PMC-X) sites: PMC Site 1 and PMC site 2. PMC Site 1 is located between Nodes A and D while PMC Site 2 is located between Nodes B and C. See Figure 1.8 on page 1-21 for an illustration of the Compact CHAMP-AV IV board layout. Each PMC site can be independently configured at the factory to support either 3.3V or 5V signaling on their PCI bus.

The PMC sites are designed to conform to the following specifications:

- PCI Local Bus Specification, PCI-SIG, Revision 2.3, March 29, 2002
- Draft Processor PMC Standard For Processor PCI Mezzanine Cards, VITA 32-2003, Rev. 1.0a; April 29, 2003
- IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC), IEEE Std 1386.1-2001, June 14, 2001
- IEEE Standard for a Common Mezzanine Card (CMC) Family, IEEE Std 1386-2001, June 14, 2001
- PCI-X Auxiliary Standard for PMCs and Processor PMCs; VITA39-2002, Draft 0.9a; September 17, 2002.
- PCI-X Electrical and Mechanical Addendum to the PCI Local Bus Specifications, PCI_SIG, Rev. 2.0, Nov. 4, 2002
- PCI-X Protocol Addendum to the PCI Local Bus Specification, PCI-SIG, Rev. 2.0, July 29, 2002

PMC Module Voltage Types

A PMC can be a 3.3V board (uses 3.3V signaling), a 5V board (uses 5V signaling), or a Universal board (auto selects and configures for the signaling level used by the PMC host). Each PMC card is required to have a keying hole to indicate the type of PCI signaling it utilizes. If the PMC's PCI bus utilizes 3.3V PCI signaling, it should provide a 3.3V keying hole. If the PMC's PCI bus utilizes 5V PCI signaling, it should provide a 5V keying hole. If both voltages can be supported, then both keying holes should be provided. Unfortunately, not all PMCs conform to the PMC standard. Figure 2.1 shows the position of the keying holes on a PMC.

When ordering the Compact CHAMP-AV IV board, the I/O signaling voltage must be specified for each PMC site. Each PMC site can be factory configured to support 3.3 V or 5.0 V I/O signaling voltage. When a PMC site is configured for 3.3 V operation, the PMC site will operate properly with a 3.3 V PMC or a Universal PMC. When PMC site is configured for 5.0 V operation, the PMC site will operate properly with a 5.0 V PMC or a Universal PMC. Note that the PMC specification requires all 5.0 V PCI buses to operate at a maximum frequency of 33 MHz.

Warning

Please note that in either the 5V or 3.3V configuration, the Compact CHAMP-AV IV does not provide a keying pin due to board real estate restrictions.

Installing a PMC with incompatible signaling levels can cause permanent damage to the Compact CHAMP-AV IV baseboard as well as the PMC.

Review your PMC module's power requirements carefully to ensure that you do not install an incorrect PMC in a Compact CHAMP-AV IV PMC site.

FIGURE 2.1: Position of 5V and 3.3V Keying Holes on a PMC Board

PMC I/O

The Compact CHAMP-AV IV board supports front panel user I/O and backplane user I/O through the J3 and J5 cPCI bus connectors. The backplane I/O for PMC Site 1 (mounted between Nodes A and D) is routed out the Compact CHAMP-AV IV cPCI bus J5 connector. The backplane I/O for the PMC Site 2 (mounted between Nodes B and C) is routed out the Compact CHAMP-AV IV cPCI J3 connector. Table A.5 on page A-7 and Table A.9 on page A-11 show the backplane I/O connections for PMC sites 1 and 2. The I/O signals are routed differentially (100 ohm differential impedance), as noted in Table A.19 on page A-29 but may also be used in a single-ended mode as seen in Table A.20 on page A-30. The differential routes are provided so that the I/O will support standard PMCs as well as high speed differential PMCs.

PMC BUSMODE Signals

On the Compact CHAMP-AV IV , the PMC BUSMODE[4:2] signals are hardwired and constantly drive the following values in accordance with the Common Mezzanine Card specification: BUSMODE[4:2] = 0b001. This signals the PMC card that it is connected to a PMC site. If the card is a PMC card, it will drive a logic "0" on BUSMODE1 (this signal has been renamed PRESENT# in the PPMC specification and is used to indicate the presence of a PMC card). Note that the Compact CHAMP-AV IV receives the BUSMODE1 signal from each PMC.

PPMC (Processor PMC) and PCI-X Support

In addition to meeting the signaling standards of PMC cards, the Compact CHAMP-AV IV provides support for th PPMC (Processor PMC) standard and the PCI-X standard. The signals used to support these standards are listed in the table below:

TABLE 2.3: PPMC and PCI-X Support

Signal Name	Description
MONARCH#	The MONARCH# signal (Jn2 pin 64) is used to enable or disable the monarch feature on a Processor PMC (PPMC). The PPMC specification defines two states for the MONARCH# signal: float to disable the monarch feature and drive low to enable the monarch feature. Since the Compact CHAMP-AV IV baseboard performs the monarch (PCI enumeration and interrupt) functions for the respective PCI buses, the baseboard allows the MONARCH# signal to float to disable the monarch feature on PPMCs. Standard PMCs (non-PPMC) function properly since the PPMC specification defines an unused PMC pin for the MONARCH# signal.
M66EN	In conventional PCI mode (PCIXCAP grounded), the M66EN signal (Jn2, pin 47) is used to select the PCI bus frequency. If the PMC grounds the signal, 33 MHz operation is selected. If not grounded by the PMC (pulled up on the baseboard) then 66 MHz operation is selected.
PCIXCAP	PCIXCAP (Jn1, pin 39) is a 3-level signal that is utilized to select between conventional PCI (PCI 33 and PCI 66), PCI-X 66, and PCI-X 100. When the PMC grounds PCIXCAP, conventional PCI mode is selected. When the PMC connects PCIXCAP to ground through a 10 KOhm ±5% resistor in parallel with a 0.01 µF ±10% capacitor, PCI-X 66 MHz mode is selected. When the PMC connects PCIXCAP to ground through a 0.01 µF ±10% capacitor, PCI-X 100 MHz mode is selected.
IDSELB	The IDSELB (Jn2 pin 34) is used to select an optional second PCI agent.
REQB#	The REQB# signal (Jn2 pin 52) is a request issued by the optional second PCI agent requesting the ownership of the PCI bus.
GNTB#	The GNTB# signal (Jn2 pin 54) is a grant issued to the optional second PCI agent requesting the ownership of the PCI bus via the corresponding REQB# signal.
RESETOUT#	The RESETOUT# signal (Jn2 pin 60) is an active low, open drain output from the PMC. When asserted by the PMC, the Compact CHAMP-AV IV will perform a board reset (same as pushing the reset switch on the Compact CHAMP-AV IV board).
EREADY	The EREADY signal (Jn2 pin 58) is an open drain output on non-monarch PMCs that indicates the PMC has completed its on-board initialization and can respond to PCI bus enumeration. The Compact CHAMP-AV IV configuration software will not perform enumeration on the respective PMC until the PMC releases this signal.

The Compact CHAMP-AV IV provides support for an optional second PCI Agent. Non-monarch PPMCs may include an optional second PCI agent. The Compact CHAMP-AV IV only supports one load per PMC PCI signal.

Warning

Per the PMC specification, the Compact CHAMP-AV IV only allows a PMC to place one load on each PCI signal. Failure to adhere to this requirement can cause timing violations on the affected signals, resulting in data loss and or corruption.

PMC Module Power Considerations

The Compact CHAMP-AV IV supplies 5V, 3.3V, VIO, +12V, and -12V power to the PMC sites. According to the PMC specification, the maximum power dissipation allowed for each PMC site is 7.5 Watts (see Table 2.4). The Compact CHAMP-AV IV is designed to follow this specification and in some cases, exceed it. Other combinations of PMCs (i.e. an 8 Watt PMC on Site 1, a 7 Watt PMC on Site 2) may be possible.

Caution

Please consult CWCEC technical support before installing a PMC that exceeds the 7.5 Watt PMC standard to determine if it can be safely supported in your specific application and configuration. Depending on the particular application and configuration, various conditions can occur that could adversely affect (and possibly damage) the baseboard, PMC(s), or chassis. These conditions include, but are not limited to: excessive current drawn from the cPCI connectors, excessive heating of baseboard and PMC components, and reduction in board voltages that can cause board resets to occur. Factors affecting this include, but are not limited to: maximum operating temperature of the board (air temperature for air-cooled boards and card edge temperature for conduction-cooled boards), airflow (air-cooled boards), baseboard power dissipation (application specific), total PMC current drawn by both PMC sites from each power supply rail, and the location and density of the hot components on the PMC(s) and/or the baseboard.

The PMC VIO voltage can be factory configured for 5V or 3.3V signaling. Please consult the user's manual for the PMC that will be installed on the baseboard to determine the VIO voltage necessary.

TABLE 2.4: Recommended Maximum Supply Current per PMC Site

Supply	Maximum Supply Current
5 V	1.5 A
3.3 V	2.3 A
+12 V	500 mA
-12 V	100 mA

CONFIGURING SWITCHES

Table 2.5 defines the switches S2[1-4] and S3[1-4] on the Compact CHAMP-AV IV that reside at the rear of the board (see Figure 2.2 on page 2-9). Switches are available for selecting various board operational modes. Switches identified as Reserved must be left in the default setting and only changed under the direction of Customer Support.

Warning

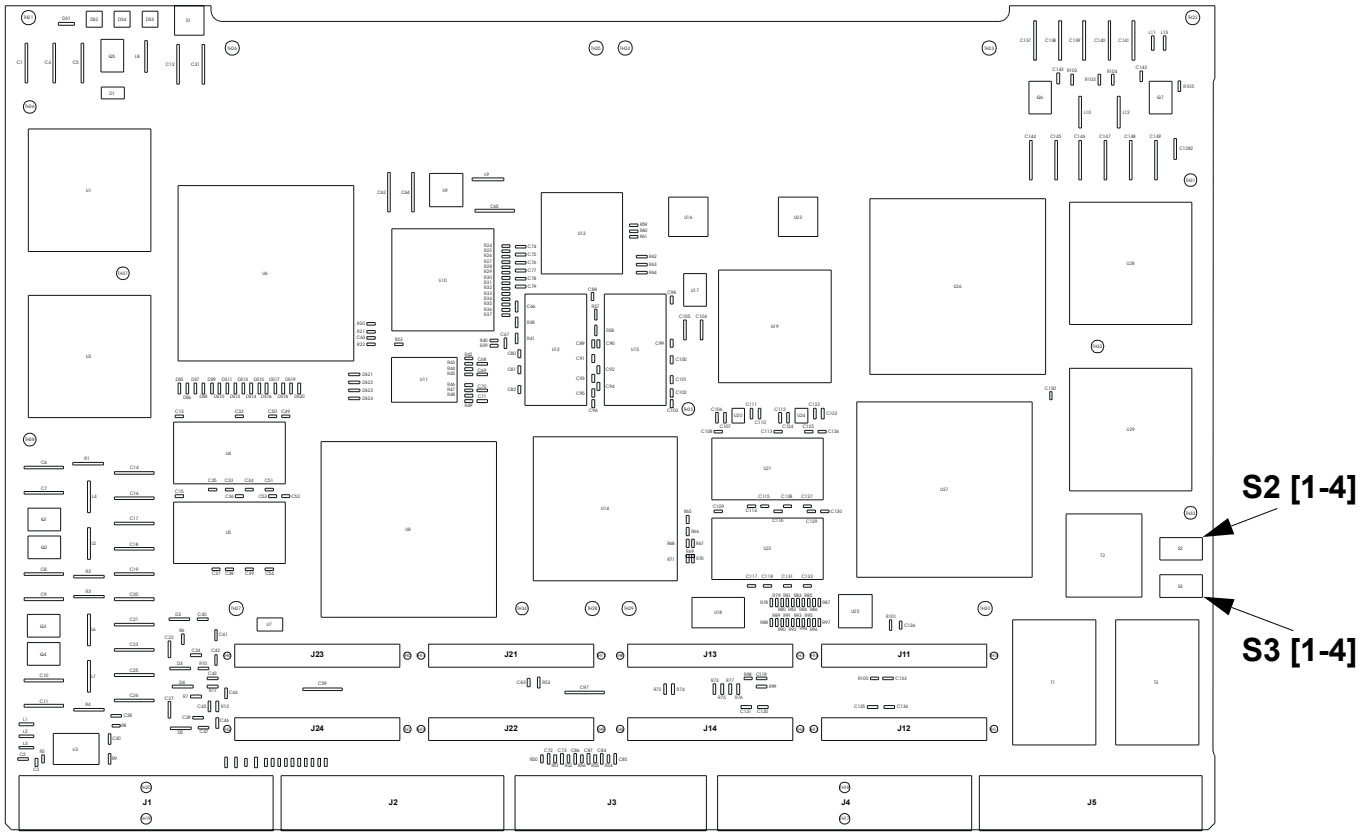
Please make sure that the board is not powered on when configuring board switches and that you observe proper static control procedures when handling the card.

TABLE 2.5: Switch Definition

Switch	On	Off	Default
S2[1] - S2[3]	User-defined. Switches are read by software on the Compact CHAMP-AV IV and left up to the application.		On
S2[4]	Alternate FPGA PROM is used to program FPGA	Main FPGA PROM is used program FPGA	Off
S3[1]	User Defined - readable by applications software	User Defined - readable by applications software	Off
S3[2]	Boot alternate files	Boot primary files	Off
S3[3] & S3[4]	These two switches are used to select the boot mode for the board **(see Note below)**. S3[3] S3[4] Mode Off Off Normal Boot Mode (loads OS or other application) Off On Recovery Mode On Off Boot Inhibit Mode On On Normal Boot Mode with Flash Locked		Off, Off

Note: See the CHAMPtools Software User's Manual for additional information describing the various boot modes.

FIGURE 2.2: Configuration Switch Locations



3 HARDWARE INSTALLATION

IN THIS CHAPTER...

This chapter provides the following information and procedures:

– "Sign-on Message Garbled" on page 3-10

Cross Reference

Please refer to the CHAMPtools Software User's Manual for more detailed information describing the Boot Monitor and the PBIT capabilities.

INSTALLATION PREREQUISITES

Before installing the Compact CHAMP-AV IV in your chassis, please take a moment to review the following items and planning considerations:

INSTALLATION CHECKLIST

Make sure you have the following items before proceeding with the installation:

- the Compact CHAMP-AV IV board
- standard cPCI chassis or PICMG 2.16 cPCI chassis
- DB9 to DB9 serial cable (not provided), attached to a computer with a terminal emulator program capable of operating at 57,600 baud
- a standard Ethernet cable having RJ-45 connectors
- the CHAMPtools CD
- A Rear Transition Module (RTM) or custom cable for the Compact CHAMP-AV IV is required in order to access the Ethernet ports and serial ports directly off the back of the board. CWCEC offers an RTM for the Compact CHAMP-AV IV (CWCEC PN TBD). A custom RTM may be developed as well. If you design your own RTM, please contact CWCEC Technical Support first to make sure that your RTM design is compatible with the Compact CHAMP-AV IV product.

Warning

This card uses components that are sensitive to electrostatic discharges. It must be kept in its conductive package until the installation begins. Remove the card from its protective package only at a grounded workstation while wearing an approved grounding wrist strap. Avoid touching any metal contacts on the card; static discharge can damage integrated circuits.

Turn the power off before inserting or removing cards from the cPCI chassis. Failure to do so could damage the card circuitry or cause personal injury.

UNPACK AND CONFIGURE THE CARD

Ensure that you complete the pre-installation tasks described in Chapter 2 of this manual and the pre-installation tasks described in the User's Manuals for any PMC modules you need to install on the Compact CHAMP-AV IV.

INSTALL THE PMC MODULES ON THE BASECARD

If the PMC modules are not already installed on the basecard, install them in a PMC slot of your basecard using the appropriate CWCEC mounting kits.

When the PMC module is mounted in slot 1 (near the backplane J4 connector), its I/O signals are available on the backplane J5 connector. When the PMC module is mounted in slot 2 (near the backplane J2 connector), its I/O signals are available on the backplane J3 connector.

CHOOSE A CPCI SLOT LOCATION

The Compact CHAMP-AV IV does not support cPCI System Slot capability, therefore it cannot be installed in the System Slot (usually marked off by different color card guides.) Additionally, in a PICMG 2.16 chassis, the Compact CHAMP-AV IV is considered a Node board and must be installed in a PCIMG 2.16 Node slot.

Caution

Ensure that the chassis your Compact CHAMP-AV IV is installed in is capable of generating a minimum of 4 CFM air flow before you apply power to the board.

QUICK INSTALLATION AND POWER UP PROCEDURE

The following steps must be performed to get the Compact CHAMP-AV IV card operational:

1. Move switch, S3[3] to the "ON" position. This position is when the switch is slid towards the upper board edge. It is also marked on the switch itself. This selects Boot Inhibit mode, which prevents the board from loading the operating system, but allows it to interact with the serial port.
2. With power off, install the Compact CHAMP-AV IV into the chassis. Ensure the cPCI connectors are fully engaged.
3. Install CWCEC or custom RTM in the back of the cPCI chassis. The RTM must be installed in the same slot as the Compact CHAMP-AV IV.
4. Connect serial port cable between RTM connector J11 and the PC.
5. Run the terminal emulation program. Set the serial port for 57.6K baud, 8 data bits, no parity, one stop bit, and Xon/Xoff flow control.
6. Apply power to the chassis. The board will initialize, displaying configuration information. The red FAIL LED will be flashing. The green LEDs will come on and then turn off to indicate a successful load of the cOBIC FPGA.
7. Confirm two-way RS-232 communication by entering "help" <CR> on the terminal emulator. This command displays other commands supported by the boot monitor.

If the red LED flashes continuously but no information is displayed, check the serial port configuration parameters and connection. The flashing indicates the board has completed initialization and is in Boot Inhibit mode.

If the red LED fails to flash, the board firmware is unable to complete board initialization. Check board seating, chassis power, and observe any messages displayed via the serial port. If the green LEDs do not turn off, it is possible the cOBIC FPGA has not loaded properly. Power off the card, then move switch S2[4] to the "ON" position, which selects the alternate SPROM (see "Configuring Switches" on page 2-8 for details). Power up the chassis.

If the Quick Installation procedure described above works as expected, you may want to try moving the S3[4] switch to the "OFF" position, then pressing the reset button to enable the Normal Boot Mode, which will prepare the card to boot an OS.

Cross Reference

Please refer to the CHAMPtools Software User's Manual for detailed software installation procedures.

DETAILED INSTALLATION PROCEDURE

INSERT THE BASECARD IN THE CHASSIS

Ensure that the chassis power is turned off before inserting the card.

An SCP basecard is equipped with a faceplate compliant with IEEE 1101.10. The large ejectors on this faceplate facilitate insertion of the basecard into the cPCI chassis.

Once the basecard is inserted in the chassis, secure it by tightening the screws at the top and bottom of the faceplate.

CONNECT A TERMINAL

In order to access the features available within the embedded firmware on the Compact CHAMP-AV IV, you'll need to attach a terminal or PC-emulated equivalent to the Serial Port A interface on the Rear Transition Module (RTM).

Tip

Default serial communication parameters are 57,600 N, 8, 1 (57600 baud, no parity, 8 bits, 1 stop bit). Flow control is via software (xon/xoff).

CONNECT ETHERNET PORT E

Connect Ethernet Port E of the Compact CHAMP-AV IV to your Ethernet LAN via the connector labelled "ENET E" on the RTM.

Cross Reference

Ethernet Port E is used in conjunction with the CHAMPtools Software Update Utility to burn programs into Flash memory on the Compact CHAMP-AV IV. See the CHAMPtools Software User's Manual for additional details.

CABLE CONNECTIONS

The following cables are required by the Compact CHAMP_AV IV board:

- Cat-5/5E Shielded Twisted Pair Ethernet Cable, with RJ-45 connectors on both ends.
- DB-9 Female to DB-9 male serial cable.

These cables may be purchased through most electronics components retailers.

Note

The Compact CHAMP-AV IV EIA-232 serial channels are configured as DCE (Data Communications Equipment). The EIA-232 serial channels on personal computers and terminals are configured as DTE, therefore a null modem is NOT required for communication between the Compact CHAMP-AV IV and a PC terminal.

RUNNING THE BOOT MONITOR

The Boot Monitor is a special embedded program that runs on Processor A after hardware reset. Two copies of the Boot Monitor reside in Flash memory. These are named .bootMon and bootMon2.exe. The secondary boot monitor, bootMon2.exe, is field-upgradeable. This approach allows the secondary boot monitor to be upgraded; errors in the upgrade process can be remedied by reverting to the primary boot monitor.

The Boot Monitor configures all on-board resources and brings the board to an operational state. Once the resources are configured, the application named pbit.exe (PBIT) is executed if it is present. PBIT validates operation of the hardware devices present on the board. After completing initialization with a satisfactory result from PBIT, the Boot Monitor either transitions to an application program (loaded in Flash memory), or interacts with the serial port, accepting and processing maintenance commands. The decision to load and start an application is based on switch settings (see the descriptions of S2[3] and S2[4] found in "Configuring Switches" on page 2-8). By setting the PBIT_IGNORE_ERRORS environment variable, the user can force the board to continue booting, even if PBIT finds an error.

The Boot Monitor has four modes of operation: Normal Mode, Boot Inhibit Mode, Recovery Mode, and Flash Write Protect Mode.

Cross Reference

Please refer to the CHAMPtools Software User's Manual for more detailed information describing the Boot Monitor and the PBIT functions.

An example of the initial screen message you will see once Boot Monitor has run is shown in "Display the Initial Screen Message" on page 3-6.

INITIATE THE POWER-UP SEQUENCE

This section describes the normal power-up behavior of the Compact CHAMP-AV IV.

The Compact CHAMP-AV IV Flash memory is managed by the A processor. As a result, processor A plays a unique role during board boot-up. After power-on or board reset, processor A loads and executes the Boot Monitor program stored in Flash memory. The Boot Monitor has four modes of operation: Normal Mode, Normal Mode with Flash Write Protection, Boot Inhibit Mode, and Recovery Mode. The mode selected is determined by switch settings (see Table 2.5 on page 2-8) and affects the degree of board initialization and startup. Please see the CHAMPtools Software User's Manual for a detailed description of these modes.

The Boot Monitor outputs progress messages through Processor A's rear panel serial port. It also logs these messages in memory for later review. These messages display configuration information, switch settings, and other information regarding the board initialization process.

DISPLAY THE INITIAL SCREEN MESSAGE

After a hardware reset, the Boot Monitor (in Boot Inhibit Mode) will display an initial sign-on message similar to the following:

```
CHAMPtools Boot Monitor Version 3.0000, Feb 18 2005 13:28:41
Copyright, 2002-2004, Dy 4 Systems, Inc.

JMP:     Boot-inhibit mode
Transitioning to bootMon2.exe...


CHAMPtools Boot Monitor Version 3.0000, Feb 18 2005 13:28:41
Copyright, 2002-2004, Dy 4 Systems, Inc.

Board:   Compact CHAMP AV-IV
Board:   rev A.1, s/n 3022232, MAC Address 00:80:7f:64:f0:10
Proc:    PowerPC 7447A,
         1066 MHz core,           PVR 0x80030101,
         HID0 0x8490812c,         Bus 133 MHz
Reset:   Power-Up
SDRAM:   256 MB,
         commercial temp range,   1.937 uS refresh (258 count),
         addr config: 0x00000002, config: 0xd8200102,
         timing hi: 0x0000000a,   timing lo: 0x01502220
Flash:   64MB
L2CR:    0x00001000 (1066 MHz)
OBIC:    OBIC NG revision 0.c
SIO:     Using default options
Bridge:  configuring A
Bridge:  configuring B
Bridge:  configuring C
Bridge:  configuring D
Bridge:  configuring E
PCI:     Bus 0 mode is 64-bit  66MHz PCI
PCI:     Bus 1 mode is 64-bit  66MHz PCI
PCI:     Bus 2 mode is 64-bit  66MHz PCI
PCI:     Bus 3 mode is 64-bit  66MHz PCI
PCI:     Scanning for devices, delay 1000 mS
PBIT:    cannot find pbit.exe; skipped
Boot Inhibit jumper installed
BootMon>
```

Note that in Normal Boot Mode, a similar sign-on message to that shown above will be displayed, followed by the following additional information:

```
Transitioning to bootA.exe...

                            VxWorks System Boot

Copyright 1984-2002  Wind River Systems, Inc.
CPU: Dy4 CompactChamp-AV IV
Version: VxWorks5.5
BSP version: 1.2/4
Creation date: February 20 2004, 15:56:27


Press any key to stop auto-boot...
 7

[VxWorks Boot]:
```

CONFIGURING AN EMULATOR FOR USE WITH COMPACT CHAMP-AV IV

A PowerPC 74xx or 8540 emulator may be used to interact with each processor and the board hardware on the Compact CHAMP-AV IV card. A COP connection is provided on the RTM for this purpose. When connecting an emulator to the RTM, make sure that pin one of the emulator pod aligns with pin one on the RTM connector.

The emulation capabilities of the Compact CHAMP-AV IV with a Wind River Wind Power ICE in combination with the Wind Power IDE software has been tested. Therefore, the information in this section is based on the use of these tools.

The COP connector is shared between the five processors and can be used to control one processor at a time (i.e. the COP connection is multiplexed). The target processor is chosen via the rotary switch on the RTM. Table 3.1 on page 3-9 shows the mapping bewteen the rotary switch and the processor.

Procedure for using the Wind River Emulator

The steps for using the Wind River emulator with the 74xx/8540 processors are outlined below. For other emulators, follow a similar procedure.

1. Turn off the board (chassis) power.
2. Connect to the COP interface of the Compact CHAMP-AV IV via the RTM.
3. Select the processor to emulate via the rotary switch on the RTM.
4. If the target processor is PPC A, configure S3[3] and S3[4] to either of the Normal Boot Modes (S3[3] and S3[4] both Off or both On). Please note that if the board is in Boot Inhibit Mode or Recovery Mode, processors B, C and D are not automatically released from reset (at power-up or board reset) since the startup code does not perform this function for these processors (this is left to the application). With the processors in reset, the emulator will not connect to them. However, if S3[3] and S3[4] are both on or both off, the board will boot application code thereby releasing the processors from reset and allowing emulation. If it is desired to use the emulator with the board in either of the two other modes, the user should contact CWCEC technical support to determine the proper procedure for releasing B, C, and/or D from reset.
5. Disable auto-voltage detection on the emulator and set it for 3.3V. See Chapter 2, Section 7, in the "Wind Power ICE for Wind Power IDE User's Guide". Please contact CWCEC technical support if there are any questions regarding this procedure.
6. Connect the emulator to the RTM.
7. Power up the Compact CHAMP-AV IV board.
8. Run the Wind Power IDE software and follow the procedures outlined in the associated Wind River documentation for opening communication with the emulator.

9. Type "inn" to get into BKM mode (do not type "in" as this command will attempt to initialize the Discovery III bridge).
10. Communication with the board should now be established. Because the "inn" command performs a processor reset, the PC counter of the target processor will be reset to location 0xFFF00100 (the PPC reset vector). Therefore, typing "go" from the BKM prompt without loading a program will cause the processor to lose connection with the emulator.
11. In order to execute user code on any of the processors, load a program into the target using the emulator and then set the PC counter to the start address of the program. To execute the code, type "go".


Warning

Make sure that the signaling level on the emulator pod connected to the COP interface on the Compact CHAMP-AV IV is set to 3.3V. Failure to do so could cause damage to the baseboard or the emulator.

TABLE 3.1: Selection of Target Processor via RTM Rotary Switch

Target Processor	Rotary Switch Position
PowerPC A	1
PowerPC B	2
PowerPC C	3
PowerPC D	4
PowerPC E	5
Serial COP	6
JTAG Mode	7
Reserved	8
Reserved	9

TROUBLESHOOTING

VERIFY INSERTION IN CHASSIS

Power down the chassis. Make sure that the card is properly seated in the cPCI chassis. Because of the five-row backplane, a considerable amount of insertion force is required.

FAIL LED BEHAVIOR

The front panel Fail LED indicates the health of the Compact CHAMP-AV IV board. The illumination pattern of this LED at power-up or reset will differ depending upon the boot mode of the board. If the board is in either of the Normal Boot Modes, the Fail LED will illuminate and stay illuminated until the board is successfully initialized and tested (the power-on self tests will run if they are enabled - see the description of PBIT in the CHAMPtools Software User's Manual).

If there is an error during initialization or testing, the red Fail LED will stay on. If PBIT detects an error, the Fail LED will illuminate but the boot sequence will continue (depending on the setting of the environment variable PBIT_IGNORE_ERRORS), if possible. In Recovery Mode or Boot Inhibit Mode, the Fail LED will turn on and stay on until board initialization and testing is complete. It will then begin to blink (regardless of the success or failure of the power-on self tests) indicating that the card is ready to accept input at the Boot Monitor prompt.

If the green Processor LEDs do not turn off, it is possible the cOBIC FPGA has not loaded properly. Power off the card, then move switch S2[4] to the On position, which selects the alternate SPROM (see Table 2.5 on page 2-8 for details). Power up the chassis.

Please see the CHAMPtools Software User's Manual to determine how to query results of the power-on self test.

If the red Fail LED does not illuminate at power up or board reset, the board has been damaged or one of the required power supply voltages is missing. If this occurs, be sure to check the +3.3V and +5V supplies.

SIGN-ON MESSAGE GARBLED

If the sign-on message is garbled, check that your terminal settings match 57600, 8, N, 1 (57600 baud, 8 data bits, no parity, 1 stop bit). Also, ensure that you are using a compatible serial cable.

THE NEXT STEP

Cross Reference

Once the hardware is correctly configured and installed in the chassis, the next step is to install the CHAMPtools software. See the section "Software Installation" in Chapter 2 of your CHAMPtools Software User's Manual, which is included in Acrobat pdf format on your CHAMPtools CD-ROM.

4 PROGRAMMING INTERFACE

IN THIS CHAPTER...

This chapter contains the following information:

COMPACT CHAMP-AV IV MEMORY MAP

The resources on the Compact CHAMP-AV IV are connected via four unique PCI buses. Since all nodes of the Compact CHAMP-AV IV are connected together by the PCI buses, all memory on the board is globally accessible.

Each processor has a specific view of the board. Differences from one processor's view to the next are due to the fact that each processor views its own memory, bridge, and FPGA port as starting at zero and extending through the first 512 MB of address space, while the PCI address space for these assets never starts at zero. PMC devices will view board resources using the PCI memory map, where all processors start at a nonzero memory address.

Table 4.1 on page 4-3 shows the physical memory maps for all processors, and for PMC-initiated transfers. No device may select itself using its own PCI address space. Entries designated "illegal" result in a PCI transfer error. Unlisted entries also result in errors. The logical address map imposed by an operating system may result in further limitations.

TABLE 4.1: Compact CHAMP-AV IV Memory Map

Address Range	Size	Processor A	Processor B	Processor C	Processor D	Processor E	PMC DMA
0000_0000 - 1FFF_FFFF	512 MB	local mem	local mem	local mem	local mem	local mem	illegal
2000_0000 - 2FFF_FFFF	256 MB	mem D	mem D	mem D	illegal	mem D	mem D
3000_0000 - 3000_FFFF	64 KB	bridge D	bridge D	bridge D	illegal	bridge D	bridge D
3010_0000 - 3010_FFFF	65 KB	OBIC D	OBIC D	OBIC D	illegal	OBIC D	OBIC D
4000_0000 - 5FFF_FFFF	512 MB	PMC-1	PMC-1	PMC-1	PMC-1	PMC-1	PMC-1
6000_0000 - 6FFF_FFFF	256 MB	mem C	mem C	illegal	mem C	mem C	mem C
7000_0000 - 7000_FFFF	64 KB	bridge C	bridge C	illegal	bridge C	bridge C	bridge C
7010_0000 - 7010_FFFF	65 KB	OBIC C	OBIC C	illegal	OBIC C	OBIC C	OBIC C
8000_0000 - 8FFF_FFFF	256 MB	mem B	illegal	mem B	mem B	mem B	mem B
9000_0000 - 9000_FFFF	64 KB	bridge B	illegal	bridge B	bridge B	bridge B	bridge B
9010_0000 - 9010_FFFF	65 KB	OBIC B	illegal	OBIC B	OBIC B	OBIC B	OBIC B
A000_0000 - BFFF_FFFF	512 MB	PMC-2	PMC-2	PMC-2	PMC-2	PMC-2	PMC-2
C000_0000 - CFFF_FFFF	256 MB	illegal	mem A	mem A	mem A	mem A	mem A
D000_0000 - D000_FFFF	64 KB	illegal	bridge A	bridge A	bridge A	bridge A	bridge A
D010_0000 - D010_FFFF	65 KB	illegal	OBIC A	OBIC A	OBIC A	OBIC A	OBIC A
E000_0000 - E7FF_FFFF	128 MB	mem E	mem E	mem E	mem E	illegal	mem E
EC00_0000 - EC0F_FFFF	64 KB	E periph.	E periph.	E periph.	E periph.	illegal	E periph.
EC10_0000 - EC10_FFFF	65 KB	OBIC E	OBIC E	OBIC E	OBIC E	illegal	OBIC E
F000_0000 - F7FF_FFFF		Flash	illegal	illegal	illegal	illegal	illegal
FE00_0000 - FE00_FFFF	64 KB	PMC 1 I/O	PMC 1 I/O	PMC 1 I/O	PMC 1 I/O	PMC 1 I/O	illegal
FE10_0000 - FE10_FFFF	64 KB	PMC 2 I/O	PMC 2 I/O	PMC 2 I/O	PMC 2 I/O	PMC 2 I/O	illegal
FE20_0000 - FE20_FFFF	64 KB	local bridge	local bridge	local bridge	local bridge	local bridge	illegal
FE40_0000 - FE40_FFFF	64 KB	local OBIC	local OBIC	local OBIC	local OBIC	local OBIC	illegal
FE60_0000 - FE63_FFFF	256 KB	local SRAM	local SRAM	local SRAM	local SRAM	illegal	illegal
FE70_0000 - FF7F_FFFF	64 KB	illegal	illegal	illegal	illegal	Lcl periph.	
FFF0_0000 - FFF0_0FFF	4 KB	illegal	mem A - 0000.0000	mem A - 0000.0000	mem A - 0000.0000	illegal	mem A - 0000.0000

1. The Compact CHAMP-AV IV supports up to 512 MB of local SDRAM memory per node. When ordered with less than 512 MB of local SDRAM memory, the local memory space always begins at address 0000_0000.

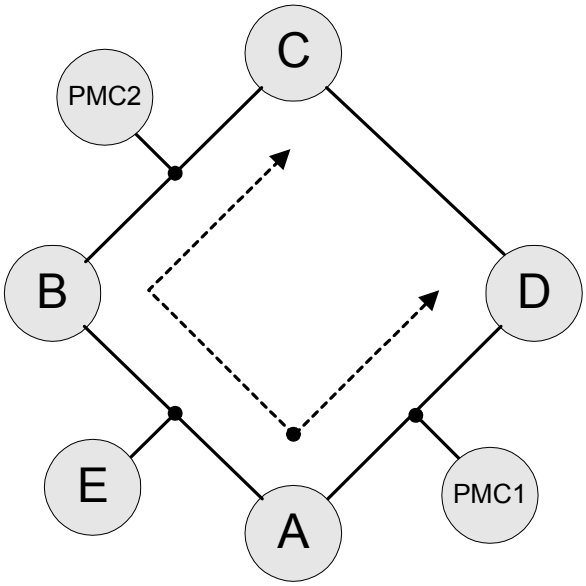
2. Only the first 256 MB of local memory is accessible by other PCI devices on the PCI bus. This corresponds to local SDRAM space 0000_0000 through 0FFF_FFFF.

3. Only the first 128 MB of local memory for node E is accessible by other PCI devices on the PCI bus. This corresponds to local SDRAM space 0000_0000 through 07FF_FFFF.

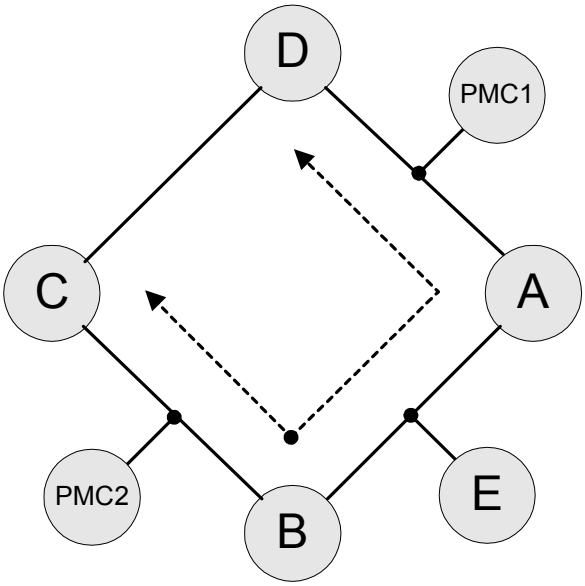
DATA FLOW DIRECTIONS

All memory-mapped resources can access all other memory-mapped resources on the Compact CHAMP-AV IV board. However, because each PCI interface on a particular Discovery controller must be assigned unique PCI address ranges (this is so that when the processor connected to the Discovery produces a PCI address, that address will go out one and only one PCI interface.), a resource will be able to get to another resource either clockwise or counter-clockwise around the ring. Figure 4.1 on page 4-5 and Figure 4.2 on page 4-6 provide diagrams that show the Discovery PCI interface used to access a particular resource. For instance, the A Node diagram in Figure 4.1 shows that Node A can get to either PMC1 or Node D counter-clockwise, while it can get to all other resources clockwise.

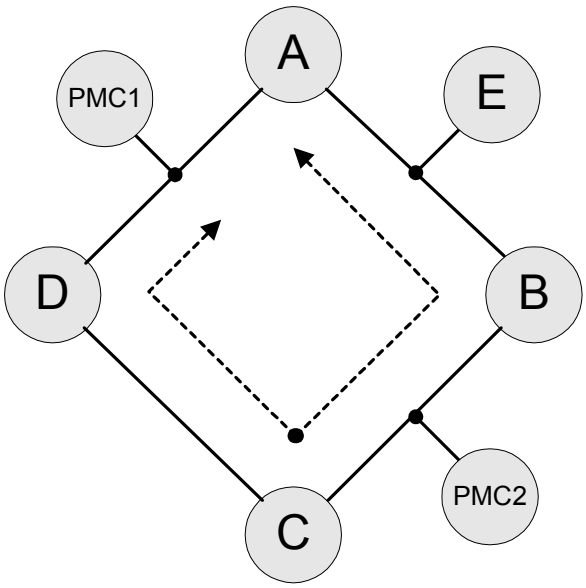
FIGURE 4.1: Data Access Directions for Processor Nodes



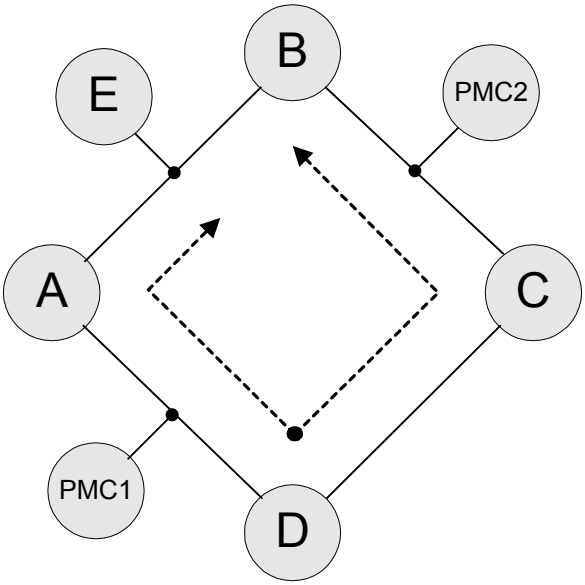
Resource Access
Directions for Node A



Resource Access
Directions for Node B

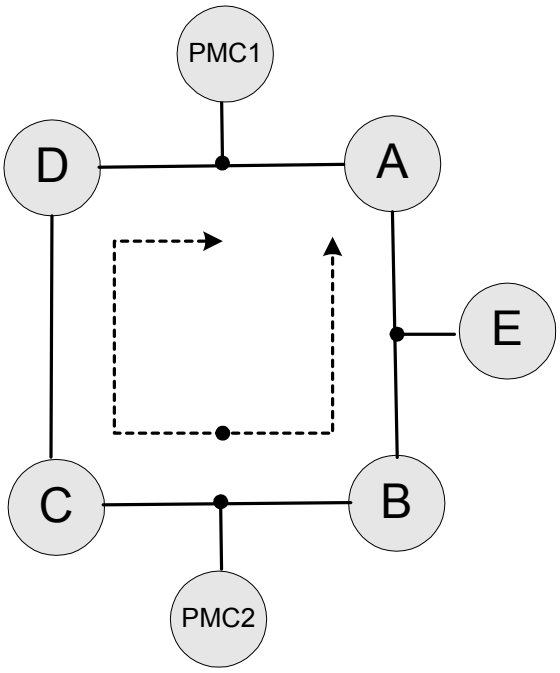


Resource Access
Directions for Node C

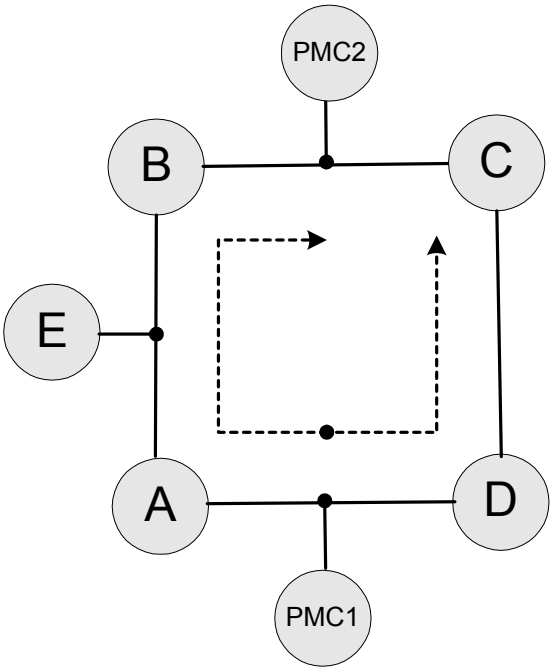


Resource Access
Directions for Node D

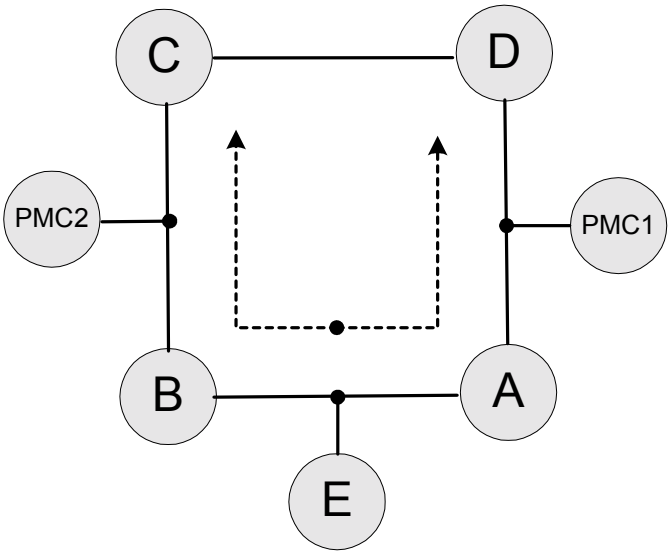
FIGURE 4.2: Data Access Directions for PMCs



Resource Access
Directions for PMC2



Resource Access
Directions for PMC1



Resource Access
Directions for Processor E

A

CONNECTOR PIN ASSIGNMENTS

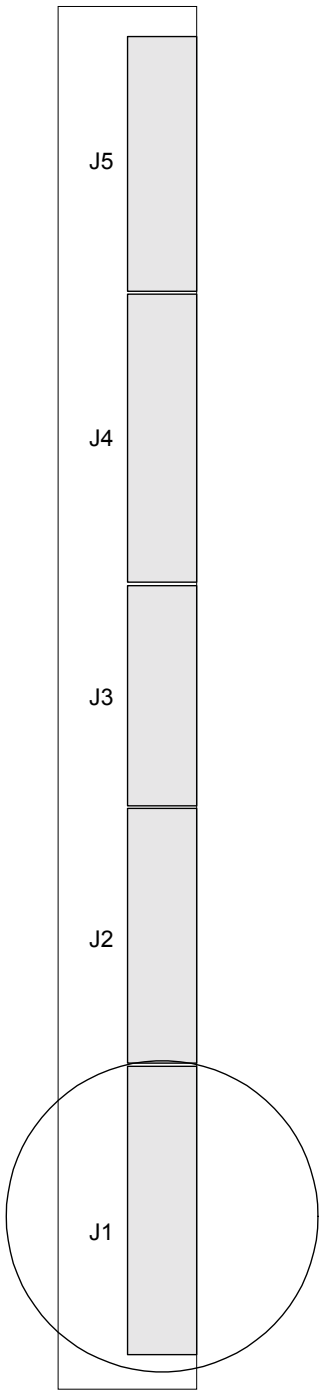
IN THIS APPENDIX...

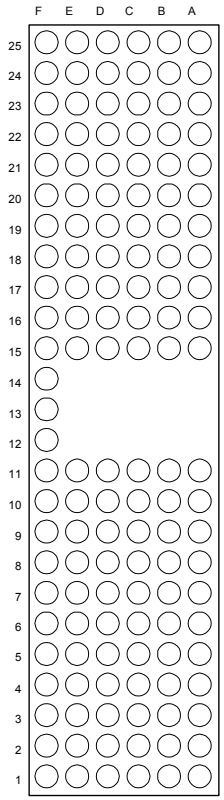
This appendix provides the interface pinout information for each of the connectors on the Compact CHAMP-AV IV. The following connectors are described:

J1 CONNECTOR PIN ASSIGNMENTS

The pinout tables are presented in the order of the rows when looking from the backplane, (i.e. E, D, C, B, A). Figure A.1 shows the location of the contacts on the J1 connector.

FIGURE A.1: J1 Connector





J1 and J4 Connector
Rear View

Table A.1 on page A-3 shows which signals are available from the J1 connector of the Compact CHAMP-AV IV.

TABLE A.1: J1 Connector Pin Assignments

Pin No.	Row E	Row D	Row C	Row B	Row A
25	5V	3.3V	NC	NC	5V
24	NC	NC	V(I/O)	5V	NC
23	NC	EP5V	NC	NC	3.3V
22	NC	NC	EP3.3V	GND	NC
21	NC	NC	NC	NC	3.3V
20	NC	NC	V(I/O)	GND	NC
19	NC	GND	NC	NC	3.3V
18	NC	NC	3.3V	GND	NC
17	NC	GND	NC	NC	3.3V
16	NC	NC	V(I/O)	GND	NC
15	NC	BD_SEL#	NC	NC	3.3V
14					
13			**Key Area**		
12					
11	NC	GND	NC	NC	NC
10	NC	NC	3.3V	GND	NC
9	NC	GND	NC	NC	NC
8	NC	NC	V(I/O)	GND	NC
7	NC	GND	NC	NC	NC
6	NC	NC	EP3.3V	PCI_PRES#	NC
5	NC	GND	CPCI_RST	RSV	NC
4	NC	NC	V(I/O)	HEALTHY#	NC
3	NC	EP5V	NC	NC	NC
2	NC	NC	NC	5V	NC
1	5V	+12V	NC	-12V	5V

Note: V(I/O) can be 3.3 or 5v to allow this to go into any slot (3.3v, 5v, universal)

ELECTRICAL CHARACTERISTICS OF J1 SIGNALS

Table A.2 provides the electrical characteristics of the basecard J1 signals.

TABLE A.2: J1 Connector Description

Signal Name	Direction	Basecard Signal Description	Electrical Characteristics
PCI_PRES#	Input	Pull up on PWB, tied low or left floating on backplane. When low indicates that the backplane supports a Compact PCI bus. Signal is not currently used on the Compact CHAMP-AV IV.	GND or floating on backplane.
HEALTHY#	Output	Active low signal indicates that on-board power is up and within specification.	open-drain
BD_SEL#	Input	Active low signal indicates that cPCI board is fully inserted into chassis, and that on-board power up may begin.	3.3v pull-up on board. Signal is either grounded on backplane or actively driven low by an open-drain driver.
CPCI_RST#	Input	Active low signal resets boards.	Open drain input. 3.3v pull-up on board.

Note: Signal details are for the basecard signals only. PMC I/O lines depend on the PMC modules installed, and are beyond the scope of this document.

J2 CONNECTOR PIN ASSIGNMENTS

The pinout tables are presented in the order of the rows when looking from the backplane, (i.e. E, D, C, B, A). Figure A.2 shows the location of the contacts on the J2 connector.

FIGURE A.2: J2 Connector

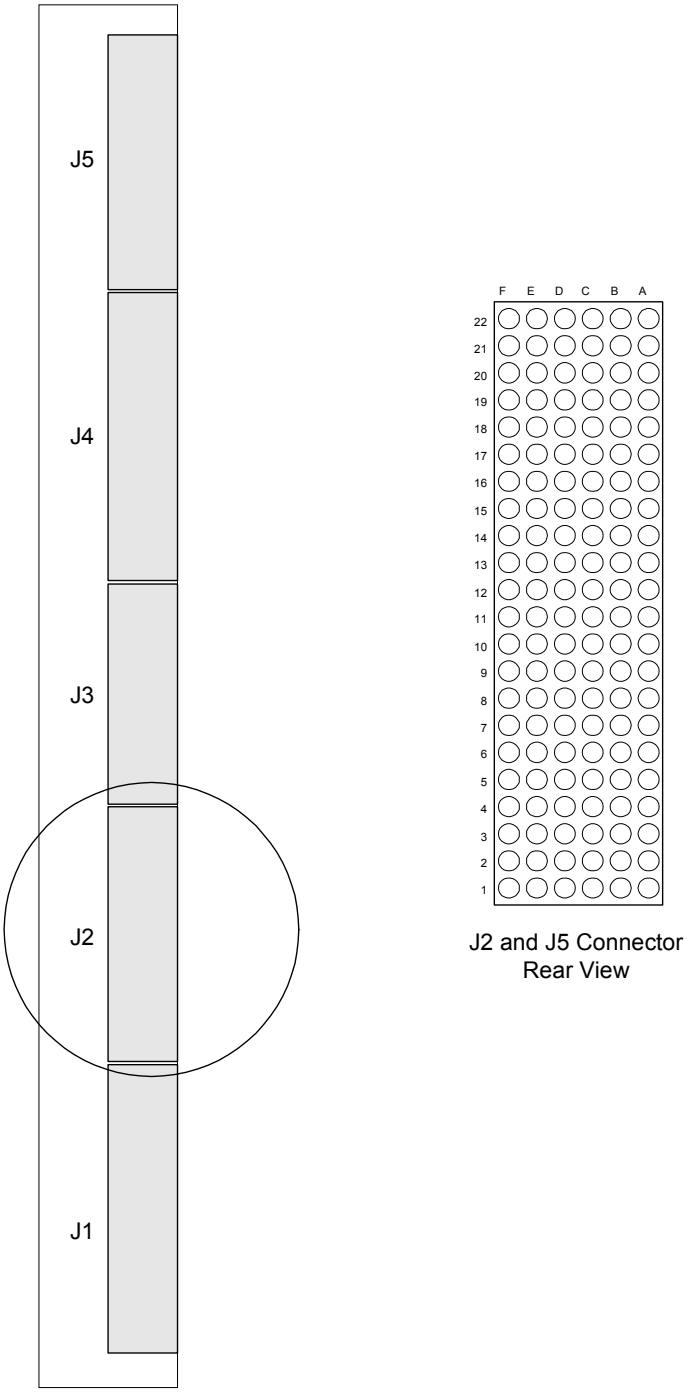


Table A.3 on page A-5 shows which signals are available from the J2 connector of the Compact CHAMP-AV IV.

TABLE A.3: J2 Connector Pin Assignments

Pin Number	Row E	Row D	Row C	Row B	Row A
22	GA0	GA1	GA2	GA3	GA4
21	NC	NC	NC	NC	NC
20	NC	GND	NC	NC	NC
19	NC	NC	NC	NC	NC
18	NC	GND	NC	NC	NC
17	NC	NC	NC	GND	NC
16	NC	GND	NC	NC	NC
15	NC	NC	NC	GND	NC
14	NC	GND	NC	NC	NC
13	NC	NC	V(I/O)	GND	NC
12	NC	GND	NC	NC	NC
11	NC	NC	V(I/O)	GND	NC
10	NC	GND	NC	NC	NC
9	NC	NC	V(I/O)	GND	NC
8	NC	GND	NC	NC	NC
7	NC	NC	V(I/O)	GND	NC
6	NC	GND	NC	NC	NC
5	NC	NC	V(I/O)	GND	NC
4	NC	GND	NC	NC	V(I/O)
3	NC	NC	NC	GND	NC
2	NC	NC	NC	NC	NC
1	NC	NC	NC	GND	NC

ELECTRICAL CHARACTERISTICS OF J2 SIGNALS

Table A.4 provides the electrical characteristics of the J2 signals.

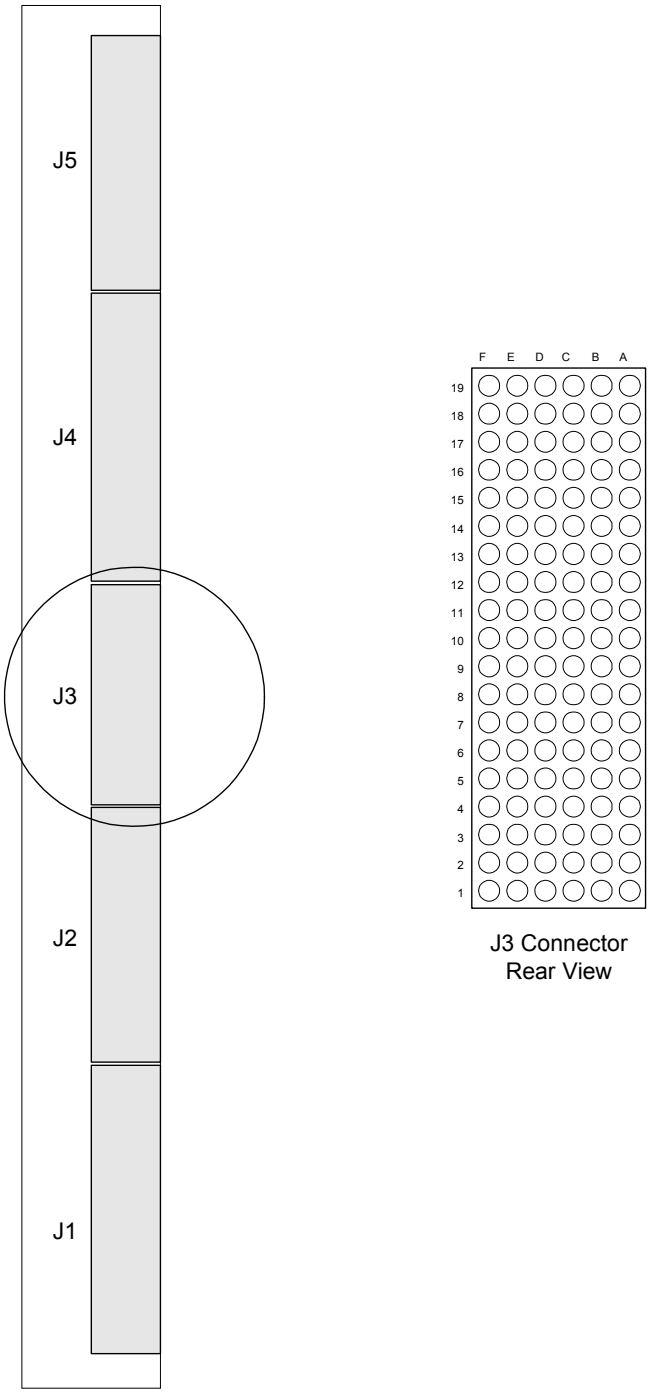
TABLE A.4: J2 Connector Description

Signal Name	Direction	Description	Electrical Characteristics
GA[4:0]	Input	Signals are pulled to 3.3v on board. Geographical Address signals are used to provide a unique slot ID for every slot in a cPCI backplane.	GND or floating on backplane.

J3 CONNECTOR PIN ASSIGNMENTS

Table A.5 lists the J3 pin assignments for the basecard. Figure A.3 shows the location of contacts on the J3 connector.

FIGURE A.3: J3 Connector



Note: The pinout tables are presented in the order of the rows when looking from the backplane, (i.e. E, D, C, B, A).

TABLE A.5: J3 Connector Pin Assignments

Pin Number	Row E	Row D	Row C	Row B	Row A
19	SGA0	SGA1	SGA2	SGA3	SGA4
18	AD0-TRX2-	AD0-TRX2+	GND	AD0-TRX0-	AD0-TRX0+
17	AD0-TRX3-	AD0-TRX3+	GND	AD0-TRX1-	AD0-TRX1+
16	BD0-TRX2-	BD0-TRX2+	GND	BD0-TRX0-	BD0-TRX0+
15	BD0-TRX3-	BD0-TRX3+	GND	BD0-TRX1-	BD0-TRX1+
14	RPMPRES	GND	GND	GND	GND
13	NC	NC		NC	NC
12	RC_RXN3	RC_RXP3	GND	RC_TXN3	RC_TXP3
11	RC_RXN2	RC_RXP2	GND	RC_TXN2	RC_TXP2
10	RC_RXN1	RC_RXP1	GND	RC_TXN1	RC_TXP1
9	RC_RXN0	RC_RXP0	GND	RC_TXN0	RC_TXP0
8	RB_RXN3	RB_RXP3	GND	RB_TXN3	RB_TXP3
7	RB_RXN2	RB_RXP2	GND	RB_TXN2	RB_TXP2
6	RB_RXN1	RB_RXP1	GND	RB_TXN1	RB_TXP1
5	RB_RXN0	RB_RXP0	GND	RB_TXN0	RB_TXP0
4	RA_RXN3	RA_RXP3	GND	RA_TXN3	RA_TXP3
3	RA_RXN2	RA_RXP2	GND	RA_TXN2	RA_TXP2
2	RA_RXN1	RA_RXP1	GND	RA_TXN1	RA_TXP1
1	RA_RXN0	RA_RXP0	GND	RA_TXN0	RA_TXP0

ELECTRICAL CHARACTERISTICS OF J3 SIGNALS

Table A.6 provides the electrical characteristics of the basecard J3 signals.

TABLE A.6: J3 Connector Description

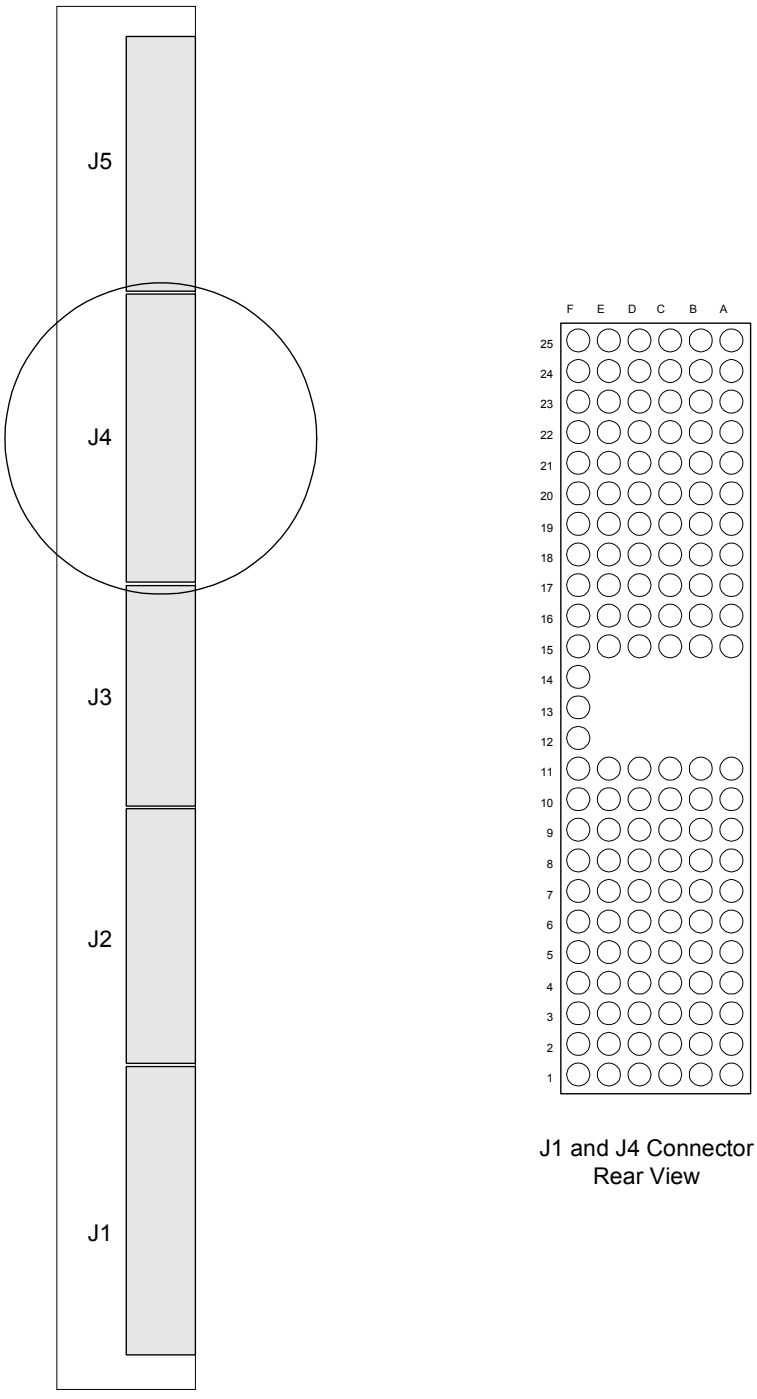
Signal Name	Direction	Description	Electrical Characteristics
SGA[4:0]	Input	Signals are pulled to 3.3v on board. Shelf Geographical Address signals are used to provide a unique shelf ID for multiple shelf systems.	GND or floating on backplane.
ADxx/BDxx	Input/Output	Gigabit Ethernet signals, comprised of Port A and Port B differential pairs.	IEEE 802.3
RAxx/RBxx/RCxx	PMC-dependent	PMC I/O Signals.	PMC-dependent

Note: Signal details are for the basecard signals only. PMC I/O lines depend on the PMC modules installed, and are beyond the scope of this document.

J4 CONNECTOR PIN ASSIGNMENTS

The pinout tables are presented in the order of the rows when looking from the backplane, (i.e. E, D, C, B, A). Figure A.4 shows the location of the contacts on the J4 connector.

FIGURE A.4: J4 Connector



J1 and J4 Connector
Rear View

Tables A.7 and A.11 show which signals are available from the J4 connector of the Compact CHAMP-AV IV.

TABLE A.7: J4 Connector Pin Assignments

Pin No.	Row E	Row D	Row C	Row B	Row A
25	GPIO3	GPIO2	GND	GPIO1	GPIO0
24	GPIO7	GPIO6	GND	GPIO5	GPIO4
23	NC	-12V	GND	NC	12V
22	GND	GND	GND	GND	GND
21	ED0-TRX2-	ED0-TRX2+	GND	ED0-TRX0-	ED0-TRX0+
20	ED0-TRX3-	ED0-TRX3+	GND	ED0-TRX1-	ED0-TRX1+
19	GND	GND	GND	GND	GND
18	DD0-TRX2-	DD0-TRX2+	GND	DD0-TRX0-	DD0-TRX0+
17	DD0-TRX3-	DD0-TRX3+	GND	DD0-TRX1-	DD0-TRX1+
16	CD0-TRX2-	CD0-TRX2+	GND	CD0-TRX0-	CD0-TRX0+
15	CD0-TRX3-	CD0-TRX3+	GND	CD0-TRX1-	CD0-TRX1+
14					
13			**Key Area**		
12					
11	XTMS	VIO	GND	JP_TCK	JP_TDI
10	XTDI	5V	GND	3.3V	JP_TRST
9	XTDO	GND	GND	JP_SRST	JP_TDO
8	XTCK	5V	GND	JP_QACK	JP_HRST
7	JTSEL	GND	GND	5V	JP_CKSTPIN
6	NC	GND	GND	JP_QREQ	JP_TMS
5	JPROC2	3.3V	GND	NC	JP_CKSTPO
4	JPROC0	3.3V	GND	5V	FL_WE
3	JPROC1	GND	GND	NC	FL_RDYBSY
2	GND	NC	GND	NC	BCFG0
1	F_ALTPROM	PBRST	GND	3.3V	BCFG1

Note: V(I/O) can be 3.3 or 5v to allow this to go into any slot (3.3v, 5v, universal)

ELECTRICAL CHARACTERISTICS OF J4 SIGNALS

Table A.8 provides the electrical characteristics of the basecard J4 signals.

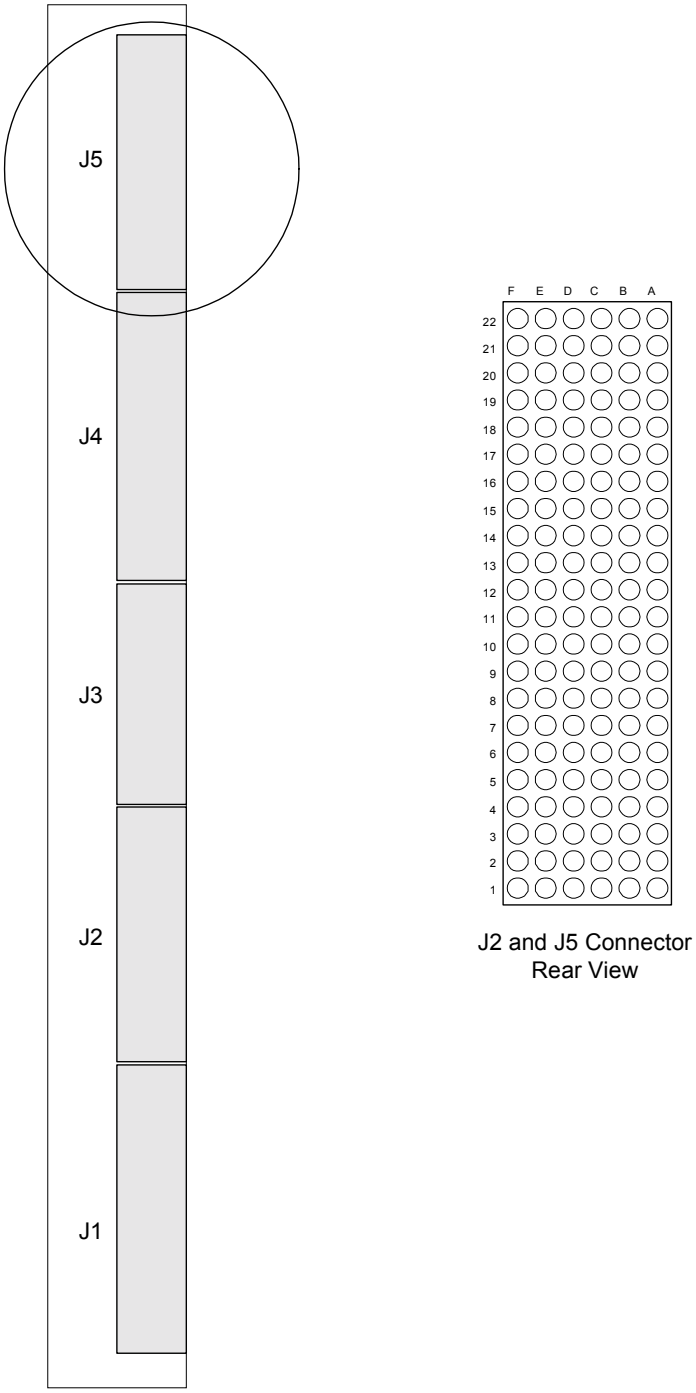
TABLE A.8: J4 Connector Description

Signal Name	Direction	Basecard Signal Description	Electrical Characteristics
CDxx/DDxx/Eexx	Input/Output	Gigabit Ethernet signals, comprised of Port C, Port D and Port E differential pairs.	IEEE 802.3
JP_xx	Input/Output	Processor COP signals/JTAG signals	LVTTL
XTxx		EPLD JTAG Chain signals. Use text from AV4 manual	
GPIOx	Input/Output	OBIC General Purpose I/O	LVTTL or Open Collector
JPROC[0:2]	Input	COP Target Processor Select	Ground or Open
JTSEL			
PBRST	Input	Pushbutton Reset, Active Low	Ground or Open
F_ALTPROM	Input		
FL_WE	Input	Flash Write enable signal. Reserved for furture use.	LVCMOS
FL_RDYBSY	Output	Flash Ready/Flash Busy signal. Reserved for future use.	LVCMOS
BCFG[1:0]	Input	Tied to SW[8:7]. SeeTable 2.5 on page 2-8 for details.	LVCMOS

J5 CONNECTOR PIN ASSIGNMENTS

Table A.9 lists the J5 pin assignments for the basecard. Figure A.5 shows the location of contacts on the J5 connector.

FIGURE A.5: J5 Connector



Note: The pinout tables are presented in the order of the rows when looking from the backplane, (i.e. E, D, C, B, A).

TABLE A.9: J5 Connector Pin Assignments

Pin Number	Row E	Row D	Row C	Row B	Row A
22	A_232TX	A_232RX	GND	E_232TX	E_232RX
21	GND	GND	GND	GND	GND
20	LD_RXN3	LD_RXP3	GND	LD_TXN3	LD_TXP3
19	LD_RXN2	LD_RXP2	GND	LD_TXN2	LD_TXP2
18	LD_RXN1	LD_RXP1	GND	LD_TXN1	LD_TXP1
17	LD_RXN0	LD_RXP0	GND	LD_TXN0	LD_TXP0
16	LC_RXN3	LC_RXP3	GND	LC_TXN3	LC_TXP3
15	LC_RXN2	LC_RXP2	GND	LC_TXN2	LC_TXP2
14	LC_RXN1	LC_RXP1	GND	LC_TXN1	LC_TXP1
13	LC_RXN0	LC_RXP0	GND	LC_TXN0	LC_TXP0
12	LB_RXN3	LB_RXP3	GND	LB_TXN3	LB_TXP3
11	LB_RXN2	LB_RXP2	GND	LB_TXN2	LB_TXP2
10	LB_RXN1	LB_RXP1	GND	LB_TXN1	LB_TXP1
9	LB_RXN0	LB_RXP0	GND	LB_TXN0	LB_TXP0
8	LA_RXN3	LA_RXP3	GND	LA_TXN3	LA_TXP3
7	LA_RXN2	LA_RXP2	GND	LA_TXN2	LA_TXP2
6	LA_RXN1	LA_RXP1	GND	LA_TXN1	LA_TXP1
5	LA_RXN0	LA_RXP0	GND	LA_TXN0	LA_TXP0
4	RD_RXN3	RD_RXP3	GND	RD_TXN3	RD_TXP3
3	RD_RXN2	RD_RXP2	GND	RD_TXN2	RD_TXP2
2	RD_RXN1	RD_RXP1	GND	RD_TXN1	RD_TXP1
1	RD_RXN0	RD_RXP0	GND	RD_TXN0	RD_TXP0

ELECTRICAL CHARACTERISTICS OF J5 SIGNALS

Table A.10 provides the electrical characteristics of the J5 signals.

TABLE A.10: J5 Connector Description

Signal Name	Dir	Description	Electrical Characteristics
E_232xx/A_232xx	Input/Output	Serial port RS-232 Signals	EIA-232
LDxx, LCxx, LBxx, LAxx	PMC-dependent	Left (PMC Site 1) I/O Signals.	PMC-dependent
RDxx	PMC-dependent	Right (PMC Site 2) I/O Signals.	PMC-dependent

Note: Signal details are for the basecard signals only. PMC I/O lines depend on the PMC modules installed, and are beyond the scope of this document.

PMC CONNECTORS

The Compact CHAMP-AV IV PMC connectors are described in the following sections.

Note

The direction of the signals in the tables describing the PMC Jn1 through Jn4 connectors is from the point of view of the baseboard.

J11 CONNECTOR

Table A.11 lists the pin assignments for the connector referenced J11. This connector is part of PMC site #1, and is referenced as Pn1/Jn1 in the PMC specification IEEE 1386.1-2001.

TABLE A.11: J11 Connector Description (Pn1/Jn1 64-bit PCI)

Pin No.	Signal	Direction	Description	Electrical Characteristics
1	TCK	I	JTAG Test Clock	PCI/PCI-X
2	-12V	N/A	-12V Supply	-12V
3	GND	N/A	GND	GND
4	INTA*	I	PMC Interrupt Request Line	PCI/PCI-X
5	INTB*	I	PMC Interrupt Request Line	PCI/PCI-X
6	INTC*	I	PMC Interrupt Request Line	PCI/PCI-X
7	PRSNT1*	I	BUSMODE1 signal, used to indicate presence of a PMC module in site 1	PMC/PPMC
8	+5V	N/A	Positive Supply	+5V
9	INTD*	I	PMC Interrupt Request Line	PCI/PCI-X
10	RESERVED	N/A	RESERVED	N/A
11	GND	N/A	GND	GND
12	NC (3.3 V AUX)	N/A	No Connect (3.3 V Auxiliary Supply)	3.3 V
13	PCICLK1	O	PCI Clock Signal	PCI/PCI-X
14	GND	N/A	GND	GND
15	GND	N/A	GND	GND
16	PMC1_GNT*	O	Arbitration Grant Signal to PMC site #1	PCI/PCI-X
17	PMC1_REQ*	I	Arbitration Request Signal from PMC site #1	PCI/PCI-X
18	+5V	N/A	Positive Supply	+5V
19	VIO	N/A	VIO Power **(see Note 1)**	+5V or +3.3V
20	AD[31]	I/O	PCI Address/Data Bus	PCI/PCI-X
21	AD[28]	I/O	PCI Address/Data Bus	PCI/PCI-X
22	AD[27]	I/O	PCI Address/Data Bus	PCI/PCI-X
23	AD[25]	I/O	PCI Address/Data Bus	PCI/PCI-X
24	GND	N/A	GND	GND
25	GND	N/A	GND	GND
26	C/BE[3]*	I/O	PCI Command/Byte Enable Bus	PCI/PCI-X
27	AD[22]	I/O	PCI Address/Data Bus	PCI/PCI-X
28	AD[21]	I/O	PCI Address/Data Bus	PCI/PCI-X
29	AD[19]	I/O	PCI Address/Data Bus	PCI/PCI-X
30	+5V	N/A	Positive Supply	+5V
31	VIO	N/A	VIO Power **(see Note 1)**	+5V or +3.3V

TABLE A.11: J11 Connector Description (Pn1/Jn1 64-bit PCI) (Continued)

Pin No.	Signal	Direction	Description	Electrical Characteristics
32	AD[17]	I/O	PCI Address/Data Bus	PCI/PCI-X
33	FRAME*	I/O	PCI Cycle Frame Signal	PCI/PCI-X
34	GND	N/A	GND	GND
35	GND	N/A	GND	GND
36	IRDY*	I/O	PCI Initiator Ready Signal	PCI/PCI-X
37	DEVSEL*	I/O	PCI Device Select Signal	PCI/PCI-X
38	+5V	N/A	Positive Supply	+5V
39	PCIXCAP	I/O	PCI-X Mode select (66 vs. 100 MHz operation)	PCI/PCI-X
40	LOCK*	I/O	PCI Lock Signal	I/O
41	RESERVED	N/A	RESERVED	N/A
42	RESERVED	N/A	RESERVED	N/A
43	PAR	I/O	PCI Parity Signal	PCI/PCI-X
44	GND	N/A	GND	GND
45	VIO	N/A	VIO Power **(see Note 1)**	+5V or +3.3V
46	AD[15]	I/O	PCI Address/Data Bus	PCI/PCI-X
47	AD[12]	I/O	PCI Address/Data Bus	PCI/PCI-X
48	AD[11]	I/O	PCI Address/Data Bus	PCI/PCI-X
49	AD[09]	I/O	PCI Address/Data Bus	PCI/PCI-X
50	+5V	N/A	Positive Supply	+5V
51	GND	N/A	GND	GND
52	C/BE[0]*	I/O	PCI Command/Byte Enable Bus	PCI/PCI-X
53	AD[06]	I/O	PCI Address/Data Bus	PCI/PCI-X
54	AD[05]	I/O	PCI Address/Data Bus	PCI/PCI-X
55	AD[04]	I/O	PCI Address/Data Bus	PCI/PCI-X
56	GND	N/A	GND	GND
57	VIO	N/A	VIO Power **(see Note 1)**	+5V or +3.3V
58	AD[03]	I/O	PCI Address/Data Bus	PCI/PCI-X
59	AD[02]	I/O	PCI Address/Data Bus	PCI/PCI-X
60	AD[01]	I/O	PCI Address/Data Bus	PCI/PCI-X
61	AD[00]	I/O	PCI Address/Data Bus	PCI/PCI-X
62	+5V	N/A	Positive Supply	+5V
63	GND	N/A	GND	GND
64	REQ64*	I/O	PCI 64-bit Request	PCI/PCI-X

Note 1: PMC site #1 can be factory configured to provide 3.3 V or 5 V PCI signaling. See "PMC Module Voltage Types" on page 2-4. VIO will supply 3.3V power when configured for 3.3 V signaling and 5 V power when configured for 5 V signaling.

J12 CONNECTOR

Table A.12 lists the pin assignments for the connector referenced J12. This connector is part of PMC site #1, and is referenced as Pn2/Jn2 in the PMC specification IEEE 1386.1-2001.

TABLE A.12: J12 Connector Description (Pn2/Jn2 64-bit PCI)

Pin No.	Signal	Direction	Description	Electrical Characteristics
1	+12V	N/A	+12V Supply	+12V
2	TRST*	O	JTAG Reset	PCI/PCI-X
3	TMS	I	JTAG Test Mode Select	PCI/PCI-X
4	TDO	O	JTAG Test Data Out	PCI/PCI-X
5	TDI	I	JTAG Test Data In	PCI/PCI-X
6	GND	N/A	GND	GND
7	GND	N/A	GND	GND
8	RESERVED	N/A	RESERVED	N/A
9	RESERVED	N/A	RESERVED	N/A
10	RESERVED	N/A	RESERVED	N/A
11	BUSMODE2	O	Basecard indicates PCI protocol used for PMC interface, by driving this line high	PMC/PPMC
12	+3.3V	N/A	Positive Supply	+3.3V
13	RST*	O	PCI Reset Signal	PCI/PCI-X
14	BUSMODE3	O	Basecard indicates PCI protocol used for PMC interface, by driving this line low	PMC/PPMC
15	+3.3V	N/A	Positive Supply	+3.3V
16	BUSMODE4	O	Basecard indicates PCI protocol used for PMC interface, by driving this line low	PMC/PPMC
17	RESERVED	N/A	RESERVED	N/A
18	GND	N/A	GND	GND
19	AD[30]	I/O	PCI Address/Data Bus	PCI/PCI-X
20	AD[29]	I/O	PCI Address/Data Bus	PCI/PCI-X
21	GND	N/A	GND	GND
22	AD[26]	I/O	PCI Address/Data Bus	PCI/PCI-X
23	AD[24]	I/O	PCI Address/Data Bus	PCI/PCI-X
24	+3.3V	N/A	Positive Supply	+3.3V
25	IDSEL	O	PCI Initialisation Device Select for PMC Site #2	PCI/PCI-X
26	AD[23]	I/O	PCI Address/Data Bus	PCI/PCI-X
27	+3.3V	N/A	Positive Supply	+3.3V
28	AD[20]	I/O	PCI Address/Data Bus	PCI/PCI-X
29	AD[18]	I/O	PCI Address/Data Bus	PCI/PCI-X
30	GND	N/A	GND	GND
31	AD[16]	I/O	PCI Address/Data Bus	PCI/PCI-X

TABLE A.12: J12 Connector Description (Pn2/Jn2 64-bit PCI) (Continued)

Pin No.	Signal	Direction	Description	Electrical Characteristics
32	C/BE[2]*	I/O	PCI Command/Byte Enable Bus	PCI/PCI-X
33	GND	N/A	GND	GND
34	IDSELB	O	IDSELB for second PCI agent	PCI/PCI-X
35	TRDY*	I/O	PCI Target Ready	PCI/PCI-X
36	+3.3V	N/A	Positive Supply	+3.3V
37	GND	N/A	GND	GND
38	STOP*	I/O	PCI Transaction Stop Signal	PCI/PCI-X
39	PERR*	I/O	PCI Data Parity Signal	PCI/PCI-X
40	GND	N/A	GND	GND
41	+3.3V	N/A	Positive Supply	+3.3V
42	SERR*	I/O	PCI System Error	PCI/PCI-X
43	C/BE[1]*	I/O	PCI Command/Byte Enable Bus	PCI/PCI-X
44	GND	N/A	GND	GND
45	AD[14]	I/O	PCI Address/Data Bus	PCI/PCI-X
46	AD[13]	I/O	PCI Address/Data Bus	PCI/PCI-X
47	M66EN	I/O	33/66 MHz PCI operation	PCI/PCI-X
48	AD[10]	I/O	PCI Address/Data Bus	PCI/PCI-X
49	AD[08]	I/O	PCI Address/Data Bus	PCI/PCI-X
50	+3.3V	N/A	Positive Supply	+3.3V
51	AD[07]	I/O	PCI Address/Data Bus	PCI/PCI-X
52	REQB*	I	arbitration request signal for second PCI agent	PCI/PCI-X
53	+3.3V	N/A	Positive Supply	+3.3V
54	GNTB*	O	arbitration grant signal for second PCI agent	PCI/PCI-X
55	RESERVED	N/A	RESERVED	N/A
56	GND	N/A	GND	GND
57	RESERVED	N/A	RESERVED	N/A
58	EREADY*	I	PMC ready signal	PPMC
59	GND	N/A	GND	GND
60	RESETOUT*	I	Reset signal from PMC to baseboard	PPMC
61	ACK64*	N/A	64-bit transfer acknowledge signal	PCI/PCI-X
62	+3.3V	N/A	Positive Supply	+3.3V
63	GND	N/A	GND	GND
64	MONARCH	O	enable/disable MONARCH feature on Processor PMCs	PPMC

J13 CONNECTOR

Table A.13 lists the pin assignments for the connector referenced J13. This connector is part of PMC site #1, and is referenced as Pn3/Jn3 in the *PMC Specification* IEEE 1386.1-2001.

TABLE A.13: J13 Connector Description (Pn3/Jn3 64-bit PCI)

Pin No.	Signal Name	Direction	Description	Electrical Characteristics
1	PCI_RSVD	N/A	Reserved	N/A
2	GND	N/A	GND	GND
3	GND	N/A	GND	GND
4	C/BE[7]*	I/O	PCI Command/Byte Enable Bus	PCI/PCI-X
5	C/BE[6]*	I/O	PCI Command/Byte Enable Bus	PCI/PCI-X
6	C/BE[5]*	I/O	PCI Command/Byte Enable Bus	PCI/PCI-X
7	C/BE[4]*	I/O	PCI Command/Byte Enable Bus	PCI/PCI-X
8	GND	N/A	GND	GND
9	VIO	N/A	VIO Power **(see Note 1)**	+5V or +3.3V
10	PAR64	I/O	PCI Parity Signal	PCI/PCI-X
11	AD[63]	I/O	PCI Address/Data Bus	PCI/PCI-X
12	AD[62]	I/O	PCI Address/Data Bus	PCI/PCI-X
13	AD[61]	I/O	PCI Address/Data Bus	PCI/PCI-X
14	GND	N/A	GND	GND
15	GND	N/A	GND	GND
16	AD[60]	I/O	PCI Address/Data Bus	PCI/PCI-X
17	AD[59]	I/O	PCI Address/Data Bus	PCI/PCI-X
18	AD[58]	I/O	PCI Address/Data Bus	PCI/PCI-X
19	AD[57]	I/O	PCI Address/Data Bus	PCI/PCI-X
20	GND	N/A	GND	GND
21	VIO	N/A	VIO Power **(see Note 1)**	+5V or +3.3V
22	AD[56]	I/O	PCI Address/Data Bus	PCI/PCI-X
23	AD[55]	I/O	PCI Address/Data Bus	PCI/PCI-X
24	AD[54]	I/O	PCI Address/Data Bus	PCI/PCI-X
25	AD[53]	I/O	PCI Address/Data Bus	PCI/PCI-X
26	GND	N/A	GND	GND
27	GND	N/A	GND	GND
28	AD[52]	I/O	PCI Address/Data Bus	PCI/PCI-X
29	AD[51]	I/O	PCI Address/Data Bus	PCI/PCI-X
30	AD[50]	I/O	PCI Address/Data Bus	PCI/PCI-X
31	AD[49]	I/O	PCI Address/Data Bus	PCI/PCI-X
32	GND	N/A	GND	GND

TABLE A.13: J13 Connector Description (Pn3/Jn3 64-bit PCI) (Continued)

Pin No.	Signal Name	Direction	Description	Electrical Characteristics
33	GND	N/A	GND	GND
34	AD[48]	I/O	PCI Address/Data Bus	PCI/PCI-X
35	AD[47]	I/O	PCI Address/Data Bus	PCI/PCI-X
36	AD[46]	I/O	PCI Address/Data Bus	PCI/PCI-X
37	AD[45]	I/O	PCI Address/Data Bus	PCI/PCI-X
38	GND	N/A	GND	GND
39	VIO	N/A	VIO Power **(see Note 1)**	+5V or +3.3V
40	AD[44]	I/O	PCI Address/Data Bus	PCI/PCI-X
41	AD[43]	I/O	PCI Address/Data Bus	PCI/PCI-X
42	AD[42]	I/O	PCI Address/Data Bus	PCI/PCI-X
43	AD[41]	I/O	PCI Address/Data Bus	PCI/PCI-X
44	GND	N/A	GND	GND
45	GND	N/A	GND	GND
46	AD[40]	I/O	PCI Address/Data Bus	PCI/PCI-X
47	AD[39]	I/O	PCI Address/Data Bus	PCI/PCI-X
48	AD[38]	I/O	PCI Address/Data Bus	PCI/PCI-X
49	AD[37]	I/O	PCI Address/Data Bus	PCI/PCI-X
50	GND	N/A	GND	GND
51	GND	N/A	GND	GND
52	AD[36]	I/O	PCI Address/Data Bus	PCI/PCI-X
53	AD[35]	I/O	PCI Address/Data Bus	PCI/PCI-X
54	AD[34]	I/O	PCI Address/Data Bus	PCI/PCI-X
55	AD[33]	I/O	PCI Address/Data Bus	PCI/PCI-X
56	GND	N/A	GND	GND
57	VIO	N/A	VIO Power **(see Note 1)**	+5V or +3.3V
58	AD[32]	I/O	PCI Address/Data Bus	PCI/PCI-X
59	RESERVED	N/A	RESERVED	N/A
60	RESERVED	N/A	RESERVED	N/A
61	RESERVED	N/A	RESERVED	N/A
62	GND	N/A	GND	GND
63	GND	N/A	GND	GND
64	RESERVED	N/A	RESERVED	N/A

Note 1: PMC site #1 can be factory configured to provide 3.3 V or 5 V PCI signaling. See "PMC Module Voltage Types" on page 2-4. VIO will supply 3.3V power when configured for 3.3 V signaling and 5 V power when configured for 5 V signaling.

J14 CONNECTOR

Table A.14 lists the pin assignments for the connector referenced J14. This connector is part of PMC site #1, and is referenced as Pn4/Jn4 in the PMC specification IEEE 1386.1-2001.

TABLE A.14: J14 Connector Description (Pn4/Jn4 User Defined I/O)

J14 Pin No.	cPCI J5 Pin Number	Direction	Description	Electrical Characteristics
1		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
2		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
3		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
4		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
5		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
6		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
7		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
8		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
9		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
10		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
11		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
12		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
13		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
14		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
15		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
16		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
17		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
18		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
19		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
20		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
21		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
22		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
23		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
24		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
25		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
26		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
27		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
28		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
29		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
30		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
31		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
32		I/O	PMC #1 connection to cPCI J5 connector	Depends on module

TABLE A.14: J14 Connector Description (Pn4/Jn4 User Defined I/O) (Continued)

J14 Pin No.	cPCI J5 Pin Number	Direction	Description	Electrical Characteristics
33		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
34		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
35		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
36		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
37		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
38		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
39		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
40		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
41		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
42		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
43		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
44		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
45		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
46		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
47		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
48		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
49		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
50		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
51		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
52		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
53		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
54		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
55		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
56		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
57		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
58		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
59		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
60		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
61		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
62		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
63		I/O	PMC #1 connection to cPCI J5 connector	Depends on module
64		I/O	PMC #1 connection to cPCI J5 connector	Depends on module

J21 CONNECTOR

Table A.15 lists the pin assignments for the connector referenced J21. This connector is part of PMC site #2, and is referenced as Pn1/Jn1 in the *PMC Specification* IEEE 1386.1-2001.

TABLE A.15: J21 Connector Description (Pn1/Jn1 64-bit PCI)

Pin No.	Signal Name	Direction	Description	Electrical Characteristics
1	TCK	I	JTAG Test Clock	PCI/PCI-X
2	-12V	N/A	-12V Supply	-12V
3	GND	N/A	GND	GND
4	INTA*	I	PMC Interrupt Request Line	PCI/PCI-X
5	INTB*	I	PMC Interrupt Request Line	PCI/PCI-X
6	INTC*	I	PMC Interrupt Request Line	PCI/PCI-X
7	PRSNT2*	I	BUSMODE1 signal, used to indicate presence of a PMC module in site 2	PMC/PPMC
8	+5V	N/A	Positive Supply	+5 V
9	INTD*	I	PMC Interrupt Request Line	PCI/PCI-X
10	RESERVED	N/A	RESERVED	N/A
11	GND	N/A	GND	GND
12	NC (3.3 V AUX)	N/A	No Connect (3.3V Auxiliary Supply)	3.3 V
13	PCICLK2	O	PCI Clock Signal	PCI/PCI-X
14	GND	N/A	GND	GND
15	GND	N/A	GND	GND
16	PMC2_GNT*	O	Arbitration Grant Signal to PMC site #2	PCI/PCI-X
17	PMC2_REQ*	I	Arbitration Request Signal from PMC site #2	PCI/PCI-X
18	+5V	N/A	Positive Supply	+5 V
19	VIO	N/A	VIO Power **(see Note 1)**	+5 V or +3.3V
20	AD[31]	I/O	PCI Address/Data Bus	PCI/PCI-X
21	AD[28]	I/O	PCI Address/Data Bus	PCI/PCI-X
22	AD[27]	I/O	PCI Address/Data Bus	PCI/PCI-X
23	AD[25]	I/O	PCI Address/Data Bus	PCI/PCI-X
24	GND	N/A	GND	GND
25	GND	N/A	GND	GND
26	C/BE[3]*	I/O	PCI Command/Byte Enable Bus	PCI/PCI-X
27	AD[22]	I/O	PCI Address/Data Bus	PCI/PCI-X
28	AD[21]	I/O	PCI Address/Data Bus	PCI/PCI-X
29	AD[19]	I/O	PCI Address/Data Bus	PCI/PCI-X
30	+5V	N/A	Positive Supply	+5V
31	VIO	N/A	VIO Power **(see Note 1)**	+5 V or +3.3V

TABLE A.15: J21 Connector Description (Pn1/Jn1 64-bit PCI) (Continued)

Pin No.	Signal Name	Direction	Description	Electrical Characteristics
32	AD[17]	I/O	PCI Address/Data Bus	PCI/PCI-X
33	FRAME*	I/O	PCI Cycle Frame Signal	PCI/PCI-X
34	GND	N/A	GND	GND
35	GND	N/A	GND	GND
36	IRDY*	I/O	PCI Initiator Ready Signal	PCI/PCI-X
37	DEVSEL*	I/O	PCI Device Select Signal	PCI/PCI-X
38	+5V	N/A	Positive Supply	+5V
39	PCIXCAP	I/O	PCI-X Mode select (66 vs. 100 MHz operation)	PCI/PCI-X
40	LOCK*	I/O	PCI Lock Signal	I/O
41	RESERVED	N/A	RESERVED	N/A
42	RESERVED	N/A	RESERVED	N/A
43	PAR	I/O	PCI Parity Signal	PCI/PCI-X
44	GND	N/A	GND	GND
45	VIO	N/A	VIO Power **(see Note 1)**	+5 V or +3.3V
46	AD[15]	I/O	PCI Address/Data Bus	PCI/PCI-X
47	AD[12]	I/O	PCI Address/Data Bus	PCI/PCI-X
48	AD[11]	I/O	PCI Address/Data Bus	PCI/PCI-X
49	AD[09]	I/O	PCI Address/Data Bus	PCI/PCI-X
50	+5V	N/A	Positive Supply	+5V
51	GND	N/A	GND	GND
52	C/BE[0]*	I/O	PCI Command/Byte Enable Bus	PCI/PCI-X
53	AD[06]	I/O	PCI Address/Data Bus	PCI/PCI-X
54	AD[05]	I/O	PCI Address/Data Bus	PCI/PCI-X
55	AD[04]	I/O	PCI Address/Data Bus	PCI/PCI-X
56	GND	N/A	GND	GND
57	VIO	N/A	VIO Power **(see Note 1)**	+5 V or +3.3V
58	AD[03]	I/O	PCI Address/Data Bus	PCI/PCI-X
59	AD[02]	I/O	PCI Address/Data Bus	PCI/PCI-X
60	AD[01]	I/O	PCI Address/Data Bus	PCI/PCI-X
61	AD[00]	I/O	PCI Address/Data Bus	PCI/PCI-X
62	+5V	N/A	Positive Supply	+5V
63	GND	N/A	GND	GND
64	REQ64*	N/A	Interfaces 64-bit PMC Module	PCI/PCI-X

Note 1: PMC site #2 can be factory configured to provide 3.3 V or 5 V PCI signaling. See "PMC Module Voltage Types" on page 2-4. VIO will supply 3.3V power when configured for 3.3 V signaling and 5 V power when configured for 5 V signaling.

J22 CONNECTOR

Table A.16 lists the pin assignments for the connector referenced J22. This connector is part of PMC site #2, and is referenced as Pn2/Jn2 in the PMC specification IEEE 1386.1-2001.

TABLE A.16: J22 Connector Description (Pn2/Jn2 64-bit PCI)

Pin No.	Signal Name	Direction	Description	Electrical Characteristics
1	+12V	N/A	+12V Supply	+12V
2	TRST*	O	JTAG Reset	PCI/PCI-X
3	TMS	I	JTAG Test Mode Select	PCI/PCI-X
4	TDO	O	JTAG Test Data Out	PCI/PCI-X
5	TDI	I	JTAG Test Data In	PCI/PCI-X
6	GND	N/A	GND	GND
7	GND	N/A	GND	GND
8	RESERVED	N/A	RESERVED	N/A
9	RESERVED	N/A	RESERVED	N/A
10	RESERVED	N/A	RESERVED	N/A
11	BUSMODE2	O	Basecard indicates PCI protocol used for PMC interface, by driving this line high	PMC/PPMC
12	+3.3V	N/A	Positive Supply	+3.3V
13	RST*	O	PCI Reset Signal	PCI/PCI-X
14	BUSMODE3	O	Basecard indicates PCI protocol used for PMC interface, by driving this line low	PMC/PPMC
15	+3.3V	N/A	Positive Supply	+3.3V
16	BUSMODE4	O	Basecard indicates PCI protocol used for PMC interface, by driving this line low	PMC/PPMC
17	RESERVED	N/A	RESERVED	N/A
18	GND	N/A	GND	GND
19	AD[30]	I/O	PCI Address/Data Bus	PCI/PCI-X
20	AD[29]	I/O	PCI Address/Data Bus	PCI/PCI-X
21	GND	N/A	GND	GND
22	AD[26]	I/O	PCI Address/Data Bus	PCI/PCI-X
23	AD[24]	I/O	PCI Address/Data Bus	PCI/PCI-X
24	+3.3V	N/A	Positive Supply	+3.3V
25	IDSEL	O	PCI Initialisation Device Select for PMC Site #2	PCI/PCI-X
26	AD[23]	I/O	PCI Address/Data Bus	PCI/PCI-X
27	+3.3V	N/A	Positive Supply	+3.3V
28	AD[20]	I/O	PCI Address/Data Bus	PCI/PCI-X
29	AD[18]	I/O	PCI Address/Data Bus	PCI/PCI-X
30	GND	N/A	GND	GND
31	AD[16]	I/O	PCI Address/Data Bus	PCI/PCI-X

TABLE A.16: J22 Connector Description (Pn2/Jn2 64-bit PCI) (Continued)

Pin No.	Signal Name	Direction	Description	Electrical Characteristics
32	C/BE[2]*	I/O	PCI Command/Byte Enable Bus	PCI/PCI-X
33	GND	N/A	GND	GND
34	IDSELB	O	IDSELB for second PCI agent	PCI/PCI-X
35	TRDY*	I/O	PCI Target Ready	PCI/PCI-X
36	+3.3V	N/A	Positive Supply	+3.3V
37	GND	N/A	GND	GND
38	STOP*	I/O	PCI Transaction Stop Signal	PCI/PCI-X
39	PERR*	I/O	PCI Data Parity Signal	PCI/PCI-X
40	GND	N/A	GND	GND
41	+3.3V	N/A	Positive Supply	+3.3V
42	SERR*	I/O	PCI System Error	PCI/PCI-X
43	C/BE[1]*	I/O	PCI Command/Byte Enable Bus	PCI/PCI-X
44	GND	N/A	GND	GND
45	AD[14]	I/O	PCI Address/Data Bus	PCI/PCI-X
46	AD[13]	I/O	PCI Address/Data Bus	PCI/PCI-X
47	M66EN	I/O	33/66 MHz PCI operation	PCI/PCI-X
48	AD[10]	I/O	PCI Address/Data Bus	PCI/PCI-X
49	AD[08]	I/O	PCI Address/Data Bus	PCI/PCI-X
50	+3.3V	N/A	Positive Supply	+3.3V
51	AD[07]	I/O	PCI Address/Data Bus	PCI/PCI-X
52	REQB*	I	arbitration request signal for second PCI agent	PCI/PCI-X
53	+3.3V	N/A	Positive Supply	+3.3V
54	GNTB*	O	arbitration grant signal for second PCI agent	PCI/PCI-X
55	RESERVED	N/A	RESERVED	N/A
56	GND	N/A	GND	GND
57	RESERVED	N/A	RESERVED	N/A
58	EREADY*	I	PMC ready signal	PPMC
59	GND	N/A	GND	GND
60	RESETOUT*	I	Reset signal from PMC to baseboard	PPMC
61	ACK64*	N/A	64-bit transfer acknowledge signal	PCI/PCI-X
62	+3.3V	N/A	Positive Supply	+3.3V
63	GND	N/A	GND	GND
64	MONARCH	O	enable/disable MONARCH feature on Processor PMCs	PPMC

J23 CONNECTOR

Table A.17 lists the pin assignments for the connector referenced J23. This connector is part of PMC site #2, and is referenced as Pn3/Jn3 in the *PMC Specification* IEEE 1386.1-2001.

TABLE A.17: J23 Connector Description (Pn3/Jn3 64-bit PCI)

Pin No.	Signal Name	Direction	Description	Electrical Characteristics
1	PCI_RSVD	N/A	Reserved	N/A
2	GND	N/A	GND	GND
3	GND	N/A	GND	GND
4	C/BE[7]*	I/O	PCI Command/Byte Enable Bus	PCI/PCI-X
5	C/BE[6]*	I/O	PCI Command/Byte Enable Bus	PCI/PCI-X
6	C/BE[5]*	I/O	PCI Command/Byte Enable Bus	PCI/PCI-X
7	C/BE[4]*	I/O	PCI Command/Byte Enable Bus	PCI/PCI-X
8	GND	N/A	GND	GND
9	VIO	N/A	VIO Power **(see Note 1)**	+5 V or +3.3V
10	PAR64	I/O	PCI Parity Signal	PCI/PCI-X
11	AD[63]	I/O	PCI Address/Data Bus	PCI/PCI-X
12	AD[62]	I/O	PCI Address/Data Bus	PCI/PCI-X
13	AD[61]	I/O	PCI Address/Data Bus	PCI/PCI-X
14	GND	N/A	GND	GND
15	GND	N/A	GND	GND
16	AD[60]	I/O	PCI Address/Data Bus	PCI/PCI-X
17	AD[59]	I/O	PCI Address/Data Bus	PCI/PCI-X
18	AD[58]	I/O	PCI Address/Data Bus	PCI/PCI-X
19	AD[57]	I/O	PCI Address/Data Bus	PCI/PCI-X
20	GND	N/A	GND	GND
21	VIO	N/A	VIO Power **(see Note 1)**	+5 V or +3.3V
22	AD[56]	I/O	PCI Address/Data Bus	PCI/PCI-X
23	AD[55]	I/O	PCI Address/Data Bus	PCI/PCI-X
24	AD[54]	I/O	PCI Address/Data Bus	PCI/PCI-X
25	AD[53]	I/O	PCI Address/Data Bus	PCI/PCI-X
26	GND	N/A	GND	GND
27	GND	N/A	GND	GND
28	AD[52]	I/O	PCI Address/Data Bus	PCI/PCI-X
29	AD[51]	I/O	PCI Address/Data Bus	PCI/PCI-X
30	AD[50]	I/O	PCI Address/Data Bus	PCI/PCI-X
31	AD[49]	I/O	PCI Address/Data Bus	PCI/PCI-X

TABLE A.17: J23 Connector Description (Pn3/Jn3 64-bit PCI) (Continued)

Pin No.	Signal Name	Direction	Description	Electrical Characteristics
32	GND	N/A	GND	GND
33	GND	N/A	GND	GND
34	AD[48]	I/O	PCI Address/Data Bus	PCI/PCI-X
35	AD[47]	I/O	PCI Address/Data Bus	PCI/PCI-X
36	AD[46]	I/O	PCI Address/Data Bus	PCI/PCI-X
37	AD[45]	I/O	PCI Address/Data Bus	PCI/PCI-X
38	GND	N/A	GND	GND
39	VIO	N/A	VIO Power **(see Note 1)**	+5 V or +3.3V
40	AD[44]	I/O	PCI Address/Data Bus	PCI/PCI-X
41	AD[43]	I/O	PCI Address/Data Bus	PCI/PCI-X
42	AD[42]	I/O	PCI Address/Data Bus	PCI/PCI-X
43	AD[41]	I/O	PCI Address/Data Bus	PCI/PCI-X
44	GND	N/A	GND	GND
45	GND	N/A	GND	GND
46	AD[40]	I/O	PCI Address/Data Bus	PCI/PCI-X
47	AD[39]	I/O	PCI Address/Data Bus	PCI/PCI-X
48	AD[38]	I/O	PCI Address/Data Bus	PCI/PCI-X
49	AD[37]	I/O	PCI Address/Data Bus	PCI/PCI-X
50	GND	N/A	GND	GND
51	GND	N/A	GND	GND
52	AD[36]	I/O	PCI Address/Data Bus	PCI/PCI-X
53	AD[35]	I/O	PCI Address/Data Bus	PCI/PCI-X
54	AD[34]	I/O	PCI Address/Data Bus	PCI/PCI-X
55	AD[33]	I/O	PCI Address/Data Bus	PCI/PCI-X
56	GND	N/A	GND	GND
57	VIO	N/A	VIO Power **(see Note 1)**	+5 V or +3.3V
58	AD[32]	I/O	PCI Address/Data Bus	PCI/PCI-X
59	RESERVED	N/A	RESERVED	N/A
60	RESERVED	N/A	RESERVED	N/A
61	RESERVED	N/A	RESERVED	N/A
62	GND	N/A	GND	GND
63	GND	N/A	GND	GND
64	RESERVED	N/A	RESERVED	N/A

Note 1: PMC site #2 can be factory configured to provide 3.3 V or 5 V PCI signaling. See "PMC Module Voltage Types" on page 2-4. VIO will supply 3.3V power when configured for 3.3 V signaling and 5 V power when configured for 5 V signaling.

J24 CONNECTOR

Table A.18 lists the pin assignments for the connector referenced J24. This connector is part of PMC site #2, and is referenced as Pn4/Jn4 in the PMC specification IEEE 1386.1-2001.

TABLE A.18: J24 Connector Description (Pn4/Jn4 User Defined I/O)

J24 Pin No.	cPCI J5, J3 Pin Number	Direction	Description	Electrical Characteristics
1		I/O	PMC #2 connection to cPCI J5 connector	Depends on module
2		I/O	PMC #2 connection to cPCI J5 connector	Depends on module
3		I/O	PMC #2 connection to cPCI J5 connector	Depends on module
4		I/O	PMC #2 connection to cPCI J5 connector	Depends on module
5		I/O	PMC #2 connection to cPCI J5 connector	Depends on module
6		I/O	PMC #2 connection to cPCI J5 connector	Depends on module
7		I/O	PMC #2 connection to cPCI J5 connector	Depends on module
8		I/O	PMC #2 connection to cPCI J5 connector	Depends on module
9		I/O	PMC #2 connection to cPCI J5 connector	Depends on module
10		I/O	PMC #2 connection to cPCI J5 connector	Depends on module
11		I/O	PMC #2 connection to cPCI J5 connector	Depends on module
12		I/O	PMC #2 connection to cPCI J5 connector	Depends on module
13		I/O	PMC #2 connection to cPCI J5 connector	Depends on module
14		I/O	PMC #2 connection to cPCI J5 connector	Depends on module
15		I/O	PMC #2 connection to cPCI J5 connector	Depends on module
16		I/O	PMC #2 connection to cPCI J5 connector	Depends on module
17		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
18		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
19		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
20		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
21		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
22		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
23		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
24		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
25		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
26		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
27		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
28		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
29		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
30		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
31		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
32		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
33		I/O	PMC #2 connection to cPCI J3 connector	Depends on module

TABLE A.18: J24 Connector Description (Pn4/Jn4 User Defined I/O) (Continued)

J24 Pin No.	cPCI J5, J3 Pin Number	Direction	Description	Electrical Characteristics
34		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
35		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
36		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
37		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
38		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
39		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
40		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
41		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
42		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
43		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
44		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
45		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
46		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
47		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
48		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
49		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
50		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
51		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
52		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
53		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
54		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
55		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
56		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
57		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
58		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
59		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
60		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
61		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
62		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
63		I/O	PMC #2 connection to cPCI J3 connector	Depends on module
64		I/O	PMC #2 connection to cPCI J3 connector	Depends on module

PMC TO CPCI CONNECTOR MAPPING FOR DIFFERENTIAL SIGNALING

TABLE A.19: PMC to cPCI Connector Mapping for Differential Signaling

J14 to cPCI Pair #	J14 Pins	cPCI J5 Pins (PMC Site 1)	J24 to cPCI Pair #	J24 Pins	cPCI J3/J5 Pins (PMC Site 2)	
1	1, 3	D20, E20	33	1, 3	D4, E4	cPCI Connector J5
2	2, 4	A20, B20	34	2, 4	A4, B4	
3	5, 7	D19, E19	35	5, 7	D3, E3	
4	6, 8	A19, B19	36	6, 8	A3, B3	
5	9, 11	D18, E18	37	9, 11	D2, E2	
6	10, 12	A18, B18	38	10, 12	A2, B2	
7	13, 15	D17, E17	39	13, 15	D1, E1	
8	14, 16	A17, B17	40	14, 16	A1, B1	
9	17, 19	D16, E16	41	17, 19	D12, E12	cPCI Connector J3
10	18, 20	A16, B16	42	18, 20	A12, B12	
11	21, 23	D15, E15	43	21, 23	D11, E11	
12	22, 24	A15, B15	44	22, 24	A11, B11	
13	25, 27	D14, E14	45	25, 27	D10, E10	
14	26, 28	A14, B14	46	26, 28	A10, B10	
15	29, 31	D13, E13	47	29, 31	D9, E9	
16	30, 32	A13, B13	48	30, 32	A9, B9	
17	33, 35	D12, E12	49	33, 35	D8, E8	
18	34, 36	A12, B12	50	34, 36	A8, B8	
19	37, 39	D11, E11	51	37, 39	D7, E7	
20	38, 40	A11, B11	52	38, 40	A7, B7	
21	41, 43	D10, E10	53	41, 43	D6, E6	
22	42, 44	A10, B10	54	42, 44	A6, B6	
23	45, 47	D9, E9	55	45, 47	D5, E5	
24	46, 48	A9, B9	56	46, 48	A5, B5	
25	49, 51	D8, E8	57	49, 51	D4, E4	
26	50, 52	A8, B8	58	50, 52	A4, B4	
27	53, 55	D7, E7	59	53, 55	D3, E3	
28	54, 56	A7, B7	60	54, 56	A3, B3	
29	57, 59	D6, E6	61	57, 59	D2, E2	
30	58, 60	A6, B6	62	58, 60	A2, B2	
31	61, 63	D5, E5	63	61, 63	D1, E1	
32	62, 64	A5, B5	64	62, 64	A1, B1	

PMC TO CPCI CONNECTOR MAPPING FOR SINGLE-ENDED SIGNALING

TABLE A.20: PMC to cPCI Connector Mapping for Single-Ended Signaling

J14/J24 Pin #	cPCI J5 Pins (PMC Site 1)	cPCI J3/J5 Pins (PMC Site 2)		J14/J24 Pin #	cPCI J5 Pins (PMC Site 1)	cPCI J3 Pins (PMC Site 2)	
1	D20	D	cPCI Connector J5 (PMC 2 only)	33	D12	D8	cPCI Connector J3 (PMC 2 only)
2	A20	A		34	A12	A8	
3	E20	E		35	E12	E8	
4	B20	B		36	B12	B8	
5	D19	D		37	D11	D7	
6	A19	A		38	A11	A7	
7	E19	E		39	E11	E7	
8	B19	B		40	B11	B7	
9	D18	D		41	D10	D6	
10	A18	A		42	A10	A6	
11	E18	E		43	E10	E6	
12	B18	B		44	B10	B6	
13	D17	D		45	D9	D5	
14	A17	A		46	A9	A5	
15	E17	E		47	E9	E5	
16	B17	B		48	B9	B5	
17	D16	D	cPCI Connector J3 (PMC 2 only)	49	D8	D4	
18	A16	A		50	A8	A4	
19	E16	E		51	E8	E4	
20	B16	B		52	B8	B4	
21	D15	D		53	D7	D3	
22	A15	A		54	A7	A3	
23	E15	E		55	E7	E3	
24	B15	B		56	B7	B3	
25	D14	D		57	D6	D2	
26	A14	A		58	A6	A2	
27	E14	E		59	E6	E2	
28	B14	B		60	B6	B2	
29	D13	D		61	D5	D1	
30	A13	A		62	A5	A1	
31	E13	E		63	E5	E1	
32	B13	B		64	B5	B1	

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