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PCI-DAS1602/16

Specifications

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Specifications

Typical for 25 °C unless otherwise specified.

Specifications in *italic text* are guaranteed by design.

All specifications are subject to change without notice.

Analog input

Table 1. Analog input specifications

A/D converter type	AD976ABN
Resolution	16 bits
Number of channels	16 single-ended / 8 differential, software selectable
Input ranges, software selectable	±10 V, ±5 V, ±2.5 V, ±1.25 V 0 to 10 V, 0 to 5 V, 0 to 2.5 V, 0 to 1.25 V
Polarity	Unipolar/bipolar, software selectable
A/D pacing (software programmable)	Internal counter - 82C54.
	External source (A/D EXTERNAL PACER)
	Software polled
Burst mode	Software selectable option, rate = 5 µs
A/D trigger sources	External digital (A/D EXTERNAL TRIGGER)
	External analog (ANALOG TRIGGER IN)
A/D triggering modes	External digital: Software configurable for: ▪ Edge (triggered) ▪ Level-activated (gated) ▪ Programmable polarity (rising/falling edge trigger, high/low gate)
	External analog: software-configurable for: ▪ Positive or negative slope. ▪ Above or below reference ▪ Positive or negative hysteresis ▪ In or out of window Trigger levels set by DAC0 and/or DAC1, 4.88 mV resolution.
	Unlimited pre- and post-trigger samples. Total # of samples must be > 256. Compatible with both Digital and Analog trigger options.
Data transfer	From 512 sample FIFO via interrupt w/ REPINSW
	Interrupt
	Software polled
A/D conversion time	*5 µs max*
Throughput	200 kHz
Calibration	Auto-calibration, calibration factors for each range stored on board in non-volatile RAM.
Common mode range	±10 V min
CMRR @ 60 Hz	-70 dB
Input leakage current	*±200 nA max*
Input impedance	*10 MΩ min*
Absolute maximum input voltage	*±15 V*

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Accuracy

Table 2. Analog input accuracy specifications

Range	**Accuracy**
BIP10	±16 LSB
BIP5	±6 LSB
BIP2.5	±16 LSB
BIP1.25	±16 LSB
UNI10	±8 LSB
UNI5	±28 LSB
UNI2.5	±28 LSB
UNI1.25	±28 LSB
Accuracy Components	
Gain error	Trimmable by potentiometer to 0
Offset error	Trimmable by potentiometer to 0
PGA linearity error	*±1.3 LSB typ , ±10.0 LSB max*
Integral linearity error	±0.5 LSB typ , ±3.0 LSB max
Differential linearity error	±0.5 LSB typ, ±2.0 LSB max

Total board error is a combination of gain, offset, differential linearity and integral linearity error. The theoretical absolute accuracy of the board may be calculated by summing these component errors. Worst case error is realized only in the unlikely event that each of the component errors is at their maximum level, and causing error in the same direction.

Analog input drift

Table 3. Analog input drift specifications

Range	**Analog input full-scale gain drift**	**Analog input zero drift**	**Overall analog input drift**
± 10.00 V	2.2 LSB/°C max	1.8 LSB/°C max	4.0 LSB/°C max
± 5.000 V	2.2 LSB/°C max	1.9 LSB/°C max	4.1 LSB/°C max
± 2.500 V	2.2 LSB/°C max	2.0 LSB/°C max	4.2 LSB/°C max
± 1.250 V	2.2 LSB/°C max	2.3 LSB/°C max	4.5 LSB/°C max
0 - 10.00 V	4.1 LSB/°C max	1.9 LSB/°C max	6.0 LSB/°C max
0 - 5.000 V	4.1 LSB/°C max	2.1 LSB/°C max	6.2 LSB/°C max
0 - 2.500 V	4.1 LSB/°C max	2.4 LSB/°C max	6.5 LSB/°C max
0 - 1.250 V	4.1 LSB/°C max	3.0 LSB/°C max	7.1 LSB/°C max

Absolute error change per °C temperature change is a combination of the Gain and Offset drift of many components. The theoretical worst case error of the board may be calculated by summing these component errors. Worst case error is realized only in the unlikely event that each of the component errors is at their maximum level, and causing error in the same direction.

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Noise performance

The following table summarizes the worst case noise performance for the PCI-DAS1602/16. Noise distribution is determined by gathering 50000 samples with inputs tied to ground at the PCI-DAS1602/16 main connector. Data is for both single-ended and differential modes of operation.

Table 4. Noise specifications

Range	±2 counts	±1 count	Max Counts	LSBrms*
± 10.00 V	97%	80%	11	1.7
± 5.000 V	97%	80%	11	1.7
± 2.500 V	96%	79%	11	1.7
± 1.250 V	96%	79%	11	1.7
0 - 10.00 V	88%	65%	15	2.3
0 - 5.000 V	88%	65%	15	2.3
0 - 2.500 V	83%	61%	15	2.3
0 - 1.250 V	83%	61%	16	2.4

* Input noise is assumed to be Gaussian. An RMS noise value from a Gaussian distribution is calculated by dividing the peak-to-peak bin spread by 6.6.

Crosstalk

Crosstalk is defined here as the influence of one channel upon another when scanning two channels at the specified per channel rate for a total of 50000 samples. A full scale 100 Hz triangle wave is input on channel 1. Channel 0 is tied to analog ground at the 100-pin user connector. Table 5 summarizes the influence of channel 1 on channel 0 and does not include the effects of noise.

Table 5. Crosstalk specifications

Range	1 kHz Crosstalk (LSB pk-pk)	10 kHz Crosstalk (LSB pk-pk)	50 kHz Crosstalk (LSB pk-pk)
±10.000 V	4	13	24
±5.000 V	2	7	18
±2.500 V	2	5	16
±1.250 V	3	4	14
0V to +10.000 V	4	8	23
0V to +5.000 V	2	5	16
0V to +2.500 V	2	4	16
0V to +1.250 V	3	3	16

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Analog output

Table 6. Analog output specifications

D/A converter type	AD669BR
Resolution	16 bits
Number of channels	2
Channel type	Single-ended voltage output
Output range (each channel independently software selectable)	±10 V, ±5 V, 0 to 10 V, or 0 to 5 V
Data transfer	From 512 sample FIFO via REPOUTSW or programmed I/O. Data interleaved for dual analog output mode.
Throughput	100 kHz, 2 channels simultaneous
Monotonicity	*16 bits at 25 °C*
Slew rate	10 V ranges: 6 V/µs
	5 V ranges: 3 V/µs
Settling time	13 µS max 20 V step to 0.0008%
	6 µS typ 10V step to 0.0008%
Current drive	±5 mA min
Output short-circuit duration	*Indefinite @ 25 mA*
Output coupling	*DC*
Output impedance	0.1 ohms max
Output stability	Any passive load
Coding	Offset binary
Output voltage on power up and reset	0 V ± 10 mV

Accuracy

Table 7. Analog output accuracy specifications

Range	**Accuracy**
BIP10	±8 LSB
BIP5	±8 LSB
UNI10	±10 LSB
UNI5	±10 LSB
Accuracy Components	
Integral linearity error	±0.5 LSB typ, ±1 LSB max
Differential linearity error	*±0.5 LSB typ, ±1 LSB max*

Analog output drift

Table 8. Analog output drift specifications

Analog output full-scale gain drift	±0.22 LSB/°C max
Analog output zero drift	±0.22 LSB/°C max
Overall analog output drift	±0.44 LSB/°C max

Absolute error change per °C temperature change is a combination of the gain and offset drift of many components. The theoretical worst case error of the board may be calculated by summing these component errors. Worst case error is realized only in the unlikely event that each of the component errors is at their maximum level, and causing error in the same direction.

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Digital input / output

Table 9. Digital input/output specifications

Digital type	82C55 emulation
	Input 74LS244
	Output 74LS373
Number of I/O	24
Configuration	2 banks of 8 and 2 banks of 4, or
	3 banks of 8, or
	2 banks of 8 with handshake
Input high	*2.0 volts min, 7 volts absolute max*
Input low	*0.8 volts max, -0.5 volts absolute min*
Output high	*2.4 volts min @ -15 mA*
Output low	*0.5 volts max @ 64 mA*
Power-up / reset state	Input mode (high impedance)
Pull-up/pull-down resistors	Provisions have been made on the board for user installed pull-up/pull-down resistor networks
Simultaneous sample and hold trigger	TTL output (SSH OUT). Logic 0 = Hold Logic 1 = Sample compatible with CIO-SSH16

Interrupts

Table 10. Interrupt specifications

Interrupt	INTA# - mapped to IRQn via PCI BIOS at boot-time
Interrupt enable	Programmable through PLX9052
Interrupt polarity	Active high level or active low level, programmable through PLX9052
Interrupt sources (software programmable)	External (rising TTL edge event)
	Residual counter
	A/D End-of-conversion
	A/D End-of-channel-scan
	A/D FIFO-not-empty
	A/D FIFO-half-full
	D/A FIFO-not-empty
	D/A FIFO-half-full

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Counter

*Note: Pins 21, 24, and 25 are pulled to logic high via 10K resistors.

Table 11. Counter specifications

Counter type	82C54	
Configuration	Two 82C54 chips containing three 16-bit down counters each	
82C54A:		
Counter 0 — ADC residual sample counter.	Source:	ADC Clock.
	Gate:	Programmable source.
	Output:	End-of-Acquisition interrupt.
Counter 1 — ADC pacer lower divider	Source:	10 MHz oscillator
	Gate:	Tied to Counter 2 gate, programmable source.
	Output:	Chained to Counter 2 Clock.
Counter 2 — ADC pacer upper divider	Source:	Counter 1 Output.
	Gate:	Tied to Counter 1 gate, programmable source.
	Output:	ADC Pacer clock (if software selected), available at user connector.
82C54B:		
Counter 0 — pretrigger mode	Source:	ADC Clock.
	Gate:	External trigger
	Output:	End-of-Acquisition interrupt.
Counter 0 — non-pretrigger mode: user counter 4	Source:	User input at 100pin connector or internal 10MHz (software selectable)
	Gate:	User input at 100pin connector.
	Output:	Available at 100pin connector.
Counter 1 — DAC pacer lower divider	Source:	10 MHz oscillator
	Gate:	Tied to Counter 2 gate, programmable source.
	Output:	Chained to Counter 2 Clock.
Counter 2 — DAC pacer upper divider	Source:	Counter 1 Output.
	Gate:	Tied to Counter 1 gate, programmable source.
	Output:	DAC Pacer clock, available at user connector.
Clock input frequency	*10 MHz max*	
High pulse width (clock input)	*30 ns min*	
Low pulse width (clock input)	*50 ns min*	
Gate width high	*50 ns min*	
Gate width low	*50 ns min*	
Input high	*2.0 volts min, 5.5 volts absolute max*	
Input low	*0.8 volts max, -0.5 volts absolute min*	
Output high	*3.0 volts min @ -2.5 mA*	
Output low	*0.4 volts max @ 2.5 mA*	
Crystal oscillator frequency	10 MHz	
Frequency accuracy	50 ppm	

Power consumption

Table 12. Power consumption specifications

+5 V operating (A/D converting to FIFO)	2 A typical, 2.1 A max

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Environmental

Table 13. Environmental specifications

Operating temperature range	0 to 70 °C
Storage temperature range	-40 to 100 °C
Humidity	0 to 95% non-condensing

Mechanical

Table 14. Mechanical specifications

Card dimensions	PCI custom type card: 107 mm (H) x 18.5 mm (W) x 292 mm (L)

Main connector and pin out

Table 15. Main connector specifications

Connector type	100-pin high-density, Robinson-Nugent
Compatible cables	C100FF-x
Compatible accessory products (with C100FF-x cable)	ISO-RACK16/P ISO-DA02/P BNC-16SE BNC-16DI CIO-MINI50 CIO-TERM100 SCB-50 SSR-RACK24 (DADP-5037 adaptor required) SSR-RACK08 (DADP-5037 adaptor required) CIO-ERB24 (DADP-5037 adaptor required) CIO-ERB08 (DADP-5037 adaptor required)

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Table 16. 8-channel differential mode

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	FIRSTPORTA Bit 0
2	CH0 HI	52	FIRSTPORTA Bit 1
3	CH0 LO	53	FIRSTPORTA Bit 2
4	CH1 HI	54	FIRSTPORTA Bit 3
5	CH1 LO	55	FIRSTPORTA Bit 4
6	CH2 HI	56	FIRSTPORTA Bit 5
7	CH2 LO	57	FIRSTPORTA Bit 6
8	CH3 HI	58	FIRSTPORTA Bit 7
9	CH3 LO	59	FIRSTPORTB Bit 0
10	CH4 HI	60	FIRSTPORTB Bit 1
11	CH4 LO	61	FIRSTPORTB Bit 2
12	CH5 HI	62	FIRSTPORTB Bit 3
13	CH5 LO	63	FIRSTPORTB Bit 4
14	CH6 HI	64	FIRSTPORTB Bit 5
15	CH6 LO	65	FIRSTPORTB Bit 6
16	CH7 HI	66	FIRSTPORTB Bit 7
17	CH7 LO	67	FIRSTPORTC Bit 0
18	LLGND	68	FIRSTPORTC Bit 1
19	N/C	69	FIRSTPORTC Bit 2
20	N/C	70	FIRSTPORTC Bit 3
21	N/C	71	FIRSTPORTC Bit 4
22	N/C	72	FIRSTPORTC Bit 5
23	N/C	73	FIRSTPORTC Bit 6
24	N/C	74	FIRSTPORTC Bit 7
25	N/C	75	N/C
26	N/C	76	N/C
27	N/C	77	N/C
28	N/C	78	N/C
29	N/C	79	N/C
30	N/C	80	N/C
31	N/C	81	N/C
32	N/C	82	N/C
33	N/C	83	N/C
34	N/C	84	N/C
35	D/A GND 0	85	N/C
36	D/A OUT 0	86	N/C
37	D/A GND 1	87	N/C
38	D/A OUT 1	88	N/C
39	CTR4 CLK	89	GND
40	CTR4 GATE	90	+12V
41	CTR4 OUT	91	GND
42	A/D EXTERNAL PACER	92	-12V
43	ANALOG TRIGGER IN	93	N/C
44	D/A EXTERNAL PACER IN	94	N/C
45	A/D EXTERNAL TRIGGER IN	95	A/D INTERNAL PACER OUTPUT
46	N/C	96	D/A INTERNAL PACER OUTPUT
47	N/C	97	EXTERNAL D/A PACER GATE
48	PC +5V	98	N/C
49	SSH OUT	99	EXTERNAL INTERRUPT
50	GND	100	GND

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Table 17. 16-channel single-ended mode

Pin	Signal Name	Pin	Signal Name
1	LLGND	51	FIRSTPORTA Bit 0
2	CH0 HI	52	FIRSTPORTA Bit 1
3	CH8 HI	53	FIRSTPORTA Bit 2
4	CH1 HI	54	FIRSTPORTA Bit 3
5	CH9 HI	55	FIRSTPORTA Bit 4
6	CH2 HI	56	FIRSTPORTA Bit 5
7	CH10 HI	57	FIRSTPORTA Bit 6
8	CH3 HI	58	FIRSTPORTA Bit 7
9	CH11 HI	59	FIRSTPORTB Bit 0
10	CH4 HI	60	FIRSTPORTB Bit 1
11	CH12 HI	61	FIRSTPORTB Bit 2
12	CH5 HI	62	FIRSTPORTB Bit 3
13	CH13 HI	63	FIRSTPORTB Bit 4
14	CH6 HI	64	FIRSTPORTB Bit 5
15	CH14 HI	65	FIRSTPORTB Bit 6
16	CH7 HI	66	FIRSTPORTB Bit 7
17	CH15 HI	67	FIRSTPORTC Bit 0
18	LLGND	68	FIRSTPORTC Bit 1
19	N/C	69	FIRSTPORTC Bit 2
20	N/C	70	FIRSTPORTC Bit 3
21	N/C	71	FIRSTPORTC Bit 4
22	N/C	72	FIRSTPORTC Bit 5
23	N/C	73	FIRSTPORTC Bit 6
24	N/C	74	FIRSTPORTC Bit 7
25	N/C	75	N/C
26	N/C	76	N/C
27	N/C	77	N/C
28	N/C	78	N/C
29	N/C	79	N/C
30	N/C	80	N/C
31	N/C	81	N/C
32	N/C	82	N/C
33	N/C	83	N/C
34	N/C	84	N/C
35	D/A GND 0	85	N/C
36	D/A OUT 0	86	N/C
37	D/A GND 1	87	N/C
38	D/A OUT 1	88	N/C
39	CTR4 CLK	89	GND
40	CTR4 GATE	90	+12V
41	CTR4 OUT	91	GND
42	A/D EXTERNAL PACER	92	-12V
43	ANALOG TRIGGER IN	93	N/C
44	D/A EXTERNAL PACER IN	94	N/C
45	A/D EXTERNAL TRIGGER IN	95	A/D INTERNAL PACER OUTPUT
46	N/C	96	D/A INTERNAL PACER OUTPUT
47	N/C	97	EXTERNAL D/A PACER GATE
48	PC +5V	98	N/C
49	SSH OUT	99	EXTERNAL INTERRUPT
50	GND	100	GND

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