Omnibyte *Omnimodule** Products

Listed below are brief descriptions of Omnibyte's current Omnimodules. Omnimodules are daughter-card style I/O expansion modules designed for Omnibyte board level computer products. If you have a upcoming requirement and would like more information on how Omnibyte can help ***you*** design a custom Omnimodule - see the Omnimodule Specification Summary, or give us a call... For information on a listed product, click on the underlined title. Please refer to our home page for e-mail address and phone and fax numbers.

- **Serial I/O**
  - **OM/2SA2** - Provides 2 RS232C buffered serial ports using a 68681 DUART.
  - **OM/2SAS2** - Provides 2 RS232C buffered serial ports using a 68564 DUSART.
  - **OM/2SA4** - Provides 2 RS422 buffered serial ports using a 68681 DUART.
  - **OM/8SA2** - Provides 8 RS232C buffered serial ports using a SCC2698 Octal UART.
- **Parallel I/O**
  - **OM/20PUB** - Provides 20 lines of unbuffered parallel I/O using a 68230 PI/T.
  - **OM/PIT-A** - This Omnimodule is the 20PUB (above) with AS645 buffers.
  - **OM/PIT-L** - This Omnimodule is the 20PUB (above) with LS645 buffers.
  - **OM/PIT-L1** - This Omnimodule is the 20PUB (above) with LS645-1 buffers.
  - **OM/PIT48** - Provides 48 lines of unbuffered parallel I/O using 2 68230 PI/Ts.
  - **OM/CPI** - Provides a Centronics compatible parallel printer interface using a 68230 PI/T.
- **Combination of Serial and Parallel I/O**
  - **OM/2SA2-20PUB** - Provides 2 RS232C serial ports using a 68681 DUART and 20 lines of unbuffered parallel I/O using a 68230 PI/T.
- **Interfaces to other buses**
  - **OM/SCSI** - Provides a SCSI interface using an AMD5380 controller.
  - **OM/488** - Provides an IEEE488 (GPIB) interface using a TMS9914A.
- **Other I/O**
  - **OM/DTMF** - Provides a DTMF (touch-tone) interface.
  - **OM/CC** - Provides a real-time calendar clock for system use.
- **Prototyping**
  - **OM/KLUGE** - This is a standard size blank Omnimodule (with holes) for prototyping use.
  - **OM/KLUGE-DW** - This is a double-wide blank Omnimodule (with holes) for prototyping use (VIO & VSBC1 only)

Omnimodule Specification Summary *(Back)*

The complete Omnimodule specification is available from Omnibyte. We recommend that you obtain a copy of this specification before you attempt to design your own Omnimodules. The following is a brief summary of this specification. It should help with the decision of determining if

Omnimodules are right choice for your project.

Introduction

An 80-pin gas tight connector electrically connects the Omnimodule to the baseboard. The Omnimodules are mechanically secured to the baseboard with four sets of nylon screws and threaded spacers.

The functionality of the interconnect signals between the baseboard and the Omnimodule are patterned after the VMEbus protocol. It is appropriate for 12 address lines, (8 dedicated and 4 user definable) and 16 bi-directional data lines, including interrupt and DMA features. The timing for the baseboard Omnimodule interface is based on the 68000-type asynchronous bus structure. The identity of individual Omnimodules can be self-recognized by the base board. The baseboard accomplishes this by reading the module identification lines (MODID0-MODID5, prespecified and user definable) from the Omnimodule.

Data Transfer Signals

- **Al-A8 (Address Lines) -** 8 dedicated address lines, 4 additional addresses A9-A12 are user definable as UDEF0-UDEF3 signals (see UDEF0-UDEF5).
- **D0-D15 (Data Lines)** - 16 bidirectional data lines organized as 8 lines each of low byte (D0-D7) and high byte (D8-D15). Byte and Word transfers are supported.

Data Transfer Control Signals

- **/MODSEL (Module Select) -** Active low generated by base-board activates expansion module.
- **R/W (Read/Write) -** Microprocessor R/W signal with low indicating write to, and high indicating read from, an Omnimodule.
- **/MDS0 and /MDS1 (Module Data Strobes) -** Active low microprocessor signals indicate byte(s) of data lines activated. Falling edge used in I/O read-write operations.
- **/MDTACK (Module Data Transfer Acknowledge) -** Open collector, active low signal used in reading of valid latched data, indicating data received and the termination of bus cycles.
- **/RESET (Reset) -** Active low signal generated from the base-board indicating a reset condition.
- **8MHz and 4MHz Clocks -** Two clock signals generated by the base-board for use by the Omnimodule.

Data Transfer DMA Signals

Functioning of the DMA request and acknowledge signals reference the 63450 four channel DMA controller communication protocol.

- **/DMAREQ0, /DMAREQ1 (Direct Memory Request)** - Two active low signals request initiation of a DMA cycle to the base-board. Upon receipt by the DMA controller, bus arbitration begins. Cycle steal and burst modes are supported.
- **/DMAACK0, DMAACK1 (Direct Memory Access Acknowledge)** - Two active low signals from the DMA controller enable the specified port on the Omnimodule to transfer data.
- **/DONE (Done) -** Bi-directional signal used with DMAACK0, DMAACK1 indicating that the last data transfer is being completed.
- **/DTC (Data Transfer Complete) -** Output signal by the DMA controller and used with DMAACK0, DMAACK1 indicating data has been successfully transferred.
- **/PCL0, /PCL1 (Peripheral Control Lines) -** Bi-directional signals to the DMA controller that control the DMA operations of specified channel.

Priority Interrupt Signals

- **/IRQ0, IRQ1 (Interrupt Request) -** Active low signals requesting interrupt servicing by the Omnimodule. The IRQ line is negated after an interrupt vector is provided by the baseboard or Omnimodule.
- **/IACK0, IACK1 (Interrupt Acknowledge) -** Active low signals to the Omnimodule that acknowledge an interrupt request from the base-board.

I/O and Utility Signals

- **I/O-1 to I/O-20 (I/O Lines)** - Twenty lines of I/O are routed and available at the user's choice of two locations which are:
  - Through the 80-pin connector for discretional connection to the P2 connector of the VME baseboard.
  - To connectors on the Omnimodule for discretionary direct connection to the module front panel.
- **/MODPRES (Module Present)** - The baseboard reads an active low signal on the Omnimodule. It is pulled low by a ground strap and indicates that a module is inserted and available for communication with baseboard.
- **MODID0-MODID5 (Module Identification)** - The base-board reads six lines from the Omnimodule to determine the identity of the inserted Omnimodule from each type of modules' unique 6 bit code. Module ID's are also user definable.
- **UDEFO-UDEF5 (User Definable Lines)** - Six lines available for user-specified interconnect to the baseboard. These are appropriate for wire wrap or jumper connect use.
- **Power Lines -** The base board supplies +5.0VDC at 2.0 A. (max.) and +12.0VDC at 1.0 A. (max.). GND is provided, with max. 3.0A. rating.

Omnimodule Electrical Specifications

The Omnimodule specification document contains timing diagrams and AC electrical specifications for read, write, interrupt acknowledge, and the DMA single address read and write operations. Driver and receiver specifications are also contained in the Omnimodule specification document. It will be necessary for anyone designing an Omnimodule to follow these specifications.

Top of page