HARDWARE COMPONENTS

Table 1.1 lists the hardware components needed to complete the development environment. Ensure you have these items before proceeding with the setup process. Place checks in the first column of each item to track each item.

TABLE 1.1: Hardware Components Checklist

✓	Quantity	Description
	1	VME chassis 64x [1]
	1	CWCEC CHAMP-FX (SVME/DMV-430) cards
	1	Serial cable (CBL-430-020)
	1	P0 Rear Panel Cable (CBL-430-000)
	1	P2 Rear Panel Cable (CBL-430-001)
	1	Host computer or laptop
	4	CAT-5E patch cables

1. A VME chassis capable of providing +5 and +3.3 volts. If you intend to use PMCs, your chassis may also need to provide +12 and -12 volts.

SOFTWARE COMPONENTS

Table 1.2 lists the software components needed to complete the development environment. Ensure you have these items before proceeding with the setup process. Place checks in the first column of each item to track each item.

TABLE 1.2: Software Components Checklist

✓	Quantity	Description
	1	CHAMPtools-FX Development tools (DSW-430-000-CD)

FPGA DEVELOPMENT ENVIRONMENT

Table 1.3 lists the FPGA development environment components needed to complete the development environment. Ensure you have these items before proceeding with the setup process. Place checks in the first column of each item to track each item.

TABLE 1.3: FPGA Development Environment Checklist

✓	Quantity	Description
	1	Xilinx ISE FPGA design implementation tools version 7.1 or later
	1	Xilinx Embedded Development Kit (EDK) version 7.1 [1]
	1	Xilinx® ChipScope™ Pro version 7.1 or later (Xilinx PN DO-CSP-PRO) [2]
	1	Xilinx Parallel Cable IV (Xilinx PN HW-PC4) [3]
	1	Model Technology™ ModelSim® for VHDL version 6.0 PE/SE (or later) [4]

1. CHAMPtools-FX Release 1.4 requires EDK version 7.1. If you would like to use a different EDK version, contact Curtiss-Wright Controls Embedded Computing.
2. ChipScope Pro is not required for development, but is highly recommended as a debugging tool.
3. This cable is required if you plan to download files to the CHAMP-FX board.
4. ModelSim PE requires SWIFT support which is a ModelSim Add-on feature.

2 HARDWARE INSTALLATION

In this chapter...

This chapter provides the instructions needed to verify the board is operational and properly configured.

INTRODUCTION

As delivered, the CHAMP-FX board is capable of interacting with a terminal emulator program before installing any software on the host system. Follow the instructions in this chapter to verify the board is operational and properly configured.

SERIAL PORT CONFIGURATION

Configure the terminal emulator program for the parameters indicated in Front Panel Serial I/O Configuration.

TABLE 2.1: Front Panel Serial I/O Configuration

Parameter	Value
Baud Rate	57,600 bps
Parity	None
Data Bits	8
Stop Bits	1 or 2
Handshake	Software (xon/xoff)

UNPACKING THE CARD

To unpack the card from its protective package, follow these steps:

1. Unpack the Circuit Card Assembly from the shipping carton in a suitable work area. If the shipping carton appears to be damaged, request that an agent of the shipper or carrier be present during unpacking and inspection.
2. Find the packing list. Make sure all the items on the list are present.
3. Save the packing material for storing or reshipping the card.
4. If your CHAMP-FX was shipped with PMC modules installed, make sure they are firmly attached to your basecard.

Warning

The PMC sites on the CHAMP-FX support 3.3V signalling only. Due to board real-estate restrictions, the CHAMP-FX does not provide 5V or 3.3V keying pins. Instead a warning label is mounted on the board to indicate that the PMC sites are 3.3V only.

CONFIGURING JUMPERS

Table 3.2 defines the jumper groups on the CHAMP-FX (see Figure 2.1 on page 2-4 to view their physical locations). Jumpers are available for selecting various board operational modes.

Warning

Please make sure that the board is not powered on when configuring board jumpers and that you observe proper static control procedures when handling the card.

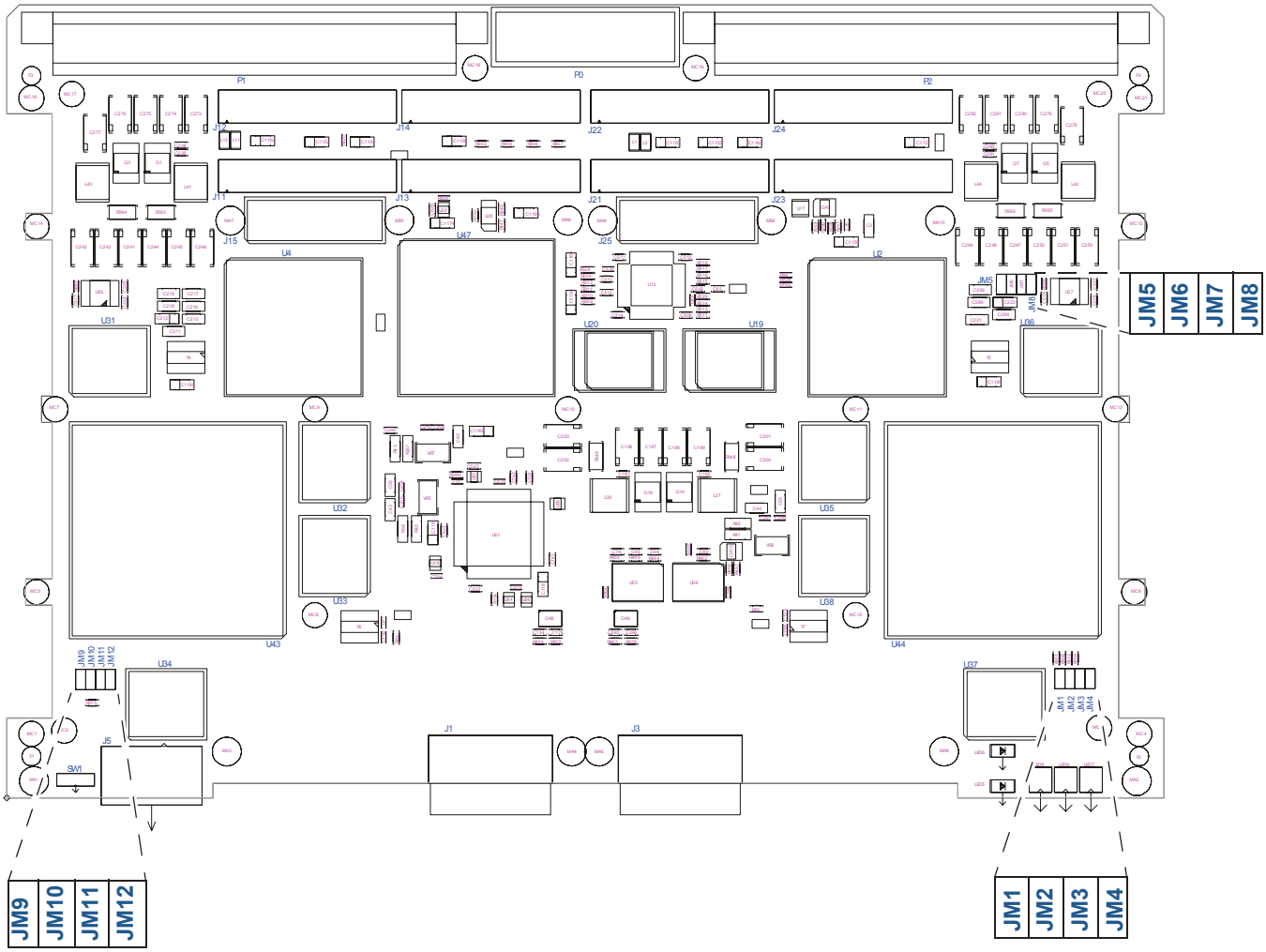
TABLE 2.2: Jumper Block Definition

Jumper	On	Off	Default
JM1	Pro A FPGA user definable, software readable jumpers		OFF
JM2			OFF
JM3	Pro B FPGA user definable, software readable jumpers		OFF
JM4			OFF
JM5	StarGen Bridge on PCI bus 1 operates as root device	StarGen Bridge on PCI bus 1 operates as leaf device	OFF
JM6	StarGen Bridge on PCI bus 1 operates in PCI legacy (address routed) Mode	StarGen Bridge on PCI bus 1 operates in Gateway (path routed) Mode	OFF
JM7	StarGen Bridge on PCI bus 2 operates as root device	StarGen Bridge on PCI bus 2 operates as leaf device	OFF
JM8	StarGen Bridge on PCI bus 2 operates in PCI legacy (address routed) Mode	StarGen Bridge on PCI bus 2 operates in Gateway (path routed) Mode	OFF
JM9	Inhibits writes to Flash	Allows writes to Flash	OFF
JM10	Execute PBIT on power up	Do not execute PBIT on power up	OFF
JM11	Enable JTAG Mode	Normal (non-JTAG) operation	OFF
JM12	Boot Inhibit Application	Boot Application	OFF

Cross Reference

Refer to the CHAMPtools-FX Software User's Manual for additional information describing the various boot modes.

FIGURE 2.1: Configuration Jumper Locations



POWERING UP A CHAMP-FX

INSERT THE BASECARD IN THE CHASSIS

Ensure that the chassis power is turned off before inserting the card.

SVME Air-Cooled L000/100 CHAMP-FX

An SVME basecard is equipped with a faceplate compliant with IEEE 1101.10. The large ejectors on this faceplate facilitate insertion of the basecard into the 160-contact, 5-row connectors for P1 and P2.

Once the basecard is inserted in the chassis, secure it by tightening the screws at the top and bottom of the faceplate.

DMV Conduction-Cooled L100/200 CHAMP-FX

With DMV basecards, you must use a significant amount of insertion force to mate the backplane connectors with the VME backplane. Use extra care when aligning and inserting your basecard into your chassis, to ensure that a secure mechanical and electrical connection is made between the card and the backplane mating connectors.

Once the basecard is inserted in the chassis, use a torque driver/wrench to tighten the wedgelocks at the top and bottom of the card. The required torque is 6 in-lbs.

CONNECT A TERMINAL

Warning

Tera Term Pro is strongly recommended for use for the terminal emulator. The CHAMP-FX board has been verified to work using this emulator; using other terminal emulators may result in undesirable results. Tera Term Pro can be downloaded and installed from the following website: http://hp.vector.co.jp/authors/VA002416/teraterm.html.

In order to access the features available within the embedded firmware on the CHAMP-FX, you'll need to attach a terminal or PC-emulated equivalent to the Serial Port 1 interface on the card. You can connect a terminal to the CHAMP-FX in one of the following ways:

- via the front panel serial port J5 connector using a serial cable such as CAFP1 (for the SVME version product only);
- via the P0 connector using a P0 interface cable such as CBL-430-000, available from Dy 4 Systems (for both SVME and DMV version products).

Tip

Default serial communication parameters are 57600, N, 8, 1 (57600 baud, no parity, 8 bits, 1 stop bit). Set flow control to "None".

CABLE CONNECTIONS

The cable assemblies described in "Hardware Components" on page 1-2 are available from Dy 4 Systems by ordering individual cables by their part numbers. Should you need to develop your own cabling solution, please refer to Appendix A of the CHAMP-FX FPGA Accelerator (SVME/DMV-430) User's Manual (document 813165) for complete interface pinout listings for the J5, P0, and P2 interfaces.

Serial Communications via the Front Panel J5 Connector

The CHAMP-FX has a 9-pin connector (J5) on the front panel that provides access to EIA-232 Configurator Serial Port. The signal mapping for Configurator Serial Port is shown in Table 2.3.

TABLE 2.3: Front Panel Cable Signal Mapping

Signal Name	CHAMP-FX Front Panel J5 Connector	Cable Micro-D, 9 Pin Connector (attaches to CHAMP-FX front panel)	Configurator Serial Port DB-09 Female Connector (attaches to terminal)
GND	J5-5	P1-5	P2-5
C_232RX	J5-3	P1-3	P2-3
C_232TX	J5-2	P1-2	P2-2

Note

The CHAMP-FX front panel connector does not provide access to the CTS and RTS signals.

Note

The CHAMP-FX EIA-232 serial channels are configured as DCE (Data Communications Equipment). The EIA-232 serial channels on personal computers and terminals are configured as DTE, therefore a null modem is NOT required for communication between the CHAMP-FX and a PC terminal.

StarFabric Connectivity

StarGen StarFabric™ is native to the CHAMP-FX baseboard so a PMC is not required. StarFabric links are accessible using CBL-430-001; or alternately using the StarFabric (P2) Rear Transition Module shown in Figure 2.2.

The Rear Transition module only supports StarFabric connectivity, i.e. it does not support any of the other P2 signals. In addition, if the StarLink Rear Transition Module is used the P0 cable cannot be used.

Cross Reference

Two backplane interface cables have been developed specifically for the CHAMP-FX, namely CBL-430-000 and CBL-430-001. Refer to "Configuring an Emulator for use with CHAMP-FX" on page 2-8 for further information about these cables and how they may be used to connect to an emulator.

FIGURE 2.2: StarLink Rear Transition Module

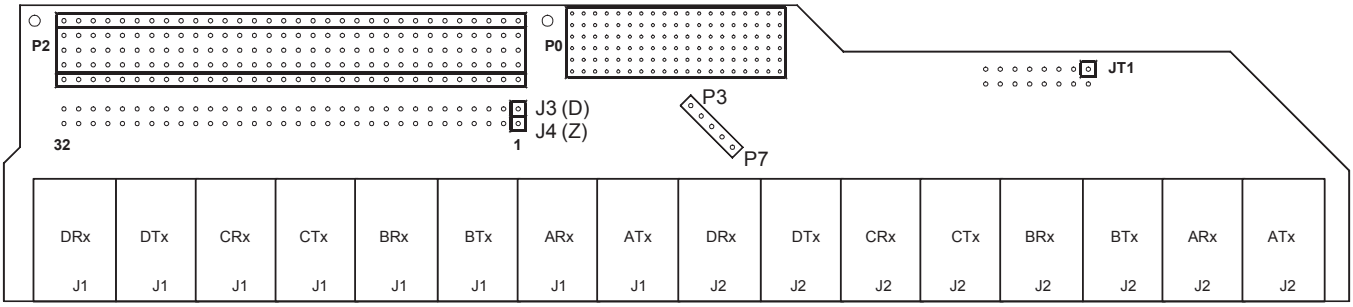


Table 2.4 summarizes the connectors provided on the rear transition module.

TABLE 2.4: Rear Transition Module Connectors

Transition Module Pin	Description
J1 and J2 RJ45 Connectors	StarLink Connections

Emulation

Each FPGA contains 1 or 2 PPC 405 processors (refer to CHAMP-FX FPGA Accelerator (SVME/DMV-430) User's Manual (document 813165) for more information). These processors are connected within the FPGA JTAG chain and can be emulated by connecting to the JTAG connector.

RUNNING THE BOOT MONITOR

The Boot Monitor is a special embedded program that runs on the PPC405 in the Configurator (after a hardware reset). The Boot Monitor is divided into two parts: one that resides in the On-Chip Memory (OCM) of the Configurator FPGA, and the other that resides in Flash memory, named .bootMon2.exe. The portion in OCM memory simply reads Flash and loads the .bootMon2.exe Boot Monitor. The secondary boot monitor, .bootMon2.exe is field-upgradeable.

The Boot Monitor configures all on-board resources and brings the board to an operational state. Once the resources are configured, the application named pbit.exe (PBIT) is executed if it is present. PBIT validates operation of the hardware devices present on the board. After completing initialization with a satisfactory result from PBIT, the Boot Monitor either transitions to an application program (loaded in Flash memory), or interacts with the serial port, accepting and processing maintenance commands. The decision to load and start an application is based on jumper settings (see the descriptions of JM12 found in "Configuring Jumpers" on page 2-3). Application loading is not necessarily inhibited if PBIT reports an error. By default, the board will continue to load the application unless a fatal error occurs. By setting a variable, the user can stop the board from booting if PBIT finds an error.

Cross Reference

Please refer to the CHAMPtools-FX Software User's Manual for more detailed information describing the Boot Monitor and the PBIT functions.

An example of the initial screen message you will see once Boot Monitor has run is shown in "Display the Initial Screen Message" on page 2-8.

INITIATE THE POWER-UP SEQUENCE

This section describes the normal power-up behaviour of the CHAMP-FX.

The CHAMP-FX Flash memory is managed by the Configurator. After power-on or board reset, the PPC405 in the Configurator loads and executes the Boot Monitor program stored in Flash memory. The Boot Monitor has three modes of operation: Normal Mode, Boot Inhibit Mode, and Flash Write-Protect Mode. The mode selected is determined by jumper settings (see Table 2.2 on page 2-3) and affects the degree of board initialization and start-up. Please refer to the CHAMPtools-FX Software User's Manual for a detailed description of these modes.

The Boot Monitor outputs progress messages through the front panel serial port. It also logs these messages in memory for later review. These messages display configuration information, jumper settings, and other information regarding the board initialization process.

DISPLAY THE INITIAL SCREEN MESSAGE

After a hardware reset, the Boot Monitor (in Boot Inhibit Mode) will display an initial sign-on message similar to the following:

```
CHAMPtools-FX Boot Monitor Version 1.0, Jun 25 2004 16:45:37
Copyright, 2003, 2004, 2005, Curtiss-Wright Controls, Inc.

Board:  rev B.1, s/n  4303005011
Proc:   PowerPC 405, 132 MHz, PVR 0x200108a0
CFGR:   version 1.0
SYS:    ProcId  0, Slot Id  6
SDRAM:  66 MHz, 64 MB, comm. temp range, 8 mS refresh
FPGA:   ProA/B successfully loaded
PCI:    Scanning for devices, delay 0 mS
FPGA:   ProA Version 1.4
FPGA:   ProB Version 1.4

BootMon>
```

Note that in Normal Boot Mode, a similar sign on message to that shown above will be displayed.

CONFIGURING AN EMULATOR FOR USE WITH CHAMP-FX

A Xilinx Parallel Cable IV may be used to interact with each processor and the board hardware on the CHAMP-FX card. A JTAG connection is provided on the cable assembly (CBL-430-000) for this purpose. When connecting an emulator to the cable, make sure that pin one of the emulator pod aligns with pin one on the connector.

The emulation capabilities of the CHAMP-FX have been tested with a Xilinx Parallel Cable IV in combination with the GNU Debugger (GDB) software provided with the Embedded Development Kit form Xilinx. Therefore, the information in this section is based on the use of these tools.

The JTAG connector is shared between all FPGAs on the CHAMP-FX board. Using the Xilinx Microprocessor Debugger (XMD) interface, an FPGA/processor can be chosen to target. In the JTAG chain, the Configurator FPGA is Device 3, Pro A is device 7, and Pro B is device 5.

Procedure for using the GNU Debugger (GBD)

The steps for using the emulator with the 405 processors are outlined below. For other emulators, follow a similar procedure.

1. Turn off the board (chassis) power.
2. Install cables CBL-430-000 and CBL-430-001 in the VME chassis behind the slot that contains the CHAMP-FX board to be used. CBL-430-000 plugs into the P0 rear backplane connector, while CBL-430-001 plugs into the P2 rear backplane connector.

FIGURE 2.3: CHAMP-FX P0 Cable (CBL-430-000)

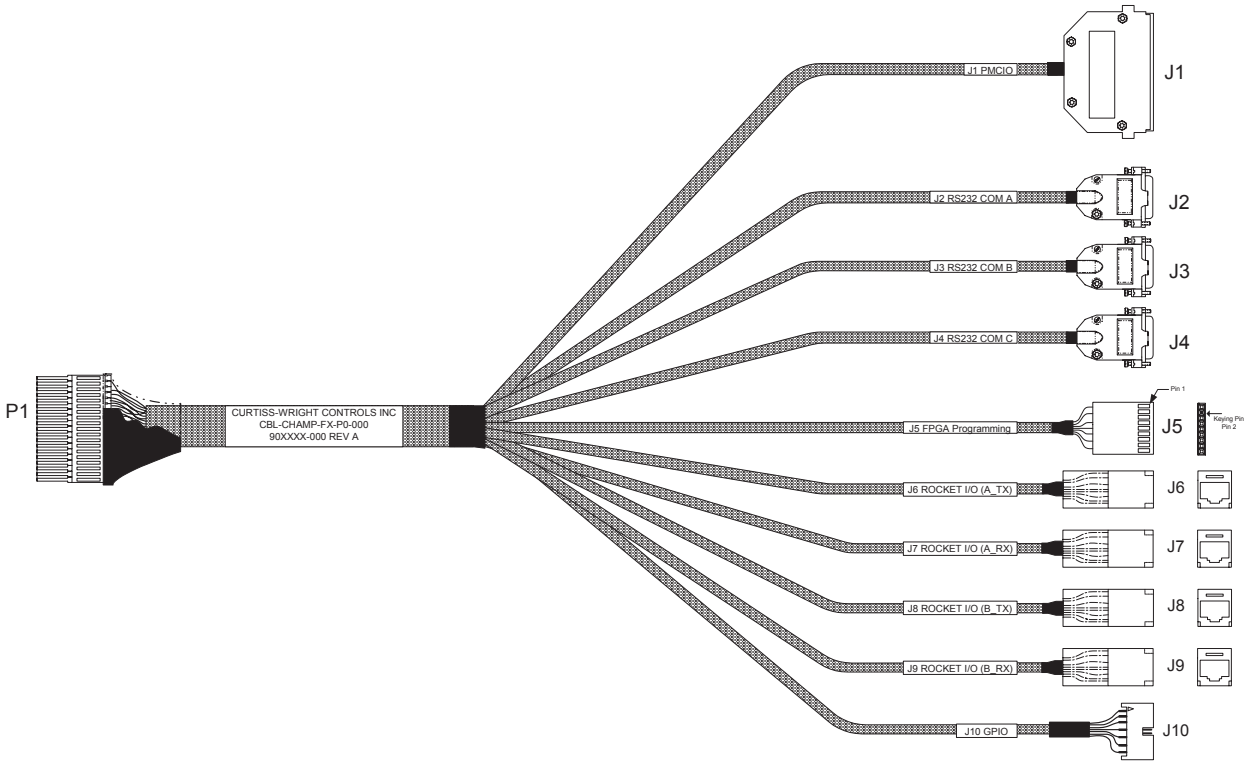
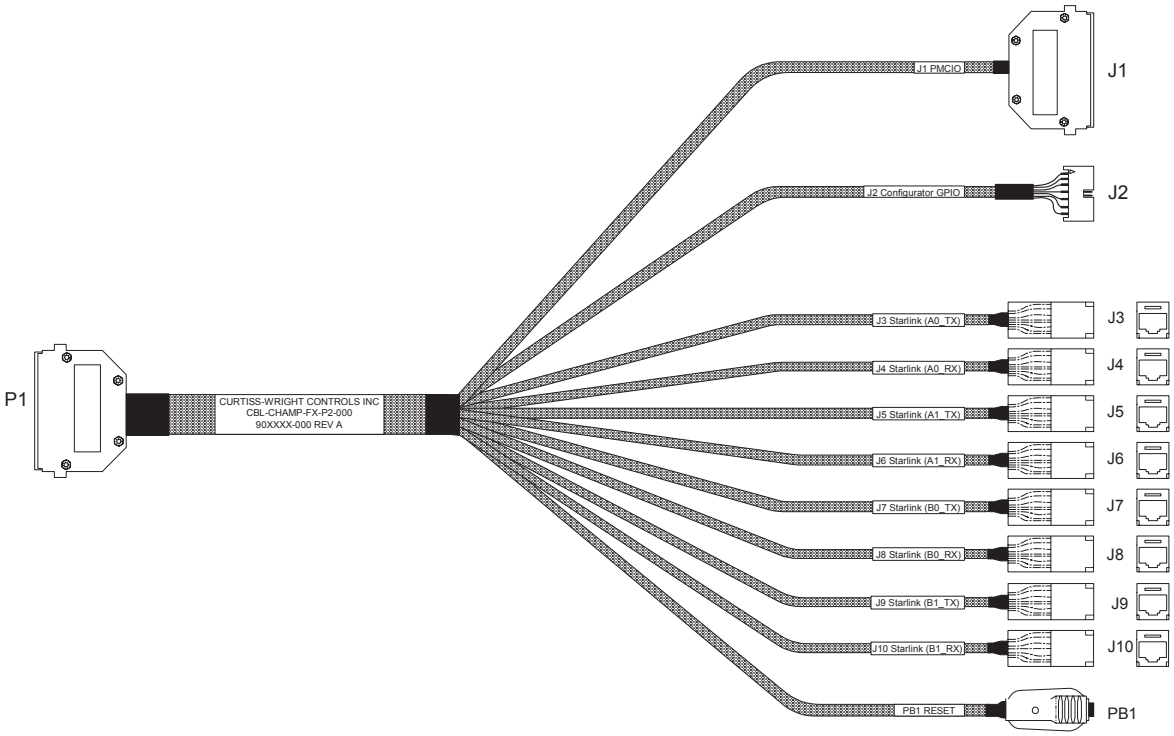


FIGURE 2.4: CHAMP-FX P2 Cable (CBL-430-001)



3. Connect the Xilinx Parallel Cable IV to the J5 connector on cable CBL-430-000. J5 is keyed so that the cable will only mate one way.
4. Power up the CHAMP-FX board.
5. Connect to a processor on the CHAMP-FX card via the XMD interface. For example, the following command can be used to connect to the processor in the Configurator FPGA:

   ```
   -cable type xilinx_parallel4 -debugdevice isocmstartadr
   0xffff0000 isocmsize 0x10000 isocmdcrstartadr 0x100 devicenr 3
   cpunr 1 dcrstartadr 0x20000000
   ```

   Consult the Xilinx Embedded Systems Tools Guide document for more information on how to download and execute an application for the target processor.

Make sure that the signaling level on the emulator pod connected to the COP interface on the CHAMP-FX is set to 3.3V. Failure to do so could cause damage to the baseboard or the emulator.