USER'S MANUAL

VXI PROTOTYPING MODULE

MODEL VX400B/C

Manual Part Number: 11026199

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INTRODUCTION

This manual describes the functional operation of the C&H Model VX400 B and C sized VXI Prototyping Modules (B-size P/N 11026195, C-size P/N 11026200). These modules are part of a number of test and data acquisition/control modules in the VME and VXI format provided by C&H.

Contained within this manual is information on the physical and electrical specifications, installation and startup procedures, operating procedures, functional analysis, and figures and diagrams required to adequately support this product.

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1.0 GENERAL DESCRIPTION

The VX400B/C VXI Prototyping Modules are VXIbus compatible B-size and C-size modules with over 22 and 78 square inches of user space, respectively. The two modules are identical, except for the physical dimensions.

1.1 PURPOSE OF EQUIPMENT

The module is well suited for applications in prototyping VXIbus designs, proof of concept testing, and design verification. The VX400 provides all necessary VXIbus register interface functions and user interconnect terminals to reduce design time and effort.

1.2 SPECIFICATIONS OF EQUIPMENT

1.2.1 Key Specifications

- Signal names silkscreened on both the component and solder sides
- Prototyping holes on a 0.1" by 0.1" grid
- VCC and GND strips along top and bottom edges
- User interface signals provided:
  - VXIbus Addresses
  - VXIbus Bi-directional Data
  - Data Strobes
  - Data Bus Direction Control
  - Write Gates
  - Read Gates
  - Delayed & Local Data Acknowledge
  - VXI Address Decode
  - Interrupt Signals
  - VXI Device Register Data Input
  - Reset
  - Upper Offset Address Decode Lines
  - VXI Register Data Inputs
  - Power
  - All P2 Signals

1.2.2 Electrical

The VXI interface circuitry provided on the module requires +4.5V to +5.5V at 0.5 amps for proper operation. The actual power requirements will depend on the user's circuitry. The connector pins are rated at 1 amp maximum.

1.2.3 Mechanical

The mechanical dimensions of the module are in conformance with the VXI bus specification for single slot B and C Size modules. The nominal dimensions are 233.35 mm (9.187 in) high x 160 mm (6.299 in) deep for the B-size module and 233.35 (9.187 in) high x 340 mm (13.386 in) deep for the C-size module. The B-size module is designed for a mainframe with 20.32 mm (0.800 in) spacing between slots and the C-size module is designed for a spacing of 30.48 mm (1.200 in). As required by the VXI bus specification, the dimensions are in accordance with those given in the VME bus specification (Rev. C.1), where applicable.

1.2.4 Environmental

The environmental specifications of the module are:

Operating Temperature: 0°C to +55°C

Storage Temperature: -40°C to +75°C

Humidity: <95% without condensation

The cooling air requirements depend on the user's circuitry.

1.2.5 Bus Compliance

The VX400 complies with the VXIbus Specification Revision 1.4 for B and C size register based modules and with VMEbus Specification ANSI/IEEE STD 1014-1987, IEC 821 and IEC 822. SYSFAIL is not supported, but can be added by the user with jumpers to the P1 connector. IACKIN is tied directly to IACKOUT and BRX is tied directly to BGX; however, these configurations are easily modified by cutting accessible circuit traces.

2.0 INSTALLATION

2.1 UNPACKING AND INSPECTION

In most cases the VX400 will have been individually sealed and packaged for shipment. Verify that there has been no damage to the shipping container. If damage exists then the container should be retained as it will provide evidence of carrier caused problems. Such problems should be reported to the carrier immediately as well as to C&H. If there is no damage to the shipping container, carefully remove the module from its box and plastic bag and inspect for any signs of physical damage. If damage exists, report immediately to C&H.

2.2 HANDLING PRECAUTIONS

The VX400 contains components that are sensitive to electrostatic discharge. When handling the module for any reason, do so at a static-controlled workstation, whenever possible. At a minimum, avoid work areas that are potential static sources, such as carpeted areas. Avoid unnecessary contact with the components on the module.

2.3 INSTALLATION

CAUTION: Read the entire User's Manual before proceeding with the installation and application of power.

Set or verify the module's logical address. Insert the module into the appropriate slot according to the desired priority. Apply power. If no obvious problems exist, proceed to communicate with the module as outlined in your host processor's user's guide.

2.4 PREPARATION FOR RESHIPMENT

If the VX400 is to be shipped separately it should be enclosed in a suitable water and vapor proof plastic bag. Heat seal or tape the plastic bag to insure a moisture-proof closure. When sealing the bag, keep trapped air volume to a minimum.

The shipping container should be a rigid box of sufficient size and strength to protect the equipment from damage. If the VX400 was received separately from a C&H system, then the original module shipping container and packing material may be re-used if it is still in good condition.

3.0 FUNCTIONAL DESCRIPTION

3.1 GENERAL

A block diagram is provided on sheet 1 of the schematics in Appendix D and a layout of the board is shown in Appendix C.

The VXI Interface provides all the electrical and mechanical connections to the VXI backplane. The P1 connector implements the bus drivers and receivers according to the VXI specification and passes the information to the remainder of the board. The P2 connector provides a 96-pin DIN type connector pattern to the user. The user can solder wires directly into these holes, or insert a header for easy access.

3.1.1 Control Logic and Address Decode

The address decode section provides an enable signal to the control logic when the address on the bus matches the settings of the logic address switch on the module. Once the module has an address match, the control logic performs the proper VXIbus handshake, timing and data transfers to or from the designated registers. Read and write strobes for all the registers are decoded in the address decode section.

3.1.2 VXI Registers and Data Buffer

All required VXI registers are provided and the user has access many of the register bits. The bi-directional data buffer is implemented to the user's logic. Refer to for the user interface signals.

3.2 SWITCHES AND JUMPERS

An 8-bit logical address switch (S1) is provided to uniquely identify the module in the system.

3.3 INDICATORS

Two LED indicators are provided on the front panel. One indicates access to the MODID, the other indicates the BOARD SELECT status.

MODID: This front panel LED illuminates whenever the host processor applies the MODID signal to the slot the VX400 is occupying.

BOARD SELECT: This front panel LED illuminates whenever the VX400 is properly accessed by the host processor.

3.4 CONNECTORS

The VX400 provides the P1 VXIbus connector and provisions to mount a P2 connector. No external connections are provided at the front panel, but provisions for two DIN41612

compatible connectors are available. Access to the buffered data and control signals is via solder tabs with plated through holes. The user may install wire-wrap posts in these locations or solder directly to the tabs. Refer to Appendix B for the P1 and P2 pin configurations.

In order to facilitate the usage of a "piggyback" board, the user signals and P2 connector signals are physically arranged to allow insertion of 96-pin DIN compatible connectors. These connectors are provided with Option 01.

3.5 VXI CONFIGURATION REGISTERS

There are several registers used to configure and control the VX400. The address map of the registers is shown in :

Table I. VXI Register Address Map

Addr (Hex)	Description
0008-001F	Unused Registers Locations
0006	VXI Offset Register
0004	VXI Status Register
0002	VXI Device Type Register
0000	VXI Identification (ID) Register

The VXI configuration registers contain basic information needed to configure a VXIbus system. The configuration information includes: manufacturer identification, product model code, device type, memory requirements, device status, and device control. The registers are briefly described below and are detailed in and :

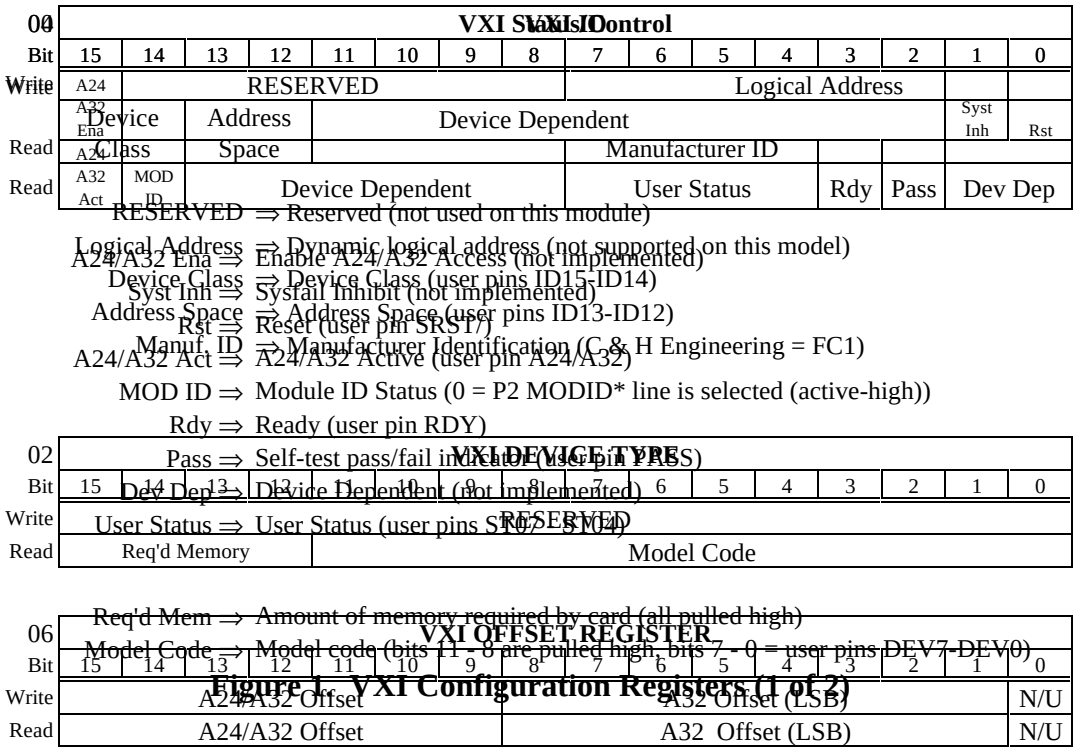

Figure 1. VXI Configuration Registers (1 of 2)

Figure 2. VXI Configuration Registers (2 of 2)

VXI Identification (ID) Register (0000h) - A read of this register provides manufacturer identification, device classification (i.e., register based), and the addressing mode (A16/A24/A32). A write to this register has no effect.

VXI Device Type Register (0002h) - A read of this register provides the model code identifier and the amount of memory required. A write to this register has no effect.

VXI Status/Control Register (0004h) - A read of this register provides the state of the A24/A32 Enable bit, the state of P2 MODID* line, and the Ready (RDY) and self-test

Passed (PASS) status. A write of this register controls the A24/A32 enable and the reset of the module. SYSFAIL* is not implemented on this module.

VXI Offset Register (0006h) - Only the control logic (WOFF0-1 and ROFF/) is implemented on this register.

3.6 USER INTERFACE SIGNALS

The VX400 performs all the VXIbus interface functions and provides a buffered set of address, data, and control signals to the user. See Appendix A for the timing relationships of the user interface signals.

3.6.1 Buffered VXIbus Addresses (A01, A02, A03)

The corresponding VXIbus address lines are latched into CMOS compatible devices on the leading edge of DLY1 and maintained until both data strobes are negated. These latched and buffered signals are provided to the user as A01, A02, and A03. This insures the address will remain stable until the VXIbus cycle is complete.

3.6.2 Non-buffered VXIbus Addresses (VA04, VA05, VA16 to VA23)

These address lines are direct connections to the corresponding VXIbus address lines and may be used if greater address range is required.

3.6.3 Buffered VXIbus Bi-directional Data (D00 to D15)

These signals are the bi-directional buffered 16-bit VXI Data bus. They have drive/receive characteristics of the ALS transceiver (74ALS245).

3.6.4 Buffered Data Strobes (DS0/, DS1/)

The data strobes are used by the VX400 to reset the latched address signals, determine valid VXIbus cycles, and to decode the write gate signals. The data strobes are buffered and provided to the user with CMOS compatible logic for additional decode or timing applications.

3.6.5 Data Bus Direction Control (WR/)

WRITE* from the VXIbus is buffered using CMOS compatible logic to produce WR/. This signal is used to control the direction of data flow to and from the VXIbus. The read gates and write gates are a function of this signal and it is also provided to the user.

3.6.6 Write Gates (WR8 to WRF, WLAR, WCNT, WOFF)

D00 through D015 are stable at the rising edge of the Write clocks. Each CMOS level active-high Write Gate corresponds to an 8-bit data register. For 16-bit writes, two write clocks occur simultaneously. See for a list of the signals and their functions.

3.6.7 Read Gates (R89, RAB, RCD, REF, RIO/, RDEV/, RSTAT/, ROFF/)

Each CMOS level active-low Read Gate corresponds to a 16-bit data register. The VXIbus data transceiver is configured to present the 16-bit data to the VXIbus while the read gate is low. All 16-bits of data are sent to the VXIbus, the host processor accepts only the byte it is seeking. See for a list of the signals and their functions.

Table II. Write Gate Decode

USER SIGNAL	REG ADDR	HIGH BYTE D15 - - - - - - - - D08	LOW BYTE D07 - - - - - - - - D00
WRE,WRF	0E,0F	User defined reg	User defined reg
WRC,WRD	0C,0D	User defined reg	User defined reg
WRA,WRB	0A,0B	User defined reg	User defined reg
WR8,WR9	08,09	User defined reg	User defined reg
WOFF1,WOFF0	06,07	VXI Offset Reg 1	VXI Offset Reg 0
WCNT1,WCNT0	04,05	VXI Control Reg 1	VXI Control Reg 0
Not Used	02,03	N/A	N/A
WLAR1,WLAR0	00,01	Logical Addr Reg 1	Logical Addr Reg 0

Notes:

1) For a 16 bit data write, both write signals are applied simultaneously. 32 bit read/writes are not supported by this module.

2) This pattern will repeat from register 10 through 3F. For additional registers the user must cut the register BDSEL/ jumper and decode the VXI base register and additional register selects.

3.6.8 Delayed and Local Data Acknowledge (DLY1/, LDTACK/)

Table III. Read Gate Decode

USER SIGNAL	REG ADDR	READ FUNCTION
REF/	E/F	User Defined Registers E and F
RCD/	C/D	User Defined Registers C and D
RAB/	A/B	User Defined Registers A and B
R89/	8/9	UserDefined Registers 8 and 9
ROFF/	6/7	VXI Offset Register
RSTAT/	4/5	VXI Status Register
RDEV/	2/3	VXI Device Register
RID/	0/1	VXI ID Register

Note:

1) This module does not support D32.

2) This pattern will repeat from register 10 through 3F. For additional registers the user must cut the etch on the BDSEL/ jumper and decode the VXI base register and additional register selects.

DLY1 occurs approximately 40 nsec after a valid VXIbus cycle to this module is detected. The low order address bits (Axx) and the valid address decode (DSSEL/) are latched. When these signals are stable, approximately 40 nsec later, Local Data Acknowledge (LDTACK/) is generated. LDTACK/ is used by the VX400 to generate the read and write gates. The user may use LDTACK/ to latch other pertinent information or to synchronize data. After an additional 120 nsec, DTACK* is sent to the host processor signaling the end of a cycle. LDTACK/ and DLY1 are driven by TTL compatible devices. DTACK* is driven by two paralleled tri-stated active-low devices.

3.6.9 VXI Address Decode (BDSEL/)

BDSEL/ is a CMOS output that is latched on the leading edge of DLY1 and maintained until both data strobes have been negated. This insures the address will remain stable until the VXIbus cycle is complete.

3.6.10 Interrupt Signals (IRQ1* to IRQ7*, IACKIN*, IACKOUT*)

These signals are available if the user requires interrupt capability. IACKIN* is connected to IACKOUT* on the solder side of the board, however this trace may be cut to enable interrupt capability. Solder terminals for these signals are located adjacent to the P1 connector and are marked "I" for IACKIN* and "O" for IACKOUT*.

3.6.11 Reset (RST/, SRST/)

The SYSRESET* from the VXIbus is buffered and supplied to the user as RST/. The VXI Control Register bit 0 is provided to the user as SRST/. These signals are driven by LS TTL compatible devices.

3.6.12 Upper Offset Address Decode Lines (UUPQ/, UPQ/)

These CMOS inputs can be used to decode the upper address bits to accommodate A24 or A32 offset addressing. These lines are pulled high on the board.

3.6.13 Chip Selects (CSA/, CSB/)

These CMOS level active-low chip selects can be used for alternate or additional register decoding. CSA/ goes low for byte register addresses $00 to $0F. CSB/ goes low for byte register addresses $10 to $1F.

3.6.14 Power (VCC, GND, +5STBY, +12, -12, -2, -5.2, +24, -24)

VCC and GND strips are provided along the top and bottom of the board and +5STBY, +12 and -12 are provided at signal points in the user signal area. Additionally, voltage/ground terminal strips for -2V, -5.2V, and ±24V are located near the P2 connector. These latter voltages are only available if the P2 connector is used.

3.6.15 P2 Signals

All P2 connector signals are provided. These signals are wired directly (not buffered) to a 96-pin hole pattern adjacent to the P2 connector.

3.6.16 VXI Register Data Inputs (ID12-ID15, A24/A32, RDY, PASS, ST07-04, DEV7-0)

These lines allow setting of various bits in the VXI configuration registers. All lines are pulled high on the board. See for additional information on these signals.

Table IV. Register Data Input Definitions

REGISTER INPUT	VXI REGISTER	FIELD	BIT(S)	NOTES
ID15-ID14	ID	Device Class	15-14	00 = Memory, 01 = Extended, 10 = Message Based, 11 = Register Based
ID13-ID12	ID	Address Space	13-12	00 = A16/A24, 01 = A16/A32, 10 = Reserved, 11 = A16 Only
A24/A32	Status/Control	A24/A32 Active	15	1 = A24 or A32 accessible
RDY	Status/Control	Ready	3	1 = Ready
PASS	Status/Control	Self-Test Pass/Fail	2	0 = executing or failed, 1 = passed
ST07-ST04	Status/Control	Device Dependent	7-4	User Dependent
DEV7-DEV0	Device Type	Model Code	7-0	User Dependent

4.0 OPERATING INSTRUCTIONS

The VX400 performs the interface functions to the VXI registers and provides a simplified set of control and data signals for user logic. Access to the module is through the VXI registers and VXI register user space. The interface section contains logical address and address modifier decode logic and circuitry for proper VXIbus interface timing. 16 bits of bi-directional data, decoded read and write strobes, and control functions are provided, along with the discrete VXIbus signals to the user interface connectors. See section for description of the user interface signals.

4.1 NORMAL OPERATION

For immediate use of the VX400, set the Logical Address, insert the module in the VXI chassis and perform a read or write command. The resultant read data is the VXI register's contents or pulled-up unused inputs. User write data to this module only goes to the user connector pins, however the operation may be considered successful if a Bus Error does not occur. For further verification the user can set the MODID to the slot containing the VX400 and read the VXI Status register.

Addressing the VX400 is a function of the logical address switch and the VXI host address modifier code. The logical address switch is located at S1 and is compared to the backplane address bits 6 through 13. Initial addressing is via A16 only, however A16/A24 and A16/A32 offset addressing can be implemented with additional logic.

The logical address has a range of 0 to 255. Any value within this range is valid, but care should be taken not to set the logical address the same as another module in the system. Position 1 on the switch is the most significant bit and has a weighted value of 128 when the switch is in the off position. Position 8 on the switch is the least significant bit and has a weighted value of 1 when the switch is in the off position. The sum of the weighted values of all the switches in the off position is the module address. See the module layout in Appendix C for switch location. The VXI secondary address is the logical address divided by 8.

4.2 SOFTWARE DRIVERS

No software drivers are supplied. Software drivers are application dependent and should be designed for the user hardware.

5.0 MAINTENANCE

5.1 BUILT IN TEST AND DIAGNOSTICS

No built in test functions are provided. The user may design in test capabilities and provide their own selftest functions.

5.2 TROUBLE ANALYSIS GUIDE

The first approach to trouble shooting the VX400 should be to try a VXIbus access. A successful access (read or write) will not produce a bus error. If a bus error occurs, insure that the modules's logical address switch is set correctly, that the card is properly installed, and the host program is properly addressing the card. If the bus error continues, contact C & H Engineering for further assistance.

APPENDIX A - ELECTRICAL AND TIMING SPECIFICATIONS

Figure A-1. User Signal Timing

APPENDIX B - CONNECTORS

PIN			
1	D08	-	D00
2	D09	-	D01
3	D10	-	D02
4	D11	BG0IN*	D03
5	D12	BG0OUT*	D04
6	D13	BG1IN*	D05
7	D14	BG10UT*	D06
8	D15	BG2IN*	D07
9	GND	BG20UT*	GND
10	-	BG3IN*	-
11	-	BG3OUT*	-
12	SYSRESET*	-	DS1*
13	LWORD*	-	DS0*
14	AM5	-	WRITE*
15	A23	-	-
16	A22	AM0	DTACK*
17	A21	AM1	_
18	A20	AM2	_
19	A19	AM3	_
20	A18	GND	IACK*
21	A17	-	IACKIN*
22	A16	-	IACKOUT*
23	A15	GND	AM4
24	A14	IRQ7*	A07
25	A13	IRQ6*	A06
26	A12	IRQ5*	A05
27	A11	IRQ4*	A04
28	A10	IRQ3*	A03
29	A09	IRQ2*	A02
30	A08	IRQ1*	A01
31	+12 V	-	-12 V
32	+5 V	+5 V	+5 V

Figure B-1. P1 Pin Configuration

• PIN	C	B	A
1	CLK10+	+5V	ECLTRG0
2	CLK10-	GND	-2V
3	GND	RSV1	ECLTRG1
4	-5.2V	A24	GND
5	LBUSC00	A25	LBUSA00
6	LBUSC01	A26	LBUSA01
7	GND	A27	-5.2V
8	LBUSC02	A28	LBUSA02
9	LBUSC03	A29	LBUSA03
10	GND	A30	GND
11	LBUSC04	A31	LBUSA04
12	LBUSC05	GND	LBUSA05
13	-2V	+5V	-5.2V
14	LBUSC06	D16	LBUSA06
15	LBUSC07	D17	LBUSA07
16	GND	D18	GND
17	LBUSC08	D19	LBUSA08
18	LBUSC09	D20	LBUSA09
19	-5.2V	D21	-5.2V
20	LBUSC10	D22	LBUSA10
21	LBUSC11	D23	LBUSA11

APPENDIX C - BOARD LAYOUT

(B-size board shown - C-size is identical, except for user area)

APPENDIX D - SCHEMATICS

The following pages contain the schematics for the VX400.

N O T E S :

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President and CEO

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