Instruction Manual

Tektronix

TLA7PG2
Pattern Generator Probes

071-1017-01

This document supports Tektronix Logic Analyzer Family Software Version 4.1 and Tektronix Pattern Generator Software Version 1.3 and above.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Ground the Product. These products (P6470, P6471, P6472, P6473, and P6474) are indirectly grounded through the grounding conductor of the mainframe power cord. The P6475 is directly grounded through the grounding conductor of the probe power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

CAUTION
Refer to Manual

Protective Ground
(Earth) Terminal

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, switch off the instrument power, then disconnect the power cord from the mains power.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface

This document provides information on using and servicing the TLA7PG2 probes.

Related Documentation

In addition to these probe instructions, the following documentation is available for your Tektronix Logic Analyzer Family:

- The *TLA7PG2 Pattern Generator and Probes Service Manual* provides service information for the pattern generator and pattern generator probes.
- The *Tektronix Logic Analyzer Family User Manual* provides overall user information for the Tektronix logic analyzers.
- The online help provides information for the probes and pattern generator user interfaces and the Pattern Generator Programmatic Interface (PPI).
- A series of instruction manuals for microprocessor support provides operating and service instructions for the individual microprocessor support packages that are available for use with the logic analyzer.
- Probe instructions accompany the logic analyzer modules to provide operating and service information.
- The *Tektronix Logic Analyzer Family Training Manual* provides training exercises to help you learn key features of the logic analyzer. The training manual is designed to be used with the TLA7QS training board.
- A series of service manuals are available that provide performance verification procedures and board-level service information for major components of the logic analyzer.

Contacting Tektronix

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Sales support	1-800-833-9200, select option 1*
Service support	1-800-833-9200, select option 2*
Technical support	Email: TechSupport@tektronix.com 1-800-833-9200, select option 3* 1-503-627-2400 6:00 a.m. – 5:00 p.m. Pacific time

* **This phone number is toll free in North America. After office hours, please leave a voice mail message.**
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Operating Basics

This section provides a brief description of the TLA7PG2 probes and information on connecting the probes from the pattern generator module to the target system.

Product Description

The pattern generator probes provide multichannel signals to simulate signals in a test environment. Following are descriptions of the probes discussed in this manual:

P6470 TTL/CMOS

The P6470 provides TTL or CMOS signals to the target system and contains 16 data outputs, 1 clock output, and 1 strobe output. The V_{CC} output driver is adjustable from 2.0 V to 5.5 V. Figure 14 on page 18 shows the P6470 input/output circuit.

The P6470 probe comes standard with 75 Ω termination resistors packs. You can change the resistor packs to provide impedance matching for the target system. Refer to *Removing the Probe Cover* on page 46 and *Changing the Series Termination Resistors* on page 47.

P6471 ECL

The P6471 ECL pattern generator probe provides ECL signals to the target system and contains 16 data outputs, 1 clock output, and 1 strobe output. Figure 15 on page 19 shows the P6471 input/output circuit.

P6472 PECL/LVPECL

The P6472 provides PECL/LVPECL signals to the target system and contains 8 data outputs, 1 clock output, and 1 strobe output. You can select PECL or LVPECL by moving a jumper in the probe. See *Configuring the P6472 for PECL or LVPECL* on page 48. Figure 16 on page 20 shows the P6472 input/output circuit.

P6473 LVDS

The P6473 provides LVDS signals to the target system and contains 16 data outputs, 1 clock output, and 1 strobe output. All inputs and outputs are LVDS level.

P6474 LVCMOS

The P6474 provides LVCMOS signals to the target system and contains 16 data outputs, 1 clock output and 1 strobe output. Figure 18 on page 22 shows the P6474 input/output circuit.

The V_{CC} of the output driver is adjustable from 1.2 V to 3.3 V.

The P6474 comes standard with 75 Ω termination resistors packs. You can change the resistor packs to provide impedance matching for the target system. Refer to *Removing Probe the Cover* on page 46 and *Changing the Series Termination Resistors* on page 47.

P6475 Variable

The P6475 provides logic family signals such as ECL, TTL/CMOS, and PECL/LVPECL and contains 8 data outputs and one clock output. The P6475 also supports variable delay (0 to 50 ns) for two channels (CH6 and CH7).

When using the P6475 probe with a P6470 (TTL/CMOS), P6473 (LVDS), or P6474 (LVCMOS) probe, it is recommended that you use a Time Alignment Cable (P/N 012-A223-00) in conjunction with the TLA7PG2 Pattern Generator Module. The Time Alignment Cable ensures that the P6475 and the P6470, P6473, or P6474 probes are time aligned and can be used together. Please order one Time Alignment Cable (P/N 012-A223-00) for each P6470, P6473, and P6474 probe.

Probe Lead Sets and Cables

Figure 1 shows a typical pattern generator probe with the lead sets and probe cable. The probe cable is included with the TLA7PG2 pattern generator module. Refer to *Probe Connectors and Signal Names*, beginning on page 7, for probe connector information.

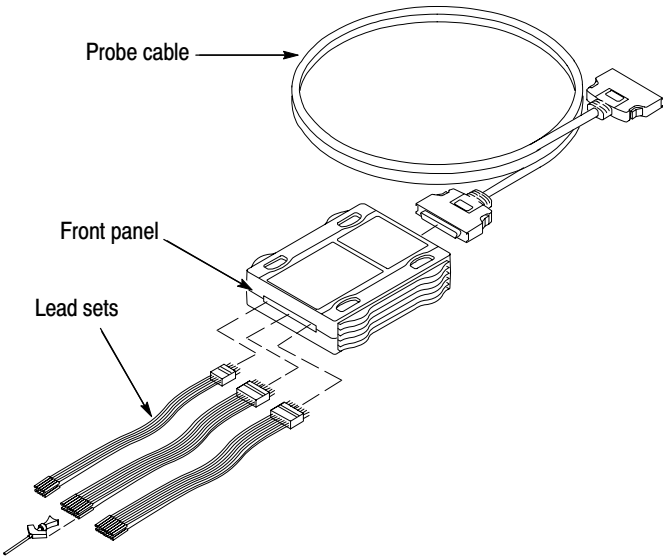

Figure 1: Standard probe, lead sets, and probe cable

Figure 2 shows the P6475 variable probe, lead sets and probe cable. The probe cable is included with the TLA7PG2 pattern generator module.

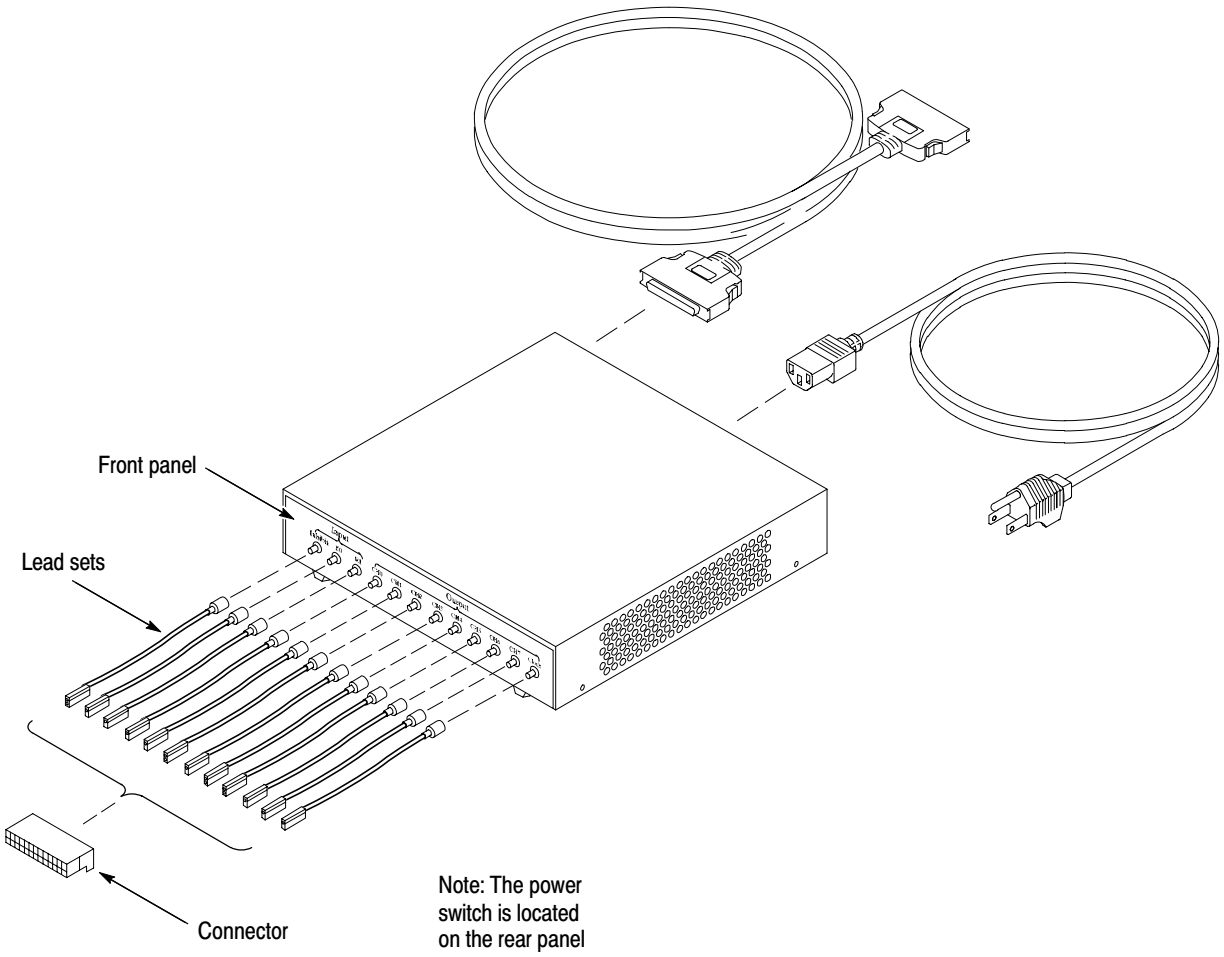

Figure 2: P6475 variable probe, lead sets, power cord, and probe cable

Connecting the Standard Probes

To connect the probes to the logic analyzer and to the target system, do the following steps:

1. Power off the logic analyzer and the target system before connecting the pattern generator probes.
2. Connect the lead sets to the target system.
3. Connect the standard probe as shown in Figure 1. The probe cable is reversible. You can connect the probe cable in either direction.

4. Connect the probe to the pattern generator module on the logic analyzer.

CAUTION. *To prevent damage to the pattern generator module or probe, do not connect or disconnect the pattern generator cables to or from the pattern generator module or probe while the logic analyzer is powered on. The recommended DUT (Device Under Test) and pattern generator power on/off sequence is as follows:*

Power on the DUT first, then power on the pattern generator. Power off the pattern generator and then power off the DUT.

Although the pattern generator probe cable appears to be a SCSI cable, it is not compatible with a SCSI cable; do not use a SCSI cable with the pattern generator module, or use the pattern generator probe cable with a SCSI instrument.

The probe is fragile; handle it carefully.

Connecting the P6475 Probe

P6475 Connections

Do the following steps to connect the P6475 to the logic analyzer, the target system, and to the power source:

1. Power off the logic analyzer and the target system before connecting the pattern generator probes.
2. Connect the lead sets to the target system.
3. Connect the P6475 as shown in Figure 2. The probe cable is reversible; either end can be connected to the P6475.
4. Connect the P6475 power cord.
5. Connect the probe to the pattern generator module on the logic analyzer.

Power On/Off

Follow the procedures below to power on and power off the P6475 variable probe:

1. Power on the DUT
2. Power on the P6475
3. Power on the TLA

1. Power off the TLA
2. Power off the P6475
3. Power off the DUT

Reference

This section provides reference information and specifications for the TLA7PG2 probes.

Probe Connectors and Signal Names

P6470 and P6474 Pin Assignments

Figure 3 shows the P6470 TTL/CMOS and P6474 LVCMOS pin assignments on the front panel.

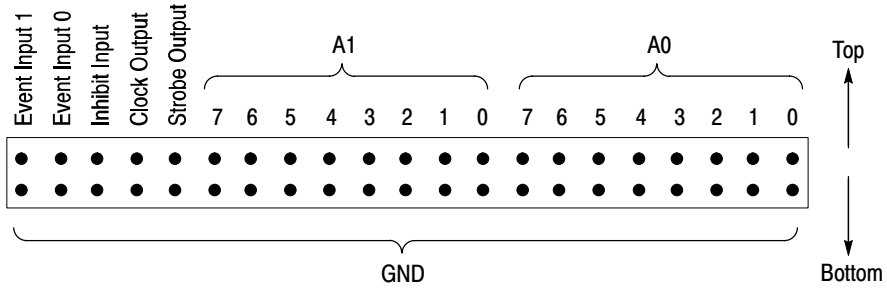

Figure 3: P6470 and P6474 output connector pin assignments

P6471 Pin Assignments

Figure 4 shows the P6471 ECL pin assignments on the front panel.

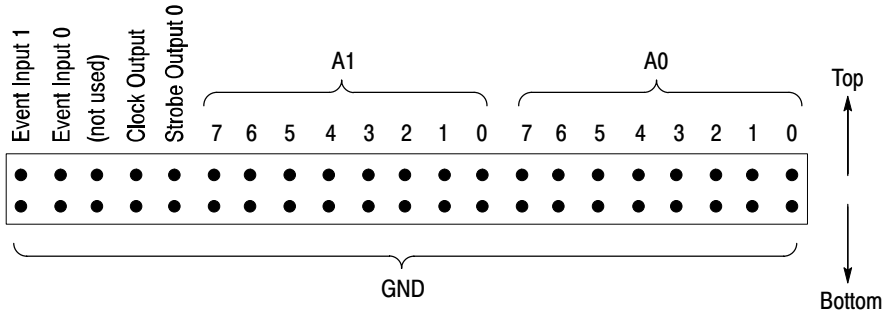

Figure 4: P6471 output connector pin assignments

P6472 Pin Assignments

Figure 5 shows the P6472 PECL/LVPECL pin assignments on the front panel.

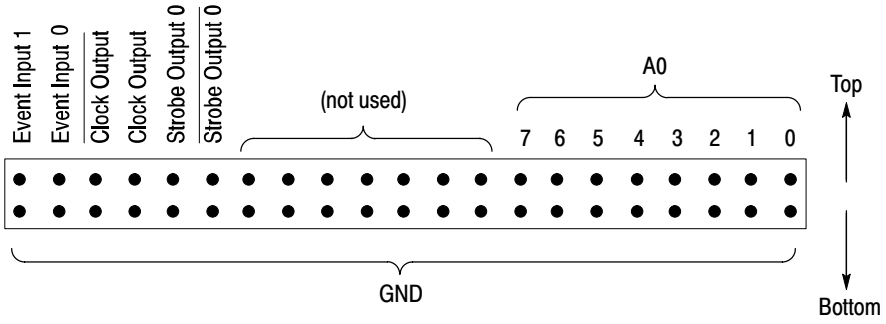

Figure 5: P6472 output connector pin assignments

P6473 Pin Assignments

Figure 6 shows the P6473 LVDS pin assignments on the front panel.

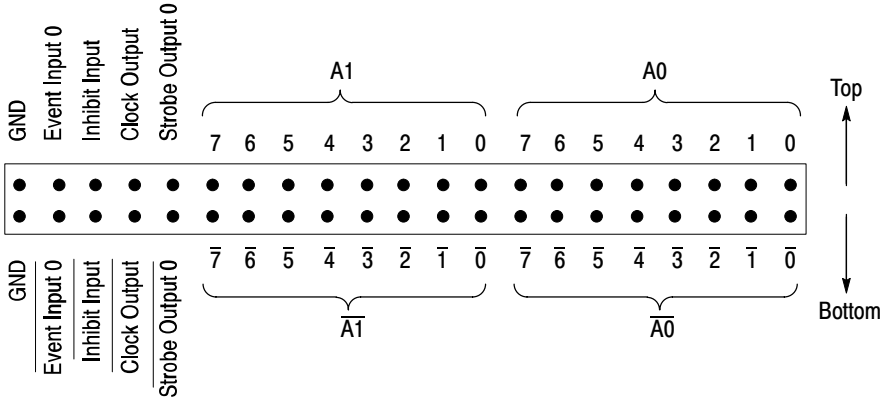

Figure 6: P6473 output connector pin assignments

P6475 Pin Assignments

Figure 7 shows the P6475 variable pin assignments on the front panel.

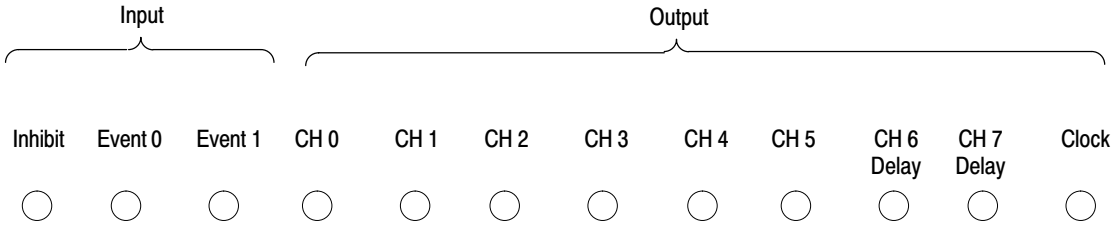

Figure 7: P6475 output connector pin assignments

Probe Overview

Table 1 shows the signal names when used with different probes. These signal names appear on the probe labels.

You can have up to four probes connected to each PG module. The leftmost probe will be the master, and the probes to the right of the master are the slaves. The probes are named Probe A, Probe B, Probe C, and Probe D, respectively. Refer to Table 1 for input and output names for each probe.

Table 1: Inputs and outputs of pattern generator probes

Characteristic	P6470 TTL/ CMOS	P6471 ECL	P6472 PECL/ LVPECL	P6473 LVDS	P6474 LVCMOS	P6475 Variable
Data Output (Full/Half)	16/8 channels	16/8 channels	8/8 channels	16/8 channels	16/8 channels	8/8 channels
Probe A	A0 (0 through 7)	A0 (0 through 7)	A0 (0 through 7)	A0 (0 through 7)	A0 (0 through 7)	A0 (0 through 7)
	A1 (0 through 7)	A1 (0 through 7)		$\overline{\text{A0 (0 through 7)}}$	A1 (0 through 7)	
				A1 (0 through 7)		
				$\overline{\text{A1 (0 through 7)}}$		
Probe B	B0 (0 through 7)	B0 (0 through 7)	B0 (0 through 7)	B0 (0 through 7)	B0 (0 through 7)	B0 (0 through 7)
	B1 (0 through 7)	B1 (0 through 7)		$\overline{\text{B0 (0 through 7)}}$	B1 (0 through 7)	
				B1 (0 through 7)		
				$\overline{\text{B1 (0 through 7)}}$		
Probe C	C0 (0 through 7)	C0 (0 through 7)	C0 (0 through 7)	C0 (0 through 7)	C0 (0 through 7)	C0 (0 through 7)
	C1 (0 through 7)	C1 (0 through 7)		$\overline{\text{C0 (0 through 7)}}$	C1 (0 through 7)	
				C1 (0 through 7)		
				$\overline{\text{C1 (0 through 7)}}$		
Probe D	D0 (0 through 7)	D0 (0 through 7)	D0 (0 through 7)	D0 (0 through 7)	D0 (0 through 7)	D0 (0 through 7)
	D1 (0 through 7)	D1 (0 through 7)		$\overline{\text{D0 (0 through 7)}}$	D1 (0 through 7)	
				D1 (0 through 7)		
				$\overline{\text{D1 (0 through 7)}}$		
Clock Output	1[1]	1[1]	1[1]	1[1]	1[1]	1
Probe A	CLK	CLK	CLK, $\overline{\text{CLK}}$	CLK/$\overline{\text{CLK}}$	CLK	CLK
Probe B	CLK	CLK	CLK, $\overline{\text{CLK}}$	CLK/$\overline{\text{CLK}}$	CLK	CLK
Probe C	CLK	CLK	CLK, $\overline{\text{CLK}}$	CLK/$\overline{\text{CLK}}$	CLK	CLK
Probe D	CLK	CLK	CLK, $\overline{\text{CLK}}$	CLK/$\overline{\text{CLK}}$	CLK	CLK

Table 1: Inputs and outputs of pattern generator probes (Cont.)

Characteristic	P6470 TTL/ CMOS	P6471 ECL	P6472 PECL/ LVPECL	P6473 LVDS	P6474 LVCMOS	P6475 Variable
Strobe Output	1	1	1	1	1	0[2]
Probe A	STRB0	STRB0	STRB0, $\overline{\text{STRB0}}$	STRB0/$\overline{\text{STRB0}}$	STRB0	
Probe B	STRB1	STRB1	STRB1, $\overline{\text{STRB1}}$	STRB2/$\overline{\text{STRB2}}$	STRB1	
Probe C	STRB2	STRB2	STRB2, $\overline{\text{STRB2}}$	STRB4/$\overline{\text{STRB4}}$	STRB2	
Probe D	STRB3	STRB3	STRB3, $\overline{\text{STRB3}}$	STRB6/$\overline{\text{STRB6}}$	STRB3	
Inhibit Input	1	0	0	1	1	1
Probe A	INHB			INHB/$\overline{\text{INHB}}$	INHB	INHB
Probe B	INHB			INHB/$\overline{\text{INHB}}$	INHB	INHB
Probe C	INHB			INHB/$\overline{\text{INHB}}$	INHB	INHB
Probe D	INHB			INHB/$\overline{\text{INHB}}$	INHB	INHB
Event Input[3]	2	2	2	1	2	2
Probe A	EVNT0, EVNT1	EVNT0, EVNT1	EVNT0, EVNT1	EVNT0/$\overline{\text{EVNT0}}$	EVNT0, EVNT1	EVNT0, EVNT1
Probe B	EVNT2, EVNT3	EVNT2, EVNT3	EVNT2, EVNT3	EVNT2/$\overline{\text{EVNT2}}$	EVNT2, EVNT3	EVNT2, EVNT3
Probe C	EVNT4, EVNT5	EVNT4, EVNT5	EVNT4, EVNT5	EVNT4/$\overline{\text{EVNT4}}$	EVNT4, EVNT5	EVNT4, EVNT5
Probe D	EVNT6, EVNT7	EVNT6, EVNT7	EVNT6, EVNT7	EVNT6/$\overline{\text{EVNT6}}$	EVNT6, EVNT7	EVNT6, EVNT7

1 **The Clock Output is disabled when Strobe Output is enabled.**

2 **CH6 and CH7 can be used as Strobe Outputs by setting the data format to RZ/R1.**

3 **The External Event Input is used to suspend/resume the sequencer (Advance function) or to jump to a specified line in the sequence or inhibit the output.**

Descriptions of the probe input and output control signals follow. For more information on using the probe signals, refer to the online help for the pattern generator.

Clock Output. Each probe has one clock output signal. The logic level of the clock output is the same as the data output.

The clock output is disabled when the strobe output is enabled.

Strobe Output. Each probe has a strobe output signal except for the P6475 variable probe. CH 6and CH7 can be used as a strobe signal by setting the data format to RZ/R1.

The logic level of the strobe output is the same as the data output.

The output format of the strobe is RZ (return to zero). The pulse width is the same as the first or the second half of the clock cycle. The pulse can be

positioned at either first half (Strobe delay: Zero) or second half (Strobe delay: Trailing Edge) of the clock cycle.

Figure 8 shows the pulse pattern of the strobe output.

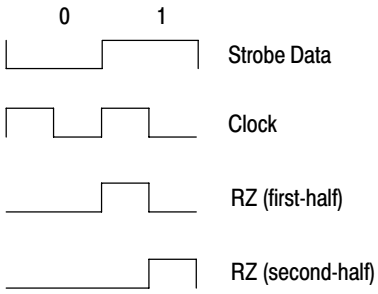

Figure 8: Strobe output pulse pattern

P6475 Variable probe Output Format. Figure 9 shows the P6475 output pulse patterns for various signals. NRZ is the output format for CH0 through CH5. You can select NRZ, RZ, and R1 from CH6 and CH7. The delay pulse width using RZ or R1 is equal to half of the clock cycle when using the internal clock mode. The clock output polarity is selectable from Normal or Invert. Refer to the TLA7PG2 for more information.

You can delay the CH6 and CH7 output up to 50 ns. Figure 9 shows the P6475 output pulse pattern.

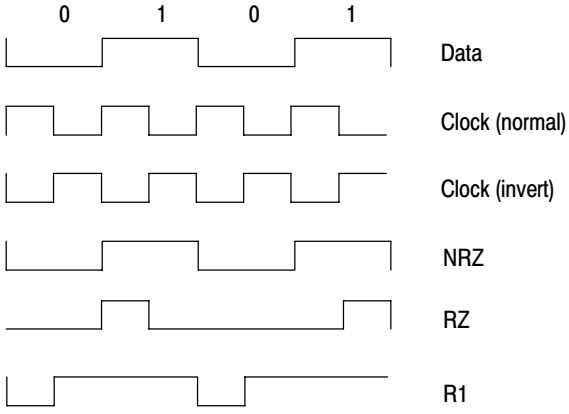

Figure 9: P6475 Variable probe output pulse pattern

By using the CH6 Output Mode control, it is possible to output a wider or narrower pulse from the CH6 output connector. Figure 11 shows the CH6 and CH7 output pulse patterns when using the CH6 Output Mode control.

For example, if the P6475 is setup as follows:

Clock Frequency: 100 MHz (10 ns period)

CH6: RZ, delay 3 ns

CH7: RZ, delay 5 ns

CH6 Output Mode: CH6 and CH7

The CH6 output will be as shown in Figure 10.

You will see an RZ pulse of 5 ns delay and a 3 ns width at the CH6 output connector

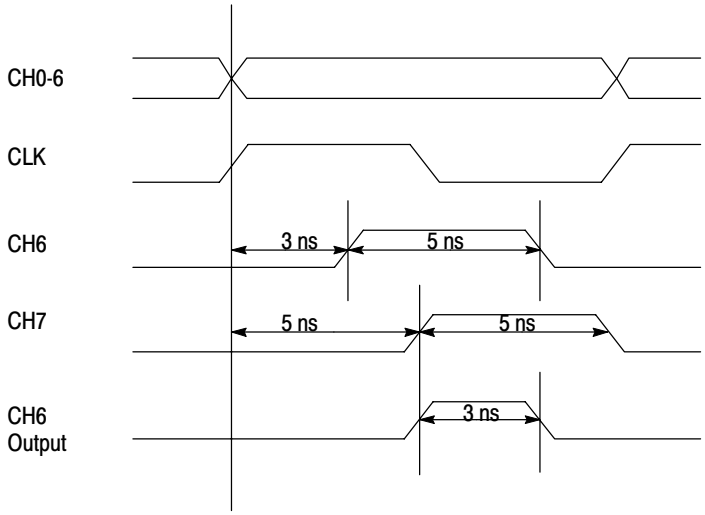

Figure 10: P6475 CH6 output example

Figure 11 shows the various CH6 pulse patterns depending on which mode is setup from the CH6 Output Mode Setup menu. See the TLA7PG2 Online Help system for more information.

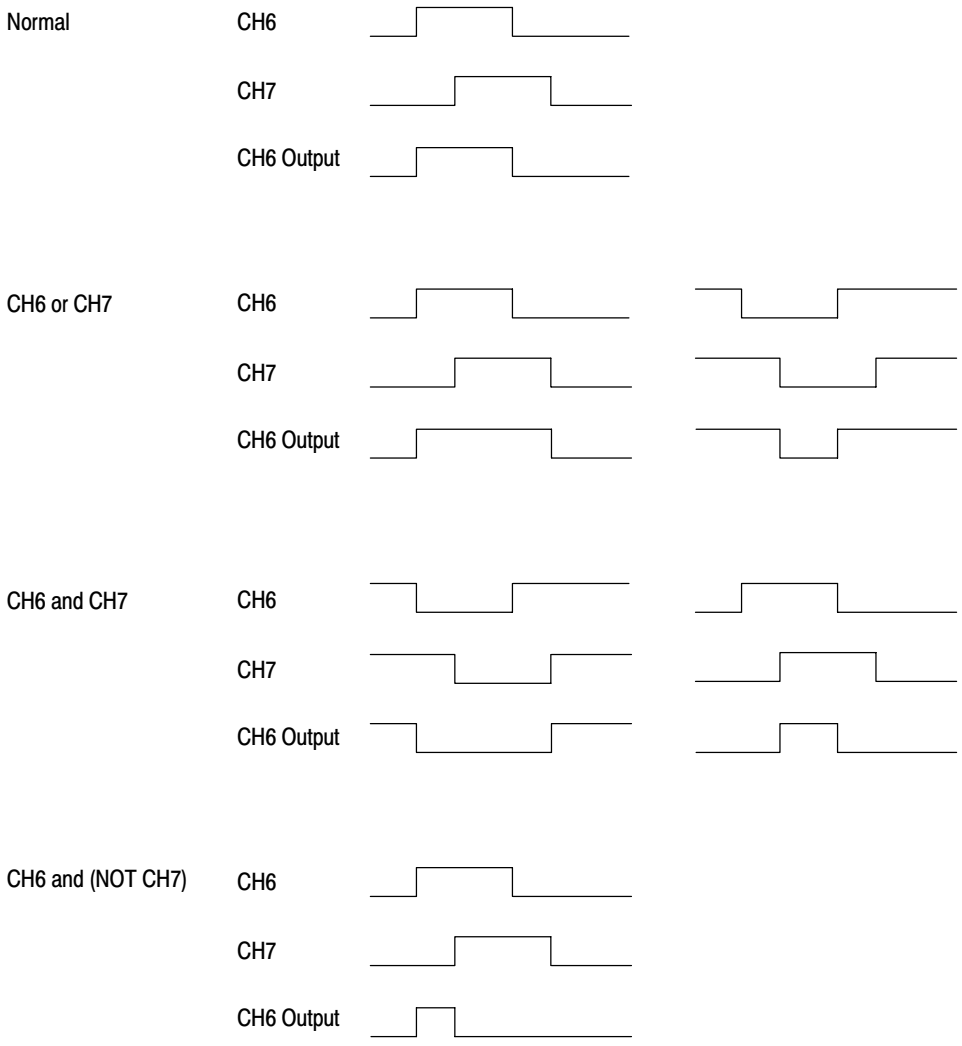

Figure 11: P6475 CH6 output mode pulse patterns

Inhibit Input. The P6470, P6473, P6474 and P6475 have an inhibit input to set the output to high impedance. The input polarity is positive true and a High input will disable the output. Low input or no connection enables the output. The P6475 input state (High or Low) with no connection will vary according to the input threshold setting.

External Event Input. All of the probes have one or two event inputs. The pattern generator detects an event when the external event input is High (True). The external event input is Low (False) when no signal is detected or when the probe

is not connected to the pattern generator. The P6475 input state (High or Low) with no connection will vary according to the input threshold setting.

The external event can be used to Jump or Advance the sequencer or disable the output. The input polarity is positive true.

Input Logic Level. All inputs are the same logic level as the output except for the P6475 Variable probe. The V_{cc} of the input circuit is the same as the V_{cc} of the output driver for the P6470 TTL/CMOS probe and the P6474 LVCMOS probe. The P6475 Variable probe input threshold level is adjustable within the range of –2.5 V to +2.5 V.

Probe Dimensions

Figure 12 shows the dimensions of the standard pattern generator probes. The physical dimensions are the same for the P6470, P6471, P6472, P6473, and P6474 probes.

***NOTE**. There are no ventilation requirements for the standard probes.*

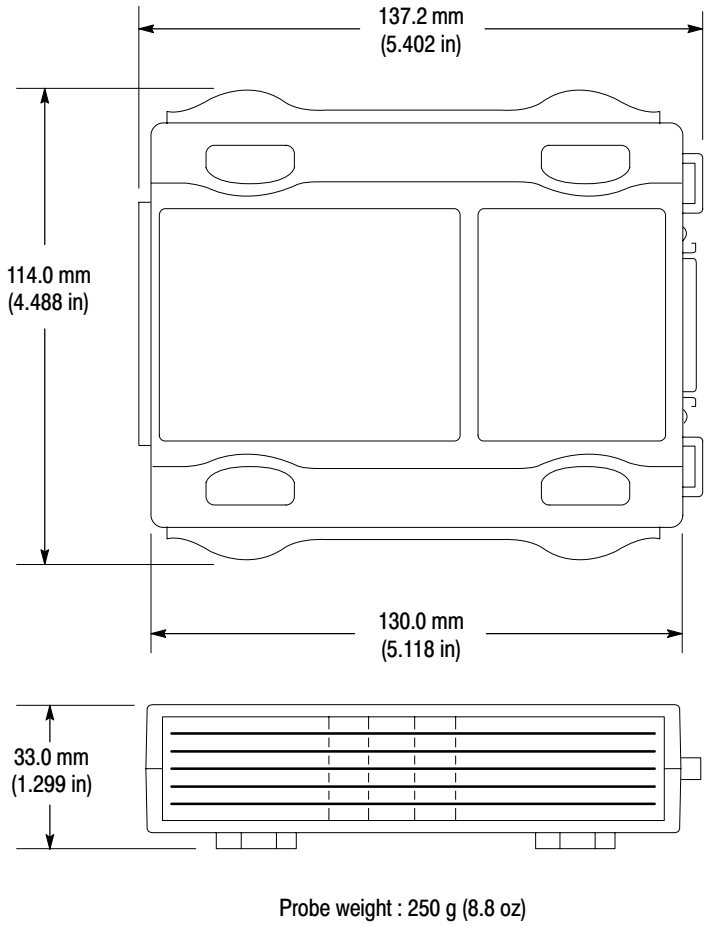

Figure 12: P6470, P6471, P6472, P6473 and P6474 probe dimensions

Figure 13 shows the dimensions of the P6475 probe.

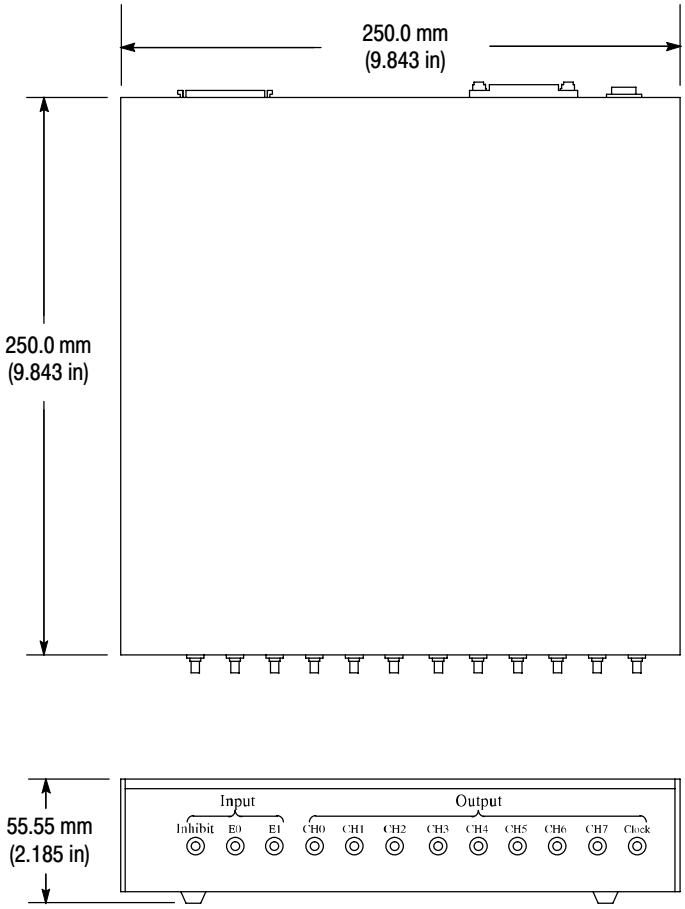

Figure 13: P6475 Variable probe dimensions

P6475 Installation Requirements

Table 2 provides information for the P6475 Variable probe installation:

Table 2: P6475 Variable probe installation requirements

Characteristics	Description
Maximum power dissipation (fully loaded)	35 W max. Maximum line current is 0.6 A_{rms} at 50 Hz, 90 V line, with 5 % clipping
Surge Current	Max 57 A peak (25° C) ≤ 5 line cycles after product has been turned off for at least 30 s
Clearance for ventilation	
Side	10 cm (3.9 in)

Input/Output Circuits

This subsection shows the input/output circuits for the P6470, P6471, P6472, P6473. and P6474 probes.

P6470

Figure 14 shows the probe input/output circuit for the P6470 TTL/CMOS pattern generator probe. The P6470 comes standard with 75 Ω resistor packs. You can change the resistor packs to provide impedance matching for the target system.

The P6470 provides 16 data outputs, 1 clock output, and 1 strobe output.

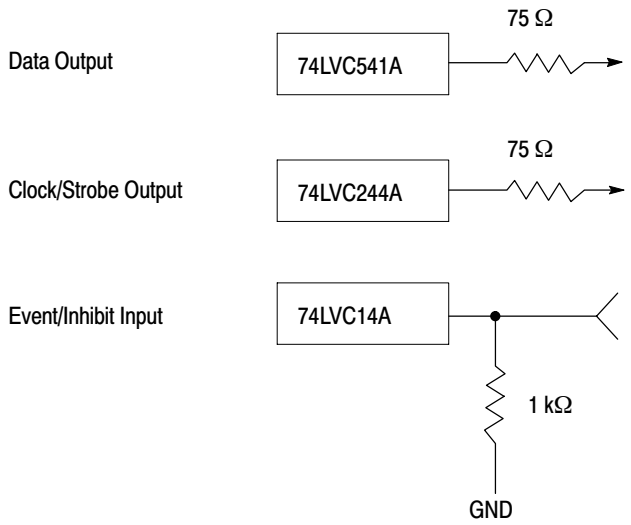

Figure 14: P6470 input/output circuit

P6471 Figure 15 shows the probe input/output circuit for the P6471 ECL pattern generator probe.

The P6471 provides 16 data outputs, 1 clock output, and 1 strobe output.

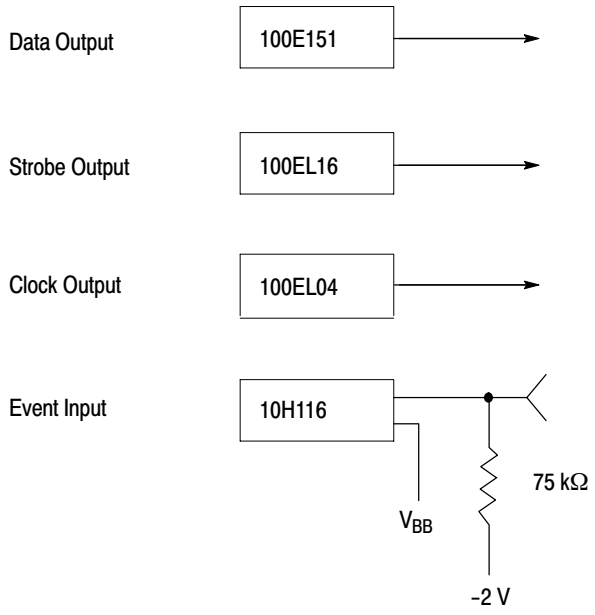

Figure 15: P6471 input/output circuit

P6472 Figure 16 shows the input/output circuit for the P6472 PECL/LVPECL pattern generator probe. The P6472 provides PECL/LVPECL signals to the target system and contains 8 data outputs, 1 clock output, and 1 strobe output.

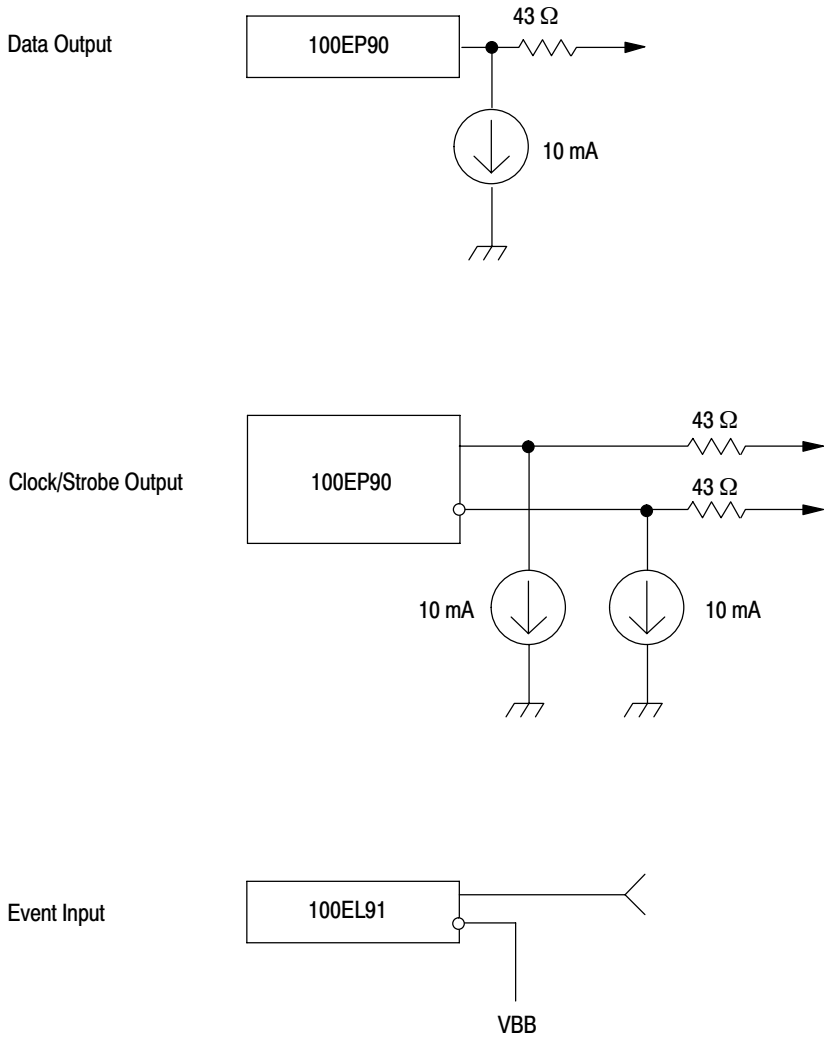

Figure 16: P6472 input/output circuit

P6473 The P6473 LVDS is compatible with the TIA/EIA-644 standard.

A generator circuit in the probe produces a balanced source that results in a differential voltage across a test termination load of 100 Ω in the range of 250 mV to 450 mV.

Figure 17 illustrates the signaling sense of the voltages appearing across the termination resistor.

- The A terminal of the generator is negative with respect to the B terminal for a binary 1 or OFF state.
- The A terminal of the generator is positive with respect to the B terminal for a binary 0 or ON state.

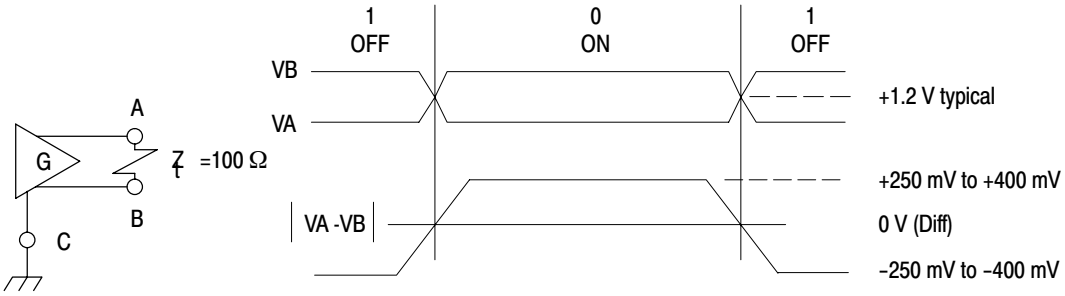

Figure 17: Signaling sense

P6474

Figure 18 shows the input/output circuit for the P6474 LVCMOS pattern generator probe. The P6474 provides LVCMOS signals to the target system and contains 16 data outputs, one clock output and one strobe output. You can adjust the V_{cc} of the output driver and the input receiver from 1.2 V to 3.3 V. The P6474 comes standard with 75 Ω resistor packs. You can change the resistor packs to provide impedance matching for the target system.

The P6474 provides 16 data outputs, 1 clock output and 1 strobe output.

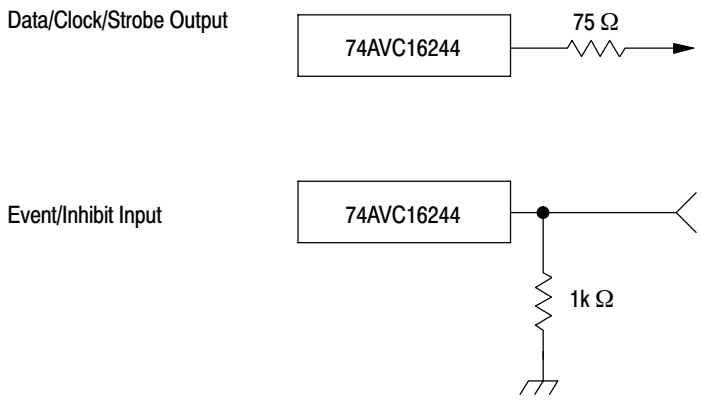

Figure 18: P6474 input/output circuit

Timing Diagrams

Figures 19 through 24 show the pattern generator timing diagrams. The diagrams apply to all probes unless otherwise stated.

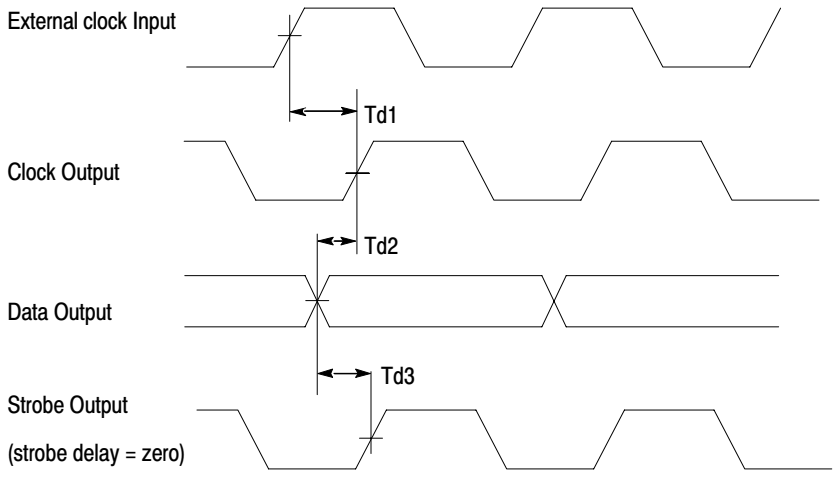

Figure 19: Clock and strobe timing diagram

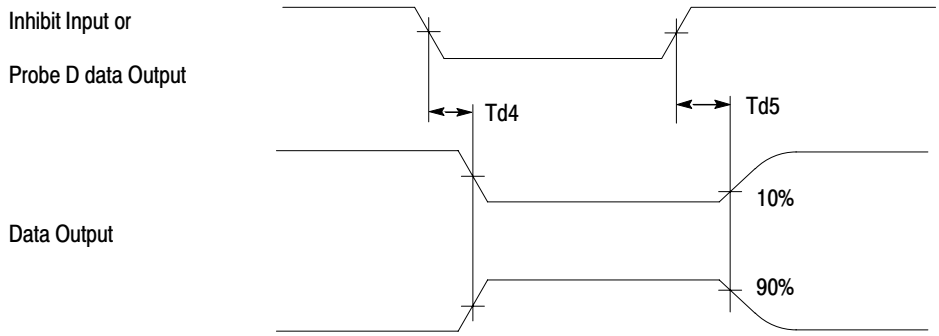

Figure 20: P6470, P6472, P6473, and P6474 inhibit timing diagram

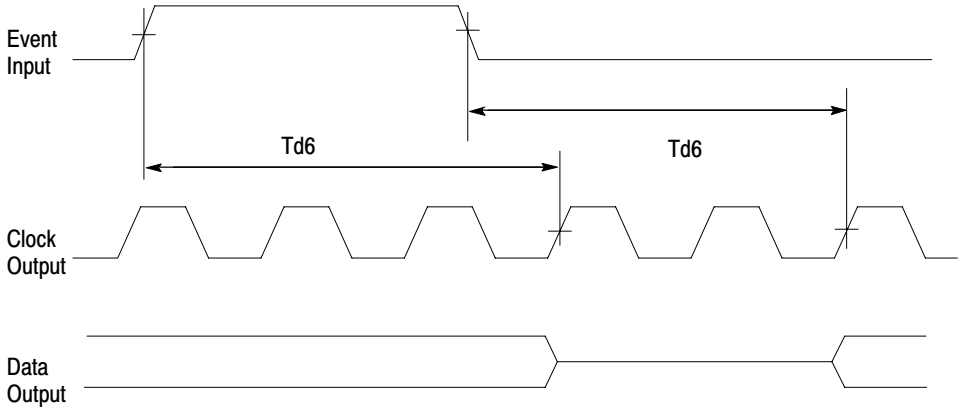

Figure 21: P6470, P6472, P6473, and P6474 external event for inhibit timing diagram

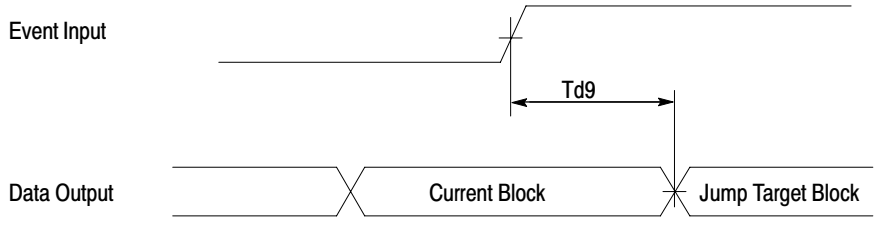

Figure 22: External event for jump timing diagram

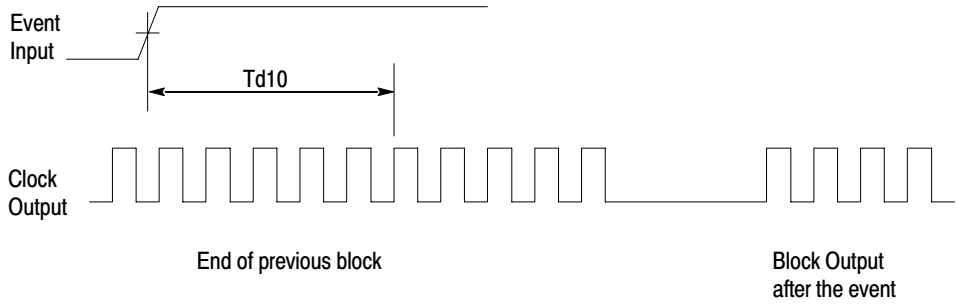

Figure 23: External event for half channel advance timing diagram

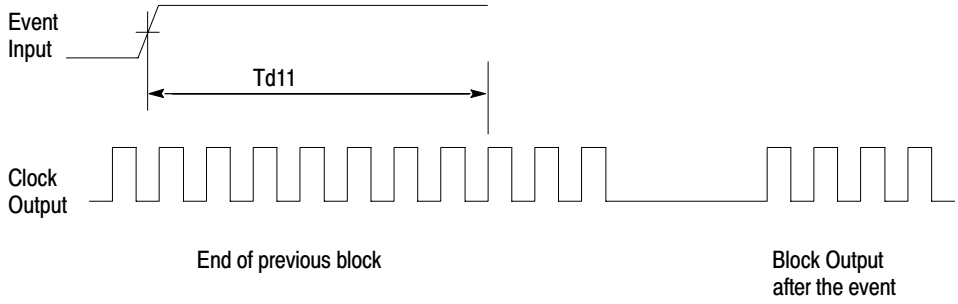

Figure 24: External event for full channel advance timing diagram

Figure 25: External event for delay to data output for advance diagram

Specifications

The specifications apply to all versions of the pattern generator unless otherwise noted.

Table 3: P6470 TTL/CMOS probe

All timing values are specified at the probe connector under the conditions listed below, unless otherwise noted:
Output Voltage setting: +5 V
Series Termination Resistor: 75 Ω
Load: 510 Ω + 50 pF

Characteristic	Description		
Maximum Clock Frequency (with series termination resistor: 75 Ω)	Output Level (V_{cc})	Full Channel mode	Half Channel mode
	Vcc ≤ 3.3 V	134 MHz	268 MHz
	3.3 V < Vcc ≤ 5 V	62.5 MHz	125 MHz
	Vcc > 5 V	52.5 MHz	105 MHz
Maximum Clock Frequency (with series termination resistor: 75 Ω, load: 10 kΩ + 15 pf, sample output pattern: 8 bit counter) *Typical*	Output Level (V_{cc})	Full Channel mode	Half Channel mode
	Vcc ≤ 5.5 V	134 MHz	268 MHz
Output Level (V_{CC})	2.0 V to 5.5 V, 25 mV step, into 1 MΩ		
Maximum Resistive Load	220 Ω		
Maximum Capacitive Load	50 pF		
Output Type	74LVC541A for Data Output 74LVC244A for Clock/Strobe Output		
Series Termination Resistor	75 Ω standard. 43, 100 and 150 Ω as optional accessories (18 pin DIP socket)		
Supported Channel Mode	Half and Full		
Number of External Inhibit Inputs	1		
Rise/Fall Time (20% to 80% load: 1 MΩ +< 1 pF) *Typical*	Clock/Strobe Output Rise 640 ps Fall 1.1 ns Data Output Rise 680 ps Fall 2.9 ns		
Rise/Fall Time (20% to 80% load: 510 Ω + 51 pF) *Typical*	Clock/Strobe Output Rise 6.5 ns Fall 6.3 ns Data Output Rise 5.2 ns Fall 4.5 ns		

Table 3: P6470 TTL/CMOS probe (Cont.)

All timing values are specified at the probe connector under the conditions listed below, unless otherwise noted:
Output Voltage setting: +5 V
Series Termination Resistor: 75 Ω
Load: 510 Ω + 50 pF

Characteristic	Description
Data Output Skew *Typical*	< 570 ps between all data output pins of all modules in the mainframe after intermodule skew is adjusted manually < 480 ps between all data output pins of all probes of single module < 440 ps between all data output pins of single probe
Data Output to Strobe Output Delay *Typical*	+ 1.7 ns when strobe delay set to zero. (Td3 in Figure 19 on page 22)
Data Output to Clock Output Delay *Typical*	+2.4 ns (Td2 in Figure 19 on page 22)
External Clock Input to Clock Output Delay *Typical*	61 ns (Td1 in Figure 19 on page 22)
External Inhibit Input to Output Enable Delay *Typical*	34 ns for Data Output (Td4 in Figure 20 on page 23)
External Inhibit Input to Output Disable Delay *Typical*	86 ns for Data Output (Td5 in Figure 20 on page 23)
Probe D Data Output to Output Enable Delay (for Internal Inhibit) *Typical*	7 ns for Data Output (Td4 in Figure 20 on page 23)
Probe D Data Output to Output Disable Delay (for Internal Inhibit) *Typical*	8 ns for Data Output (Td5 in Figure 20 on page 23)
External Event Input to Clock Output Setup (for inhibit) (event-filter: off) *Typical*	Full channel mode: 1.5 clocks + 240 ns (Td6 in Figure 21 on page 23) Half channel mode: 2 clocks + 240 ns
External Event Input and Inhibit Input Input Type Minimum Pulse Width	 74LVC14A, Positive True, 1 kΩ to GND 200 ns (event filter: off)
External Event Input Delay to Data Output for Advance	230 ns to 330 ns + 1.5 to 2.5 CLK2 (Td12 in Figure 25 on page 24) (CLK2 is from 2.5 ns to 5 ns when Internal Clock is used. It is the same as one clock period when the External Clock is used.)
External Event Input Number of Inputs Setup Time of Event *Typical* Input for Event Jump	 2 Half Channel Mode 54 to 61 clocks + 240 ns before the next block Full Channel Mode 27.5 to 31 clocks + 240 ns before the next block (Td9 in Figure 22 on page 23)

Table 3: P6470 TTL/CMOS probe (Cont.)

All timing values are specified at the probe connector under the conditions listed below, unless otherwise noted:
Output Voltage setting: +5 V
Series Termination Resistor: 75 Ω
Load: 510 Ω + 50 pF

Characteristic	Description
Setup Time of Event Input for Event Advance *Typical*	In Half Channel Mode, 240 ns before the rising edge of 5th clock output pulse from the last of the previous block (Td10 in Figure 23 on page 24) In Full Channel Mode, 240 ns before the rising edge of 3rd clock output pulse from the last of the previous block (Td11 in Figure 24 on page 24)
Mainframe External Signal Input to PG Probe data output for Advance via Signal 1, 2 *Typical* via Signal 3, 4 *Typical*	 200 ns to 300 ns + 1.5 to 2.5 CLK2 230 ns to 330 ns + 1.5 to 2.5 CLK2 (CLK2 is from 2.5 ns to 5 ns when the Internal Clock is used. It is the same as one clock period when the External Clock is used)
for Inhibit via Signal 1, 2 *Typical*	 100 ns to 200 ns + 2 to 3 CLK (Half Channel Mode) 100 ns to 200 ns + 1.5 to 2.5 CLK (Full Channel Mode)
via Signal 3, 4 *Typical*	130 ns to 230 ns+ 2 to 3 CLK (Half Channel Mode) 130 ns to 230 ns + 1.5 to 2.5 CLK (Full Channel Mode)
PG Probe Clock Output to Mainframe External Signal Output via Signal 1, 2 *Typical* via Signal 3, 4 *Typical*	 18 ns – 5 CLK (Half Channel Mode) 18 ns – 3 CLK (Full Channel Mode) 29 ns – 5 CLK (Half Channel Mode) 29 ns – 3 CLK (Full Channel Mode)
Number of Data Outputs	16 in Full Channel Mode 8 in Half Channel Mode
Number of Clock Outputs	1
Number of Strobe Outputs	1 (Only one Clock Output or Strobe Output can be enabled at one time per probe)
Number of External Event Inputs	2
Clock Output Polarity	Positive
Strobe Type	RZ only

Table 4: P6471 ECL probe

All timing values are specified at the probe connector under the condition listed below, unless otherwise noted:
Load: 51 Ω terminated to –2 V

Characteristic	Description
Maximum Clock Frequency	134 MHz in Full Channel mode 268 MHz in Half Channel mode
Output Level	ECL
Output Type	100E151 for data output 100EL16 for strobe output 100EL04 for clock output outputs are unterminated
Supported Channel Mode	Half and Full
Rise/Fall Time (20% to 80%) *Typical*	Clock Output Rise 320 ps Fall 330 ps Data Output Rise 1,200 ps Fall 710 ps Strobe Output Rise 290 ps Fall 270 ps
Data Output Skew *Typical*	< 255 ps between all data output pins of all modules in the mainframe after intermodule skew is adjusted manually < 240 ps between all data output pins of all probes of single module < 210 ps between all data output pins of a single probe
Data Output to Strobe Output Delay *Typical*	+2.94 ns when strobe delay set to zero (Td3 in Figure 19 on page 22)
Data Output to Clock Output Delay *Typical*	+780 ps (Td2 in Figure 19 on page 22)
External Clock Input to Clock Output Delay *Typical*	50 ns (Td1 in Figure 19 on page 22)
External Event Input Delay to Data Output for Advance	170 ns to 270 ns + 1.5 to 2.5 CLK2 (Td12 in Figure 25 on page 24) (CLK2 is from 2.5 ns to 5 ns when Internal Clock is used. It is the same as one clock period when the External Clock is used.)
External Event Input Input Level Input Type Minimum Pulse Width	 ECL 10H116 with 75 kΩ to –2 V 150 ns (Event filter: off)
External Event Input Number of Inputs Setup Time of Event Input for Event Jump *Typical*	 2 Half Channel Mode, 54 to 61 clocks + 180 ns before the next block Full Channel Mode, 27.5 to 31 clocks + 180 ns before the next block (Td9 in Figure 22 on page 23)

Table 4: P6471 ECL probe (Cont.)

All timing values are specified at the probe connector under the condition listed below, unless otherwise noted:
Load: 51 Ω terminated to –2 V

Characteristic	Description
Setup Time of Event Input for Event Advance *Typical*	Half Channel Mode: 80 ns before the rising edge of 5th clock output pulse from the last of the previous block (Td10 in Figure 23 on page 24) Full Channel Mode 80 ns before the rising edge of 3rd clock output pulse from the last of the previous block (Td11 in Figure 24 on page 24)
Mainframe External Signal Input to PG Probe data output for Advance via Signal 1, 2 *Typical* via Signal 3, 4 *Typical*	 200 ns to 300 ns + 1.5 to 2.5 CLK2 230 ns to 330 ns + 1.5 to 2.5 CLK2 (CLK2 from 2.5 ns to 5 ns when Internal Clock is used. It is same as one clock period when External Clock is used.)
PG Probe Clock Output to Mainframe External Signal Output via Signal 1, 2 *Typical* via Signal 3, 4 *Typical*	 28 ns – 5 CLK (Half Channel Mode) 28 ns – 3 CLK (Full Channel Mode) 38 ns – 5 CLK (Half Channel Mode) 38 ns – 3 CLK (Full Channel Mode)
Number of Data Outputs	16 in Full Channel Mode 8 in Half Channel Mode
Number of Clock Outputs	1
Number of Strobe Outputs	1 (Only one Clock Output or one Strobe Output can be enabled at one time per probe)
Number of External Event Inputs	2
Clock Output Polarity	Positive
Strobe Type	RZ only

Table 5: P6472 PECL/LVPECL probe

All timing values are specified with a load condition of 1 M Ω + ≤ 1 pF with PECL mode.

Characteristic	Description	
Maximum Clock Frequency	Full Channel Mode	Half Channel Mode
	134 MHz	268 MHz
Number of Data Outputs	8 Full Channel 8 Half Channel	
Number of Clock Outputs	1 differential	
Number of Strobe Outputs	1 differential (Only one Clock Output or one Strobe Output can be enabled at one time per probe)	
Number of External Event Inputs	2	
Clock Output Polarity	Positive	
Strobe Type	RZ (return to zero) only	
Strobe Delay	Zero or Trailing Edge	
Output Level	PECL, LVPECL (selectable by moving a jumper in the probe)	
Output Type	100EL90 (all outputs are terminated)	
Supported Channel Mode	Half and Full	
Rise/Fall Time (20% to 80%)	Rise 430 ps Fall 970 ps	
Data Output Skew	< 385 ps between all data output pins of all modules in the mainframe after intermodule skew is adjusted manually < 370 ps between all data output pins of all probes of single module < 340 ps between all data output pins of a single probe	
Data Output to Strobe Output Delay	+ 2.93 ns when strobe delay is set to zero (See Td3 in Figure 19 on page 22)	
Data Output to Clock Output Delay	+ 1.12 ns (Td2 in Figure 19 on page 22)	
External Clock Input to Clock Output Delay	50 ns (See Td1 in Figure 19 on page 22)	
External Event Input Delay to Data Output for Advance	170 ns to 270 ns + 1.5 to 2.5 CLK2 (Td12 in Figure 25 on page 24) (CLK2 is from 2.5 ns to 5 ns when Internal Clock is used. It is the same as one clock period when the External Clock is used.)	
External Event Input		
Input Level	PECL, LVPECL (selectable by moving a jumper in the probe)	
Input Type	100EL91, unterminated	
Minimum Pulse Width (event filter: off)	150 ns	

Table 5: P6472 PECL/LVPECL probe (Cont.)

All timing values are specified with a load condition of 1 M Ω + ≤ 1 pF with PECL mode.

Characteristic	Description
External Event Input	
Setup Time of Event Input for Event Jump	Half Channel Mode: 54 to 61 Clocks + 180 ns before the next block Full Channel Mode: 27.5 to 31 Clocks + 180 ns before the next block (see Td9 in Figure 22 on page 23)
Setup Time of Event Input for Event Advance	Half Channel Mode: 180 ns before the rising edge of the 5th clock output pulse from the last of the previous block (See Td10 in Figure 23 on page 24) Full Channel Mode: 180 ns before the rising edge of the 3rd clock output pulse from the last of the previous block (see Td11 in Figure 24 on page 24)
Mainframe External Signal Input to PG Probe Data Output	
For Advance:	
Using signal 1 or 2	200 ns to 300 ns + 1.5 to 2.5 CLK2
Using signal 3 or 4	230 ns to 330 ns + 1.5 to 2.5 CLK2 (CLK2 is from 2.5 ns to 5 ns when Internal Clock is used. It is the same as one clock period when the External Clock is used.)
PG Probe Clock Output to Mainframe External Signal Output	
Using signal 1 or 2	31 ns –5 CLK (Half Channel Mode) 31 ns –3 CLK (Full Channel Mode)
Using signal 3 or 4	40 ns –5 CLK (Half Channel Mode) 40 ns –3 CLK (Full Channel Mode)

Table 6: P6473 LVDS probe

All timing values are specified at the probe connector under the condition listed below, unless otherwise noted:
Load: 100 Ω + < 1 pF

Characteristic	Description	
Maximum Clock Frequency	Full Channel Mode	Half Channel Mode
	134 MHz	268 MHz
Number of Data Outputs	16 Full Channel 8 Half Channel	

Table 6: P6473 LVDS probe (Cont.)

All timing values are specified at the probe connector under the condition listed below, unless otherwise noted:
Load: 100 Ω + < 1 pF

Characteristic	Description
Number of Clock Outputs	1 (Only one Clock Output or One Strobe Output can be enabled at one time per probe.)
Number of Strobe Outputs	1 (Only one Clock Output or One Strobe Output can be enabled at one time per probe.)
Number of External Event Inputs	1
Number of External Inhibit Inputs	1
Clock Output Polarity	Positive
Strobe Type	RZ (return to zero) only
Strobe Delay	Zero or Trailing Edge
Maximum Capacitive Load	10 pF
Output Type	LVDS (TIA/EIA-644 compatible)
Supported Channel Mode	Half and Full
Rise/Fall Time (20% to 80%)	Rise: 910 ps Fall: 750 ps
Data Output Skew	< 365 ps between all data output pins of all modules in the mainframe after intermodule skew is adjusted manually < 350 ps between all data output pins of all probes of single module < 320 ps between all data output pins of a single probe
Data Output to Strobe Output Delay	-280 ns when strobe delay is set to zero (See Td3 in Figure 19 on page 22)
Data Output to Clock Output Delay	1.2 ns (Td2 in Figure 19 on page 22)
External Clock Input to Clock Output Delay	55 ns (See Td1 in Figure 19 on page 22)
External Inhibit Input to Output Enable Delay	9 ns for Data Output (See Td4 in Figure 20 on page 23)
External Inhibit Input to Output Disable Delay	12 ns for Data Output (See Td5 in Figure 20 on page 23)
Probe D Data Output to Output Enable Delay (for Internal Inhibit)	2 ns for Data Output (See Td4 in Figure 20 on page 23)
Probe D Data Output to Output Disable Delay (for Internal Inhibit)	5 ns for Data Output (See Td5 in Figure 20 on page 23)
External Event Input to Clock Output Setup (for inhibit) event-filter: off	Full Channel mode: 1.5 Clocks + 180 ns Half Channel mode: 2 Clocks + 180 ns (See Td6 in Figure 21 on page 23)
External Event Input Delay to Data Output for Advance	170 ns to 270 ns + 1.5 to 2.5 CLK2 (Td12 in Figure 25 on page 24) (CLK2 is from 2.5 ns to 5 ns when Internal Clock is used. It is the same as one clock period when the External Clock is used.)

Table 6: P6473 LVDS probe (Cont.)

All timing values are specified at the probe connector under the condition listed below, unless otherwise noted:
Load: 100 Ω + < 1 pF

Characteristic	Description
External Event Input and Inhibit Input	
Input Type	LVDS (TIA/EIA-644 compatible), positive true
Minimum Pulse Width (event filter: off)	150 ns
External Event Input Setup Time of Event Input for Event Jump	Half Channel Mode: 54 to 61 Clocks + 180 ns before the next block Full Channel Mode: 27.5 to 31 Clocks + 180 ns before the next block (See Td9 in Figure 22 on page 23)
External Event Input Setup Time for Event Advance	Half Channel Mode: 180 ns before the rising edge of the 5th clock output pulse from the last of the previous block (See Td10 in Figure 23 on page 24) Full Channel Mode: 180 ns before the rising edge of the 3rd clock output pulse from the last of the previous block (See Td11 in Figure 24 on page 24)
Mainframe External Signal Input to PG Probe Data Output	
For Advance:	
Using signal 1 or 2	200 ns to 300 ns + 1.5 to 2.5 CLK2
Using signal 3 or 4	230 ns to 330 ns + 1.5 to 2.5 CLK2
	(CLK2 is from 2.5 ns to 5 ns when Internal Clock is used. It is the same as one clock period when the External Clock is used.)
For Inhibit:	
Using signal 1 or 2	100 ns to 200 ns + 2 to 3 CLK (Half Channel Mode) 100 ns to 200 ns +1.5 to 2.5 CLK (Full Channel Mode)
Using signal 3 or 4	130 ns 230 ns + 2 to 3 CLK (Half Channel Mode) 130 ns to 230 ns + 1.5 to 2.5 CLK (Full Channel Mode)
PG Probe Clock Output to Mainframe External Signal Output	
Using signal 1 or 2	26 ns -5 CLK (Half Channel Mode) 26 ns -3 CLK (Full Channel Mode)
Using signal 3 or 4	35 ns -5 CLK (Half Channel Mode) 35 ns -3 CLK (Full Channel Mode)

Table 7: P6474 LVCMOS probe

All timing values are specified at the probe connector under the conditions listed below, unless otherwise noted:

Output Voltage setting: +3.3 V

Series Termination Resistor: 75 Ω

Load: 510 Ω + 20 pF

Characteristic	Description	
Maximum Clock Frequency	Full Channel Mode	Half Channel Mode
	134 MHz	268 MHz
Number of Data Outputs	16 Full Channel 8 Half Channel	
Number of Clock Outputs	1 (Only one Clock Output or One Strobe Output can be enabled at one time per probe.)	
Number of Strobe Outputs	1 (Only one Clock Output or One Strobe Output can be enabled at one time per probe.)	
Number of External Event Inputs	2	
Number of External Inhibit Inputs	1	
Clock Output Polarity	Positive	
Strobe Type	RZ (return to zero) only	
Strobe Delay	Zero or Trailing Edge	
Output Level (V_{cc})	1.2 V to 3.3 V, 25 mV step, into 1 M Ω	
Maximum Resistive Load	510 Ω	
Maximum Capacitive Load	20 pF	
Output Type	74AVC16244	
Series Termination Resistor	75 Ω standard. 43, 100 and 150 Ω as optional accessories (18 pin DIP socket)	
Supported Channel Mode	Half and Full	
Rise/Fall Time (20 % to 80 %, load: 1M Ω + < 1 pF)	Rise 1200 ps Fall 610 ps	
Rise/Fall Time (20 % to 80 %, load: 510 Ω + 50 pF)	Rise 3.4 ns Fall 3.2 ns	
Data Output Skew	< 590 ps between all data output pins of all modules in the mainframe after intermodule skew is adjusted manually < 500 ps between all data output pins of all probes of single module < 460 ps between all data output pins of a single probe	
Data Output to Strobe Output Delay	460 ps when strobe delay is set to zero (See Td3 in Figure 19 on page 22)	
Data Output to Clock Output Delay	1.84 ns (Td2 in Figure 19 on page 22)	
External Clock Input to Clock Output Delay	55 ns (See Td1 in Figure 19 on page 22)	

Table 7: P6474 LVCMOS probe (Cont.)

All timing values are specified at the probe connector under the conditions listed below, unless otherwise noted:

Output Voltage setting: +3.3 V

Series Termination Resistor: 75 Ω

Load: 510 Ω + 20 pF

Characteristic	Description
External Inhibit Input to Output Enable Delay	36 ns for Data Output (See Td4 in Figure 20 on page 22)
External Inhibit Input to Output Disable Delay	18 ns for Data Output (See Td5 in Figure 20 on page 22)
Probe D Data Output to Output Enable Delay (for Internal Inhibit)	6 ns for Data Output (See Td4 in Figure 20 on page 22)
Probe D Data Output to Output Disable Delay (for Internal Inhibit)	7 ns for Data Output (See Td5 in Figure 20 on page 22)
External Event Input to Clock Output Setup (for inhibit) event-filter: off	Full Channel mode: 1.5 Clocks + 180 ns Half Channel mode: 2 Clocks + 180 ns (See Td6 in Figure 21 on page 23)
External Event Input Delay to Data Output for Advance	170 ns to 270 ns + 1.5 to 2.5 CLK2 (Td12 in Figure 25 on page 24) (CLK2 is from 2.5 ns to 5 ns when Internal Clock is used. It is the same as one clock period when the External Clock is used.)
External Event Input and Inhibit Input	
Input Type	74AVC16244, Positive True, 1 k Ω to GND The V_{cc} of the input receiver is variable and the same as the V_{cc} of the output driver.
Minimum Pulse Width	150 ns (event filter: off)
External Event Input	
Setup Time of Event	Half Channel Mode: 54 to 61 Clocks + 180 ns before the next block
Input for Event Jump	Full Channel Mode: 27.5 to 31 Clocks + 180 ns before the next block (See Td9 in Figure 22 on page 23)
External Event Input Setup Time for Event Advance	Half Channel Mode: 180 ns before the rising edge of the 5th clock output pulse from the last of the previous block (See Td10 in Figure 23 o n page 24) Full Channel Mode: 180 ns before the rising edge of the 3rd clock output pulse from the last of the previous block (See Td11 in Figure 24 on page 24)

Table 7: P6474 LVCMOS probe (Cont.)

All timing values are specified at the probe connector under the conditions listed below, unless otherwise noted:

Output Voltage setting: +3.3 V

Series Termination Resistor: 75 Ω

Load: 510 Ω + 20 pF

Characteristic	Description
Mainframe External Signal Input to PG Probe Data Output	
For Advance:	
Using signal 1 or 2	200 ns to 300 ns + 1 to 2 CLK2
Using signal 3 or 4	230 ns to 330 ns + 1 to 2 CLK2
	(CLK2 is from 2.5 ns to 5 ns when the Internal Clock is used. It is the same as one clock period when the External Clock is used.)
For Inhibit:	
Using signal 1 or 2	100 ns to 200 ns + 2 to 3 CLK (Half Channel Mode)
	100 ns to 200 ns + 1.5 to 2.5 CLK (Full Channel Mode)
Using signal 3 or 4	130 ns to 230 ns + 2 to 3 CLK (Half Channel Mode)
	130 ns to 230 ns + 1.5 to 2.5 CLK (Full Channel Mode)
PG Probe Clock Output to Mainframe External Signal Output	
Using signal 1 or 2	25 ns –5 CLK (Half Channel Mode)
	25 ns –3 CLK (Full Channel Mode)
Using signal 3 or 4	34 ns –5 CLK (Half Channel Mode)
	34 ns –3 CLK (Full Channel Mode)

Table 8: P6475 Variable probe

All timing values are specified at the probe connector under the conditions listed below, unless otherwise noted:

Output Voltage setting: Voh +2 V, Vol 0 V

Slew Rate: 2.5 V/ns

Delay Range: 0

Delay Time: 0 ns

Load: 50 Ω

Characteristic	Description		
Maximum Clock Frequency		**Full CH Mode**	**Half CH Mode**
	Delay Range: 0 Delay ≤ 10 ns	134 MHz	268 MHz
	Delay Range: 0 Delay ≥ 10 ns	134 MHz	268 MHz
	Delay Range: 1,2,3	30 MHz	30 MHz
Number of Data Outputs	8 (CH0 to CH7)		
Number of Clock Outputs	1		
Number of Strobe Outputs	0		
Number of External Event Inputs	2		
Number of External Inhibit Inputs	1		
Clock Output Polarity	Positive or Negative		
Data Format	CH0 to CH5: NRZ CH6 and CH7: NRZ, R1 or RZ (independent)		
Output Impedance	50 Ω		
Output Level			
Vol	-3 V to +6.75, 10 mV step, into 1 M Ω		
Voh	-2.75 V to +7 V, 10 mV step, into 1 M Ω		
Voltage Swing	250 mV_{p-p} to 9 V_{p-p}		
Control	CH0 to CH5: Common CH6, CH7, CLK: Independent		
Accuracy	± 3% of value ± 0.1 V		
Output Current			
Sink	<-30 mA		
Source	<+30 mA		
Supported Channel Mode	Half and Full		

Table 8: P6475 Variable probe (Cont.)

All timing values are specified at the probe connector under the conditions listed below, unless otherwise noted:

Output Voltage setting: Voh +2 V, Vol 0 V

Slew Rate: 2.5 V/ns

Delay Range: 0

Delay Time: 0 ns

Load: 50 Ω

Characteristic	Description		
Delay Channel	CH6 and CH7 (Independent)		
Delay Time	**Delay Range**	**Minimum Delay**	**Maximum Delay**
	0	0 ns	20 ns
	1	15 ns	30 ns
	2	25 ns	40 ns
	3	35 ns	50 ns
	With reference to CH0, CH6, CH7 independent.		
Delay Resolution	10 ps		
Delay Accuracy	± (3% of Delay Time) ± 0.8 ns (to CH0) (For delay range of 1, 2, and 3 this is only for rising edge. The falling edge will be delayed approximately 4 ns from the setting value.)		
CH6 Output Mode	The following five modes are available: Normal CH6 or CH7 CH6 and CH7 CH6 or (not CH7) CH6 and (not CH7)		
Slew Rate Control	0.5 V/ns to 2.5 V/ns, 100 mV step		
Rise/Fall Time 20 % to 80 % at maximum slew rate, load: 1 M Ω + < 10 pF	Rise 550 ps Fall 640 ps		
Rise/Fall Time 20 % to 80 % at maximum slew rate, load: 50 Ω	Rise 430 ps Fall 510 ps		

Table 8: P6475 Variable probe (Cont.)

All timing values are specified at the probe connector under the conditions listed below, unless otherwise noted:

Output Voltage setting: Voh +2 V, Vol 0 V

Slew Rate: 2.5 V/ns

Delay Range: 0

Delay Time: 0 ns

Load: 50 Ω

Characteristic	Description
Data Output Skew	< 295 ps between all data output pins of all modules in the mainframe after intermodule skew is adjusted manually < 280 ps between all data output pins of all probes of single module < 250 ps between all data output pins of a single probe
Data Output to Clock Output Delay	940 ps (See Td2 in Figure 19 on page 22)
External Clock Input to Clock Output Delay	62 ns (See Td1 in Figure 19 on page 22)
External Inhibit Input to Output Enable Delay	30 ns for Data Output (See Td4 in Figure 20 on page 23)
External Inhibit Input to Output Disable Delay	28 ns for Data Output (See Td5 in Figure 19 on page)
Probe D Data Output to Output Enable Delay (for Internal Inhibit)	-100 ps for Data Output (See Td4 in Figure 20 on page 23)
Probe D Data Output to Output Disable Delay (for Internal Inhibit)	-4.4 ns for Data Output (See Td5 in Figure 20 on page 23)
External Event Input to Clock Output Setup (for inhibit) event-filter: off	Full Channel mode: 1.5 Clocks +180 ns Half Channel mode: 2 Clocks + 180 ns (See Td6 in Figure 21 on page 23)
External Event Input Delay to Data Output for Advance	170 ns to 270 ns + 1.5 to 2.5 CLK2 (Td12 in Figure 25 on page 24) (CLK2 is from 2.5 ns to 5 ns when Internal Clock is used. It is the same as one clock period when the External Clock is used.)
External Event Input and Inhibit Input	
Polarity	Positive True
Impedance	1 k Ω to GND
Threshold:	
Level	-2.5 V to +2.5 V Event and Inhibit are independent
Resolution	20 mV
Minimum Pulse Width	150 ns (event filter: off)

Table 8: P6475 Variable probe (Cont.)

All timing values are specified at the probe connector under the conditions listed below, unless otherwise noted:

Output Voltage setting: Voh +2 V, Vol 0 V

Slew Rate: 2.5 V/ns

Delay Range: 0

Delay Time: 0 ns

Load: 50 Ω

Characteristic	Description
External Event Input	
Setup Time of Event Input for Event Jump	Half Channel Mode: 54 to 61 Clocks + 180 ns before the next block Full Channel Mode: 27.5 to 31 Clocks + 180 ns before the next block (See Td9 in Figure 22 on page 23)
Setup Time of Event Input for Event Advance	Half Channel Mode: 180 ns before the rising edge of the 5th clock output pulse from the last of the previous block (See Td10 in Figure 23 on page 24) Full Channel Mode: 180 ns before the rising edge of the 3rd clock output pulse from the last of the previous block (See Td11 in Figure 24 on page 24)

Table 8: P6475 Variable probe (Cont.)

All timing values are specified at the probe connector under the conditions listed below, unless otherwise noted:

Output Voltage setting: Voh +2 V, Vol 0 V

Slew Rate: 2.5 V/ns

Delay Range: 0

Delay Time: 0 ns

Load: 50 Ω

Characteristic	Description
Mainframe External Signal Input to PG Probe Data Output	
For Advance:	
Using signal 1 or 2	200 to 300 ns + 1.5 to 2.5 CLK2
Using signal 3 or 4	230 to 330 ns + 1.5 to 2.5 CLK2
	(CLK2 is from 2.5 ns to 5 ns when the Internal Clock is used. It is the same as one clock period when the External Clock is used.)
For Inhibit: (Output Enable)	
Using signal 1 or 2	100 to 200 ns + 2 to 3 CLK (Half Channel Mode)
	100 to 200 ns +1.5 to 2.5 CLK (Full Channel Mode)
Using signal 3 or 4	130 to 230 ns + 2 to 3 CLK (Half Channel Mode)
	130 to 230 ns + 1.5 to 2.5 CLK (Full Channel Mode)
For Inhibit: (Output Disable)	
Using signal 1 or 2	100 to 200 ns + 2 to 3 CLK (Half Channel Mode)
	100 to 200 ns +1.5 to 2.5 CLK (Full Channel Mode)
Using signal 3 or 4	130 to 230 ns + 2 to 3 CLK (Half Channel Mode)
	130 to 230 ns + 1.5 to 2.5 CLK (Full Channel Mode)
PG Probe Clock Output to Mainframe External Signal Output Delay	
Using signal 1 or 2	19 ns –5 CLK (Half Channel Mode)
	19 ns –3 CLK (Full Channel Mode)
Using signal 3 or 4	28 ns –5 CLK (Half Channel Mode)
	28 ns –3 CLK (Full Channel Mode)

Table 9: Power Supply (P6475 only)

Characteristic	Description
AC Line Power	
Voltage rating	100 – 240 V AC
Voltage range	90 – 250 V AC
Frequency range	50 to 60 Hz
Maximum power	35 W
Maximum current	2 A

Table 10: Atmospherics

Characteristic	Description
Temperature	
Operating:	+0°C to + 50°C
Nonoperating:	–20°C to + 60°C
Relative Humidity	
Operating:	20% to 80% (No condensation)
	Maximum wet-bulb temperature 29.4°C
Nonoperating:	5% to 90% (No condensation)
	Maximum wet-bulb temperature 40.0°C
Altitude	
Operating:	Up to 4.5 km (15,000 ft)
	Maximum operating temperature decreases 1°C
Nonoperating:	Up to 15 km (50,000 ft)

Table 11: Dynamics characteristics (P6470, P6471, P6472, P6473, P6474)

Characteristic	Description
Vibration	
Operating:	3.038 m/s^2 (0.31 G_{rms}), 5 Hz to 500 Hz
Nonoperating:	24.108 m/s^2 (2.46 G_{rms}), 5 Hz to 500 Hz
Shock	
Nonoperating:	294 m/s^2 (30G), half-sine, 11 ms duration, 3 shocks per axis in each direction (18 shocks total)

Table 12: Dynamics characteristics (P6475)

Characteristic	Description
Vibration	
Operating:	3.038 m/s^2 (0.31 G_{rms}), 5 Hz to 500 Hz
Nonoperating:	24.108 m/s^2 (2.46 G_{rms}) , 5 Hz to 500 Hz
Shock (P6475 only)	
Nonoperating:	588 m/s^2 (60G), half-sine, 11 ms duration, 3 shocks per axis in each direction (18 shocks total)

Table 13: Probe cables

Characteristic	Description
Dimensions Length	1.5 m (5 ft) Standard probe cable
Length	3.3 m (10.83 ft) Time alignment cable

Table 14: Twisted lead set

Characteristic	Description
Dimensions Length	25.4 cm (10 in)

Table 15: Certifications and compliances for P6475

Category	Standards or description
Safety	
Third party certification	UL 3111-1
	CSA C22.2 No.1010.1
Self-Declaration	EN61010-1 with second amendment

Maintenance

The pattern generator probes do not require scheduled or periodic maintenance.

Functional Check

To verify the functionality of the pattern generator probe, you can set up the pattern generator to output a simple data pattern and use an oscilloscope or a logic analyzer to verify the data changes at the probe tips. For more extensive checks, refer to the *TLA7PG2 Pattern Generator and Probes Service Manual*

Inspection and Cleaning

To maintain good electrical contact, keep the probes free of dirt, dust, and contaminants. Remove dirt and dust with a soft brush. For more extensive cleaning use only a damp cloth. Never use abrasive cleaners or organic solvents. See the *TLA7PG2 Pattern Generator and Probes Service Manual* for more extensive cleaning instructions.

Static Discharge Information

Read the *General Safety Summary* and the *Service Safety Summary* at the front of this manual before attempting any procedures in this chapter.

- Minimize handling of static-sensitive circuit boards.
- Discharge the static voltage from your body by wearing a grounded antistatic wrist strap while handling these circuit boards. Service static-sensitive circuit boards only at a static-free work station.
- Nothing capable of generating or holding a static charge should be allowed on the work station surface.
- Avoid handling circuit boards in areas that have a floor or work-surface covering capable of generating a static charge.

Configuring Probes

This subsection provides instructions for changing the resistor packs on the P6470 and P6474 and instructions for configuring the P6472 for PECL or LVPECL.

CAUTION. *To prevent possible injury, disconnect the pattern generator and DUT from the probes prior to removing the probe cover.*

Removing the Probe Cover

Follow the steps below to remove the probe cover. See Figure 26.

1. Remove the four screws securing the probe cover.
2. Release the cover latches by pushing the tip of a small flat-blade screwdriver into the cutouts on each side of the probe. Do not pry.
3. Remove the top cover.

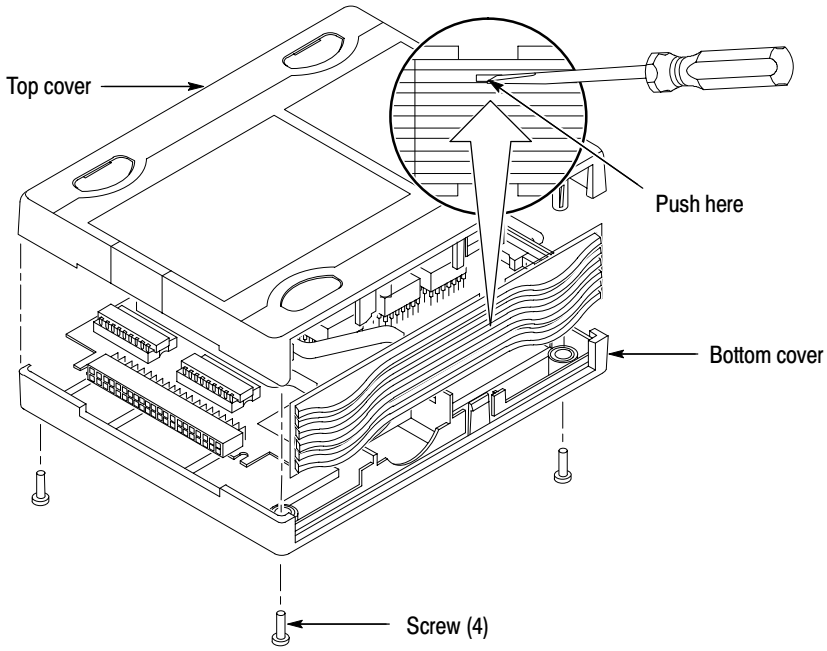

Figure 26: Removing the standard probe cover

Changing the Series Termination Resistors (P6470 and P6474 only)

Table 16 lists the various resistor packs available for the P6470 and P6474 probes (see Figure 27 for the P6470 and Figure 28 for the P6474). These resistor packs are a subpart of the 015-A095-00 kit.

Table 16: P6470 series termination resistors

Part number	Value
307-1683-00	43 Ω
307-1684-00	75 Ω
307-1686-00	100 Ω
307-1687-00	150 Ω

***NOTE**. Be careful not to bend the resistor pack pins when installing the replacement resistors in sockets.*

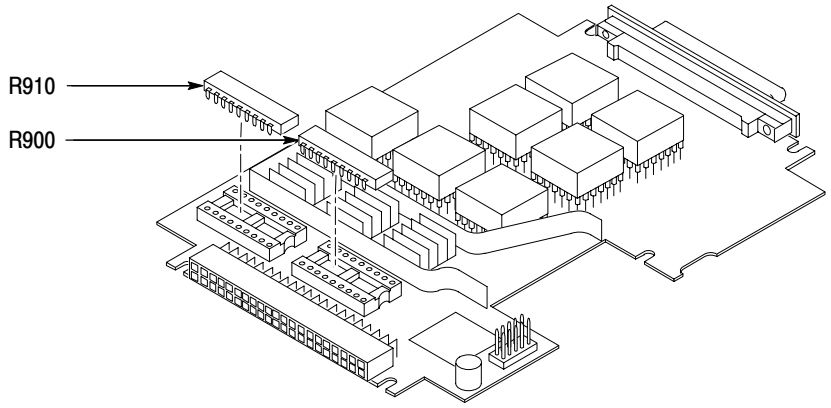

Figure 27: P6470 series termination resistors

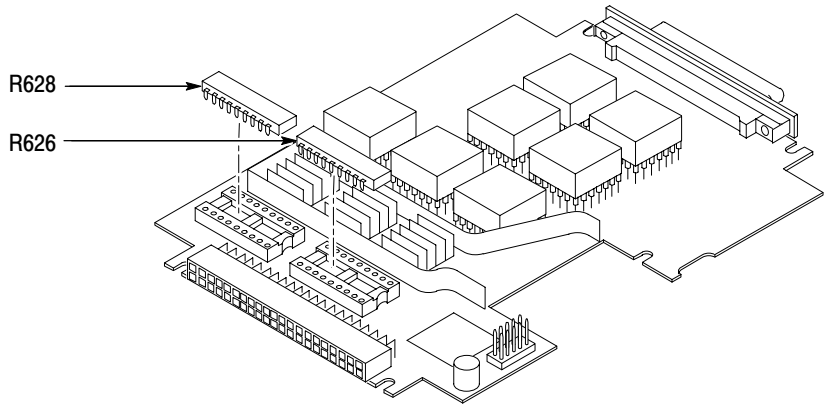

Figure 28: P6474 series termination resistors

Configuring the P6472 for PECL or LVPECL

You can select the PECL or LVPECL circuit by moving the J300 jumper inside the probe to the J300 pin locations as shown in Figure 29.

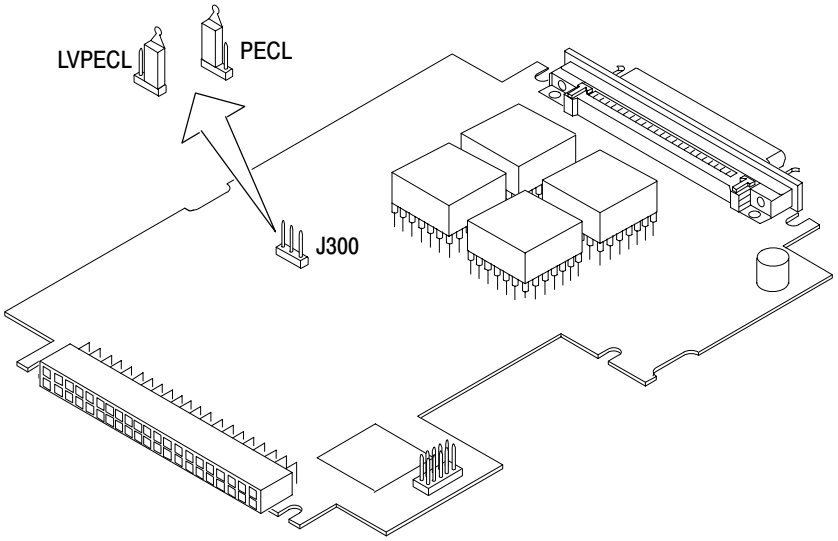

Figure 29: P6472 PECL and LVPECL jumper position

Fuses

Refer to the *TLA7PG2 Pattern Generator and Probes Service Manual for probe* fuse ratings and characteristic information.

Tektronix does not recommend the replacement of these fuses by the customer due to possible damage to the circuit boards. If these probes need repair, contact your local Tektronix Service Center.

Repackaging

If at all possible, use the original packaging to ship or to store the probes. If the original packaging is not available, use a corrugated cardboard shipping carton. Add cushioning material to prevent the probes from moving around in the shipping container.

Enclose the following information when shipping the probe to a Tektronix Service Center:

- The owner's name
- The name and phone number of a contact person
- The type and serial number of the probe
- Reason for returning
- A complete description of the service required

Seal the shipping carton with an industrial stapler or strapping tape.

Mark the address of the Tektronix Service Center and your own return address on the shipping carton in two prominent locations.

保証規定

保証期間 (納入後 1 年間) 内に、通常の取り扱いによって生じた故障は無料で修理いたします。

1. 取扱説明書、本体ラベルなどの注意書きに従った正常な使用状況で保証期間内に故障した場合には、販売店または当社に修理をご依頼下されば無料で修理いたします。なお、この保証の対象は製品本体に限られます。
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   - 移動時の落下などによる故障および損傷の修理
   - 火災、地震、風水害、その他の天変地異、公害、塩害、異常電圧などによる故障および損傷の修理
   - 消耗品、付属品などの消耗による交換
   - 出張修理(ただし故障した製品の配送料金は、当社負担)
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5. この規定は、日本国内においてのみ有効です。(This warranty is valid only in Japan.)

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お問い合わせ

製品についてのご相談・ご質問につきましては、下記までお問い合わせください。

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修理・校正につきましては、お買い求めの販売店または下記サービス受付センターまでお問い合わせください。

（ご連絡の際に、型名、故障状況等を簡単にお知らせください）

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