PANTHER DUAL DISPLAY BOARD

TECHNICAL MANUAL

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CONTENTS

1. Introduction

This document describes the Panther Dual Display Board, part of the C.A.T. family of products. The board drives two independent high resolution colour display monitors with multiple video layers for applications such as:

- High Performance Graphics - Primalib, X-Windows
- Mixed Graphics and Radar displays
- Mixed Graphics and Video displays

This manual describes the operation and use of the Panther Dual Display Board, this will always be used in combination with the C.A.T. processor card, but the C.A.T. is not described here - for details of the C.A.T. processor and it operation see the C.A.T. Processor Technical Manual.

1.1 Features

The Panther is implemented as a full sized 6U VME card, but it will always be used as a part of a two slot module with the C.A.T. Processor. The Panther is completely controlled by the C.A.T. and only connects to the backplane for power.

Features of the Panther are:

- Two separate Video Outputs using standard 15W H:D connectors
- Three separate 8 bit frame stores for each output
- Separate R.G.B. LUT and DAC for each output
- SVC interface for external 8 bit digital video source
- Screen resolutions up to 1600x1280
- Fully programmable display formats
- Independent hardware cursor for each output
- Both video outputs use the same format
- Compatible with Vortex Video Keyer

1.2 Applications

The Panther Dual Display Board is aimed at applications where two display monitors need to be driven by the same graphics processor. The multi-layering capability of the Panther allows each monitor to display an independent mix of text, graphics, radar and live video. One daughterboard can be fitted to the CAT base card when using Panther in the standard configuration.

A typical application would be for a twin display monitor console. A single operator would use both monitors as individual screens of a dual-headed X-Server. One of these screens could be displaying live radar overlaid with graphics within an X-Window, whilst the other screen could be displaying live video within an X-Window.

A mixed radar/video system such as this may optionally be implemented with an external radar scan converter. Scan converted radar video would be input via the SVC, and the Panther frame stores would be used as follows:

Output 0		Output 1	
Overlay:	X-Windows (screen 0)	Overlay:	X-Windows (screen 1)
SVC:	Radar	SVC:	not used
Middle:	not used	Middle:	Video high byte
Underlay:	Background Map	Underlay:	Video lo byte

In this application the video layers are controlled by index values in the two overlay frame stores. Index values 0 to 248 are used for drawing text and graphics, but values above 248 are used for enabling the other video layers. Thus drawing a rectangle filled with the index value 249 would display radar data from the SVC, whilst a fill value of 254 would display 16 bit colour video.

The usage of the frame stores, and the way that the data from them is combined and displayed, is controlled by the Panther's FPGA Multiplexers. By loading different FPGA codes, normally at the time of manufacture, any number of multi-layer display applications may be addressed.

1.3 Performance

The measured drawing performance for a C.A.T. and Panther combination are:

Line Drawing (10 Pixel Vectors, 8 bits per pixel)

- Vectors per second 1.2 Million

Image Copy (500 pixel x 500 pixel, 8 bits per pixel)

- On screen to on screen 66 Million pixels/second
- Off screen to on screen 100 Million pixels/second

1.4 Related Documents

C.A.T. Processor Technical Manual, Document No. 495-701000
C.A.T. Monitor and Support Utilities User Guide, Document No. 494-538000

2. Installation

2.1 Getting Started

The Panther Dual Display Board will normally be supplied already attached to a C.A.T. Processor Card, in which case simply follow the C.A.T. installation instructions with the following additions:

Forced air cooling may be required in systems where high ambient temperatures are likely within the VME rack, see the Specification, section **3.4 Environmental** of this manual.

The display format and video timings for the Panther are defined in the C.A.T.=s EERAM, see section **2.4 EERAM Settings** below.

If the Panther is not already fitted to a C.A.T. or it is desired to separate a C.A.T. and a Panther see section **2.5 Panther and C.A.T. Assembly**.

2.2 Front Panel

The front panel of a C.A.T. + Panther combination is shown in Figure 2.1. The connectors SVC INTERFACE, VIDEO O/P 0, VIDEO O/P 1 are mounted on the Panther. The RST switch, LEDs and SERIAL I/O are mounted on the C.A.T. card.

Each VIDEO O/P connector should be connected to a display monitor using a suitable video cable. The video and sync signal levels conform to industry standards and are detailed in section **3.1.2 Video Outputs.** The connector pinout conforms to the industry standard VGA definition, see **Appendix C.**

The SVC interface is only intended to be connected to other Primagraphics cards, for example a 895000 Vantage SVC Daughterboard. The SVC interface carries high speed digital signals, and so the SVC source card should be as close to the Panther as possible in the VME rack.

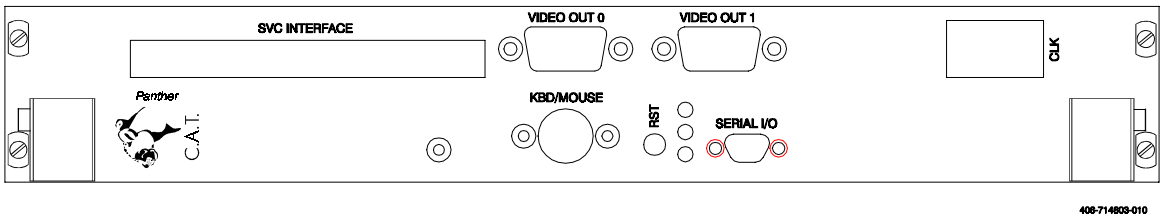


Figure 2.1 Front Panel

2.3 I/O Connectors

The Panther Dual Display board I/O connectors are shown in Figure 2.2.

P1 and P2, the VME backplane connectors are only used by the Panther to obtain power (+5V). VME daisy chain signals e.g. BUSGRANT0, are linked through by the Panther. See **Appendix C** for the full list of P1 and P2 connections.

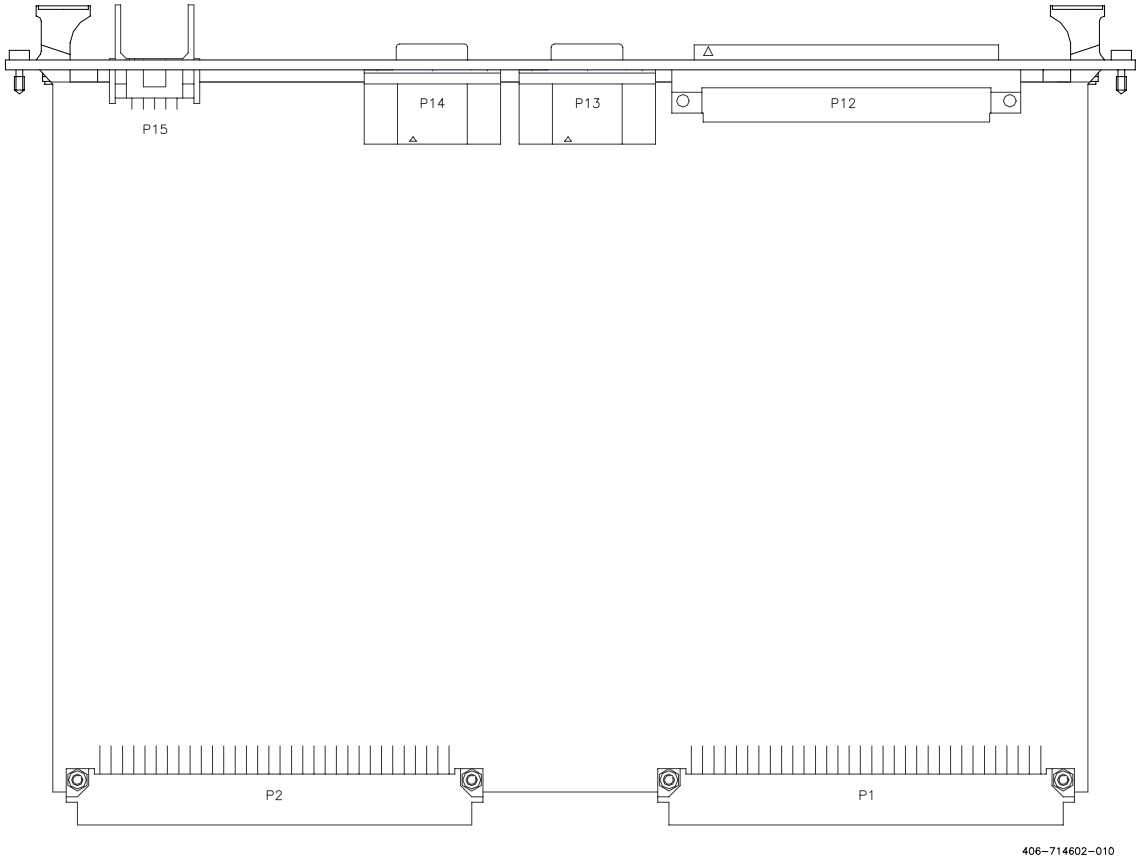


Figure 2.2 Panther Card Connectors

P9 and P10 on the back of the board are the Display Board Interface connectors to the C.A.T. Processor. Via this interface the C.A.T. initialises the Panther, accesses its frame stores and provides the video timing signals.
P13 and P14 are the two video output connectors. The two hi density 15 way D-Types each carry separately generated analogue Red, Green and Blue video and TTL horizontal and vertical sync. The pin out of these connectors is given in **Appendix C**, it conforms to the industry standard VGA style video connector pin out.

P12 is the 100 way SVC input. This is an 8 bit digital video input, and the incoming data may be mixed with the on board generated video. **WARNING** - when connecting a Panther to a Vantage Scan Converter ALWAYS check that the Vantage is fitted with the correct interface daughterboard. The Vantage should be fitted with a 895000 Vantage SVC Daughterboard. **Do Not** connect the Panther to a 841000 Vantage Buffer Daughterboard.

P15 is the clock/sync connector for connecting the Panther to a Video Keyer. When a Keyer is connected the Panthers pixel clock is supplied by the Keyer.

P11 is the in circuit programming connector for the FPGAs.

2.4 EERAM Settings

The Panther=s display format and video timings are all set by software. To allow the C.A.T. + Panther combination to initialise itself, the C.A.T.=s EERAM has a section devoted to storing the parameters required to define the display format.

NOTE: as both video outputs of the Panther are completely synchronised, and are driven by the same video timing signals, only ONE set of video timing parameters is required.

The EERAM parameters that define the Panther display format are listed in **Appendix B**. The standard C.A.T. firmware contains a menu driven programme to edit these parameters, the menus also include a number of predefined formats. The human interface to this programme is a Terminal (or a PC with terminal emulation S/W) connected to the C.A.T. RS-232 serial line channel A.

When the C.A.T. is fitted with the standard firmware, the EERAM can be edited as follows:

1. Fit the EERAM Write Enable >B= link to LK1 - D2.
2. Connect a Terminal (or PC with Terminal Emulation S/W) via an RS-232 cable to the front panel micro D-Type (channel A).
3. Configure the Terminal/PC for 9600 Baud, 7 bits, no parity, 1 stop bit.
4. Power-up the C.A.T. and follow the on-screen menus to edit the various Display Board parameters. (typing **? rtn** will display the current menu).
5. Power-down the C.A.T. and remove the EERAM Write enable link.

For a full description of this process, and listings of all the menu options see the **C.A.T. Monitor and Support Utilities User Guide** (Document Number 494-538000).

2.5 Panther and C.A.T. Assembly

A Panther Dual Display Board can only be fitted to a C.A.T. that has a suitable front panel. It must be a two slot module and have the correct cut outs for the SVC INTERFACE connector and the two VIDEO O/P D-Types. The front panel illustrated in Figure 2.1 is a typical example.

Additionally two transition board assemblies (Primagraphics part number 723000) will be required to interconnect the C.A.T. and Panther.

Note: The following procedures should only be performed in an ESD protected environment, electrostatic handling precautions should always observed when handling either board.

2.5.1 To Assemble a Panther and C.A.T.

Firstly attach the front panel to the C.A.T. in the normal manner, noting that there is an additional front panel fixing in the middle of the front panel.

Secondly fit any daughterboard that is required to the C.A.T. The daughter board is mounted on four 10 mm, tapped, nylon pillars - all four pillars should be screwed onto the C.A.T. before the daughterboard is fitted. Use 6 mm long M2.5 screws. Fit the daughter board and secure it with two screws - those nearest to the front panel, do not fit screws to the rear mounting pillars (adjacent to P2) at this stage.

Screw the Panther mounting pillars to C.A.T. The C.A.T. and Panther are fixed together with 18 mm, tapped, brass pillars - five are used if there is no daughterboard on the C.A.T., otherwise three are used. The pillars are screwed onto the C.A.T. with 6 mm long M2.5 screws. The locations are either side of P1 and P2, and in the middle of the card adjacent to the front panel.

Fit the transition board assemblies to the C.A.T. The 723000 transition boards plug into P9 and P10 of the C.A.T. The transition boards must be fitted in the correct orientation, they are labelled >CAT= on one edge and >Display= on the other edge. The edge labelled >CAT= must go nearest to the C.A.T. processor board.

Panther mounting brackets. The Panther is attached to the front panel by two right angle brackets, one at each front corner. Screw these onto the Panther using 6 mm long M2.5 screws and M2.5 nuts before attaching the Panther to the C.A.T.

Keyboard/Mouse connector. If the 8 way mini DIN keyboard/mouse connector is to be fitted to the front panel, do it now before fitting the Panther.

Fit the Panther. Slide the Panther front panel connectors through the appropriate cut-outs in the front panel, and then ease the Panther down onto the transition boards. Adjust the position of the transition boards to align them with the Panther connectors and then push the Panther home.

Fit fixing screws. Screw the Panther down onto the steel mounting pillars with 6 mm long M2.5 screws. If a daughterboard is fitted, two 7 mm nylon spacers must be fitted between the daughterboard and the Panther. These are fitted directly above the daughterboard rear mounting pillars and held in place by two 12 mm long M2.5 screws that go through the Panther, through the spacers, through the daughterboard and into the tapped nylon mounting pillars under the daughterboard.

Front panel fixings. Screw the two Panther corner brackets to the front panel with 6 mm long M2.5 countersunk screws. Fit the screw locks to the two D-Types.

2.5.2 **To Separate a Panther and C.A.T.**

Firstly disconnect the Panther from the front panel by removing the four screw locks and two corner bracket screws.

Secondly remove the five M2.5 screws that hold the Panther on to its mounting pillars.

Finally separate the C.A.T. and Panther by lifting back edge of the Panther up off the transition connectors. The inter-board connectors do not have a high insertion force, it should be possible to separate the two cards with only minimal finger pressure.

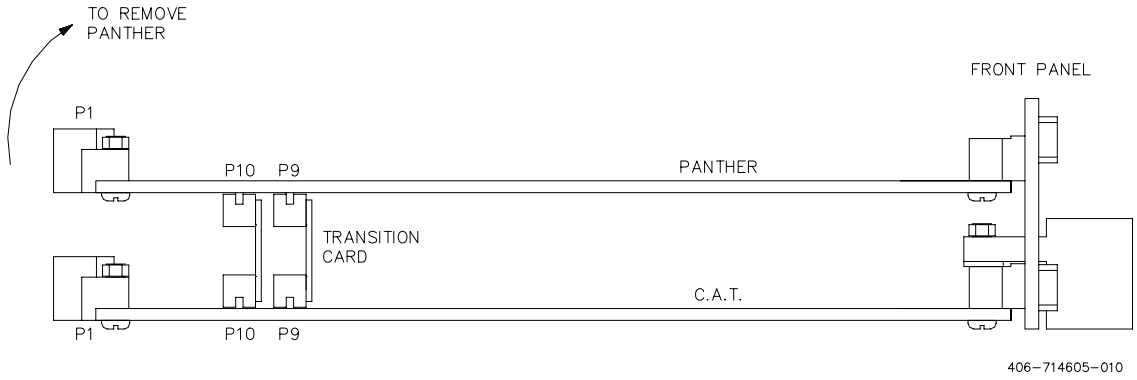


Figure 2.3 Panther and C.A.T. Assembly

3. Specification

3.1 Functional

3.1.1 Display Formats

Display Formats are programmable with:

Pixel Clock Speed

100 MHz to 200 MHz (Board versions 714000, 714003)
10 MHz to 135 MHz (Board versions 714002)

Horizontal Timing

Visible Pixels per line: programmable in increments of 8 pixels.
Horizontal Blanking width: programmable in increments of 8 pixels.
Horizontal Sync width: programmable in increments of 8 pixels.

Vertical Timing

Visible lines per frame: programmable in increments of 1 line.
Vertical Blanking width: programmable in increments of 1 line.
Vertical Sync width: programmable in increments of 1 line.

Interlaced/Non-Interlaced

Programmable.

3.1.2 SVC Input

The SVC input allows digital video from an external source, such as the Primagraphics Vantage Radar Scan Converter, to be mixed with the onboard video. The external video can be displayed on either screen, but this does limit the permissible pixel clock speed.

SVC data on screen 0

Maximum pixel clock speed 160 MHz

SVC data on screen 1

Maximum pixel clock speed 108 MHz

3.1.3 Video Outputs

Video

Red, Blue	0 - 0.7V +/- 5% into 75R.
Green (no sync)	0 - 0.7V +/- 5% into 75R.
Green (composite sync)	0 - 1.0V +/- 5% into 75R.

Video polarity	Positive White.
Sync polarity	Negative going.

Sync

VSYNC	TTL, negative going (i.e. active low).
HCSYNC	TTL, negative going (i.e. active low).

HCSYNC is programmable as horizontal or composite sync.
Sync outputs are TTL levels, but are rated to drive 75R Terminators.

3.1.4 Frame store Access

The six onboard Frame stores are each 2 MBytes, and are configured for 8 bits per pixel. The C80 processor on the C.A.T. may access the frame stores as follows:

Burst Write
200 MBytes per second.

Burst Read
133 MBytes per second.

The Frame stores also support the >Block Write= capabilities of the VRAMs fitted:

Block Write:
800 MBytes per second

3.2 **Mechanical** (Panther only)

Board dimensions	:	233 mm x 160 mm (Double Eurocard, single slot)
VME Connectors	:	2 x DIN41612 96 Way
C.A.T. Connectors	:	2 x 80 Way
Card Front	:	Two 15 Way high density D-Type Socket (Video O/Ps). 100 Way (SVC I/P).
Weight	:	320 grammes.

3.3 **Mechanical** (Panther and C.A.T.)

Module dimensions	:	233mm x 160mm x 40mm
	:	Double Eurocard, Two Slot Module.
VME Connectors	:	4 x DIN41612 96 Way
Card Front	:	Two 15 Way high density D-Type Socket (Video O/Ps).
	:	100 Way (SVC I/P).
	:	9 Way Micro D-Type (SERIAL I/O).
	:	8 Way mini DIN (KBD/MOUSE).
Weight	:	800 grammes.

Note: A C.A.T. + Panther module has room for only *one* application daughterboard to be mounted on the C.A.T. in the standard configuration.

3.4 **Power**

The following defines the power drawn by the Panther *only*, it does not include the C.A.T.

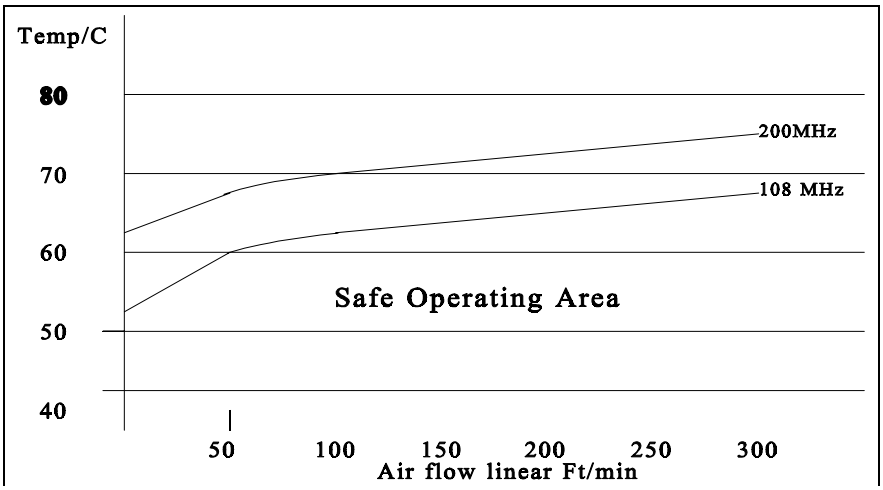
SUPPLY	TOLERANCE	CURRENT TYP	CURRENT MAX
+5V	± 5%	5 A	12 A

Note: The typical current consumption above was measured with a typical screen display, and a pixel clock of 200MHz. Lower pixel clock speeds will reduce the current consumption. The maximum current consumption figure was measured with a 200MHz pixel clock, and with the worst case 4 pixels at 0x00, 4 pixels at 0xFF vertical stripes test pattern in all six frame stores.

3.5 **Environmental**

Storage only	:	Ambient temperature -40EC to +75EC
Storage and operating :		Humidity 5% to 95%, non-condensing
Operating	:	Ambient temperature 0EC to +55EC
Maximum shock	:	30G Peak, 11ms duration.

Normally the Panther would be expected to operate with a small amount of forced air cooling. The only components on the Panther that require special consideration are the video DACs. See the graph below.



The video DAC power dissipation is dependent upon the pixel clock speed of the display format chosen, operation at the higher pixel clock speeds will always require forced air cooling.

4. Principles of Operation

The block diagram Figure 4.1 shows a Panther Dual Display card and C.A.T. Processor card. The Panther has two identical video subsystems for each output. Each subsystem contains the following circuit blocks:

- Three Frame stores: Overlay, Middle, Underlay
- The FPGA Multiplexers
- The Colour Look Up Tables (CLUTs)
- The Video DAC

The two subsystems are identical and share the same pixel clock and the same video timing signals from the C80. The frame stores, CLUTs and Video DAC of each subsystem are separately mapped into the C80 address space, see **Appendix A - Memory Map**. However, the facility of writing to both subsystems simultaneously has also been provided to speed initialisation.

The frame stores are all identical, but are named as Overlay, Middle and Underlay for convenience. Each is mapped to a separate base address in the C80 memory map. The frame stores are fixed by the design of the card as 8 bits per pixel. The frame stores have a full 64 bit interface to the C80 data bus. Burst write transfers from the C80 internal RAM to the frame store Video RAM are at 200 MBytes/sec. The frame store memory supports block write (from a colour register within the Video RAMs).

The four video sources, Overlay, Middle, Underlay and SVC are combined in the FPGA Multiplexers to produce an index (address) into the Colour Look Up Table. The CLUTs store a 24 bit R.G.B. value for each index. This R.G.B. value is clocked into the DAC and output as analog video. Within the DAC a hardware generated cursor is superimposed on top of the video.

The only circuitry on the Panther that is common to both video subsystems is the pixel clock generator and the SVC interface. The Pixel clock is an ECL programmable clock generator that may be programmed to generate almost any frequency in the range 10 MHz to 200 MHz. The ECL pixel clock is fed to both video DACs, but the other video circuitry is driven by a quarter speed TTL clock. To maintain the data rate, four pixels are clocked out of the frame stores on each of the TTL clock edges. The FPGA multiplexer and CLUT circuitry is all duplicated four times (for each channel), so that four pixels may be processed at a time, and four pixels are clocked into each DAC on each TTL clock rising edge.

The C80 Video Controller generates the basic video timing signals - HSYNC, VSYNC, HBLANK, VBLANK, from a divided down version of the pixel clock. The C80 video controller also generates the Video RAM DRAM -> SAM transfers that keep the display refreshed.

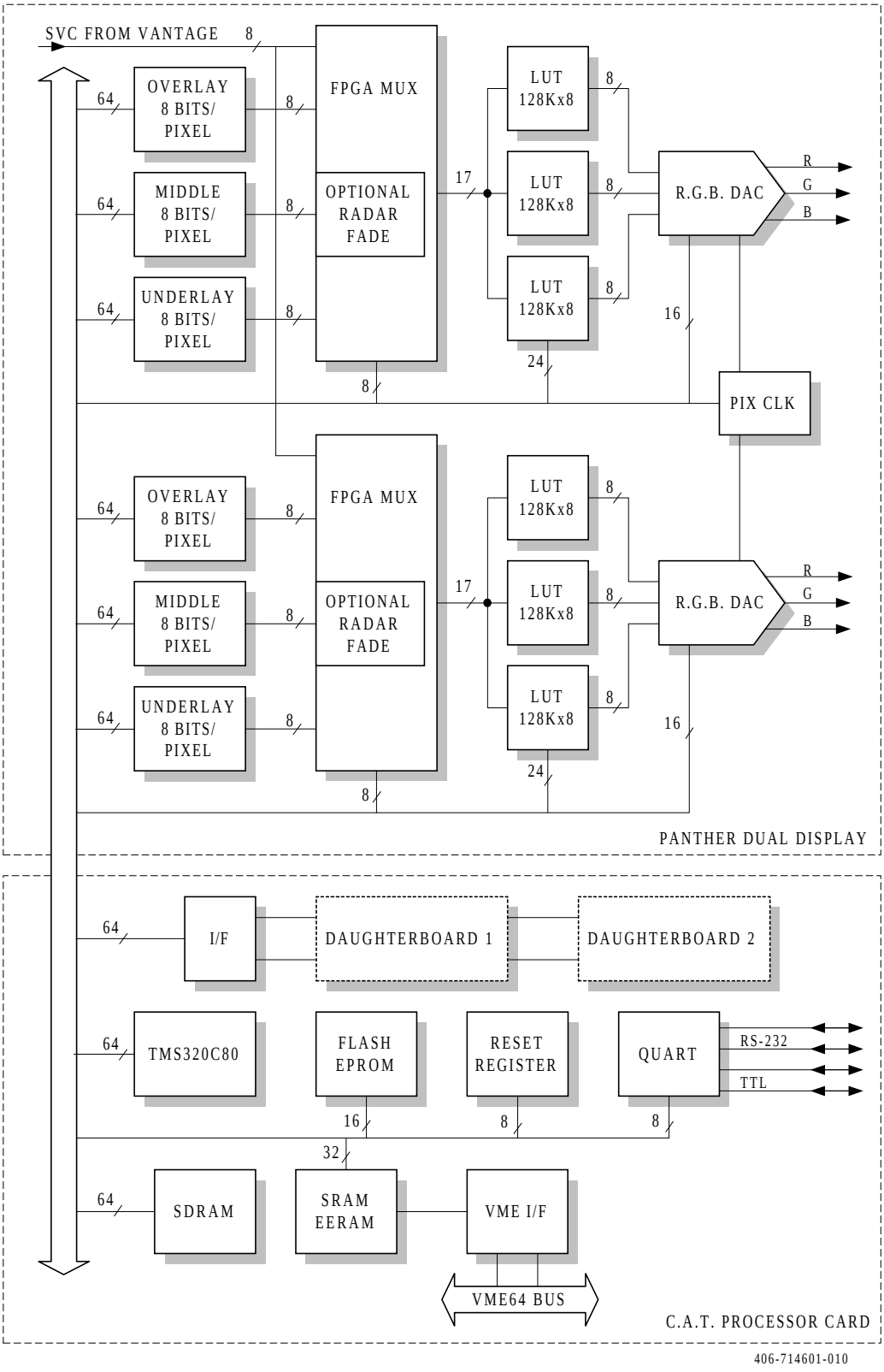


Figure 4.1 C.A.T. With Panther Dual Display Card

The Panther's video output may be >Genlocked< to an external video source using the Primagraphics Vortex video Keyer. In this mode an ECL pixel clock is fed from the Vortex to the Panther in place of the on-board pixel clock generator.

4.1 Frame stores

The frame stores are each composed of 2 MBytes of Video RAM. The memory is 64 bits wide, and has individual byte write enables to allow single bytes of data to be written. The memory supports block write. The frame stores are fixed at eight bits per pixel.

The frame stores each have separate base addresses in memory, but the C80 Video Controller can only be programmed to generate DRAM -> SAM transfers for one address. To overcome this, the Panther hardware activates all six frame stores when the C80 generates a DRAM -> SAM transfer cycle.

Different manufacturers Video RAMs have different block write capabilities, some do not support the block write feature, others write four pixels per cycle, others write eight pixels per cycle. To handle these options there is a register on the C.A.T. main board that must be programmed to match the capabilities of the RAMs on the Panther (see Section **5.6 Block Writes**).

4.2 Pixel Clock Generation

The on board programmable pixel clock generator is an ICS1562A-201. This single chip device uses a high speed Voltage Controlled Oscillator (VCO), an external reference crystal, and a number of programmable digital dividers to produce the required pixel clock frequency.

The final pixel clock frequency is only fed to the two Video DACs, the other board hardware is supplied with a TTL clock running at a quarter of the pixel clock speed. (The quarter speed clock is generated by one of the Video DACs).

A block diagram of the pixel clock generator is shown in Figure 4.2. By programming different values into the reference and feedback dividers a wide range of different pixel clock speeds may be selected. The VCO is optimised for operation from 40 MHz to 260 MHz thus an output divider is included so that lower frequencies may be generated.

The operational range of the pixel clock generator is 10 MHz to 260 MHz however these extremes may lie outside the operational range of the Panther, see section **3.1.1.**

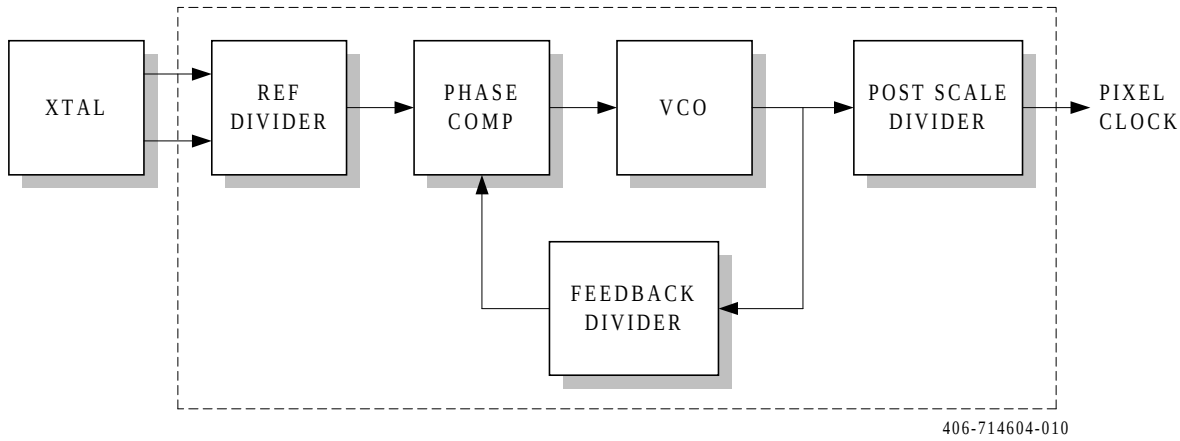


Figure 4.2 Pixel Clock Generator

The PLL reference frequency is derived from a crystal external to the chip. This is normally expected to be 16 MHz, but could be changed on a particular board if an unusual pixel clock frequency needed to be generated.

The Pixel Clock frequency is equal to

$$\text{Pixel Clock} = \frac{\text{VCO}}{\text{Post Scale Divider}}$$

The VCO frequency is given by:

$$\text{VCO} = \text{PLL}_{\text{REF}} \; H \; \frac{\text{Feedback Divider}}{\text{Reference Divider}}$$

The VCO has an operational range of 40 MHz to 260MHz.

The dividers may be set to:

Post Scale Divider:	1 or 2 or 4
Reference Divider:	1 to 128 (steps of 1)
Feedback Divider:	37 to 448 (steps of 1)

4.3 Serial Clock Generation

In addition to the FPGA Multiplexers, each video subsystem has an extra FPGA that generates the serial clocks for the VRAMs and which passes the sync and blanking signals to the DAC. By introducing differing pipeline delays into the various SCLK and DAC signals these FPGAs ensure that the video sources are aligned on the display.

The serial clock generator FPGA for output 0 also generates the HBLANK, VBLANK and clock signals for the SVC interface.

4.4 FPGA Multiplexers

The FPGA Multiplexers combine the four 8 bit video sources to produce an index into the CLUT, where the index value is mapped into 24 bit R.G.B. The way the four sources are combined is set in the FPGA Multiplexers code, and this may vary from application to application. Different versions of the FPGA Multiplexers will use the CLUT=s differently - thus the S/W that uses the Panther must know which version of FPGA code has been programmed into the board. The FPGAs have a read back register to allow this to be determined.

The video data on the Panther is interleaved four way, i.e. four pixels are clocked out of memory on each clock edge. Thus there are in fact four FPGA Multiplexers, all identical, working on four different pixels at a time.

The FPGAs contain registers that may be written to by the C80. The data path to the FPGA=s is 8 bits. The number of registers within an FPGA, and their purpose, depends on the application and the FPGA code. The registers in the FPGA Multiplexer share the same read and write line as the registers in the serial clock generator FPGA, and form a continuous block of registers.

4.5 CLUTs

The CLUTs appear to the C80 memory map as a series of 24 bit words on 32 bit intervals. Each 24 bit word defines 8 bits of Red, Green and Blue. The CLUTS have individual byte write enables, so a Red value may be written without affecting the Green or Blue values. The CLUTs are not dual ported, thus when the C80 reads or writes from the CLUTs the video data to the DAC is interrupted. To avoid screen disturbance, application software should synchronise CLUT accesses to the vertical blanking period.

The C80 read/write address to the CLUT is routed via the FPGA Multiplexers. On the faster Panther cards (pixel clocks 100 to 200 MHz) the address is registered by the pixel clock. On these boards it is necessary for the pixel clock to be operating before the CLUTs can be loaded. On slower versions of the card (pixel clocks 10 to 135 MHz) the address is transferred asynchronously and is independent of the pixel clock.

Like the FPGA Multiplexers, the CLUTs are interleaved four ways, however this is hidden from the C80 which only sees a single CLUT within its address map. This is arranged by writing to all four banks of CLUTs simultaneously during write operations, and by only reading one of the banks during a read. A register within the SCLK FPGA selects which of the four banks is to be read by the C80, thus allowing the CLUTs to be fully tested.

The CLUTs for each output are implemented separately and each may be accessed independently of the other, however to speed initialisation, both CLUTs have also been mapped to a third common address to allow both CLUTs to be written to simultaneously.

The CLUTs for each output have a depth of 128k locations (512k bytes):

Output 0

Index	C80 Address	Address+0	Address+1	Address+2	Address+3
0x00000	0x1000 0000	N/C	Blue	Green	Red
0x00001	0x1000 0004	N/C	Blue	Green	Red
0x1FFFE	0x1007 FFF8	N/C	Blue	Green	Red
0x1FFFF	0x1007 FFFC	N/C	Blue	Green	Red

Output 1

Index	C80 Address	Address+0	Address+1	Address+2	Address+3
0x00000	0x1040 0000	N/C	Blue	Green	Red
0x00001	0x1040 0004	N/C	Blue	Green	Red
0x1FFFE	0x1047 FFF8	N/C	Blue	Green	Red
0x1FFFF	0x1047 FFFC	N/C	Blue	Green	Red

Both Outputs

Index	C80 Address	Address+0	Address+1	Address+2	Address+3
0x00000	0x1080 0000	N/C	Blue	Green	Red
0x00001	0x1080 0004	N/C	Blue	Green	Red
0x1FFFE	0x1087 FFF8	N/C	Blue	Green	Red
0x1FFFF	0x1087 FFFC	N/C	Blue	Green	Red

4.6 Video DAC

The Video DACs on the Panther are Analog Devices ADV7162s. In addition to converting the 24 bit R.G.B. output of the CLUT to analogue, each video DAC contains a hardware cursor and the gamma correction LUTs. Additionally a register within each DAC can be programmed to enable sync on to the Green video output, and other registers allow signature analysis of the digital video data going into the DACs.

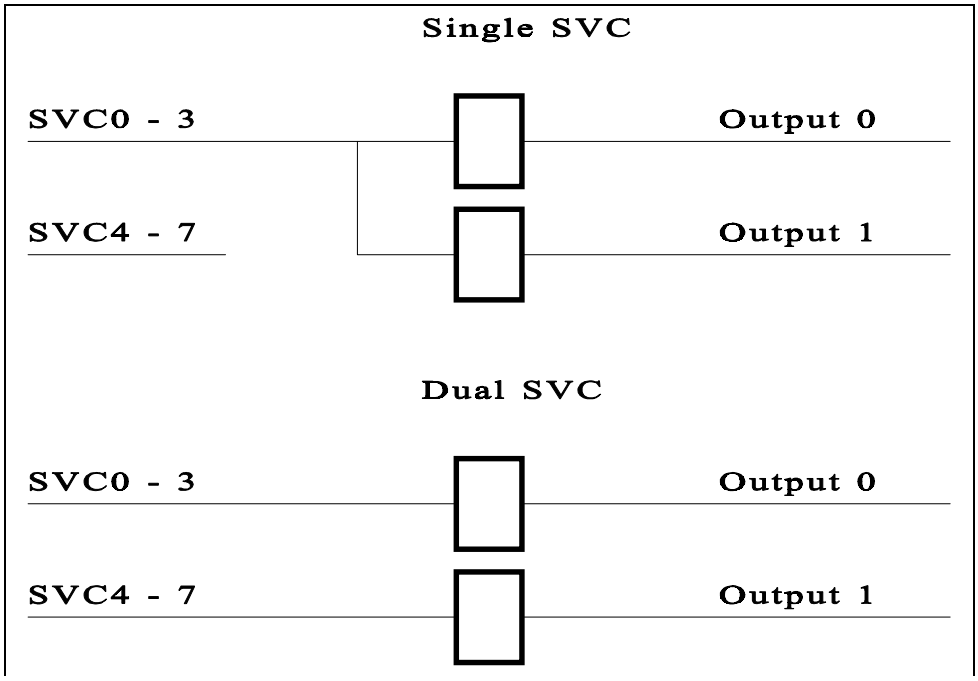
The ADV7162 has a built in pixel clock generator, but this should NOT be used on the Panther. Instead both DACs should be programmed to use the external pixel clock source, on the Panther this is provided by the ICS1562 chip.

The LUTs within the video DACs will only be used to Gamma Correct the Red, Green and Blue video data. The three LUTs (Red, Green, Blue) are each 256 locations by 10 bits. The LUTs are not mapped into C80 memory space but are instead accessed using a pointer register and a data register.

The hardware generated cursor consists of a 64x64 pixel, 2 bits per pixel block that may be moved around the screen by writing to X and Y position registers. The 64x64x2 cursor RAM is not mapped into C80 memory space but is instead accessed using a pointer register and a data register. There is a separate colour LUT within the DAC that defines the cursor colours.

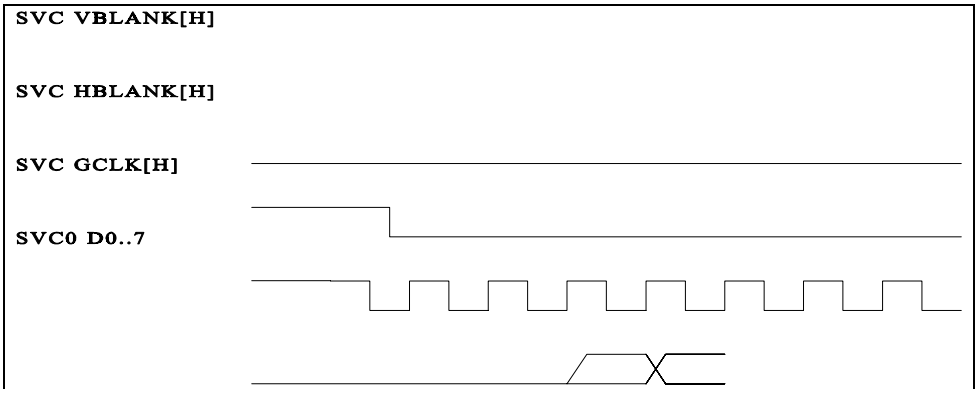
4.7 SVC Interface

The SVC interface allows 8 bit pixel data from an external frame store to be fed into the FPGA Multiplexers and thus mixed and combined with the on-board video sources. With a single SVC source, the data is fed to both Output 0 and Output 1, thus the SVC data may be displayed on either screen. Where a dual SVC source is available, the standard SVC data is routed to Output 0, the extended data to Output 1. Like the on-board sources the SVC data is interleaved by four, i.e. four pixels are input on each clock edge.



The interface consists of three control signals, generated by the Panther, and 32 data lines from each SVC source. The SVC source is an 8 bit frame store similar to those on the Panther. The control signals from the Panther are used to clock data out of this frame store in step with the data being clocked out of the Panthers own frame stores.

The control signals are a clock, horizontal blanking and vertical blanking. The clock is gated and only runs during the visible period. The interface does not support interlaced video. The control signals are generated by the SCLK FPGA for output 0.



5. Software Specification

The software driving the Panther will need to:

Initialise the:
- Pixel clock generator
- C80 Video Controller Registers
- FPGA registers
- Video DAC Command Registers
- Video DAC Gamma Correction table (optional)
- Set the type of Block Write required

Load and update the:
- Colour LUTs
- Cursor
- FPGA registers

The initialisation phase will be the same for all Panthers but the values loaded into various registers will depend on the selected display format and video timing, normally these will be defined by parameters stored in EERAM.

Loading the CLUTs and FPGA registers will depend on the application and version of FPGA Multiplexer code. The version of FPGA code on a board can be determined by reading the FPGA board identity registers, see section **5.3.1 Fixed Registers**.

The hardware cursor and gamma correction tables are all built into the Video DAC and share a common interface, for this reason they are described together in section **5.1 ADV7162**.

How to program the C.A.T. *Reset Register* is described in section **5.6 Block Write**s.

5.1 ADV7162

Information on programming the ADV7162 can be found in the Analog Devices data sheet for the ADV7160/7162 Rev 0 1995.

5.1.1 Video DAC Modes

On the Panther the DACs are always operated in 24 bit input R.G.B. mode. The three internal 256x10 LUTs may be used as gamma correction tables, or these can be bypassed to connect the 24 bit input directly to the DACs.

The selection of 24 bit True Colour or 24 bit Bypass Mode is controlled by CR24..CR27 in *Command Register 2*. This register also contains the bit (CR22) that enables Sync onto the Green video output, and the bit (CR23) that enables the pedestal offset onto the three video outputs.

If 24 bit True Colour is selected then it is necessary to load the LUTs inside the ADV7162 with a Gamma Correction Curve. The LUTs are not mapped into the C80 address space, but are instead accessed by a pointer register and data register. After the pointer has been loaded, three successive writes to the data register will write to the Red LUT, the Green LUT and finally to the Blue LUT. The LUT values are 10 bits wide, but the C80 must write each individual entry as a 16 bit quantity to ensure that the pointer is correctly incremented.

5.1.2 **Cursor Generator**

Each of the cursors is loaded and controlled using the following registers:

Cursor Control Register	Enables cursor, selects cursor style, sets interlaced mode.
Cursor X-Lo, X-Hi	These two registers set the X location of the cursor.
Cursor Y-Lo, Y-Hi	These two registers set the Y location of the cursor.
Cursor Colour 1,2	Two registers, each defines one of the cursor colours.

The 64x64 cursor image is loaded into RAM within the ADV7162 using an address pointer register and an 8 bit data register.

The position registers are loaded with 12 bit signed values (2's complement) to define the position of the cursor with respect to the top left hand corner of the display.

The colour registers are each 10 bits wide, and need to be written to three times, in sequence to define Red, Green, Blue.

Two different styles of cursor are supported,

Cursor Bit 1	Cursor Bit 0	X-11 Style Cursor	XGA Style Cursor
0	0	Transparent	Colour 1
0	1	Transparent	Colour 2
1	0	Colour 1	Transparent
1	1	Colour 2	Bit-Wise Complement

5.1.3 **Interface and Registers**

On the Panther the read/write interface of the ADV7162 is set to 10 bits wide operation. The C80 must always access the ADV7162 as 16 bit words due to the self incrementing address pointer. Each ADV7162 appears to the C80 as four locations.

Video DAC interface registers

C80 Address	ADV7162 Register
0x1200 0000	Address Register, output 0
0x1200 0002	Colour Palette, output 0
0x1200 0004	Control Registers, output 0
0x1200 0006	Mode Register, output 0
0x1240 0000	Address Register, output 1
0x1240 0002	Colour Palette, output 1
0x1240 0004	Control Registers, output 1
0x1240 0006	Mode Register, output 1

The Mode Register is an 8 bit register that may be written to or read at any time, it is independent of the Address Register. The Mode Register controls the width of the R/W data path and the resolution of the digital to analogue convertors - on the Panther these should both be set to 10 bits. Additionally two of the Mode Register bits must be toggled at power-up to fully reset the DAC, thus the Mode Register should be:

Set to 0x07
then to 0x26
then to 0x07

The Address Register is loaded to point to a particular control register or palette location which may then be read or written to. The address pointer within the ADV7162 is in fact 11 bits, thus two writes to the Address Register are required to set the pointer. The first write sets the least significant byte of the pointer, the second sets the 3 most significant bits.

When loading the palette with Gamma Correction values, the address pointer is set to 0, and then the 10 bit palette values are written into the Colour Palette register in Red, Green, Blue sequence. After three writes (or reads) to the Colour Palette register the address pointer is automatically incremented, so it is possible to fully load the palette without reloading the Address Register.

The Control Register is used to access the five Command Registers, the Test registers, the cursor control registers and the cursor image RAM. Each register has a unique address within the DAC (see below), that is selected using the Address Register.

ADV7162 internal registers

Address Pointer	Control Register	Usage/Default Value
0x000 to 0x002	Test Registers	Test only
0x003	ID register (read only)	0x79
0x004	Pixel Mask	0xFF
0x005	Command Register 1	0xB9
0x006	Command Register 2	see below
0x007	Command Register 3	0xC3
0x008	Command Register 4	0x88
0x009	PLL Command Register	0
0x00A	Status Register (read only)	
0x00B	Revision Register (read only)	
0x00C	PLL R Register	0
0x00D	Command Register 5	0
0x00E	Test Register	Test only
0x00F	PLL V Register	0
0x010 to 0x013	Signature Registers	Test only
0x014 to 0x015	Test Registers	Test only
0x016 to 0x1FF	Reserved	
0x200	Cursor X position Low Byte	
0x201	Cursor X position High Byte	
0x202	Cursor Y position Low Byte	
0x203	Cursor Y position High Byte	
0x204	Cursor Control Register	See below
0x205 to 0x302	Reserved	
0x303	Cursor Colour 2	
0x304	Cursor Colour 1	
0x305 to 0x3FF	Reserved	
0x400 to 0x7FF	Cursor Image RAM	

Command Register 2

CR27	CR26	CR25	CR24	CR23	CR22	CR21	CR20
1	1	1	1/0	1/0	1/0	0	0

CR27...CR24 Set to 0xE for 24 bit True colour (i.e. using palette)
Set to 0xF for 24 bit Bypass Mode.

CR23 Set to 1 for 7.5IRE pedestal on video.
Set to 0 for no pedestal.

CR22 Set to 1 for Sync on green.
Set to 0 for no Sync on green.

CR21...20 Always write 0.

Cursor Control Register

CCR7	CCR6	CCR5	CCR4	CCR3	CCR2	CCR1	CCR0
0	0	0	0	1/0	1/0	1/0	1/0

CCR7...4 Always write 0.

CCR3 Set to 1 for interlaced displays.
Set to 0 for non-interlaced displays.

CCR2 Set to 1 to enable cursor.
Set to 0 to disable cursor.

CCR1...CCR0 Sets the cursor style:
0, 0 Reserved.
0, 1 X11 Cursor
1, 0 XGA cursor
1, 1 Reserved.

5.2 C80 Video Controller

The Display Board interface connects to Video Controller 0 within the C80. The sync and blanking signals between the C80 and the Display Board are bi-directional, normally they will be driven by the C80, but when a Vortex Keyer is attached the Vertical sync on the C80 will be an input. The Panther uses the four timing signals from the C80 differently in different modes:

C80 Timing Signal	Non-Interlaced usage	Interlaced usage
CSYNC/HBLNK	HBLANK	CSYNC
CBLNK/VBLNK	VBLANK	CBLANK
HSYNC	HSYNC	n/c
VSYNC	VSYNC	n/c

The Video Controller timing circuits are driven by a clock that is derived from the pixel clock on the display board. This clock is referred to as FCLK in the C80 documentation, and on the Panther it runs at one eighth of the pixel clock frequency.

To allow the Video Controller to generate mid line reloads for the Video RAMS, a second clock is fed from the display board to the C80. This is referred to as the SCLK, and is a copy of one of the serial clocks that drive the Video RAMS serial output.

5.2.1 Frame Timing Registers

The Frame Timing registers control the generation of the four sync and blanking signals from the FCLK generated by the Display Board. Thus they are programmed with the horizontal and vertical timing parameters, the required sync mode and whether the display is to be interlaced or non-interlaced.

Frame Timer registers

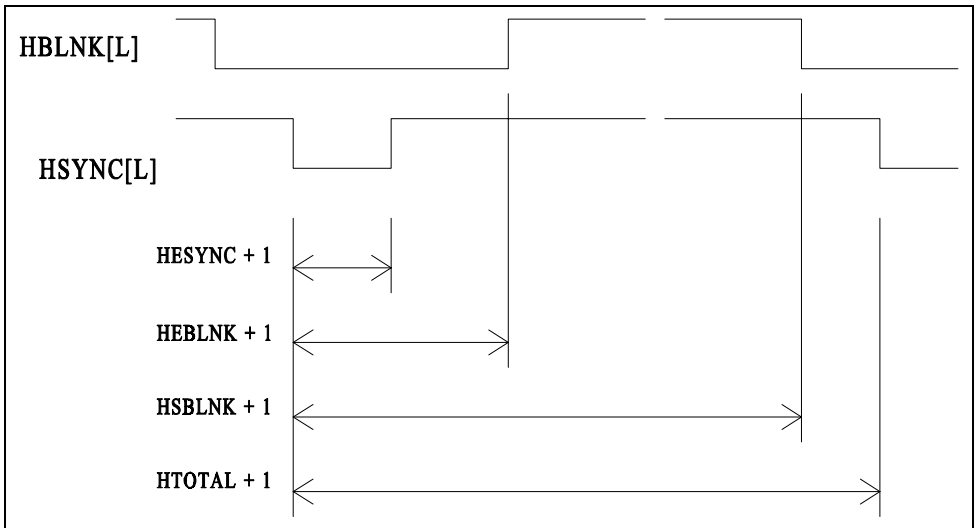
Addr	Reg	Use	Addr	Reg	Use
0x01820200	FTCTL0	see below			
0x01820204	SETHCT0	initialise horz counter	0x01820206	SETVCT0	initialise vert counter
0x01820208	HESERR0	serration pulse width	0x0182020A	VFINT0	vblank interrupt
0x0182020C	HESYNC0	Hsync pulse width	0x0182020E	VESYNC0	Vsync pulse width
0x01820210	HEBLNK0	Hsync + Back porch	0x01820212	VEBLNK0	Vsync + Back porch
0x01820214	HSAREA0	n/a	0x01820216	VSAREA0	n/a

Addr	Reg	Use	Addr	Reg	Use
0x01820218	HEAREA	n/a	0x0182021A	VEAREA	n/a
0x0182021C	HSBLNK0	defines front porch	0x0182021E	VSBLNK0	defines front porch
0x01820220	HTOTAL0	total pixels per line	0x01820222	VTOTAL0	total lines per field
0x01820224	HALINE0	see below			
0x01820228	HBLINE0	see below			

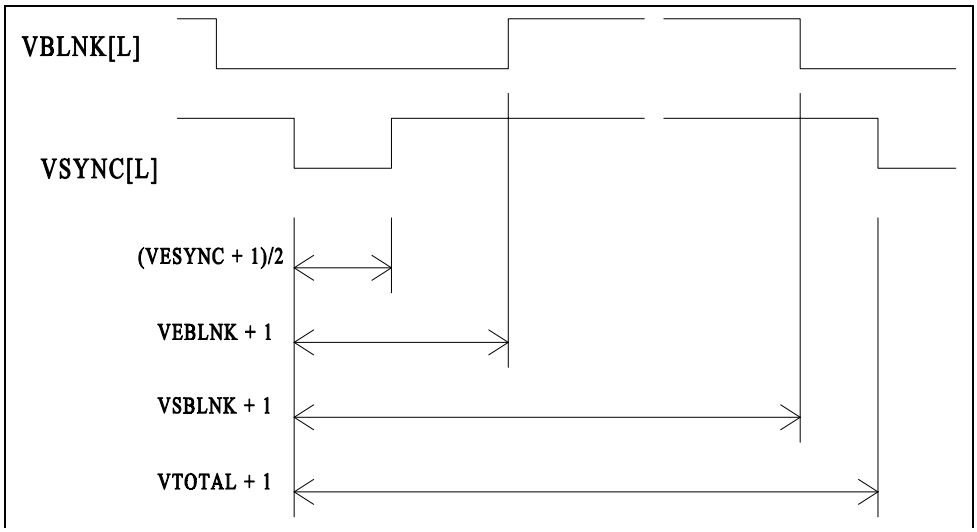
The horizontal timing is defined in units of 8 pixels. HESERR is used to define the serration pulse width for interlaced video it may be calculated as:

HESERR = (HTOTAL + 1)/2 - HESYNC

HALINE and HBLINE are used to define the point at which the Video Controller requests a DRAM -> SAM screen refresh cycle. For high line rate displays, this should be one clock after the start of blanking. For slower displays it should be set the same as HTOTAL to allow the video pipeline to empty.



The vertical timing is defined in lines for non-interlaced video, and in half lines for interlaced video.



The Frame Timer Control Register (FTCTL0) contains control bits that specify the function and direction of the video controllers sync and blank pins, that control synchronisation to external video sources and which enable interlaced operation:

FTCTL0

D15	D14	D13	D12 D11 D10	D9	D8 D7 D6	D5 D4	D3 D2	D1 D0
FTE	IFD	IIM		SSE		CPM	VPM	HPM

D1..0 HPM Sets HSYNC[L] pin mode: (0, 0) High Impedance
(0, 1) Input
(1, 0) Output

D3..2 VPM Sets VSYNC[L] pin mode: (0, 0) High Impedance
(0, 1) Input
(1, 0) Output

D5..4 CPM Sets CSYNC/HBLANK[L] and CBLNK/VBLNK[L] pin mode:

	CSYNC/HBLANK[L]	CBLNK/VBLNK[L]
(0, 0)	High Impedance	Composite blank output
(0, 1)	Composite sync input	Composite blank output
(1, 0)	Composite sync output	Composite blank output
(1, 1)	Horizontal sync output	Vertical blank output

D9 SSE Sets external synchronisation mode, normally set to 0.

D13	IIM	Sets Interlaced Interrupt Mode:	0 Interrupt once per frame. 1 Interrupt once per field.
D14	IFD	Disables interlaced operation:	0 Interlaced operation. 1 Non-interlaced operation.
D15	FTE	Enables Frame Timer:	0 Disabled. 1 Enabled.

For displays without external synchronisation (i.e. no Keyer):

Non-interlaced	FTCTL0 = 0xC03A
Interlaced	FTCTL0 = 0x802A

For full details of Video Controller programming, and examples of both interlaced and non-interlaced video timing see the **TMS320C80 (MVP) Video Controller User Guide** - Texas Instruments publication SPRU111A.

5.2.2 **Serial Register Transfer Controller Registers**

The SRT registers are concerned with generating the DRAM -> SAM transfers that keep the display data on the screen. The SRT control registers may be programmed to two different modes of operation. In the simplest mode of operation the SRT controller only generates DRAM -> SAM transfers at the start of each display line (in the horizontal blanking period). In the alternative mode of operation, split line transfers are generated whenever one half of the SAM is empty. This mode is more sophisticated, and more economical of bus bandwidth. Either mode may be used with the Panther.

When operating in the split transfer mode the SRT controller keeps track of the amount of data in the video RAMS SAM. To manage this the SRT is clocked by a copy of one of the serial clocks on the Display Card, however the SRT must also be programmed with the length of the SAM via the SAMMASK0 register.

SRT registers

Addr	Reg
0x01820300	FMEMCTL0
0x01820304	F0STADR0
0x01820308	F1STADR0
0x0182030C	LINEINC0
0x01820310	SAMMASK0
0x01820314	NEXTADR0
0x0182033C	CRNTADR0

These registers are set as follows:

FMEMCTL0 Set to 0x4021 for non-interlaced displays with 256 bit SAM VRAMs (Texas)
Set to 0x4020 for non-interlaced displays with 512 bit SAM VRAMs (OKI)
Set to 0x4001 for interlaced displays with 256 bit SAM VRAMs
Set to 0x4000 for interlaced displays with 512 bit SAM VRAMs

F0STADR0 Set to 0x0400 0000 for non-interlaced displays (top of VRAM memory)
Set to 0x0400 0000 + 2 (Display Pitch) for interlaced displays.

F1STADR0 Set to 0x0400 0000 for non-interlaced displays.
Set to 0x0400 0000 + LINEINC for interlaced displays.

LINEINC0 Set to the Drawing Pitch i.e. the number of pixels in RAM from one line to next.

SAMMASK0 Set to 0x03F8 for 256 bit SAM VRAMs (Texas)
Set to 0x03F0 for 512 bit SAM VRAMs (OKI)

NEXTADR0 Only used during initialisation, set to same as F0STADR0.

CRNTADR0 Only used during initialisation, set to same as F0STADR0.

For full details of Video Controller programming, and examples of both interlaced and non-interlaced video timing see the **TMS320C80 (MVP) Video Controller User Guide** - Texas Instruments publication SPRU111A.

5.3 FPGA Registers

The FPGA registers are located within different FPGAs on the Panther card. The registers within the SCLK FPGA will always have the same functions irrespective of the version of Video Multiplexer FPGA code. These are described in the section **Fixed Registers** below. The FPGA Multiplexer register functions may vary and are described in section **5.5** below.

5.3.1 Fixed Registers

None of the registers are read/write. Some are read only, some are write only.

Read Only

Addr	Reg	Usage
0x1100 0000	Board Id (hi)	0x07 Identifies Display Board as 714
0x1100 0004	Board Id (lo)	0x14
0x1100 0008	Board Version	0x00 Identifies board Version
0x1100 000C	FPGA Version	0x00 Identifies FPGAVersion.

Write Only

Addr	Reg	Usage
0x1100 0000	Sync Mode Register	Sets separate/composite/interlaced sync
0x1100 000C	CLUT Readback Register	Test use only
0x1100 0010	Clock Select Register	Selects between onboard and external pixel clock
0x1100 0014	Pixel Clock Register	Used to programme the ICS clock generator chip
0x1100 0018	SVC select Register	Selects normal or extended SVC for channel 1 output

Sync Mode Register

D7	D6	D5	D4	D3	D2	D1	D0
						Mode	

D1..0 Mode Sets sync/blank mode
(0, 0) Composite Sync, Non-interlaced
(0, 1) Separate Sync, Non-interlaced
(1, 0) Composite Sync, Interlaced
(1, 1) Reserved.

This register tells the SCLK FPGAs how to interpret the sync and blanking signals from the C80, and whether to generate composite sync, or separate horizontal and vertical sync.

CLUT Readback Register

D7	D6	D5	D4	D3	D2	D1	D0
				Output 1		Output 0	

D1..0 Output 0 CLUT Readback (0, 0) read bank A
(0, 1) read bank B
(1, 0) read bank C
(1, 1) read bank D

D3..2 Output 1 CLUT Readback (0, 0) read bank A
(0, 1) read bank B
(1, 0) read bank C
(1, 1) read bank D

This register is used when testing the CLUTs to ensure that all four banks are working.

Clock Select Register

D7	D6	D5	D4	D3	D2	D1	D0
							EXT

D0 EXT Pixel clock source 0 - On board clock generator
1 - External clock generator (Vortex Keyer)

This register selects between the on board pixel clock generator and an external clock source supplied via the Keyer connector (P14).

Pixel Clock Register

D7	D6	D5	D4	D3	D2	D1	D0
						Hold	Data

D0 Data Serial setup data to Pixel Clock Generator (ICS1562A-201)

D1 Hold Serial data control bit to ICS chip 0 - Load new data.
1 - Hold loaded data.

The ICS1562A-201 programmable pixel clock generator is serially programmed via these two bits, see section **5.4 Pixel Clock Generator**.

SVC Select Register

D7	D6	D5	D4	D3	D2	D1	D0
							N/E

D0 N/E SVC channel 1 select 0 - Normal.
1 - Extended.

5.4 Pixel Clock Generator

The ICS1562A-201 pixel clock generator is programmed by writing a 56 bit serial stream of data to the chip via the Panther *Pixel Clock Register*. On the first 55 writes to the chip the >Hold= bit is kept low, and the data is loaded into a shift register within the ICS chip without affecting its operation. On the 56th write the >Hold= bit is set high and this causes all 56 bits of data to be transferred from the shift register to the chips internal control registers.

Full programming details of the chip can be found in the ICS data sheet. The following lists the set-up for the chip relevant to the Panther.

Pixel Clock Generator setup

WRITE	DATA	SETUP
1..4	0xF	Set N1 divider to max (not used on Panther)
5..12	0	Sets various optional features to OFF
13..14	S0..S1	PLL post-scaler, set according to required pixel clock speed. (S1, S0) (0 , 0)) by 1 for pixel clocks over 100MHz (0 , 1)) by 2 for pixel clocks between 50MHz and 100MHz (1 , 0)) by 4 for pixel clocks below 50MHz
15..25	0	Sets optional features to OFF
25..27	V0..V2	VCO gain, set according to VCO frequency. (V2..V0) (1, 0, 0) for VCO frequencies up to 120MHz (1, 0, 1) for VCO frequencies up to 200MHz (1, 1, 0) for VCO frequencies up to 260MHz
28	0	
29..30	2	Phase detector gain.

WRITE	DATA	SETUP
31	0	
32	1	
33..38	M0..M5	M counter modulus register, see below
39, 40	0	
41..44	A0..A3	A counter register, see below
45	0	
46	1	
47, 48	0	
49..55	R0..R6	Reference divider register, see below
56	0	

The pixel clock frequency generated by the chip will be given by:

$$F_{PIXEL} = F_{REF} \times \frac{\text{Feedback Divider}}{\text{Post Scale} \times \text{Reference Divider}}$$

Where, F_{REF} = 16MHz
Post Scale = 1 or 2 or 4.
Reference Divider = 1 to 128.
Feedback Divider = 37 to 448.

The Feedback Divider value may be set to any value in the range 37 to 448. The value is set by programming the M counter register (M5..M0) and the A counter register (A3..A0). These two counters are combined into a single divider such that:

Feedback Divider = [(M + 1) H 6] + A For the case A … 0.
= [(M + 1) H 7] For the case A = 0.

Note: the M value must always be greater or equal to the A value, and must be greater than 0.

The Reference Divider value is equal to one plus the value entered into the reference divider register (R0..R6), e.g. if a Reference Divider value of 9 were required, the value 8 would be programmed into the register. When choosing a Reference Divider value, the aim should be to use as small a value as possible, preferably in the range 1 to 20.

The Post Scaler Divider (S1, S0) should be used to keep the VCO frequency as high as possible.

5.5 FPGA Multiplexer and CLUTs

The FPGA Multiplexers define the layering of the final display and the contents of the CLUTs, additionally the registers within the FPGA Multiplexers may vary from one application to another. Thus to drive a Panther card the S/W will need to recognise the version of FPGA code, and act appropriately. The FPGA version can be determined by reading one of the fixed FPGA registers, see section **5.3.1 Fixed Registers**.

5.5.1 Version 0 FPGA code

Here both outputs have the same functionality. It is intended for applications with Graphics superimposed upon Radar and Video windows.

The Radar data may be from a Vantage, via the SVC, or may be written directly into the Middle frame store by the C80. The Radar data may be displayed against a black background as 8 bit data, or it may be merged with the a background map in the underlay. Owing to space considerations within the CLUT, only one Radar+Underlay LUT is implemented which is common to both S/W scan converted radar and SVC radar. The Video layer is 16 bits, composed of 8 bits from the Middle frame store and 8 bits from the underlay.

The keying of the display layers is controlled by indices within the Overlay frame store:

Overlay Index	Display	Usage
0xFF	Overlay Colour 0xFF	Graphical Overlay
0xFE	Middle + Underlay (16 bit)	Colour Video
0xFD	SVC + Underlay (15 bit)	External radar on background map
0xFC	Faded Middle + Underlay (15 bit)	S/W scan converted radar on background map
0xFB	Underlay (8 bit)	Map only
0xFA	Middle (8 bit)	S/W scan converted radar only
0xF9	SVC (8 bit)	External radar only
0xF8	Overlay Colour 0xF8	Graphical Overlay
0xF7	Overlay Colour 0xF7	Graphical Overlay
0x01	Overlay Colour 0x01	Graphical Overlay
0x00	Overlay Colour 0x00	Graphical Overlay

The FPGA Multiplexers also have two write-only registers inside:

Addr	Reg	Usage
0x1100 0040	Fade Value, Output 0	This value is added to the Middle o/p for faded radar.
0x1100 0048	Layer Enable, Output 0	Turns on lower layers.
0x1100 0050	Fade Value, Output 1	This value is added to the Middle o/p for faded radar.
0x1100 0058	Layer Enable, Output 1	Turns on lower layers.

The Fade value is added to the 8 bit output of the Middle frame store for S/W scan conversion applications. The LSB of the 8 bit result is discarded and the resulting 7 bits are combined with the 8 bits of Underlay to index into the Radar+Underlay LUT.

The two Layer Enable registers each contains two bits. When both bits are 0, only the Overlay is displayed. When D0 is set the index 0xFE enables the 16 bit Middle+Underlay layer. When D1 is set indices 0xF9 to 0xFD are used to enable the video layers defined above.

The colour LUT is divided into six separate LUTs, one for each of the four individual 8 bit layers, one for the 16 bit (colour video) layer and one 15 bit table for radar+map. The radar+map LUT is used for both S/W scan converted and external radar.

CLUT indexing Output 0

C80 Addr	Index	FPGA Input Data	Function
0x1000 0000	0x00000	Middle = 0x00 Underlay = 0x00	Middle+Underlay 64k LUT
0x1000 0004	0x00001	Middle = 0x00 Underlay = 0x01	Middle+Underlay 64k LUT
0x1003 FFF8	0x0FFFE	Middle = 0xFF Underlay = 0xFE	Middle+Underlay 64k LUT
0x1003 FFFC	0x0FFFF	Middle = 0xFF Underlay = 0xFF	Middle+Underlay 64k LUT
0x1004 0000	0x10000	SVC = 0x00 Underlay = 0x00	Radar+Underlay 32k LUT
0x1004 0004	0x10001	SVC = 0x00 Underlay = 0x01	Radar+Underlay 32k LUT
0x1005 FFF8	0x17FFE	SVC = 0x7F Underlay = 0xFE	Radar+Underlay 32k LUT
0x1005 FFFC	0x17FFF	SVC = 0x7F Underlay = 0xFF	Radar+Underlay 32k LUT
0x1006 0000	0x18000	Underlay = 0x00	Underlay 256 LUT

C80 Addr	Index	FPGA Input Data	Function
0x1006 0400	0x18100	Middle = 0x00	Middle 256 LUT
0x1006 07FC	0x181FF	Middle = 0xFF	Middle 256 LUT
0x1006 0800	0x18200	SVC = 0x00	SVC 256 LUT
0x1006 0BFC	0x182FF	SVC = 0xFF	SVC 256 LUT
0x1006 0C00	0x18300	Overlay = 0x00	Overlay 256 LUT
0x1006 0FFC	0x183FF	Overlay = 0xFF	Overlay 256 LUT
0x1006 1000 to 0x1007 FFFC	0x18400 to 0x18FFF	not defined	

The indexing for output 1 is identical, however the C80 addresses are in the form 0x104X XXXX.

5.5.2 **Version 2 FPGA code**

Again both outputs have the same functionality. This version is similar to Version 0 FPGA code in that all of the Overlay key indices have the same functions. Version 2 is different in that the Middle layer may also be used for graphics, and that this Middle graphics layer has a >Key= value that allows radar+background map (SVC+Underlay) to be displayed. Thus if the Overlay is filled with 0xFA (Middle only), and the Middle is filled with the new >Key= value of 0xFE the display will show Radar+Map (SVC+Underlay 15 bits).

The Overlay Keying indices are:

Overlay Index	Display	Usage
0xFF	Overlay Colour 0xFF	Graphical Overlay
0xFE	Middle + Underlay (16 bit)	Colour Video
0xFD	SVC + Underlay (15 bit)	External radar on background map
0xFC	Faded Middle + Underlay (15 bit)	S/W scan converted radar on background map
0xFB	Underlay (8 bit)	Map only
0xFA	Middle (8 bit)	S/W scan converted radar only

Overlay Index	Display	Usage
0xF9	SVC (8 bit)	External radar only
0xF8	Overlay Colour 0xF8	Graphical Overlay
0xF7	Overlay Colour 0xF7	Graphical Overlay
0x01	Overlay Colour 0x01	Graphical Overlay
0x00	Overlay Colour 0x00	Graphical Overlay

The Middle Keying indices are:

Overlay Index	Display	Usage
0xFF	Middle Colour 0xFF	Graphics
0xFE	SVC + Underlay (15 bit)	Radar + Map
0xFD	Middle Colour 0xFD	Graphics
0xFC	Middle Colour 0xFC	Graphics
0x01	Middle Colour 0x01	Graphics
0x00	Middle Colour 0x00	Graphics

The FPGA Multiplexers have two write-only registers inside, these are the same as Version 0 FPGA.

The CLUT addressing and functions are unchanged from Version 0 FPGA.

5.6 Block Writes

Bits 5 and 6 of the *Reset Register* on the C.A.T. main board must be programmed to match the Block Write capability of video RAMS fitted to the Panther. The type of VRAMs fitted to the Panther can be determined by reading the board identity and version from the fixed FPGA registers (see section **5.3.1**).

The types of VRAMs fitted to each version are defined in Appendix E.

Texas VRAM have a x4 Block Write facility, those from OKI have a x8 Block Write.

The *Reset Register* is programmed thus:

D6	D5	VRAM Block Write Capability
0	0	none
1	0	x4
1	1	x8

6. Logic Description

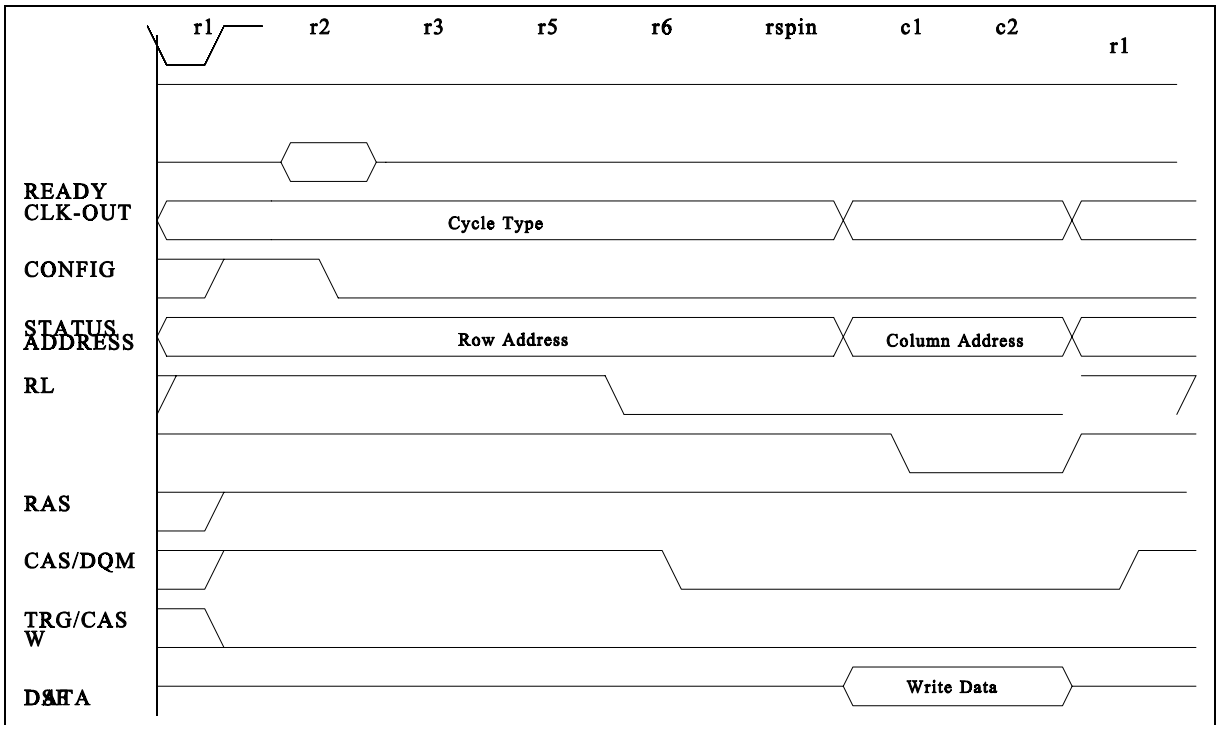
The circuitry for the Panther is quite straight forward, as many of the circuits elements are duplicated a number of times. The two display channels are identical, apart from their respective memory addressees. The frame stores are all identical, and the four FPGA Multiplexers and CLUTs within each channel are also identical to each other.

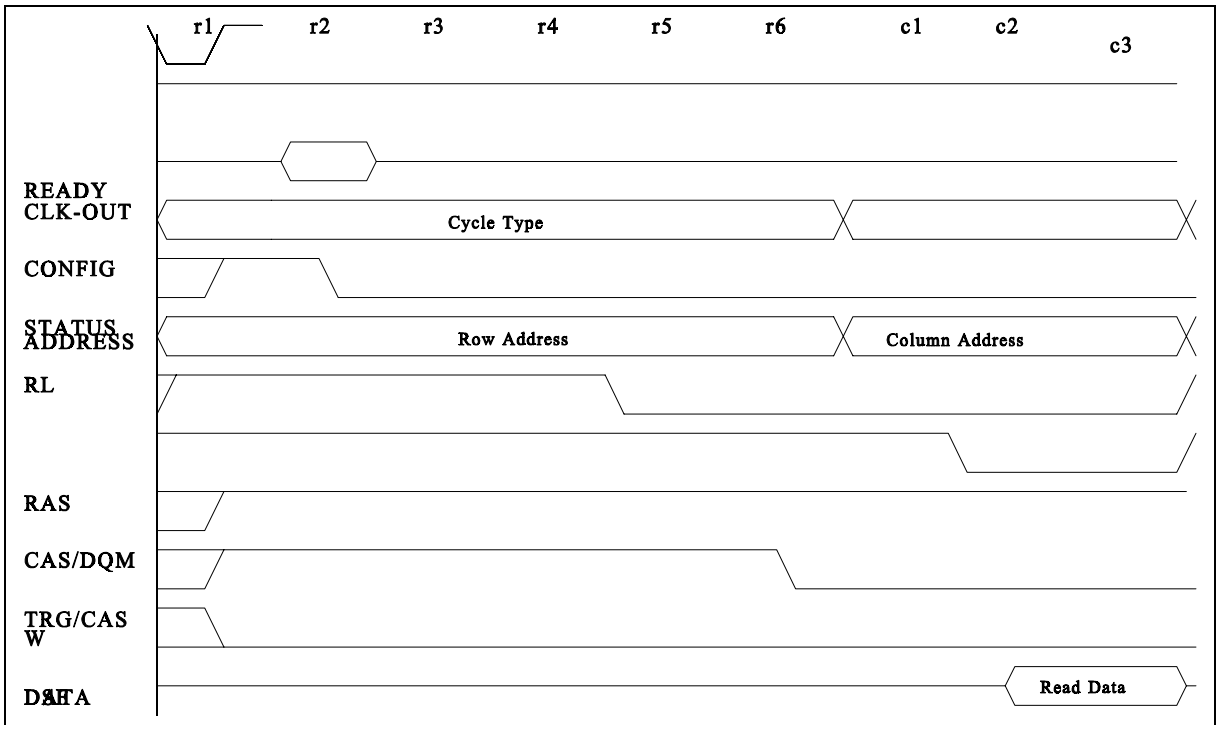
6.1 Frame stores

The frame stores are identical, each consists of four 256kx16 VRAMs, arranged to give a 64 bit interface to the C.A.T. The C.A.T. generates three row address strobes, one for Overlay, one for Middle and one for Underlay. On the Panther these three signals are qualified by the C80 row address to produce six individual RAS signals. This done by P714_5 [1E5]. The address and control lines to the VRAMs are all buffered on the Panther, excepting the eight column address strobes VDB CAS0..7[L] which are routed straight to the VRAMs. The four buffers, K2 [2B4], J2 [2B3], G2 [8B4] and H2 [8B3] are identical and each drives six VRAMs. The data lines of the VRAMs connect directly to the C.A.T.

Considering the Overlay frame store for output 0 on page 2 of the schematics, the four VRAMs S11..S14 have identical control and address signals, apart from the eight CAS signals. The eight CAS signals are used as byte write enables. As the C.A.T. has a big endian bus, VDB CAS7[L] is associated with the least significant byte, and VDB CAS0[L] the most significant byte. The order that the pixels appear on the screen is similar: VDB CAS7[L] and VDB DATA56..63[H] define the left hand pixel of each group of eight pixels, whilst VDB CAS0[L] and VDB DATA0..7[H] define the right hand pixel of each group of eight pixels.

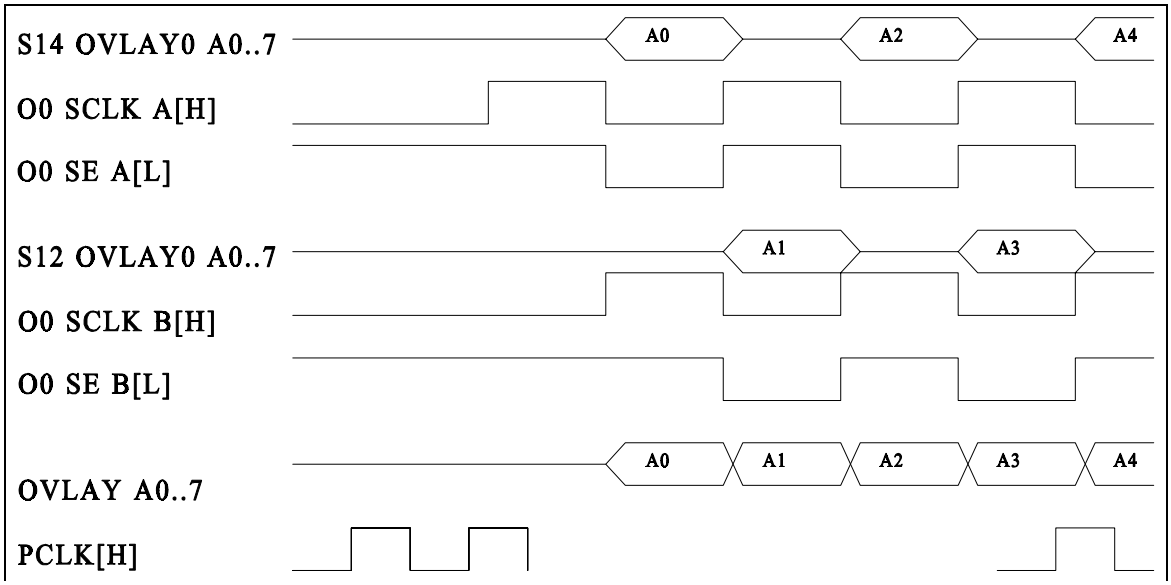
The read/write timing of the frame stores is controlled entirely by the C.A.T. Write cycles to the frame store use the C80 preset timing mode of 2 cycles per column, reads are slower at 3 cycles per column.





Video data is clocked out of the VRAMs four pixels at a time, and each frame store has two unique serial clocks. Considering the output 0 Overlay frame store again, four pixels are first clocked out of S14 and S13 by O0 SCLK A[H], then four more are clocked out of S12 and S11 by O0 SCLK B[H].

The two banks of VRAMs have their serial data outputs connected together, and each bank is enabled in turn to allow the data to be clocked into the next stage. The serial clocks and enables for output 0 are generated by the SCLK FPGA (P714_2) [6B5], the serial clocks and enables for output 1 are generated by the SCLK FPGA (P714_4) [12B5]. The four pixels clocked out of the VRAMs are labelled A, B, C and D on the schematics, and there are associated FPGA Multiplexers and CLUTs for each of these pixel streams. Of this group of four >A= is the left hand pixel and >D= is the right hand pixel. The serial data outputs of the VRAM=s are connected directly to the FPGA Multiplexers.



6.2 FPGA Multiplexers and LUTs

There are four interleaved FPGA Multiplexers and CLUTs per channel, all running at a quarter of the true pixel clock rate and each processing one of four adjacent pixels on the rising edge of PCLK[H]. The four banks of Multiplexers and CLUTs on sheets 3 and 4 of the schematics are for output 0, the banks are labelled >A=, >B=, >C= and >D=. In relation to the display >A= processes the left hand most pixel of each group of four, whilst >D= processes the right hand most pixel.

The four FPGA within each channel are all programmed with the same code. The four CLUTs are all written to simultaneously when the CLUT=s are loaded and thus always contain the same data. The following description refers to Bank A, operation of the other three banks is identical.

Pixel data from the three frame stores and the SVC interface is latched into the FPGA Multiplexer N3 (P714_1) [4A5] on the rising edge of PCLK0[H]. The pixel data from the four sources is combined in the FPGA in a way defined by the FPGA code to produce a 17 bit index into the CLUT. The CLUT address is clocked out of the FPGA on the rising edge of PCLK[H]. Note that the pipeline delays through the FPGA may vary from version to version of the FPGA, and on some versions the delays will be different for each of the frame stores. It is the job of the SCLK FPGAs (P714_2 and P714_4) to compensate for the differing pipeline delays by delaying the start of each of the frame store serial clocks.

The index clocked out of the Multiplexer FPGA is fed to three 8 bit SRAMs, T4, S4, N4 which map the index into a 24 bit Red, Green, Blue value. The resultant 24 bit R.G.B. value is clocked into the pipeline registers K4, K5, K6, M4, M5, M6 (sheet 7) on the next rising edge of PCLK[H].

Some versions of the Multiplexer FPGAs contain registers that may be written to by the C.A.T. This happens to all four Multiplexer FPGAs simultaneously. The write enable line to the FPGAs is the signal WR FPGA[L], this qualified by the address on VDB ADDR11..19[H], to differentiate between output 0 and output 1.

When the C.A.T. wants to read or write to the CLUTs it asserts the signal CE CLUT[L], this signal goes to the four Multiplexer FPGAs which generate the addresses for the SRAMs and to the SCLK FPGA which controls the data buffers to the SRAMs. The C.A.T. generated read/write address is fed to the SRAMs via the Multiplexer FPGAs. To save pins on the FPGAs the address is fed across as a row/column multiplexed address, the row portion of the address being latched inside the FPGAs by the signal VDB RL[L].

NOTE: On faster versions of the Panther e.g. 714000 the read/write address is registered by PCLK[H] before it is fed to the SRAMs. Thus before the LUTs can be loaded the pixel clock must be running reliably, and must be faster than 50MHz.

On slower versions of the Panther e.g. 714002 the read/write address is fed to the SRAMs asynchronously and thus the pixel clock is irrelevant to loading the LUTs.

On assertion of CE CLUT[L] the Multiplexer FPGAs feed the C80 generated address to the SRAMs and the SCLK FPGA enables the data buffers (N8, Q8, Q9, S8, T8, T9).

For a write operation all twelve buffers are enabled, there are however three write enable lines to the SRAMs WE RED[L], WE GREEN[L], WE BLUE[L]. These are derived from the C.A.T. signals WE5, WE6, WE7 gated with CE CLUT[L].

For a read operation only the data buffers for one of the banks of SRAMs are enabled to avoid contention. As all four banks should contain the same data, it does not matter which is read, however for test purposes a register within the SCLK FPGA allows the software to nominate which bank is to be read.

6.3 SCLK FPGAs

The SCLK FPGA for output 0 is P714_2 [6B5], for output 1 it is P714_4 [12B5]. One part of the FPGA is associated with buffering the video sync/blanking signals, generating the serial clocks for the frame stores, the other part of the FPGA controls the data buffers to the CLUTs. P714_4 also generates the signals for the SVC interface.

Registers within the FPGAs allow selection of different video sync modes, set the LUT bank to be read, and allow the version of board and FPGA code to read by the C.A.T.

6.3.1 Sync and Blanking Signals

The sync and blanking signals are all derived from signals generated by the C80 Video Controller on the C.A.T. The four signals from the C.A.T. are:

VDB HBLANK[L]
VDB VBLANK[L]
VDB HSYNC[L]
VDB VSYNC[L]

The above signals perform as named when the Panther is operating with a non-interlaced display. For interlaced displays VDB HBLANK[L] becomes a composite sync signal and VDB VBLANK[L] becomes composite blanking. The four signals are generated synchronously to the falling edge of the frame timer clock VDB FCLK[H]. This clock is generated by P714_2 and runs at half the rate of PCLK[H].

P714_2 generates composite sync for the Keyer I/F, vertical sync for the video output, and a programmable horizontal or composite sync for the video DAC. For non-interlaced displays these are generated from separate horizontal and vertical syncs from the C80 Video Controller. For interlaced displays the C80 generates composite sync, and this is used directly (the vertical sync output is disabled).

The FPGA also generates three blanking signals, a composite blanking signal for the DAC, and separate horizontal and vertical sync signals for the SVC interface. For non-interlaced displays these are generated from the C80 Video Controller HBLANK and VBLANK. For interlaced displays the DAC is fed the composite blanking from the C80, and the SVC horizontal and vertical blanking signals are disabled.

The horizontal/composite sync to the video DAC and the composite blanking to the DAC are both delayed within SCLK FPGAs to compensate for pipeline delays across the card.

There are two serial clocks for each frame store running at half the PCLK[H] rate. The two clocks are of alternate phase to produce four pixels on every PCLK[H] edge. The serial clocks only run during the visible period and are enabled by the composite blanking signal. The three pairs of serial clocks per channel do not have to start together, one or more pair may be delayed to compensate for differing pipeline delays through the Multiplexer FPGAs. A fourth serial clock, VDB SCLK[H] is generated by P714_2 and sent to the C80 Video Controller so that it can keep track of the amount of data left in the VRAM serial port.

6.3.2 **LUT Read/Write Signals**

Each SCLK FPGA generates four data buffer enable signals, CLUT EN A[L]....D[L], one for each bank of the CLUTs. They are activated by the assertion of CE CLUT[L] which comes from the C.A.T. For write operations all four are activated, for reads only one is activated. Which of the four is activated during a read is determined by a register within the FPGA.

The three CLUT write enables are also generated by the SCLK FPGAs, by gating WE7[L]..5[L] with CE CLUT[L].

6.4 Video DACs

The video DACs on the Panther, one per channel, also contain the hardware generated cursor circuits.

The read/write interface to the DAC is via four registers within the DAC, so aside from the ten data lines only four signals are involved. Two address lines, VDB ADDR1, 2[H] select which of the registers is accessed, R/W[H] controls the data direction and CE DAC[L] is the write strobe/ read enable. These signals all come from the C.A.T. which controls the timing, CE DAC[L] will be asserted for 120ns.

The full speed ECL pixel clock produced by the clock generator is fed to both DACs. The rest of the Panther circuitry runs on a quarter speed TTL version of this clock. This comes out of the LOADOUT pin of the channel 1 DAC (G8/47), and is driven around the board as PCLKn[H] by the buffer F8 [6B3]. The video data from the pipeline registers is clocked into the DACs by an inverted version of the pixel clock PCLK6[H].

The analogue video outputs are intended to be doubly terminated with 75R, i.e. they are terminated at source on the Panther with 75R, but it is also mandatory to terminate the three video signals with 75R at the display monitor.

6.5 SVC Interface

The SVC interface allows 8 bit digital video to be fed onto the Panther from an external frame store. To allow high speed video to be transferred, four pixels are transferred in parallel on each rising clock edge. The external frame store is synchronised to the Panther's frame stores by three signals generated by the Panther, these are:

SVC GCLK[H]
SVC HBLANK[H]
SVC VBLANK[H]

The clock signal runs at a quarter of the true pixel clock speed, and is a gated version of PCLKn[H] that only runs during the visible period. The horizontal and vertical blanking signals are derived from those produced by the C80 video Controller. All three signals are generated by the SCLK FPGA (P714_2) [6B5] .

6.5.1 Channel 0

The data from the external frame store is returned on SVC0 D0..7[H], SVC1 D0..7[H], SVC2 D0..7[H] and SVC3 D0..7[H], see sheet 14. Each group represents one 8 bit pixel, SVC0 D0..7[H] is the left most pixel of each group of four. The four pixels are clocked into the two registers N9 and S9 [14C5]. These registers are driven not by PCLK[H], but a clock signal from P714_2 called CCLK[H]. This clock runs continuously, but has minimal skew to SVC GCLK[H], thus giving the maximum amount of time to clock data across the interface. The four registered pixels are each routed to a different bank of the Multiplexer FPGAs.

6.5.2 Channel 1

The SVC data for channel 1 may be taken from the same set of pins as channel 0, or from a different set of pins. This allows different SVC data to be supplied to each channel. The switch between >normal= and >extended= SVC data is controlled by a register bit in P714_4. When >normal= SVC data is to used registers N10 and Q10 are enabled, when >extended= data is to be used S10 and T10 are enabled. (see sheet 14).

6.6 Pixel Clock Generator

The on board pixel clock generator for the Panther is an ICS1562 clock generator, E10 [15C5]. The clock chip has its own 16MHz reference crystal XT1. Using this reference it can be programmed to generate any pixel clock frequency in the range 10 to 260MHz. The differential PECL clock output is fed to multiplexer B10 [15E5], and thence to both video DACs. The multiplexer is used route an external pixel clock onto the Panther when a Vortex Video Keyer is being used. The ICS1562 contains numerous registers, see section **5.4 Pixel Clock Generator**. These are programmed using a serial data stream and clock - CLK DATA[H], CLK CE[H]. A third signal CLK HOLD[H] is used to load the serial data into the ICS1562 internal registers. The three signals are generated by P714_4 [12B5].

APPENDIX A - Memory Map

C80 address map detailing Panther Display Board addresses.

Base Address (hex)	Width/bits	Size/Bytes	Function
0400 0000	64	2M	Read/Write Underlay frame store, Output 0
0440 0000	64	2M	Read/Write Underlay frame store, Output 1
0480 0000	64	2M	Write both Underlay frame stores
0500 0000	64	2M	Read/Write Middle frame store, Output 0
0540 0000	64	2M	Read/Write Middle frame store, Output 1
0580 0000	64	2M	Write both Middle frame stores
0600 0000	64	2M	Read/Write Overlay frame store, Output 0
0640 0000	64	2M	Read/Write Overlay frame store, Output 1
0680 0000	64	2M	Write both Overlay frame stores
1000 0000	32	512K	Read/Write Video CLUTs, Output 0
1040 0000	32	512K	Read/Write Video CLUTs, Output 1
1080 0000	32	512K	Write both Video CLUTs
1100 0000	8	0 - 512	Video FPGAs
1200 0000	16	8	Video Palette DAC and Cursor, Output 0
1240 0000	16	8	Video Palette DAC and Cursor, Output 1.

APPENDIX B - EERAM Format

The following is a list of locations in the C.A.T.'s EERAM that store the video timing information for the Panther Display Board. The C.A.T. Processor card has two EERAM write protect jumpers. Jumper A protects those parameters that are set at the time of manufacture. Jumper B protects the user defined Video Timing and VME I/F parameters.

Addr	Use	Write protect	Typ value	Default value	Comment
0x20	Pixelclk PLL ref/MHz (msb)	A	0x10		This parameter is loaded
0x24	Pixelclk PLL ref freq/MHz	A	0x00		during board test.
0x28	Pixelclk PLL ref freq/MHz (lsb)	A	0x00		E.g 16.0000MHz
0x2C	Maximum Pixel Clk/MHz	A	0xC8		Depends on RAMS fitted.
0x30	VRAM SAM size Pixels/8	A	0x20		Depends on RAMs fitted.
0x34	*Reserved*	A	0x00		
0x38	*Reserved*	A	0x00		
0x3C	Checksum for locations 20 - 3C	A			
0x40	Drawing Page Width (Msb)	B		0x08	2048 pixels
0x44	Drawing Page Width (Lsb)	B		0x00	
0x48	Visible Screen Width Pixels/8	B		0xA0	1280 pixels
0x4C	Screen Height (Msb)	B		0x04	1024 lines
0x50	Screen Height (Lsb)	B		0x00	
0x54	H blank width Pixels/8	B		0x34	416 pixels
0x58	H sync width Pixels/8	B		0x18	192 pixels
0x5C	H back porch Pixels/8	B		0x14	160 pixels
0x60	V blank width Lines	B		0x2A	42 lines
0x64	V sync width Lines	B		0x03	3 lines
0x68	V back porch Lines	B		0x24	36 lines
0x6C	Pixel Clock Ref divider	B		0x0A	Pix clk = 108MHz
0x70	Pixel Clock Feedback divider	B		0x87	clk =16MHz * 135 / (2 * 10)
0x74	Pixel Clock post scaler	B		0x02	
0x78	Miscellaneous video setups	B		0x0E	
0x7C	Checksum for locations 40 - 7C	B			

Miscellaneous video setups

D7	D6	D5	D4	D3	D2	D1	D0
-	-	Vsync direction	Hsync direction	Composite Sync	Sync on Green	Pedestal	Interlace

D0	Interlace	1 = Interlaced	0 = Non-interlaced.
D1	Pedestal	1 = Pedestal ON	0 = Pedestal OFF
D2	Sync on Green	1 = ON	0 = OFF
D3	Composite Sync	1 = Composite	0 = Separate H & V
D4	HSYNC Direction	1 = Input	0 = Output
D5	VSYNC Direction	1 = Input	0 = Output

APPENDIX C - Connector Pinouts

Video O/P Connectors - P11, P15

Both video output connector on the Panther are identical 15 Way high density D-Type sockets.

Pin	Signal
1	Red
2	Green
3	Blue
4	n/c
5	n/c
6	Gnd
7	Gnd
8	Gnd
9	n/c
10	Gnd
11	n/c
12	n/c
13	Hsync/Csync
14	Vsync
15	n/c

Video Keyer Connector - P14

The connector on the Panther is a 10 way 0.1" boxed header.

Pin	Signal	Pin	Signal
1	VSYNC[L]	2	TTLCLK[H]
3	GND	4	PIXCLK[H]
5	GND	6	PIXCLK[L]
7	GND	8	HSYNC[L]
9	GND	10	CSYNC[L]

C.A.T. Display Board I/F Connectors

Note: Due to the transition board assemblies between the Panther and the C.A.T. the pin out on the Panther is the reverse of that on the C.A.T.

P9

Pin	Signal	Pin	Signal
79	+5V	80	+5V
77	VDB_DATA0	78	VDB_DATA1
75	GND	76	VDB_DATA2
73	VDB_DATA3	74	VDB_DATA4
71	VDB_DATA5	72	VDB_DATA6
69	VDB_DATA7	70	GND
67	VDB_DATA8	68	VDB_DATA9
65	VDB_DATA10	66	VDB_DATA11
63	GND	64	VDB_DATA12
61	VDB_DATA13	62	VDB_DATA14
59	VDB_DATA15	60	VDB_DATA16
57	VDB_DATA17	58	GND
55	VDB_DATA18	56	VDB_DATA19
53	VDB_DATA20	54	VDB_DATA21
51	GND	52	VDB_DATA22
49	VDB_DATA23	50	VDB_DATA24
47	VDB_DATA25	48	VDB_DATA26
45	VDB_DATA27	46	GND
43	VDB_DATA28	44	VDB_DATA29
41	VDB_DATA30	42	VDB_DATA31
39	GND	40	VDB_DATA32
37	VDB_DATA33	38	VDB_DATA34
35	VDB_DATA35	36	VDB_DATA36
33	VDB_DATA37	34	GND
31	VDB_DATA38	32	VDB_DATA39

P10

Pin	Signal	Pin	Signal
79	+5V	80	+5V
77	VDB_ADDR0	78	VDB_ADDR1
75	GND	76	VDB_ADDR2
73	VDB_ADDR3	74	VDB_ADDR4
71	VDB_ADDR5	72	VDB_ADDR6
69	VDB_ADDR7	70	GND
67	VDB_ADDR8	68	VDB_ADDR9
65	VDB_ADDR10	66	VDB_ADDR11
63	GND	64	VDB_ADDR12
61	VDB_ADDR13	62	VDB_ADDR14
59	VDB_ADDR15	60	VDB_ADDR16
57	VDB_ADDR17	58	GND
55	VDB_ADDR18	56	VDB_ADDR19
53	VDB_ADDR20	54	VDB_ADDR21
51	GND	52	VDB_ADDR22
49	VDB_ADDR23	50	RAS_VU[L]
47	RAS_VO[L]	48	RAS_VR[L]
45	VDB_RL[L]	46	GND
43	VDB_WE[L]	44	VDB_TRG[L]
41	VDB_DSF[H]	42	VDB_CAS0[L]
39	GND	40	VDB_CAS1[L]
37	VDB_CAS2[L]	38	VDB_CAS3[L]
35	VDB_CAS4[L]	36	VDB_CAS5[L]
33	VDB_CAS6[L]	34	GND
31	VDB_CAS7[L]	32	FPGA_RD[H]

P9

Pin	Signal	Pin	Signal
27	GND	28	VDB_DATA42
25	VDB_DATA43	26	VDB_DATA44
23	VDB_DATA45	24	VDB_DATA46
21	VDB_DATA47	22	GND
19	VDB_DATA48	20	VDB_DATA49
17	VDB_DATA50	18	VDB_DATA51
15	GND	16	VDB_DATA52
13	VDB_DATA53	14	VDB_DATA54
11	VDB_DATA55	12	VDB_DATA56
9	VDB_DATA57	10	GND
7	VDB_DATA58	8	VDB_DATA59
5	VDB_DATA60	6	VDB_DATA61
3	GND	4	VDB_DATA62
1	VDB_DATA63	2	+5V

P10

Pin	Signal	Pin	Signal
27	GND	28	WE7[L]
25	WE6[L]	26	WE5[L]
23	WE4[L]	24	DAC_CE[L]
21	R/W[H]	22	GND
19	VDB_DIR[H]	20	VDB_DEN[L]
17	VDB_VSYNC[L]	18	VDB_HSYNC[L]
15	GND	16	VDB_HBLANK[L]
13	VDB_FCLK[H]	14	VDB_CAREA[H]
11	VDB_SCLK[H]	12	VDB_VBLANK[L]
9		10	GND
7	-12V	8	+12V
5		6	
3	+3V3	4	+3V3
1	+5V	2	+5V

SVC Connector - P12

The connector on the Panther is a 100 Way plug: Robinson Nugent P50E-100P1-SR1-TG

Row A	Signal	Row B	Signal
1	GND	1	VBLANK[H]
2	HBLANK[H]	2	CLOCK[H]
3	GND	3	SVC0 D1[H]
4	SVC0 D0[H]	4	SVC0 D3[H]
5	SVC0 D2[H]	5	SVC0 D5[H]
6	SVC0 D4[H]	6	GND
7	SVC0 D6[H]	7	SVC0 D7[H]
8	SVC1 D0[H]	8	SVC1 D1[H]
9	SVC1 D2[H]	9	GND
10	SVC1 D4[H]	10	SVC1 D3[H]
11	SVC1 D6[H]	11	SVC1 D5[H]
12	SVC1 D7[H]	12	SVC2 D0[H]
13	GND	13	SVC2 D1[H]
14	SVC2 D2[H]	14	SVC2 D3[H]
15	SVC2 D4[H]	15	SVC2 D5[H]
16	GND	16	SVC2 D7[H]
17	SVC2 D6[H]	17	SVC3 D1[H]
18	SVC3 D0[H]	18	SVC3 D3[H]
19	GND	19	SVC3 D5[H]
20	SVC3 D2[H]	20	SVC3 D7[H]
21	SVC3 D4[H]	21	SVC3 D6[H]
22	SVC4 D1[H]	22	GND
23	SVC4 D0[H]	23	SVC4 D3[H]
24	SVC4 D2[H]	24	SVC4 D5[H]
25	SVC4 D4[H]	25	GND

Row A	Signal	Row B	Signal
26	SVC4 D6[H]	26	SVC4 D7[H]
27	SVC5 D0[H]	27	SVC5 D1[H]
28	SVC5 D2[H]	28	GND
29	SVC5 D4[H]	29	SVC5 D3[H]
30	SVC5 D6[H]	30	SVC5 D5[H]
31	SVC5 D7[H]	31	SVC6 D0[H]
32	GND	32	SVC6 D1[H]
33	SVC6 D2[H]	33	SVC6 D3[H]
34	SVC6 D4[H]	34	SVC6 D5[H]
35	GND	35	SVC6 D7[H]
36	SVC6 D6[H]	36	SVC7 D1[H]
37	SVC7 D0[H]	37	SVC7 D3[H]
38	GND	38	SVC7 D5[H]
39	SVC7 D2[H]	39	SVC7 D7[H]
40	SVC7 D4[H]	40	SVC7 D6[H]
41		41	GND
42		42	
43		43	
44		44	GND
45		45	
46		46	
47		47	GND
48		48	
49		49	
50	GND	50	

VME P1 and P2 Connectors

Only those signals that connect to the Panther are shown.

P1

Pin	Row A	Row B	Row C
1			
2			
3			
4		BG0IN[L]	
5		BG0OUT[L]	
6		BG1IN[L]	
7		BG1OUT[L]	
8		BG2IN[L]	
9	GND	BG2OUT[L]	GND
10		BG3IN[L]	
11	GND	BG3OUT[L]	
12			
13			
14			
15	GND		
16			
17	GND		
18			
19	GND		
20		GND	
21	IACKIN[L]		
22	IACKOUT[L]		
23		GND	
24			
25			
26			
27			

P2

Row A	Row B	Row C
	+5V	
	GND	
	GND	
	+5V	
	GND	

28						
29						
30						
31					GND	
32	+5V	+5V	+5V		+5V	

APPENDIX D - Cables and Accessories

Primagraphics Part Number	Description
400266	Video output cable - 15W Hi-Density D-Type to BNC.
701503	Panther SVC cable.
701501	C.A.T. serial cable. 9 Way Micro D-Type to 25 Way D-Type.
723000	C.A.T. Display Board transition Card.

APPENDIX E - Panther Dual Display Board Versions

Panther Versions

Part Number	Bd Version	FPGA Version	Pixel clock speed	PLL Ref	VRAMs
714000	0	0	100 to 200 MHz	16.00 MHz	Texas
714002	2	0	10 to 135 MHz	16.00 MHz	Texas
714003	3	2	100 to 200 MHz	16.00 MHz	Texas

714000 and 714003 EERAM settings

Addr	Use	Value	Comment
0x20	Pixclk PLL ref/MHz (msb)	0x10	16.0000 MHz
0x24	Pixclk PLL ref/MHz	0x00	
0x28	Pixclk PLL ref/MHz (lsb)	0x00	
0x2C	Maximum Pixel Clk/MHz	0xC8	200 MHz
0x30	VRAM SAM size Pixels/8	0x20	256 pixels/SAM

714002 EERAM settings

Addr	Use	Value	Comment
0x20	Pixclk PLL ref/MHz (msb)	0x10	16.0000MHz
0x24	Pixclk PLL ref/MHz	0x00	
0x28	Pixclk PLL ref/MHz (lsb)	0x00	
0x2C	Maximum Pixel Clk/MHz	0x87	135 MHz
0x30	VRAM SAM size Pixels/8	0x20	256 pixels/SAM

APPENDIX F - Circuit Diagrams and Assembly Drawings

