HARDWARE REFERENCE MANUAL

PMAC 1.5 Lite

Programmable Multi-Axis Controller

3Ax-602402-xHxx

July 10, 2003

DELTA TAU
Data Systems, Inc.
NEW IDEAS IN MOTION ...

Single Source Machine Control *Power // Flexibility // Ease of Use*
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Operating Conditions

All Delta Tau Data Systems, Inc. motion controller products, accessories, and amplifiers contain static sensitive components that can be damaged by incorrect handling. When installing or handling Delta Tau Data Systems, Inc. products, avoid contact with highly insulated materials. Only qualified personnel should be allowed to handle this equipment.

In the case of industrial applications, we expect our products to be protected from hazardous or conductive materials and/or environments that could cause harm to the controller by damaging components or causing electrical shorts. When our products are used in an industrial environment, install them into an industrial electrical cabinet or industrial PC to protect them from excessive or corrosive moisture, abnormal ambient temperatures, and conductive materials. If Delta Tau Data Systems, Inc. products are exposed to hazardous or conductive materials and/or environments, we cannot guarantee their operation.

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INTRODUCTION

Overview

The PMAC-Lite is a member of the PMAC(1) family of boards optimized for interface to traditional servo drives with single analog inputs representing velocity or torque commands. Its software is capable of eight axes of control. It has four channels of on-board axis interface circuitry. It can also support up to 8 channels of off-board axis interface circuitry through its expansion port, connected to an ACC-24P board.

The PMAC-Lite is a full-sized ISA-bus expansion board. While the PMAC-Lite is capable of ISA bus communications, with or without the optional dual-ported RAM, it does not need to be inserted into an ISA expansion slot. Communications can be done through an RS-232 or RS-422 serial port; standalone operation is possible.

The new "Universal" PMAC-Lite board replaces the previous PMAC-Lite board with battery-backed RAM and the PMAC1.5-Lite board with flash-backed RAM. The Universal PMAC-Lite can be built to use either type of memory.

Board Configuration

Base Version

The base version of the PMAC-Lite provides a 1-slot board with:

- 20 MHz DSP56002
- 128k x 24 SRAM active memory
- Battery-backup circuitry for SRAM (PMAC-Lite)
- 128k x 8 EPROM for firmware (PMAC-Lite)
- 512k x 8 flash memory for SRAM backup & firmware (PMAC1.5-Lite)
- Latest released firmware version
- RS-232/422 serial interface, ISA (PC) bus interface
- Four channels axis interface circuitry, each including:
  - 16-bit +/-10V analog output
  - 3-channel differential/single-ended encoder input
  - Four input flags, two output flags
  - Interface to external 16-bit serial ADC
- Display, control panel, muxed I/O, direct I/O interface ports
- PID/notch/feedforward servo algorithms

The unit has a 1-year limited warranty from date of shipment, and includes one manual per set of one to four PMACs in shipment.

Cables, mounting plates, and mating connectors are not included.

If the PMAC(1)-Lite version (battery-backed memory) of the board is ordered, the standard configuration will have SRAM ICs in U6, U9, and U15, filling the full footprint, and a battery in BT1. There will be no SRAM ICs in U7, U10, and U16. There will be an EPROM IC in the U5 socket.

If the PMAC1.5-Lite version (flash-backed memory) of the board is ordered, the standard configuration will have SRAM ICs in U7, U10, and U16. There will be a flash-memory IC in the U5 socket. There will be no SRAM ICs in U6, U9, and U15, and no battery in BT1, unless Option 16 is ordered.

Option 2: Dual Ported RAM

Dual-ported RAM provides a high-speed communications path for bus communications with the host computer through a bank of shared memory. DPRAM is advised if more than about 100 data items per second are to be passed between the controller and the host computer in either direction.

Option 2 provides an on-board 8k x 16 bank of dual-ported RAM. The key component on the board is U46. (Note that for previous versions of the PMAC-Lite, this was a separate board.)

Option 5: CPU & Memory Configurations

The standard PMAC-Lite has a 20-MHz CPU. Options 5A, 5B and 5C are available for applications requiring more computing power. These options provide faster CPU ICs in U13 and faster SRAM ICs in U7, U10, and U16. They are only available with flash-memory backup of the SRAM.

- **Option 5A** provides a 40 MHz CPU with zero-wait-state SRAM active memory and flash backup.
- **Option 5B** provides a 60 MHz CPU with zero-wait-state SRAM active memory and flash backup.
- **Option 5C** provides an 80 MHz CPU with zero-wait-state SRAM active memory and flash backup.

Option 6: Extended Servo Algorithm

The standard PID servo algorithm with feedforward and notch filter is suitable for most applications. Systems with difficult dynamics, especially with significant flexibility, may require a more powerful servo algorithm, such as the Extended Servo Algorithm (ESA).

Option 6 provides firmware in the PMAC-Lite that replaces the standard PID servo algorithm with the Extended Servo Algorithm. This option provides different firmware in the U5 flash-memory/EPROM IC. If loaded at the factory, this IC will have a "1" suffix on the labeled and reported version number (e.g. V1.16D1).

Option 7: Plate Mounting

If the PMAC-Lite is used as an ISA bus expansion board, the standard hardware provides for proper mounting of the board in the bus. However, if it is not installed in an ISA expansion slot, other provisions must be made for mounting.

Option 7 provides a mounting plate connected to the PMAC-Lite with standoffs. It is used to install the PMAC-Lite in standalone applications.

Option 8: High-Accuracy Clock Crystal

The PMAC-Lite has a clock crystal (component Y1) of nominal frequency 19.6608 MHz (~20 MHz). The standard crystal's accuracy specification is +/-100 ppm. Long-term velocity accuracy is limited by the accuracy of the crystal, unless an external time base is used.

Option 8A provides a nominal 19.6608 MHz crystal with a +/-15 ppm accuracy specification.

Option 9: RS-422 Interface (now standard)

The RS-422 interface now comes standard with the PMAC-Lite in addition to the RS-232 interface. There is no need to order Option 9L as before.

Option 10: Firmware Version Specification

Normally the PMAC-Lite is provided with the newest released firmware version. A label on the U5 flash-memory/EPROM IC shows the firmware version loaded at the factory.

Option 10 provides for a user-specified firmware version.

Option 14: Replacement of flag Opto-Isolators with Socketed Shunts

Normally, the flag inputs on all servo channels have opto-isolator circuits that require 12 to 24V inputs to turn on. When the ACC-8D Option 8 Analog Encoder Interpolator is used on a pair of channels, it uses the flag inputs on the second (even-numbered) channel to provide "sub-count" information at 5V levels referenced to digital ground.

Option 14 replaces the opto-isolators on the even-numbered channels of PMAC-Lite with socketed shunts that permit the input of 5V non-isolated signals from the ACC-8D Option 8 board.

Option 15: V-to-F Converter for Analog Input

The JPAN control panel port on the PMAC-Lite has an optional analog input called WIPER (because it is often tied to a potentiometer's wiper pin). PMAC-Lite can digitize this signal by passing it through an optional voltage-to-frequency converter, using E-point jumpers to feed this into the Encoder 4 circuitry (no other use is then permitted), and executing frequency calculations using the "time base" feature of the encoder conversion table.

Option 15 provides a voltage-to-frequency converter that permits the use of the WIPER input on the control panel port.

Option 16: Battery-Backed Parameter Memory

The contents of the main flash-backed memory (components U7, U10, and U16) of the PMAC1.5-Lite are not retained through a power-down or reset unless they have been saved to flash memory first. Option 16 provides supplemental battery-backed RAM for real-time parameter storage that is ideal for holding machine-state parameters in case of an unexpected power-down. It can only be used when the main memory is flash-backed.

Option 16 provides a 16k x 24 bank of battery-backed parameter RAM in components U6, U9, U15 (smaller than the full footprint), with the battery in BT1.

Hardware Updates

Significant upgrades were made to the PMAC-Lite board in the 602402-102 version. This new version replaces earlier versions of the 602402 board (PMAC1.5-Lite – flash-backed memory), and the 602399 board (PMAC(1)-Lite – battery-backed memory). The ability to configure 602402-102 (and newer) in either battery-backed or flash-backed memory configurations leads to it being called the "Universal" PMAC-Lite.

Improvements on the Universal PMAC-Lite include:

- **Universality.** Formerly different board designs were used for battery-backed (602399-10x) and flash-backed (PMAC1.5-Lite: 602402-101) versions of the PMAC-Lite. Now both configurations can be built on the same board, for cost savings that are passed on to you.
- **80-MHz CPU.** The new PMAC-Lite supports the Option 5C 80 MHz CPU for high-end operations.
- **Supplemental Battery-Backed Parameter Memory.** The new PMAC-Lite supports the Option 16 supplemental battery-backed parameter memory when the main memory is flash-backed.
- **On-board Dual-Ported RAM.** The new PMAC-Lite has optional on-board dual-ported RAM, whereas the old PMAC-Lite required a separate board. On-board DPRAM saves an expansion slot and is less expensive.
- **Raised Bottom Edge.** The bottom edge of the board has been raised so that it can clear high-profile parts on the PC motherboard – up to 25mm (1 inch) high.
- **Standard RS-422 Serial Port.** An RS-422 serial interface, which formerly required the Option 9L piggyback board, now is standard. Jumpers E107 and E108 select between the RS-232 port and the RS-422 port.

- **24V Amplifier-Enable Capability.** New Jumper E100 permits use of up to 24V supply for the amplifier-enable signal, compared to a maximum of 15V on the older version.
- **Sinking or Sourcing Input Flags.** The new ACC-24P permits the use of either sinking or sourcing input flags (home, limits, fault); the old ACC-24P permitted only sinking input flags.
- **Voltage Interlock Circuit**. The new ACC-24P has an interlock circuit that shuts down the analog outputs if it detects anything wrong with the power supply, preventing runaway on partial supply loss.
- **Surface-Mount Technology.** Most components are surface mounted for higher reliability and greater long-term part availability.
- **In-System-Programmable Logic.** Interface logic ICs now can be programmed when installed in the PMAC-Lite, permitting elimination of sockets for higher reliability, and easier manufacturing and upgradability.

Compatibility Issues

The new PMAC-Lite can be operated in a manner that is 100% compatible with the old PMAC-Lite. The board is shipped from the factory with settings for 100% compatible operation. To ensure your operation is compatible, double-check the following settings:

- **Raised Bottom Edge.** The higher bottom edge moves the lower left mounting hole for standoffs up 12.7 mm (0.5 in). If you are using standoff mounting, and cannot move the matching mounting hole, contact Delta Tau for free offset standoffs.
- **Serial Port Choice.** Because both RS-232 and RS-422 ports are always provided, jumpers must be set correctly to use the port of your choice. Jumpers E107 and E108 must connect pins 1 and 2 to use the RS-232 port on the J4 connector; they must connect pins 2 and 3 to use the RS-422 port on the J4A connector.
- **On-Board Dual-Ported RAM.** If you wish to use dual-ported RAM with your new PMAC-Lite, you must order Option 2 at the time you order the board. The new PMAC-Lite is not compatible with the off-board DPRAM, and the on-board DPRAM option cannot be installed in the field.
- **24V Amplifier Enable Capability.** In order for the amplifier enable outputs to use the +12V to +15V analog supply voltage for a high-side clamping supply, jumper E100 must connect pins 1 and 2.
- **Sinking/Sourcing Input Flags.** To use sinking input flags, connect the flags as you have done before.
- **Firmware Reload.** Putting jumper E51 ON is now for re-initialization to factory default values only. Firmware reload is set up by jumping pins 2 and 3 of E106.

Basic Specifications

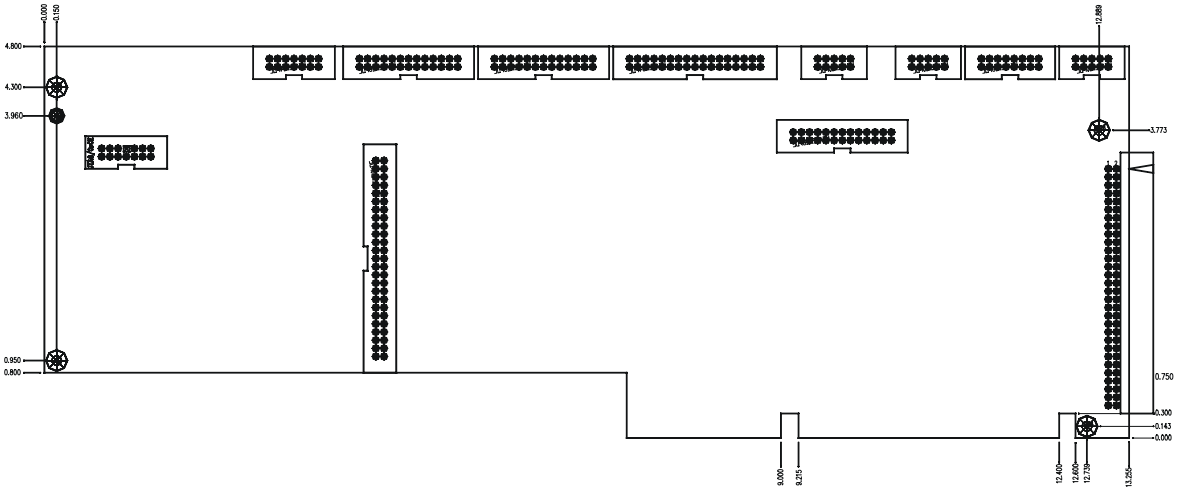
Physical Specifications

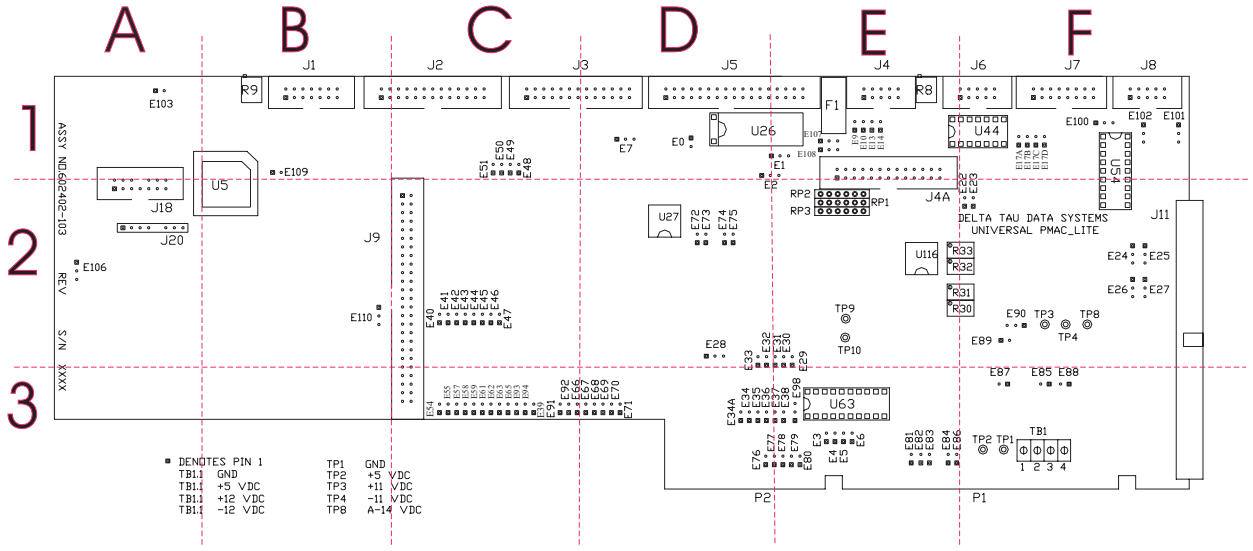
Size: 33.5cm x 9.9cm x 3.8cm (13.2" x 3.9" x 1.4")
Weight: ¾ lb.
Temperature
Operating: 0°C to 60°C (32°)F to 140°F)
Storage: 12°C to 82°C (10°F to 180°F)
Humidity: 10% to 95%, noncondensing

Electrical Specifications

Power:	1.5A @ +5V (±5%) (7.5W) 0.3A @ +12 to +15V (4.5W) 0.25A @ -12 to –15V (3.8W)	Pertains to 8-channel configuration, with a typical load of encoders
Battery	**3.**0V Lithium Cell, 1200 mAh, 2/3 A-size, no tabs, or 3.6V Lithium Cell, 1000 mAh, 1.00" can Expected battery life: 10 years (standard), 6-9 months (Opt. 5). Recommended replacement: 24 months (standard, (3-6 months (Opt. 5)	

LAYOUT DIAGRAM





E-POINT DESCRIPTIONS

E1 - E2: Machine Output Supply Voltage Configure

E Point & Physical Layout	Location	Description	Default
E1 	E1	***CAUTION*** The jumper setting must match the type of driver IC, or damage to the IC will result. Jump pin 1 to 2 to apply +V (+5V to 24V) to pin 11 of "U26" (should be ULN2803A for sink output configuration) JOPTO "Machine" outputs M01-M08 Jump pin 2 to 3 to apply GND to pin 11 of U26 (should be UDN2981A for source output configuration)	1-2 Jumper installed
E2 	D1	***CAUTION*** The jumper setting must match the type of driver IC, or damage to the IC will result. Jump pin 1 to 2 to apply GND to pin 10 of "U26" (should be ULN2803A for sink output configuration). Jump pin 2 to 3 to apply +V (+5V to 24V) to pin 10 of "U26" (should be UDN2981A for source output configuration).	1-2 Jumper installed

E3 - E6: Servo Clock Frequency Control

The servo clock (which determines how often the servo loop is closed) is derived from the phase clock (see E98, E29 - E33) through a "divide-by-N" counter. Jumpers E3 through E6 control this dividing function.

E3	E4	E5	E6	Servo Clock = Phase Clock Divided by N	Default & Physical Layout E3 E4 E5 E6  LOC.: E3 E3 E3 E3
ON	ON	ON	ON	N = Divided by 1	
OFF	ON	ON	ON	N = Divided by 2	
ON	OFF	ON	ON	N = Divided by 3	
OFF	OFF	ON	ON	N = Divided by 4	Only E5 and E6 ON
ON	OFF	ON	ON	N = Divided by 5	
OFF	ON	OFF	ON	N = Divided by 6	
ON	OFF	OFF	ON	N = Divided by 7	
OFF	OFF	OFF	ON	N = Divided by 8	
ON	ON	ON	OFF	N = Divided by 9	
OFF	ON	ON	OFF	N = Divided by 10	
ON	OFF	ON	OFF	N = Divided by 11	
OFF	OFF	ON	OFF	N = Divided by 12	
ON	ON	OFF	OFF	N = Divided by 13	
OFF	ON	OFF	OFF	N = Divided by 14	
ON	OFF	OFF	OFF	N = Divided by 15	
OFF	OFF	OFF	OFF	N = Divided by 16	

Adjust the setting of I-variable I10 to match the servo interrupt cycle time set by E98, E29 -- E33, and E3 -- E6. I10 holds the length of a servo interrupt cycle, scaled so that 8,388,608 equals one millisecond. Since I10 has a maximum value of 8,388,607, the servo interrupt cycle time should always be less than a millisecond (unless you want to make your basic unit of time on PMAC something other than a millisecond). If you wish a servo sample time greater than one millisecond, the sampling may be slowed in software with variable Ixx60.

Frequency can be checked on J4 pins 21 & 22. It can also be checked from software by typing RX:0 in the PMAC terminal at 10-second intervals and dividing the difference of successive responses by 10000. The resulting number is the approximate Servo Clock frequency kHz.

If E40-E43 are not all ON, the phase clock is received from an external source through the J4 serial-port connector, and the settings of E3 – E6 are not relevant.

E7: Machine Input Source/Sink Control

E Point & Physical Layout	Location	Description	Default
E7 	D1	Jump pin 1 to 2 to apply +5V to input reference resistor sip pack; this will bias MI1 to MI8 inputs to +5V for "OFF" state; input must then be grounded for "ON" state. Jump pin 2 to 3 to apply GND to input reference resistor sip pack; this will bias MI1 to MI8 inputs to GND for "OFF" state; input must then be pulled up for "ON" state (+5V to +24V).	1-2 Jumper installed

E9, E10, E13, E14: Serial Interface Direction Control

The E9, E10, E13, and E14 jumpers control whether the RS-232 serial port will be in DCE or DTE format. The default configuration permits straight-across connection to a PC DB-9 serial port.

E Point & Physical Layout	Location	Description	Default
E9 E10 	E1	Jump E9-1 to E9-2 to allow RXD/ to be input on J4-3. Jump E10-1 to E10-2 to allow TXD/ to be output on J4-5. Jump E9-1 to E10-1 to allow TXD/ to be output on J4-3. Jump E9-2 to E10-2 to allow RXD/ to be input on J4-5.	1-2 Jumpers installed
E13 E14 	E1	Jump E13-1 to E13-2 to allow RTS to be input on J4-7. Jump E14-1 to E14-2 to allow CTS to be output on J4-9. Jump E13-1 to E14-1 to allow CTS to be output on J4-7. Jump E13-2 to E14-2 to allow 'RTS' to be input on J4-9.	1-2 Jumpers installed

E17A-D: Amplifier Enable/Direction Polarity Control

E Point & Physical Layout	Location	Description	Default
E17A 	F1	Jump 1-2 for high-true AENA1 Remove jumper for low-true AENA1	No jumper installed
E17B 	F1	Jump 1-2 for high-true AENA2 Remove jumper for low-true AENA2	No jumper installed
E17C 	F1	Jump 1-2 for high-true AENA3 Remove jumper for low-true AENA3	No jumper installed
E17D 	F1	Jump 1-2 for high-true AENA4 Remove jumper for low-true AENA4	No jumper installed
Note: Low-true enable is the fail-safe option with the default sinking ULN2803A output driver IC. High-true enable is the fail-safe option with the alternate sourcing UN2981A.			

E22 - E23: Control Panel Handwheel Enable

E-Point & Physical Layout	Location	Description	Default
E22 	F2	Jump pin 1 to 2 to obtain handwheel encoder signal from front panel at J2-16 for CHB2 (ENC2-B).	No jumper
E23 	F2	Jump pin 1 to 2 to obtain handwheel encoder signal from front panel at J2-22 for CHA2 (ENC2-A).	No jumper
Note: With these jumpers ON, no encoder should be wired into ENC2 on JMACH1. Jumper E26 must connect pins 1-2, because these are single-ended inputs. This function is unrelated to the encoder brought in through ACC-39 on J2.			

E24 - E27: Encoder Single-Ended/Differential Control

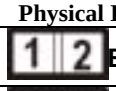
E-Point & Physical Layout	Location	Description	Default
E24 	F2	ENC 4 through 1: Jump pin 1 to 2 to tie complementary encoder inputs to 2.5V	1-2 Jumper installed for E24 - E27
E25 	F2	Jump pin 2 to 3 to tie complementary encoder inputs to 5V For no encoder connection: Jump pin 1 to 2	E24: ENC 4 E25: ENC 3 E26: ENC 2 E27: ENC 1
E26 	F2	For single-ended encoders: Jump pin 1 to 2. For differential line-driver encoders: Don't care	
E27 	F2	For complementary open-collector encoders: Jump pin 2 to 3	

E28: Following Error/Watchdog Timer Signal Control

E-Point & Physical Layout	Location	Description	Default
E28 	D2	Jump pin 1 to 2 to allow warning following error (Ix12) for the selected coordinate system to control FEFCO/ on J8-57 Jump pin 2 to 3 to cause Watchdog timer output to control FEFCO/. Low TRUE output in either case	2-3 Jumper installed

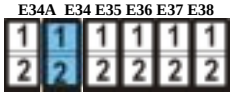
E29 - E33: Phase Clock Frequency Control

Jumpers E29 through E33 control the speed of the phase clock, and, indirectly, the servo clock, which is divided down from the phase clock (see E3 - E6). No more than 1 of these 5 jumpers may be on at a time.

E29	E30	E31	E32	E33	PHASE Clock Frequency		Default & Physical Layout	LOC
					E98 Connects Pins 1 and 2	E98 Connects Pins 2 And 3		
ON	OFF	OFF	OFF	OFF	2.26 kHz	1.13 kHz	 E29	E2
OFF	ON	OFF	OFF	OFF	4.52 kHz	2.26 kHz	 E30	E2
OFF	OFF	ON	OFF	OFF	9.04 kHz	4.52 kHz	 E31	E2
OFF	OFF	OFF	ON	OFF	18.07 kHz	9.04 kHz	 E32	D2
OFF	OFF	OFF	OFF	ON	36.14 kHz	18.07 kHz	 E33	D2
Note: If E40-E43 are not all ON, the phase clock is received from an external source through the J4 serial-port connector, and the settings of E29 – E33 are not relevant.								

E34 - E38: Encoder Sampling Clock Frequency Control

Jumpers E34 - E38 control the encoder sampling clock (SCLK) used by the gate array ICs. No more than 1 of these 6 jumpers may be on at a time.

E34A	E34	E35	E36	E37	E38	SCLK Clock Frequency	Default & Physical Layout
							E34A E34 E35 E36 E37 E38  Location; all at D/E3
ON	OFF	OFF	OFF	OFF	OFF	19.6608 MHz	
OFF	ON	OFF	OFF	OFF	OFF	9.8304 MHz	E34 ON
OFF	OFF	ON	OFF	OFF	OFF	4.9152 MHz	
OFF	OFF	OFF	ON	OFF	OFF	2.4576 MHz	
OFF	OFF	OFF	OFF	ON	OFF	1.2288 MHz	
OFF	OFF	OFF	OFF	OFF	ON	External Clock 1 to 30 MHz maximum input on CHC4 & CHC4/	

E39: Reset-From-Bus Enable

E-Point & Physical Layout	Location	Description	Default
E39 	C3	Jump pin 1 to 2 to allow PMAC to derive its reset from the PC backplane. Remove jumper to allow PMAC to power up in normal way; PCbus hardware reset will not reset PMAC; it must be removed for standalone operation. Only one of E39, E93, and E94 should be on at once. See also E93 & E94	No jumper

E40 - E43: Servo and Phase Clock Direction Control

E40	E41	E42	E43	Card Address	Servo & Phase Clock Direction	Default & Physical Layout E40 E41 E42 E43  C2 C2 C2 C2
ON	ON	ON	ON	@0	Output	(ALL ON)
OFF	ON	ON	ON	@1	Input	
ON	OFF	ON	ON	@2	Input	
OFF	OFF	ON	ON	@3	Input	
ON	ON	OFF	ON	@4	Input	
OFF	ON	OFF	ON	@5	Input	
ON	OFF	OFF	ON	@6	Input	
OFF	OFF	OFF	ON	@7	Input	
ON	ON	ON	OFF	@8	Input	
OFF	ON	ON	OFF	@9	Input	
ON	OFF	ON	OFF	@A	Input	
OFF	OFF	ON	OFF	@B	Input	
ON	ON	OFF	OFF	@C	Input	
OFF	ON	OFF	OFF	@D	Input	
ON	OFF	OFF	OFF	@E	Input	
OFF	OFF	OFF	OFF	@F	Input	
Note: If any jumper E40 – E43 is removed and the servo and phase clocks are not brought in on the J4A serial port, the watchdog timer will trip immediately.						

E44 - E47: Serial Baud Rate Control

Jumpers E44 - E47 control what baud rate to use for serial communications. Any character received over the bus causes PMAC to use the bus for its standard communications. The serial port is disabled when E44-E47 are all on.

Baud Rate Control "E" Points				Baud Rate				Default & Physical Layout
E44	**E45**	**E46**	**E47**	**20 MHz Flash CPU (OPT 4A)**	**Battery CPU, 40 MHz Flash CPU (Opt 5A)**	**60 MHz Flash CPU (Opt 5B)**	**80 MHz Flash CPU (Opt 5C)**	**E44 E45 E46 E47**  **C2 C2 C2 C2**
ON	ON	ON	ON	Disabled	Disabled	Disabled	Disabled	
OFF	ON	ON	ON	300	600	900	1200	
ON	OFF	ON	ON	400*	800*	1200	1600*	
OFF	OFF	ON	ON	600	1200	1800	2400	
ON	ON	OFF	ON	800*	1600*	2400	3200*	
OFF	ON	OFF	ON	1200	2400	3600	4800	
ON	OFF	OFF	ON	1600*	3200*	4800	6400*	
OFF	OFF	OFF	ON	2400	4800	7200	9600	Opt 5C
ON	ON	ON	OFF	3200*	6400*	9600	12800*	Opt 5B
OFF	ON	ON	OFF	4800	9600	14400	19200	Standard, Opt 5A
ON	OFF	ON	OFF	6400*	12800*	19200	25600*	
OFF	OFF	ON	OFF	9600	19200	28800	38400	Opt 4A (1.5-Lite)
ON	ON	OFF	OFF	12800*	25600*	38400	51200*	
OFF	ON	OFF	OFF	19200	38400	57600	76800	
ON	OFF	OFF	OFF	25600*	51200*	76800	102400*	
OFF	OFF	OFF	OFF	38400	76800	115200	153600	

***Non-standard baud rate

Note: These jumpers are only read at power-up/reset to set the baud rate at that time.

E48: CPU Clock Frequency Control

E Point & Physical Layout	Location	Description	Default
E48 	C1	Jump pins 1 and 2 to multiply crystal frequency by 3 inside CPU for 60 MHz operation Remove jumper to multiply crystal frequency by 2 inside CPU for 40 MHz operation Don't care for 20 MHz CPU versions For 80 MHz operation, set jumper for 40 MHz, then increase speed in software (WX$FFFD,$750003)	No jumper installed (20, 40 & 80 MHz versions) Jumper installed (60 MHz version)
Note: It may be possible to operate a board at a frequency higher than that for which its components are are rated. However, this uses the components outside of their specified operating range, and proper execution of the PMAC under these conditions is not guaranteed. PMAC software failure is possible, even probable, under these conditions, and this can lead to very dangerous machine failure. Operation in this mode is done completely at the user's own risk; Delta Tau can accept no responsibility for the operation of the PMAC or the machine under these conditions.			

E49: Serial Communications Parity Control

E Point & Physical Layout	Location	Description	Default
E49 	C1	Jump pin 1 to 2 for NO serial parity; remove jumper for ODD serial parity	Jumper installed

E50: Non-Volatile Memory Save Control

E Point & Physical Layout	Location	Description	Default
E50 	C1	Jump pin 1 to 2 to enable save to EAROM or flash memory Remove jumper to disable save to EAROM or flash memory	Jumper installed

E51: Normal/Re-initializing Power-Up

E Point & Physical Layout	Location	Description	Default
E51 	C1	Jump pin 1 to 2 to re-initialize on power-up/reset, loading factory default parameters Remove jumper for normal power-up/reset, loading last saved parameters	No jumper installed
Note: On the Universal PMAC-Lite, the board is put in "bootstrap mode" for the loading of new firmware by connecting pins 2 and 3 of E106. E51 is for re-initialization of parameters only.			

E54 - E65: Host Interrupt Signal Select

E Point & Physical Layout	Location	Description	Default
E55 	C3	Jump pin 1 to 2 to allow EQU4 to interrupt host-PC at PMAC interrupt level IR7	No jumper installed
E57 	C3	Jump pin 1 to 2 to allow EQU3 to interrupt host-PC at PMAC interrupt level IR7	No jumper installed
E58 	C3	Jump pin 1 to 2 to allow MI2 to interrupt host-PC at PMAC interrupt level IR6	No jumper installed
E59 	C3	Jump pin 1 to 2 to allow AXIS EXPANSION INT-0 to interrupt host-PC at PMAC interrupt level IR6	No jumper installed
E61 	C3	Jump pin 1 to 2 to allow EQU2 to interrupt host-PC at PMAC interrupt level IR6	No jumper installed
E62 	C3	Jump pin 1 to 2 to allow MI1 to interrupt host-PC at PMAC interrupt level IR5	No jumper installed
E63 	C3	Jump pin 1 to 2 to allow AXIS EXPANSION INT-1 to interrupt host-PC at PMAC interrupt level IR5	No jumper installed
E65 	C3	Jump pin 1 to 2 to allow “EQU1” to interrupt host-PC at PMAC interrupt level “IR5”.	No jumper installed

E66 - E71: Bus Base Hardware Address (Low Bits)

These jumpers work with E91 & E92 to set the base address of PMAC-Lite on the PC bus. See *PMAC-Lite Bus Addressing* below for details on how to set these jumpers.

E Point & Physical Layout	Location	Description	Default
E66 E67 E68 E69 E70 E71 	C3/D3	E66-Bit 9 PC bus base address E67-Bit 8 PC bus base address E68-Bit 7 PC bus base address E69-Bit 6 PC bus base address E70-Bit 5 PC bus base address E71-Bit 4 PC bus base address ON = 0; OFF = 1 for calculating bus address	E67-E70 installed

E72 - E73: Panel Analog Time Base Signal Enable

E Point & Physical Layout	Location	Description	Default
E72 	D2	Jump pin 1 to 2 to allow V to F converter FOUT derived from Wiper input on J2 to connect to CHA4	No jumper installed
E73 	D2	Jump pin 1 to 2 to allow V to F converter sign out derived from `Wiper` input on J2 to connect to CHB4	No jumper installed
Note: With these jumpers ON, no encoder should be wired into ENC4 on JMACH1. E27 must connect pins 1 to 2 because these are single-ended inputs. Variable I915 should be set to 4 to create a positive voltage (frequency) number in PMAC.			

E74 - E75: Clock Output Control for Ext. Interpolation

E Point & Physical Layout	Location	Description	Default
E74 	D2	Jump pin 1 to 2 to allow SCLK/ to output on CHC4/	No jumper installed
E75 	D2	Jump pin 1 to 2 to allow SCLK to output on CHC4	No jumper installed
Note: SCLK out permits synchronous latching of analog encoder interpolators such as ACC-8D Opt 8.			

E76 - E84: Host Interrupt Signal Select

E Point & Physical Layout	Location	Description	Default
E76 	D3	Jump pin 1 to 2 to allow PMAC-Interrupt to host-PC on IRQ14	No jumper installed
E77 	D3	Jump pin 1 to 2 to allow PMAC-Interrupt to host-PC on IRQ15	No jumper installed
E78 	E3	Jump pin 1 to 2 to allow PMAC-Interrupt to host-PC on IRQ12	No jumper installed
E79 	E3	Jump pin 1 to 2 to allow PMAC-Interrupt to host-PC on IRQ11	No jumper installed
E80 	E3	Jump pin 1 to 2 to allow PMAC-Interrupt to host-PC on IRQ10	No jumper installed
E81 	E3	Jump pin 1 to 2 to allow PMAC-Interrupt to host-PC on IRQ3	No jumper installed
E82 	E3	Jump pin 1 to 2 to allow PMAC-Interrupt to host-PC on IRQ4	No jumper installed
E83 	E3	Jump pin 1 to 2 to allow PMAC-Interrupt to host-PC on IRQ5	No jumper installed
E84 	E3	Jump pin 1 to 2 to allow PMAC-Interrupt to host-PC on IRQ7	No jumper installed
Note: Only one of the jumpers from E76 to E84, and E86, should be ON at one time.			

E85: Host-Supplied Analog Power Source Enable

E Point & Physical Layout	Location	Description	Default
E85 	F3	Jump pin 1 to pin 2 to allow A+14V to come from PC bus (ties amplifier and PMAC-Lite power supply together. Defeats OPTO coupling) Note that if E85 is changed, E88 and E87 must also be changed. Also, see E90	No jumper

E86: Host Interrupt Signal Select

E Point & Physical Layout	Location	Description	Default
E86 	E3	Jump pin 1 to 2 to allow PMAC-Interrupt to host-PC on IRQ2	No jumper

E87 - E88: Host-Supplied Analog Power Source Enable

E Point & Physical Layout	Location	Description	Default
E87 	F3	Jump pin 1 to pin 2 to allow AGND to come from PC bus (ties amplifier and PMAC-Lite GND together. Defeats OPTO coupling.). Note that if E87 is changed, E85 and E88 also must be changed. Also, see E90	No jumper
E88 	F3	Jump pin 1 to pin 2 to allow A-14V to come from PC bus (ties amplifier and PMAC-Lite power supply together. Defeats OPTO coupling). Note that if E88 is changed, E87 and E85 must also be changed. Also, see E90.	No jumper

E89: Amplifier-Supplied Switch Pull-Up Enable

E Point & Physical Layout	Location	Description	Default
E89 	F2	Jump pin 1 to 2 to use A+15V on J8 (JMACH1) pin 59 as supply for input flags. Remove jumper to use A+15V/OPT+V from J7 pin 59 as supply for input flags. **Note:** This jumper setting is only relevant if E90 connects pin 1 to 2	Jumper installed

E90: Host-Supplied Switch Pull-Up Enable

E Point & Physical Layout	Location	Description	Default
E90 	F2	Jump pin 1 to 2 to use A+15V from J8 pin 59 as supply for input flags (E89 ON) {flags should be tied to AGND} or A+15V/OPT+V from J8 pin 11 as supply for input flags (E89 OFF) {flags should be tied to separate 0V reference}. Jump pin 2 to 3 to use +12V from PC bus connector P1-pin B09 as supply for input flags {flags should be tied to GND}. Also, see E85, E87, E88 and PMAC Opto-isolation diagram.	1-2 Jumper installed

E91 - E92: Bus Base Address Select (High Bits)

E Point & Physical Layout	Location	Description	Default
E91 E92 	C3	E91 - Bit 11 PC bus base address E92 - Bit 10 PC bus base address ON = 0 OFF = 1	Jumper installed
These jumpers work with E66 - E71 to set the base address of PMAC-Lite on the PC bus. See PMAC-Lite PC Bus Addressing below for details on how to set these jumpers.			

E93 - E94: Reset from Bus by Software Enable

E Point & Physical Layout	Location	Description	Default
E93 	C3	Jump 1-2 to provide hardware reset of PMAC-Lite under the software control of the host-PC. PMAC-Lite will power up and stay in the reset state until PC software writes 40 HEX to Base +12. PMAC-Lite can be put in reset state by PC writing 40 HEX to Base +10 Remove jumper to disable this function Only one of E39, E93, E94 should be ON at the same time	No jumper
E94 	C3	Jump 1-2 to provide hardware reset of PMAC-Lite under the software control of the host-PC. PMAC-Lite will power up in Normal mode. PMAC-Lite can be put in reset state by PC writing 40 HEX to Base +12. PMAC-Lite can be released from reset state by PC writing 40 HEX to Base+10 Remove jumper to disable this function Only one of E39, E93, E94 should be ON at the same time	No jumper

E98: DAC/ADC Clock Frequency Control

E Point & Physical Layout	Location	Description	Default
E98 	E3	Jump 1-2 to provide a 2.45 MHz DCLK signal to DACs and ADCs Jump 2-3 to provide a 1.22 MHz DCLK signal to DACs and ADCs. Important for high accuracy A/D conversion on ACC-28.	1-2 Jumper installed
Note: This also divides the phase and servo clock frequencies in half. See E29-E33, E3-E6, I10			

E100: Output Flag Supply Select

E Point & Physical Layout	Location	Description	Default
E100 	F1	Jump pin 1 to 2 to apply analog supply voltage A+15V to U54 flag output driver IC. Jump pin 2 to 3 to apply flag supply voltage OPT+V to U54 flag output driver IC.	1-2 Jumper installed

E101 – E102: Output Flag Supply Voltage Configure

E Point & Physical Layout	Location	Description	Default
E101  	F1	***CAUTION*** The jumper setting must match the type of driver IC, or damage to the IC will result. Jump pin 1 to 2 to apply +V (12V to 24V) to pin 10 of U54 (should be ULN2803A for sink output configuration) for AENA1-4 and EQU1-4 flag outputs. Jump pin 2 to 3 to apply AGND to pin 10 of U54 (should be UDN2981A for source output configuration) for AENA1-4 and EQU1-4 flag outputs.	1-2 Jumper installed
E102  	F1	***CAUTION*** The jumper setting must match the type of driver IC, or damage to the IC will result. Jump pin 1 to 2 to AGND to pin 9 of U54 (should be ULN2803A for sink output configuration) for AENA1-4 and EQU1-4 flag outputs. Jump pin 2 to 3 to apply +V (12V to 24V) to pin 9 of U54 (should be UDN2981A for source output configuration) for AENA1-4 and EQU1-4 flag outputs.	1-2 Jumper installed

E103: Watchdog Disable Jumper

E Point & Physical Layout	Location	Description	Default
E103  	A1	Jump pin 1 to 2 to disable Watchdog timer (for test purposes only). Remove jumper to enable Watchdog timer.	No jumper installed

E106: Firmware Reload Enable

E Point & Physical Layout	Location	Description	Default
E106 	A2	Remove jumper for normal operation. Jump pin 1 to 2 to lock card in reset state for programming of on-board logic (for factory use only). Jump pin 2 to 3 to reload firmware through serial or bus port on power-up/reset.	No jumper installed

E110: Expansion Port Configuration

E Point & Physical Layout	Location	Description	Default
E110 	B2	Jump pin 1 to 2 to bring address line BA04 to JEXP pin 31 to support interface to ACC-24P2 board Jumper pin 2 to 3 to bring chip select line CS02/ to JEXP pin 31	1-2 jumper installed

HOST PC-AT I/O ADDRESS MAP

Hex Range	Dec Range	Usage
000-01F	0-31	DMA Controller 1 8237A-5
020-03F	32-63	Interrupt Controller 1 8259A
040-05F	64-67	Timer 8254-2
060-06F	96-111	8042 (Keyboard)
070-07F	112-127	Real-time clock, NMI mask
080-09F	128-159	DMA Page Registers
0A0-0BF	160-191	Interrupt Controller 2 8259A
0C0-0DF	192-223	DMA Controller 2 8237A-5
0F0-0FF	240-255	Math CO processor
1F0-1F8	496-504	Fixed Disk
200-20F	512-527	Game Control
210-217	528-535	Expansion Unit (usually open)
278-27F	632-639	Parallel Printer: LPT2
2B0-2DF	688-735	Alternate EGA
2F8-2FF	760-767	Asynchronous Common: COM2
300-31F	768-799	Prototype Card (usually open)
360-36F	864-879	PC Network
378-37F	888-895	Parallel Printer: LPT1
380-38F	896-911	SDLC Communications 2
390-393	912-915	Cluster
3A0-3A9	928-937	SDLC Communications 1
3B0-3BF	944-959	IBM Monochrome Display/Printer
3C0-3CF	960-975	Enhanced Graphics Adapter
3D0-3DF	976-991	Color/Graphics
3F0-3F7	1000-1015	Diskette Controller
3F8-3FF	1016-1023	Asynchronous Common.: COM1
x2E1		GPIB Adapter
x390-x393		Cluster Adapter

Contention is exhibited by:
1) Total Malfunction.
2) Partial Function, Input O.K., Output bad or vice versa.
3) Intermittent operation.

BUS ADDRESS JUMPER SETUP

Jumpers E91, E92, E66, E67, E68, E69, E70, and E71 on the PMAC-Lite determine the base address of the card in the I/O space of the host PC's expansion bus. Together, they form a binary number that specifies the 16 consecutive addresses on the bus where the card can be found.

The jumpers form the base address in the following fashion:

Jumper	E91	E92	E66	E67	E68	E69	E70	E71
Bit #	11	10	9	8	7	6	5	4
Dec Value	2048	1024	512	256	128	64	32	16
Hex Value	800	400	200	100	80	40	20	10

If a jumper is ON, the value it contributes to the base address is ZERO.

If a jumper is OFF, the value it contributes to the base address is given in the table above.

On the PMAC-Lite, the jumpers are physically arranged in the same order they are presented in the above table.

From Jumper Configuration To Address

To determine the address specified by a given jumper configuration, use the following formula:

(Decimal)
Address = 2048*E91 + 1024*E92 + 512*E66 + 256*E67 + 128*E68 + 64*E69 + 32*E70 + 16*E71
(Hexadecimal)
Address = $800*E91 + $400*E92 + $200*E66 + $100*E67 + $80*E68 + $40*E69 + $20*E70 + $10*E71
In each case, Exx = 1 if the jumper is OFF; Exx = 0 if the jumper is ON.

Example: On a PMAC card, the jumpers are in the following configuration:

E91	**E92**	**E66**	**E67**	**E68**	**E69**	**E70**	**E71**
ON	ON	OFF	OFF	ON	ON	ON	ON

The address can be computed as:

Decimal Address = 0 + 0 + 512 + 256 + 0 + 0 + 0 + 0 = 768
Hex Address = 0 + 0 + $200 + $100 + 0 + 0 + 0 + 0 = $300

From Address to Jumper Configuration

Once an I/O address on the PC expansion port has been selected, the following procedure can be used for setting the address jumpers.

1. Convert the address to a 3-digital hexadecimal value ($000 to $FFF, representing 0 to 4095). If the value does not fit in this range, you will not be able to set PMAC for this address. Make sure the last digit is 0; only addresses divisible by 16 are permitted as PMAC base addresses.
2. Take the first hex digit and convert it to binary. The binary digits represent bits 11 through 8 of the base address. Assign each binary digit to jumpers as follows:

Bit #	11(MSB)	10	9	8(LSB)
Jumper	E91	E92	E66	E67
Digit Value	8	4	2	1
Setting for 1	OFF	OFF	OFF	OFF
Setting for 0	ON	ON	ON	ON

3. Take the second hex digit and convert it to binary. The binary digits represent bits 7 through 4 of the base address. Assign each binary digit to jumpers as follows:

Bit #	7(MSB)	6	5	4(LSB)
Jumper	E68	E69	E70	E71
Digit Value	8	4	2	1
Setting for 1	OFF	OFF	OFF	OFF
Setting for 0	ON	ON	ON	ON

Example 1: You wish to set up the card to be at base address 992 decimal on the PC expansion bus.

1. 992 decimal is equal to 3E0 hexadecimal.
2. The first digit of 3 is binary 0011. This sets E91 ON, E92 ON, E66 OFF, E67 OFF.
3. The second digit of E is binary 1110. This sets E68 OFF, E69 OFF, E70 OFF, E71 ON.

Example 2: You wish to set up the card to be at base address 528 decimal on the PC expansion bus.

1. 528 decimal is equal to 210 hexadecimal.
2. The first digit of 2 is binary 0010. This sets E91 ON, E92 ON, E66 OFF, E67 ON.
3. The second digit of E is binary 0001. This sets E68 ON, E69 ON, E70 ON, E71 OFF.

Example 3: You wish to set up the card to be at base address 544 decimal on the PC expansion bus.

1. 544 decimal is equal to 220 hexadecimal.
2. The first digit of 2 is binary 0010. This sets E91 ON, E92 ON, E66 OFF, E67 ON.
3. The second digit of E is binary 0010. This sets E68 ON, E69 ON, E70 OFF, E71 ON.

MATING CONNECTORS

This section lists several options for each connector. Choose an appropriate one for your application.

J1 (JDISP)/Display Port

1. Two 14-pin female flat cable connector Delta Tau P/N 014-R00F14-0K0 T&B Ansley P/N 609-1441
2. 171-14 T&B Ansley standard flat cable stranded 14-wire
3. Phoenix varioface modules type FLKM14 (male pins) P/N 22 81 02 1

J2 (JPAN)/Control Panel Port

1. Two 26-pin female flat cable connector Delta Tau P/N 014-R00F26-0K0 T&B Ansley P/N 609-2641
2. 171.26.T&B Ansley standard flat cable stranded 26-wire
3. Phoenix varioface module type FLKM 26 (male pins) P/N 22 81 05 0

J3 (JTHW)/Multiplexer Port

1. Two 26-pin female flat cable connector Delta Tau P/N 014-R00F26-0K0 T&B Ansley P/N 609-2641
2. 171-26 T&B Ansley standard flat cable stranded 26-wire
3. Phoenix varioface module type FLKM 26 (male pins) P/N 22 81 05 0

J4 (JRS232)/RS232 Serial Communications

1. Two 10-pin female flat cable connector Delta Tau P/N 014-R00F10-0K0 T&B Ansley P/N 609-1041
2. 171-10 T&B Ansley standard flat cable stranded 10-wire
3. Phoenix varioface module type FLKM 10 (male pins) P/N 22 81 01 8

J4A (JRS422)/RS422 Serial Communications

1. Two 26-pin female flat cable connector Delta Tau P/N 014-R00F26-0K0 T&B Ansley P/N 609-2641
2. 171-26 T&B Ansley standard flat cable stranded 26-wire
3. Phoenix varioface module type FLKM 26 (male pins) P/N 22 81 05 0

J5 (JOPT)/General-Purpose I/O

1. Two 34-pin female flat cable connector Delta Tau P/N 014-R00F34-0k0 T&B Ansley P/N 609-3441
2. 171-34 T&B Ansley standard flat cable stranded 34-wire
3. Phoenix varioface module type FLKM 34 (male pins) P/N 22 81 06 3

J6 (JXIO)/Auxiliary Port

1. Two 10-pin female flat cable connector Delta Tau P/N 014-R00F10-0K0 T&B Ansley P/N 609-1041
2. 171-10 T&B Ansley standard flat cable stranded 10-wire
3. Phoenix varioface module type FLKM 10 (male pins) P/N 22 81 01 8

J7 (JS1)/A-D Inputs

1. Two 16-pin female flat cable connector Delta Tau P/N 014-R00F16-0K0 T&B Ansley P/N 609-1641
2. 171-16 T&B Ansley standard flat cable stranded 16-wire
3. PHOENIX varioface module type FLKM 16 (male pins) P/N 22 81 03 4

J8 (JEQU)/Position Compare

1. Two 10-pin female flat cable connector Delta Tau P/N 014-R00F10-0K0 T&B Ensley P/N 609-1041
2. 171-10 T&B Ansley standard flat cable stranded 10-wire
3. Phoenix varioface module type FLKM 10 (male pins) P/N 22 81 01 8

J9 (JEXP)/Expansion Port

1. Two 50-pin female flat cable connector Delta Tau P/N 014-R00F50-0K0 T&B Ansley P/N 609-5041
2. 171-50 T&B Ansley standard flat cable stranded 50-wire
3. Phoenix varioface module type FLKM 50 (male pins) P/N 22 81 08 9 used for daisy chaining acc-14 I/0, -23 A and D connectors -24 expansion

J11 (JMACH1)/First Machine Connector

1. Two 60-pin female flat cable connector Delta Tau P/N 014-R00F60-0K0 T&B Ansley P/N 609-6041 available as ACC 8P or 8D
2. 171-60 T&B Ansley standard flat cable stranded 60-wire
3. Phoenix varioface module type FLKM 60 (male pins) P/N 22 81 09 2

Note

Normally, J11 is used with accessory 8P or 8D with Option P, which provides complete terminal strip fan-out of all connections.

P1 (PC Bus)

One 62-pin card edge connector with solder pierced eyelets Delta Tau P/N 014-000F62-SCO Viking P/N 3KH 31/9 JN12 card edge connector pierced solder eyelets.

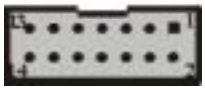
P2 (AT Bus)

One 36-pin card edge connector with solder pierced eyelets Delta Tau P/N 014-000 F36-SCO Viking P/N 3KH 18/9 JN12 card edge connector pierced solder eyelets.

CONNECTOR PINOUTS

J1 (JDISP): Display Port Connector

J1 JDISP (14-Pin Connector)



Front View

Pin #	Symbol	Function	Description	Notes
1	VDD	Output	+5V Power	Power Supply Out
2	VSS	Common	PMAC Common	
3	RS	Output	Read Strobe	TTL Signal Out
4	VEE	Output	Contrast Adjust VEE	0 to+5Vdc *
5	E	Output	Display Enable	High is Enable
6	R/W	Output	Read or Write	TTL Signal Out
7	DB1	Output	Display Data1	
8	DB0	Output	Display Data0	
9	DB3	Output	Display Data3	
10	DB2	Output	Display Data2	
11	DB5	Output	Display Data5	
12	DB4	Output	Display Data4	
13	DB7	Output	Display Data7	
14	DB6	Output	Display Data6	

The JDISP connector is used to drive the 2-line x 24-character (Acc-12), 2 x 40 (Acc-12A) LCD, or the 2 x 40 vacuum fluorescent (Acc 12C) display unit. The DISPLAY command may be used to send messages and values to the display.

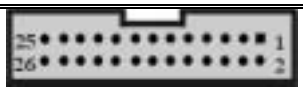
* **Note**; Controlled by potentiometer R1

See Also:

Program Commands: Display
Accessories; ACC-12, 12A, 12C, ACC16D
Memory Map: Y:$0780 - $07D1

J2 (JPAN): Control Panel Port Connector

J2 JPAN (26-Pin Connector)



Front View

Pin #	Symbol	Function	Description	Notes
1	+5V	Output	+5V Power	For remote panel
2	GND	Common	PMAC Common	
3	FPD0/	Input	Motor/C.S. Select Bit 0	Low is TRUE
4	JOG-/	Input	JOG IN - DIR.	Low is "JOG –"
5	FPD1/	Input	Motor/C.S. Select Bit 1	Low is TRUE
6	JOG+/	Input	Jog In + Dir.	Low is "JOG +"
7	PREJ/	Input	Return to Prejog Position	Low is "RETURN" Equiv to "J=" CMD
8	STRT/	Input	Start Program Run	Low is "START" Equiv to "R" CMD
9	STEP/	Input	Step through Program	Low is "STEP" Equiv to "S" OR "Q"
10	STOP/	Input	Stop Program Run	Low is "STOP" Equiv to "A"
11	HOME/	Input	Home Search Command	Low is "GO HOME" Equiv to "HM"
12	HOLD/	Input	Hold Motion	Low is "HOLD" Equiv to "H"
13	FPD2/	Input	Motor/C.S. Select Bit 2	Low is TRUE
14	FPD3/	Input	Motor/C.S. Select Bit 3	Low is TRUE
15	INIT/	Input	Reset PMAC	Low is "RESET" Equiv to "$$$"
16	HWCA	Input	Handwheel Enc. A Channel	5V TTL SQ. pulse must use E23 (CHA2)
17	IPLD/	Output	In Position Ind. (C.S.)	Low Lights LED
18	BRLD/	Output	Buffer Request Ind.	Low Lights LED
19	ERLD/	Output	Fatal Follow Err (C.S.)	Low Lights LED
20	WIPER	Input	Feed Pot Wiper	0 to +10V input must use E72, E73 (CHA4)
21	(SPARE)	N.C.		
22	HWCB	Input	Handwheel Enc. B Channel	5V TTL SQ. pulse must use E22 (CHB2)
23	F1LD/	Output	Warn Follow Err (C.S.)	Low Lights LED
24	F2LD/	Output	Watchdog Timer	Low Lights LED
25	+5V	Output	+5V Power	For remote panel
26	GND	Common	PMAC Common	

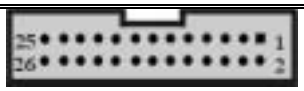
The JPAN connector can be used to connect the Accessory 16 (Control Panel), or customer-provided I/O, to the PMAC, providing manual control of PMAC functions via simple toggle switches. If the automatic control panel input functions are disabled (I2=1), the inputs become general-purpose TTL inputs, and the coordinate system (C.S.) specific outputs pertain to the *host*-addressed coordinate system.

See Also:

Control panel inputs, Accessories: ACC-16, ACC-39
I-variables: I2, Ixx06

J3 (JTHW): Multiplexer Port Connector

J3 JTHW (26-Pin Connector)



Front View

Pin #	Symbol	Function	Description	Notes
1	GND	Common	PMAC Common	
2	GND	Common	PMAC Common	
3	DAT0	Input	Data-0 Input	Data input from multiplexed accessory
4	SEL0	Output	Select-0 Output	Multiplexer select output
5	DAT1	Input	Data-1 Input	Data input from multiplexed accessory
6	SEL1	Output	Select-1 Output	Multiplexer select output
7	DAT2	Input	Data-2 Input	Data input from multiplexed accessory
8	SEL2	Output	Select-2 Output	Multiplexer select output
9	DAT3	Input	Data-3 Input	Data input from multiplexed accessory
10	SEL3	Output	Select-3 Output	Multiplexer select output
11	DAT4	Input	Data-4 Input	Data input from multiplexed accessory
12	SEL4	Output	Select-4 Output	Multiplexer select output
13	DAT5	Input	Data-5 Input	Data input from multiplexed accessory
14	SEL5	Output	Select-5 Output	Multiplexer select output
15	DAT6	Input	Data-6 Input	Data input from multiplexed accessory
16	SEL6	Output	Select-6 Output	Multiplexer select output
17	DAT7	Input	Data-7 Input	Data input from multiplexed accessory
18	SEL7	Output	Select-7 Output	Multiplexer select output
19	N.C.	N.C.	No Connection	
20	GND	Common	PMAC Common	
21	BRLD/	Output	Buffer Request	Low is Buffer Request
22	GND	Common	PMAC Common	
23	IPLD/	Output	In Position	Low is In Position
24	GND	Common	PMAC Common	
25	+5V	Output	+5VDC Supply	Power supply out
26	INIT/	Input	PMAC Reset	Low is "RESET"

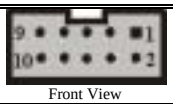
The JTHW multiplexer port provides eight inputs and eight outputs at TTL levels. While these I/O can be used in unmultiplexed form for 16 discrete I/O points, most users will utilize PMAC software and accessories to use this port in multiplexed form to greatly multiply the number of I/O that can be accessed on this port. In multiplexed form, some of the SELn outputs are used to select which of the multiplexed I/O are to be accessed.

See also:

I/O and Memory Map Y:$FFC1
Suggested M-variables M40 - M58
M-variable formats TWB, TWD, TWR, TWS
ACC-8D Opt 7, ACC-8D Opt 9, ACC-18, ACC-34x, NC Control Panel

J4 (JRS232) Serial Port Connector

J4 JRS232 (10-Pin Connector)



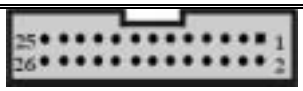
Front View

Pin #	Symbol	Function	Description	Notes
1	PHASE	Output	Phasing Clock	
2	DTR	Bidirect	Data Term Ready	Tied to "DSR"
3	TXD/	Input	Receive Data	Host transmit data
4	CTS	Input	Clear to Send	Host ready bit
5	RXD/	Output	Send Data	Host receive data
6	RTS	Output	Req. to Send	PMAC ready bit
7	DSR	Bidirect	Data Set Ready	Tied to "DTR"
8	SERVO	Output	Servo Clock	
9	GND	Common	PMAC Common	
10	+5V	Output	+5VDC Supply	Power supply out

The JRS232 connector provides the PMAC2-PC with the ability to communicate serially with an RS232 port. E107 and E108 must connect pins 1 and 2 to use this connector. This connector cannot be used for daisychain interconnection of multiple PMACs – the J4A RS422 connector must be used for daisychaining.

J4A (JRS422): Serial Port Connector

J4A JRS422 (26-Pin Connector)



Front View

Pin #	Symbol	Function	Description	Notes
1	CHASSI	Common	PMAC Common	
2	S+5V	Output	+5VDC Supply	Deactivated by “E8”
3	RD-	Input	Receive Data	Diff. I/O Low True= **
4	RD+	Input	Receive Data	Diff. I/O High True *
5	SD-	Output	Send Data	Diff. I/O Low True **
6	SD+	Output	Send Data	Diff. I/O High True *
7	CS+	Input	Clear to Send	Diff. I/O High True **
8	CS-	Input	CLEAR TO Send	Diff. I/O Low True
9	RS+	Output	Req. to Send	Diff. I/O High True **
10	RS-	Output	Req. to Send	Diff. I/O Low True *
11	DTR	Bidirect	Data Term Read	Tied to “DSR”
12	INIT/	Input	PMAC Reset	Low is “RESET”
13	GND	Common	PMAC Common	**
14	DSR	Bidirect	Data Set Ready	Tied to “DTR”
15	SDIO-	Bidirect	Special Data	Diff. I/O Low True
16	SDIO+	Bidirect	Special Data	Diff. I/O High True
17	SCIO-	Bidirect	Special CTRL.	Diff. I/O Low True
18	SCIO+	Bidirect	Special CTRL.	Diff. I/O High True
19	SCK-	Bidirect	Special Clock	Diff. I/O Low True
20	SCK+	Bidirect	Special Clock	Diff. I/O High True
21	SERVO-	Bidirect	Servo Clock	Diff. I/O Low True ***
22	SERVO+	Bidirect	Servo Clock	Diff. I/O High True ***
23	PHASE-	Bidirect	Phase Clock	Diff. I/O Low True ***
24	PHASE+	Bidirect	Phase Clock	Diff. I/O High True ***
25	GND	Common	PMAC Common	
26	+5V	Output	+5VDC Supply	Power supply out

The JRS422 connector provides the PMAC with the ability to communicate both in RS422 and RS232. In addition, this connector is used to daisy chain interconnect multiple PMACs for synchronized operation. Jumpers E107 and E108 must connect pins 2 and 3 to use this port.

* **Note:** Required for communications to an RS-422 host port

** **Note:** Required for communications to an RS-422 or RS-232 host port

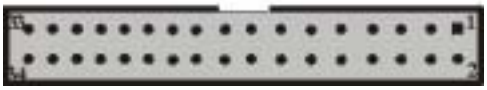
*** **Note:** Output on card @0; input on other cards. These pins are for synchronizing multiple PMACs together by sharing their phasing and servo clocks. The PMAC designated as card 0 (@0) by its jumpers E40-E43 outputs its clock signals. Other PMACs designated as cards 1-15 (@1-@F) by their jumpers E40-E43 take these signals as inputs. If synchronization is desired, these lines should be connected even if serial communications is not used.

See Also:

Serial Communications
Synchronizing PMAC to other PMACs

J5 (JOPTO): I/O Port Connector

J5 JOPTO (34-Pin Connector)



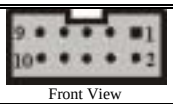
Front View

Pin #	Symbol	Function	Description	Notes
1	MI8	Input	Machine Input 8	Low is True
2	GND	Common	PMAC Common	
3	MI7	Input	Machine Input 7	Low is True
4	GND	Common	PMAC Common	
5	MI6	Input	Machine Input 6	Low is True
6	GND	Common	PMAC Common	
7	MI5	Input	Machine Input 5	Low is True
8	GND	Common	PMAC Common	
9	MI4	Input	Machine Input 4	Low is True
10	GND	Common	PMAC Common	
11	MI3	Input	Machine Input 3	Low is True
12	GND	Common	PMAC Common	
13	MI2	Input	Machine Input 2	Low is True
14	GND	Common	PMAC Common	
15	MI1	Input	Machine Input 1	Low is True
16	GND	Common	PMAC Common	
17	MO8	Output	Machine Output 8	Low-True (Sinking); High-True (Sourcing)
18	GND	Common	PMAC Common	
19	MO7	Output	Machine Output 7	“ “
20	GND	Common	PMAC Common	
21	MO6	Output	Machine Output 6	“ “
22	GND	Common	PMAC Common	
23	MO5	Output	Machine Output 5	“ “
24	GND	Common	PMAC Common	
25	MO4	Output	Machine Output 4	“ “
26	GND	Common	PMAC Common	
27	MO3	Output	Machine Output 3	“ “
28	GND	Common	PMAC Common	
29	MO2	Output	Machine Output 2	“ “
30	GND	Common	PMAC Common	
31	MO1	Output	Machine Output 1	“ “
32	GND	Common	PMAC Common	
33	+V	Input/ Output	+V Power I/O	+V = +5V to +24V +5V out from PMAC, +5 to +24V in from external source, diode isolation from PMAC
34	GND	Common	PMAC Common	

This connector provides means for eight general-purpose inputs and eight general-purpose outputs. Inputs and outputs may be configured to accept or provide either +5V or +24V signals. Outputs can be made sourcing with an IC (U11 to UDN2981) and jumper (E1 & E2) change. E7 controls whether the inputs are pulled up or down internally. Outputs are rated at 100mA per channel.

J6 (JXIO): Auxiliary I/O Port Connector

J6 JXIO (10-Pin Connector)



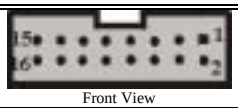
Front View

Pin #	Symbol	Function	Description	Notes
1	CHA1	Input	Enc. A CH. Pos.	From ACC-14 board
2	CHB1	Input	Enc. B CH. Pos.	From ACC-14 board
3	CHC1	Input	Enc. C CH. Pos.	From ACC-14 board
4	CHA3	Input	Enc. A CH. Pos.	From ACC-14 board
5	CHB3	Input	Enc. B CH. Pos.	From ACC-14 board
6	CHC3	Input	Enc. C CH. Pos.	From ACC-14 board
7	E63	Input	Interrupt IR4	From ACC-14 board
8	E59	Input	Interrupt IR5	From ACC-14 board
9	SCLK	Output	Encoder Clock	To ACC-24, ACC-8D OPT 8 boards
10	DCLK	Output	D to A, A to D Clock	To ACC-24 board

This connector is used for miscellaneous I/O functions related to expansion cards which are used with PMAC.

J7 (JS1): A/D Port Connector

J7 JS1 (16-Pin Header)



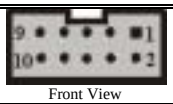
Front View

Pin #	Symbol	Function	Description	Notes
1	DCLK	Output	D to A, A to D Clock	DAC and ADC clock for Chan. 1, 2, 3, 4
2	BDATA1	Output	D to A Data	DAC data for Chan. 1, 2, 3, 4
3	ASEL0/	Output	Chan. Select Bit 0	Select for Chan. 1, 2, 3, 4
4	ASEL1/	Output	Chan. Select Bit 1	Select for Chan. 1, 2, 3, 4
5	CNVRT01	Output	A to D Convert	ADC convert sig. Chan. 1, 2, 3, 4
6	ADCIN1	Input	A to D Data	ADC data for Chan. 1, 2, 3, 4
7	OUT1/	Output	Amp. Enable/Dir	Amp. Enable/Dir for Chan. 1
8	OUT2/	Output	Amp. Enable/Dir	Amp. Enable/Dir for Chan. 2
9	OUT3/	Output	Amp. Enable/Dir	Amp. Enable/Dir for Chan. 3
10	OUT4/	Output	Amp. Enable/Dir	Amp. Enable/Dir for Chan. 4
11	HF41	Input	Amp. Fault	Amp Fault Input for Chan. 1
12	HF42	Input	Amp. Fault	Amp Fault Input for Chan. 2
13	HF43	Input	Amp. Fault	Amp Fault Input for Chan. 3
14	HF44	Input	Amp. Fault	Amp Fault Input for Chan. 4
15	+5V	Output	+5V Supply	Power supply out
16	GND	Common	PMAC Common	

ACC-28A/B connection; digital amplifier connection.

J8 (JEQU): Position-Compare Connector

J8 JEQU (10-Pin Connector)



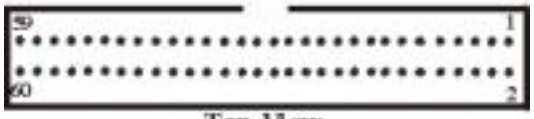
Front View

Pin #	Symbol	Function	Description	Notes
1	EQU1/	Output	Enc. 1 Comp-EQ	Low is True
2	EQU2/	Output	Enc. 2 Comp.-EQ	Low is True
3	EQU3/	Output	Enc. 3 Comp.-EQ	Low is True
4	EQU4/	Output	Enc. 4 Comp.-EQ	Low is True
5	AENA1/	Output	Amp. Enable 1	Low is True
6	AENA2/	Output	Amp. Enable 2	Low is True
7	AENA3/	Output	Amp. Enable 3	Low is True
8	AENA4/	Output	Amp. Enable 4	Low is True
9	A+V	Supply	Power Supply	+5V to +24V
10	AGND	Common	Analog Ground	

This connector provides the position-compare outputs and the amplifier enable outputs for the four servo interface channels. The board is shipped by default with a ULN2803A or equivalent open-collector driver IC. It may be replaced with UDN2891A or equivalent open-emitter driver (E101 and E102 must be changed; see **E-Point Descriptions** for details), or a 74ACT563 or equivalent 5V CMOS driver.

J11 (JMACH1): Machine Port Connector

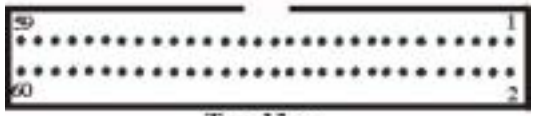
J11 JMACH1 (60-Pin Header)



Top View

Pin #	Symbol	Function	Description	Notes
1	+5V	Output	+5V Power	For encoders, 1
2	+5V	Output	+5V Power	For encoders, 1
3	GND	Common	Digital Common	
4	GND	Common	Digital Common	
5	CHC3	Input	Encoder C CH. POS	2
6	CHC4	Input	Encoder C CH. POS	2
7	CHC3/	Input	Encoder C CH. NEG	2,3
8	CHC4/	Input	Encoder C CH. NEG	2,3
9	CHB3	Input	Encoder B CH. POS	2
10	CHB4	Input	Encoder B CH. POS	2
11	CHB3/	Input	Encoder B CH. NEG	2,3
12	CHB4/	Input	Encoder B CH. NEG	2,3
13	CHA3	Input	Encoder A CH. POS	2
14	CHA4	Input	Encoder A CH. POS	2
15	CHA3/	Input	Encoder A CH. NEG	2,3
16	CHA4/	Input	Encoder A CH. NEG	2,3
17	CHC1	Input	Encoder C CH. POS	2
18	CHC2	Input	Encoder C CH. POS	2
19	CHC1/	Input	Encoder C CH. NEG	2,3
20	CHC2/	Input	Encoder C CH. NEG	2,3
21	CHB1	Input	Encoder B CH. POS	2
22	CHB2	Input	Encoder B CH. POS	2
23	CHB1/	Input	Encoder B CH. NEG	2,3
24	CHB2/	Input	Encoder B CH. NEG	2,3
25	CHA1	Input	Encoder A CH. POS	2
26	CHA2	Input	Encoder A CH. POS	2
27	CHA1/	Input	Encoder A CH. NEG	2,3
28	CHA2/	Input	Encoder A CH. NEG	2,3
29	DAC3	Output	Analog out Pos. 3	4
30	DAC4	Output	Analog out Pos. 4	4
31	DAC3/	Output	Analog out Neg. 3	4,5
32	DAC4/	Output	Analog out Neg. 4	4,5
33	AENA3/DIR3	Output	Amp-Ena/Dir. 3	6
34	AENA4/DIR4	Output	Amp-Ena/Dir. 4	6
35	FAULT3	Input	Amp-Fault 3	7
36	FAULT4	Input	Amp-Fault 4	7
37	+LIM3	Input	Neg. End Limit 3	8,9
38	+LIM4	Input	Neg. End Limit 4	8,9
39	-LIM3	Input	Pos. End Limit 3	8,9
40	-LIM4	Input	Pos. End Limit 4	8,9
41	HMFL3	Input	Home-Flag 3	10
42	HMFL4	Input	Home-Flag 4	10
43	DAC1	Output	Analog Out Pos. 1	4
44	DAC2	Output	Analog Out Pos. 2	4

J11 JMACH1 (60-Pin Header) (Continued)



Top View

Pin #	Symbol	Function	Description	Notes
45	DAC1/	Output	Analog Out Neg. 1	4,5
46	DAC2/	Output	Analog Out Neg. 2	4,5
47	AENA1/DIR1	Output	Amp-Ena/Dir. 1	6
48	AENA2/DIR2	Output	Amp-Ena/Dir. 2	6
49	FAULT1	Input	Amp-Fault 1	7
50	FAULT2	Input	Amp-Fault 2	7
51	+LIM1	Input	Neg. End Limit 1	8,9
52	+LIM2	Input	Neg. End Limit 2	8,9
53	-LIM1	Input	Pos. End Limit 1	8,9
54	-LIM2	Input	Pos. End Limit 2	8,9
55	HMFL1	Input	Home-Flag 1	10
56	HMFL2	Input	Home-Flag 2	10
57	FEFCO/	Output	Fe/Watchdog Out	Indicator/Driver
58	AGND	Input	Analog Common	
59	A+15V/OPT+V	Input	Analog +15V Supply	
60	A-15V	Input	Analog -15V Supply	

The J8 connector is used to connect PMAC to the first 4 channels (Channels 1, 2, 3, and 4) of servo amps, flags, and encoders.

***Note 1*:** In standalone applications, these lines can be used as +5V power supply inputs to power PMAC's digital circuitry. However, if a terminal block is available on your version of PMAC, it is preferable to bring the +5V power in through the terminal block.

***Note 2*:** Referenced to digital common (GND). Maximum of ± 12V permitted between this signal and its complement.

***Note 3*:** Leave this input floating if not used (i.e. digital single-ended encoders). In this case, jumper (E18 - 21, E24 - 27) for channel should hold input at 2.5V.

***Note 4*:** ± 10V, 10mA max, referenced to analog common (AGND).

***Note 5*:** Leave floating if not used; do not tie to AGND. In this case, AGND is the return line.

***Note 6*:** Functional polarity controlled by jumper(s) E17. Choice between AENA and DIR use controlled by Ix02 and Ix25.

***Note 7*:** Functional polarity controlled by variable Ix25. Must be conducting to 0V (usually AGND) to produce a '0' in PMAC software. Automatic fault function can be disabled with Ix25.

Note 8: Pins marked *-LIMn* should be connected to switches at the *positive* end of travel. Pins marked *+LIMn* should be connected to switches at the *negative* end of travel.

***Note 9*:** Must be conducting to 0V (usually AGND) for PMAC to consider itself not into this limit. Automatic limit function can be disabled with Ix25.

***Note 10*:** Functional polarity for homing or other trigger use of HMFLn controlled by Encoder/Flag Variable 2 (I902, I907, etc.) HMFLn selected for trigger by Encoder/Flag Variable 3 (I903, I908, etc.). Must be conducting to 0V (usually AGND) to produce a '0' in PMAC software.

TB1 (JPWR): Power Supply

Pin #	Symbol	Function	Description	Notes
1	GND	Common	Reference Voltage	
2	+5V	Input	Positive Supply Voltage	Supplies all PMAC digital circuits
3	+12V	Input	Positive Supply Voltage	Ref to digital GND
4	-12V	Input	Negative Supply Voltage	Ref to digital GND

This terminal block can be used to provide the input for the power supply for the circuits on the PMAC board when it is not in a bus configuration. When the PMAC2 is in a bus configuration, these supplies automatically come through the bus connector from the bus power supply; in this case, this terminal block should not be used.

If you desire to keep the optical isolation between the digital and analog circuits on PMAC, you must provide analog power (+/-12V to +/-15V & AGND) through the JMACH connector, instead of the bus connector or this terminal block.