U S E R ' S M A N U A L

VXI 8-BIT FIBER OPTIC I/O MODULE FAMILY

MODEL VX431C

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INTRODUCTION

This manual describes the operation and maintenance requirements of the C&H model VX431C 8-Bit Fiber Optic Input/Output (I/O) Family of VXI modules. These modules represent a subset of the test and data acquisition/control modules in the VME and VXI format provided by C&H.

Contained within this document is information on the physical and electrical specifications, installation and startup procedures, operating procedures, functional description, figures and diagrams required to adequately use this product.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1.0 GENERAL DESCRIPTION

The 8-bit fiber optic I/O module is a VXIbus compatible module that provides general purpose optical drive/receive capability.

1.1 PURPOSE OF EQUIPMENT

This module is well suited for applications within ATE systems, data acquisition systems, communications interface, hardware-in-the-loop simulation systems as well as development laboratory environments.

1.2 SPECIFICATIONS OF EQUIPMENT

1.2.1 Key Specifications

- Eight (8) Fiber Optic Driver and Eight (8) Receivers Capability
- Versatile triggering allows synchronization of multiple boards
- Immediate and Delayed Trigger (Data Latch) Capability
- VXI Interrupt Support
- Read back capability of all driver states
- Output drive enable/disable
- Industry standard [1]ST® connectors
- Optional output optical power adjustment

1.2.2 Electrical

The module only requires the +5V supply from the VXI backplane. The peak module current

INPUT CHARACTERISTICS:

Input Device:	HFBR-2412
Wavelength:	820 nanometers
Connection Repeatability:	within 0.2 dB (typical)

1.2.3 Mechanical

The mechanical dimensions of the module are in conformance with the VXIbus specification Rev 1.4 for single slot size 'C' modules. The nominal dimensions are 233.35 (9.187 in) high x 340 mm (13.386 in) deep.

1.2.3 Environmental

The environmental specifications of the module are:

Operating Temperature:	0°C to +55°C
Storage Temperature:	-40°C to +75°C
Humidity:	<95% without condensation

1.2.4 Bus Compliance

This module complies with the VXIbus Specification Revision 1.4 for C size register based modules.

Manufacturer ID:	FC1 hex
Model Code:	FF9 hex
Access Type:	Register Based
Addressing:	A16
Data Transfer:	D16
Sysfail:	not supported
Interrupts:	RORA

2.0 INSTALLATION

2.1 UNPACKING AND INSPECTION

In most cases the VX431C is individually sealed and packaged for shipment. Verify that there has been no damage to the shipping container. If damage exists then the container should be retained as it will provide evidence of carrier caused problems. Such problems should be reported to the carrier immediately as well as to C&H. If there is no damage to the shipping container, carefully remove the module from its box and plastic bag and inspect for any signs of physical damage. If damage exists, report immediately to C&H.

2.2 HANDLING PRECAUTIONS

The VX431C contains components that are sensitive to electrostatic discharge. When handling the module for any reason, do so at a static-controlled workstation, whenever possible. At a minimum, avoid work areas that are potential static sources, such as carpeted areas. Avoid unnecessary contact with the components on the module.

2.3 INSTALLATION

CAUTION: Read the entire User's Manual before proceeding with the installation and application of power.

Set or verify the module's logical address. Insert the module into the appropriate slot according to the desired priority. Apply power. If no obvious problems exist, proceed to communicate with the module as outlined in Section 4.0 (Operating Instructions).

2.4 PREPARATION FOR RESHIPMENT

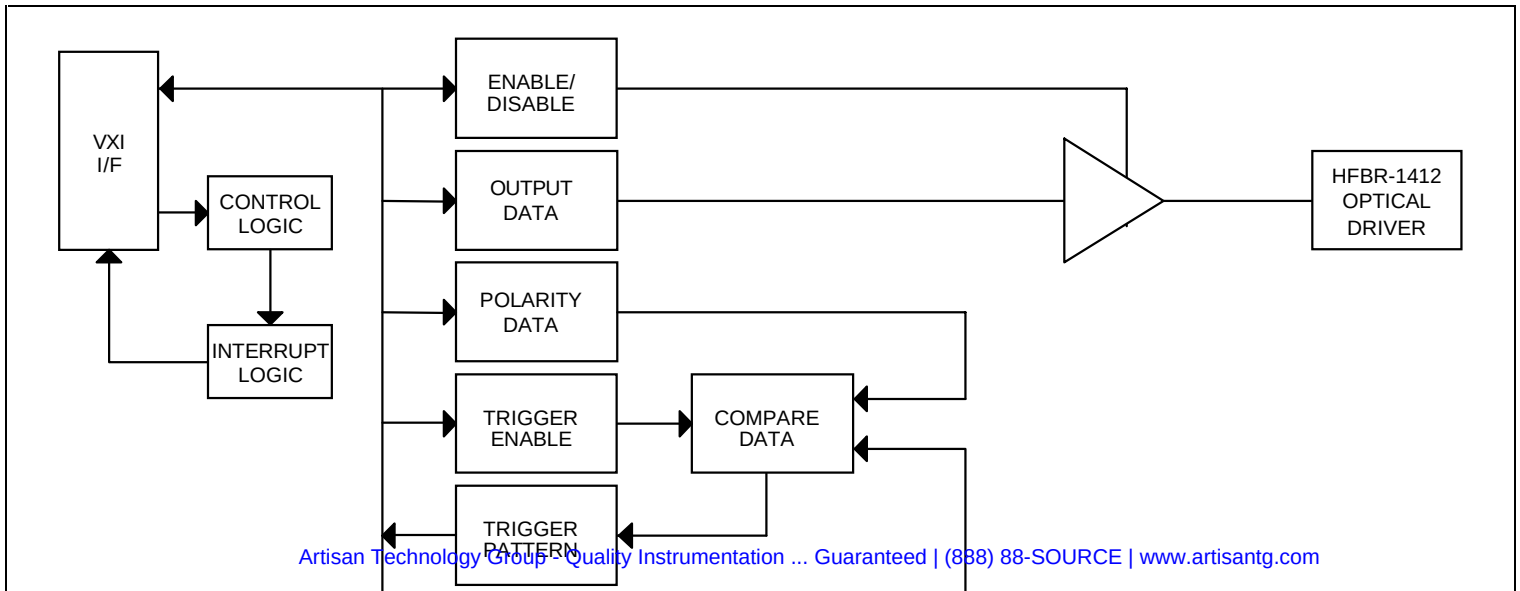
3.0 FUNCTIONAL DESCRIPTION

3.1 GENERAL

The VXI-compatible VX431C provides eight fiber optic drivers and eight fiber optic receivers. The module is configured, controlled, and statused through on-board registers accessible through the VXI backplane.

The digital output level of each optical driver is controlled by writing to an 8-bit output register. The input values of the optical receivers can be read on-the-fly or configured to latch their value on software command, on receipt of an external VXI trigger, or on an input change. Data can be latched immediately on receipt of a trigger or be latched after a programmed delay following a trigger. A trigger signal can also be generated on one of the P2 TTLTRG* lines. This versatile trigger and data hold capability allows a system of multiple cards to latch data synchronously across the backplane. A host interrupt can also be generated in conjunction with a trigger.

A functional block diagram of the module is shown in 1



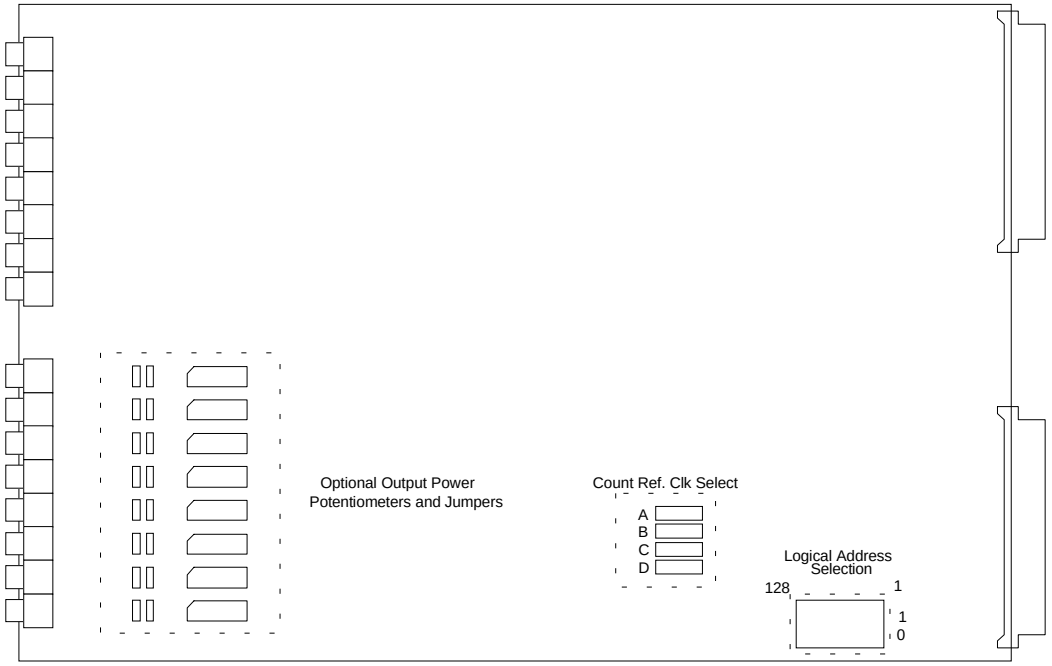


Figure 4. Hardware Configurable Controls

3.2.1 Logical Address Selection

An 8-bit logical address switch is provided to uniquely identify the module in the system.

3.2.2 Delay Count Reference Clock Selection

Jumpers A through D are used to select the divide value for the trigger delay count reference clock. The location of the jumpers is shown in Figure 4.5 The default setting is all jumper links out (1 µs period).

3.2.3 Output Power Adjustment

A potentiometer can be added by the user if the output optical power must be lowered. The

3.3 INDICATORS

Two LED indicators are provided on the front panel. One indicates access to the MODID, the other indicates the BOARD_SELECT status.

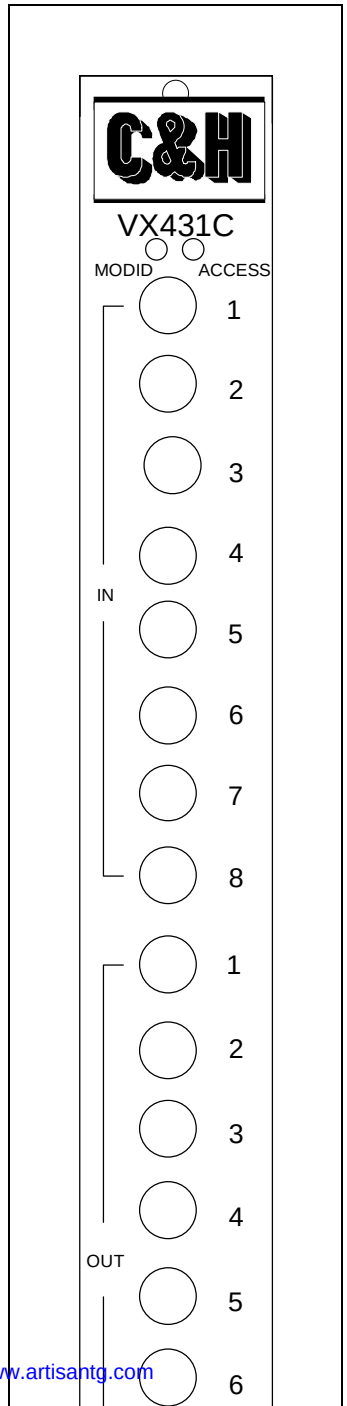
MODID: This front panel LED illuminates whenever the host processor applies the MODID signal to the slot the module is occupying.

BOARD SELECT: This front panel LED illuminates whenever the module is properly accessed by the host processor.

3.4 CONNECTORS

3.4.1 Front Panel Connectors

The fiber optic interface is provided through sixteen ST® type connectors. The connectors are arranged in two groups of eight. One group for the eight receivers, the other group for the eight drivers. The connectors are marked 1 through 8 corresponding to data bits 15 through 8, respectively. A detail of the front panel is shown in Figure 6.



3.4.2 Rear Connectors

3.4.2.1 P1 Connector

The P1 connector is configured in accordance with the VXI P1 specification (See Appendix B).

3.4.2.2 P2 Connector

3.5 CONFIGURATION REGISTERS

There are several types of registers used to configure and control the VX431C. The VXI configuration registers provide for control and status as required by the VXIbus specification. The General Status/Control register provides board-level control and status and the Port Register(s) provides port level control and status. An address map of the registers is shown in Table I.

Table I. VXI Register Address Map

Addr (Hex)	Register Write Description		Register Read Description	
Base + 0C	Write Port	N/A	Read Port	N/A
Base + 0A	Interrupt Control Register		Interrupt Control Register	
Base + 08	General Control Register		General Status Register	
Base + 06	VXI Unused Register		VXI Unused Register	
Base + 04	VXI Control Register		VXI Status Register	
Base + 02	VXI Read Only Register		VXI Device Type Register	
Base + 00	VXI Read Only Register		VXI ID Register	
Bit	15 08	07 00	15 08	07 00

3.5.1 VXI Configuration Registers

The VXI configuration registers contain basic information needed to configure a VXIbus system. The configuration information includes: manufacturer identification, product model code, device type, memory requirements, device status, and device control. The registers are briefly described below and are detailed in Figure **Error! Bookmark not defined.**.

VXI Identification (ID) Register (Base + 00h) - A read of this register provides manufacturer identification, device classification (i.e., register based), and the addressing mode (A16). A write to this register has no effect.

00	VXI ID															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used								Not Used							
Read	Device Class		Address Space		Manufacturer ID											

Device Class ⇒ Device Class (Register Based = binary 11)
Address Space ⇒ Address Space (A16 Only = binary 11)
Manuf. ID ⇒ Manufacturer Identification (C & H Technologies = hex FC1)

02	VXI DEVICE TYPE															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	RESERVED															
Read	1	1	1	1	Model Code											

Model Code ⇒ Model code (C&H Model VX431C = hex FF9)

04	VXI Status/Control															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Not Used															Rst
Read	0	MOD ID*	1	1	1	1	1	1	0	0	0	0	Rdy	Pass	1	1

Rst ⇒ Reset
MOD ID* ⇒ Module ID Status (0 = P2 MODID* line is selected (active-high))
Rdy ⇒ Ready
Pass ⇒ Self-test pass/fail indicator

Figure 7. VXI Configuration Registers

3.5.2 General Status/Control Register

This register provides control and status of the board-level trigger and comparison options. It also is used to select the function of the Port Register. Details are shown in Figure 8.

08	GENERAL STATUS/CONTROL															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	SBT	TE	-	-	TS	Trig Sel			Trig Count				-	Port Function		
Read	SBT	TE	-	TRG *	TS	Trig Sel			Trig Count				-	Port Function		

SBT ⇒ Software Board Trigger (1 = Generate trigger level, must be reset to 0)
TE ⇒ Output Trigger Enable (1 = Enable, 0 = Disable)
TRG* ⇒ Trigger Compare Status (0 = Trigger occurred, 1 = No trigger)
TS ⇒ Trigger Source (0 = Board Trigger, 1 = TTLTRGx*)
Trig Sel ⇒ TTLTRGx* Select

bit 10	9	8	
0	0	0	TTLTRG0*
0	0	1	TTLTRG1*
	:		
1	1	1	TTLTRG7*

Trig Count ⇒ Trigger Delay Count (Delay = Count Ref. Clk Period X Count Value)
Port Function ⇒ Port Function Select

bit 2	1	0	
0	0	0	Read Data / Write Data
0	0	1	Read Feedback / Write Data
0	1	0	Read Enable / Write Enable
0	1	1	Read Polarity / Write Polarity
1	0	0	Read Trig Enable / Write Trig Enable
1	0	1	Read Trig Pattern / Write Trig Enable
1	1	X	Read Status /Write Control

Figure 8. General Status/Control Register

3.5.3 Port Registers

Port Enable/Disable Register (010) This read/write register enables or disables the output drivers. A low (0) disables the output of the respective driver, a high (1) enables the output driver.

Polarity Register (011) This read/write register is used to determine the input level of a port that should generate a trigger and/or interrupt. A low (0) in a bit will cause a trigger when the input value goes low (absence of light). A high (1) will produce a trigger when the input value goes high (presence of light). A read of this registers provides feedback of the registers contents.

Trigger Enable Register (100) This read/write register is used to enable triggers on one or more bit level changes. A read of this registers provides feedback of the registers contents.

Trigger Pattern Register (101) A write to this register performs the same function as writing to the Trigger Enable Register. A read provides the bit pattern of the channel(s) that produced a trigger. For a trigger to be produced, the bit pattern must be enabled with the Trigger Enable function. A 1 in a bit indicates that a level change occurred on the corresponding input.

Port Status/Control Register (110 or 111) This read/write register controls and provides status of various trigger, latching, and read modes.

0A	**INTERRUPT CONTROL**															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	-			-	-	IRQ Sel			IRQ Vector/L. A.							
Read	-			IP*	-	IRQ Sel			IRQ Vector/L. A.							

IP* ⇒ Interrupt Pending (0 = Interrupt Pending, Read Only)

IRQ Sel ⇒ Interrupt Channel Select

bit 10	9	8	
0	0	0	Interrupt Disabled
0	0	1	IRQ1*
	.		
	.		
	.		
1	1	1	IRQ7*

IRQ Vector/L.A. ⇒ Interrupt Vector / Logical Address (For VXI compliant interrupts, set these bits equal to the

Func: 000	PORT DATA REGISTER															
Port	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**Not Used**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Output Data Pattern								Not Used							
Read	Input Bits Data Pattern								$FF							

On write - Data written is output to driver
On read - Data pattern read

Func: 001	PORT OUTPUT READBACK REGISTER															
Port	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**Not Used**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Output Data Pattern								Not Used							
Read	Latched Output Pattern								$FF							

Func: 010	PORT ENABLE/DISABLE REGISTER															
Port	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**Not Used**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Enable/Disable Output Driver Pattern								Not Used							
Read	Enable/Disable Pattern								$FF							

Func: 011	PORT POLARITY REGISTER															
Port	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**Not Used**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Polarity Pattern								Not Used							
Read	Polarity Pattern								$FF							

Func: 100	PORT TRIG ENABLE REGISTER															
Port	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**Not Used**							

Func: 11x	PORT STATUS/CONTROL REGISTER															
Port	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**Not Used**							
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	OT		IT		SPT	Not Used		HLD	Not Used							
Read	OT		IT		HS	Not Used		HLD	$FF							

OT ⇒ Output Trigger Function* (see below)

bit 15	14	Function
0	0	Output data normal
0	1	Output data on immediate trigger
1	0	Output data on delayed trigger
1	1	Not Used

IT ⇒ Input Trigger Function (see below)

bit 13	12	Function
0	0	Input data normal
0	1	Latch input data on immediate trigger
1	0	Latch input data on delayed trigger
1	1	Not Used

SPT ⇒ Software Port Trigger (a 1 generates a TTLTRGx* pulse (~100 ns))

HS ⇒ Hold Status (1 = data is being held)

HLD ⇒ Hold Mode (HMODE) (0 = hold disabled/reset, 1 = hold on trigger)

*Note: An immediate trigger produces a 50ns wide pulse. Data is output on the leading edge and input data is latched on the trailing edge.

Figure 10. Port Registers (2 of 2)

3.6 TRIGGER AND DATA LATCH FUNCTIONALITY

The VX431C provides a number of triggering and data latching capabilities. A functional diagram showing the operation and configuration settings is shown in Figure 11.

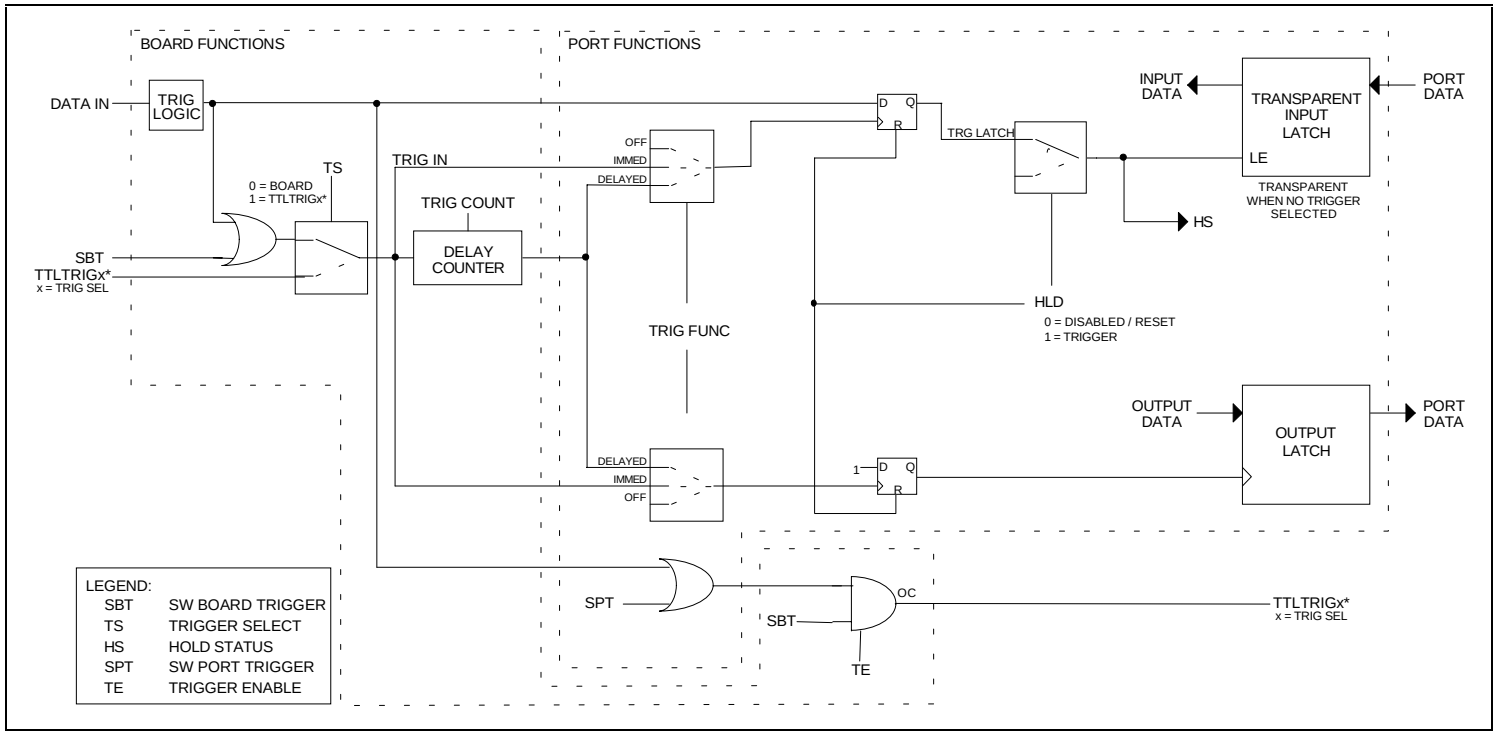


Figure 11. Trigger and Data Latch Functionality

3.6.1 Trigger Modes

A trigger can be caused by a high-to-low transition on the TTLTRGx* line on the VXI P2 connector, by software setting the board trigger (SBT) bit in the General Status/Control Register (Base + $08), or by front panel data signal. This TTLTRGx* or SBT may be applied immediately or delayed a programmed amount of time. The delay time is controlled by selecting the desired count period using jumpers A through D and by programming the Trigger Count value in the General Status/Control Register. The delay time is equal to the Trigger Count value multiplied by the clock period set using jumpers A-D as shown in Table **Error! Bookmark not defined.**. The default setting is all jumper links out (1 µs period). Note that the Trigger Count must be greater than zero to use any internal trigger. Also the trigger delay uses an asynchronous clock and, therefore, may be up to one Count Ref. Clock

be held. See Figure 10 for the possible settings.

3.6.3 Output Latch

Output data may be output to the front panel upon register write or on the occurrence of a trigger. A trigger may originate from a software operation, a VXI P2 TTLTRGx* line, or from the front panel. This capability allows data to be output to the front panel synchronously across all ports and across multiple VXI modules. See Figure 10 for the possible settings.

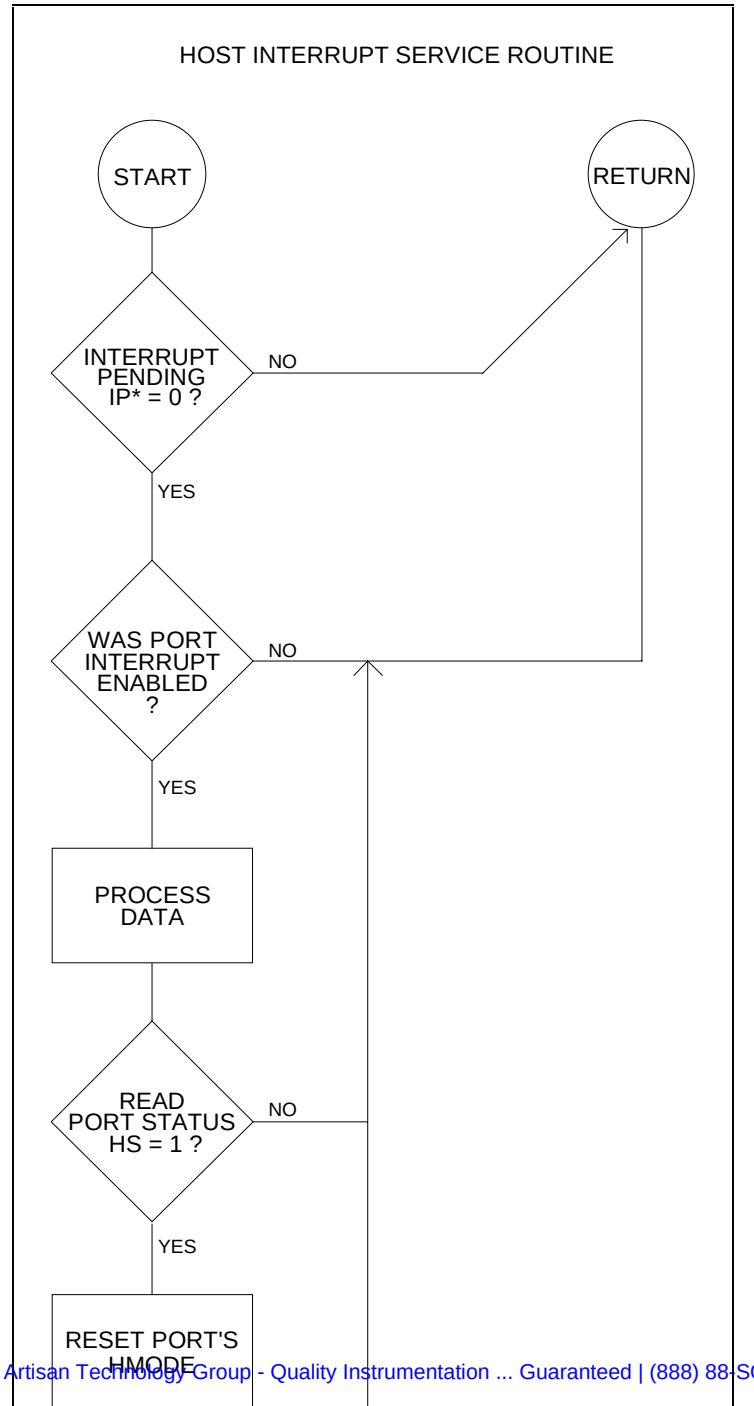
3.6.4 Data Comparison

When an input data change occurs, the input data is compared to the expected polarity (if trigger enable is set to 1). The expected polarity pattern is the pattern that was written to the port polarity register. The bit positions set to a 0 in the trigger enable pattern in the Port Trigger Enable Register are ignored during this comparison. If one or more bits match, the Trigger Status (TRG bit in the General Status/Control Register) is cleared (set to 0) and the bits positions failing the comparison are set to a 1 and saved in a separate register. This "fail bit" pattern is provided in the Trigger Pattern Register.

3.6.5 Interrupts

An interrupt is generated according to the Hold Mode (HMODE) in the Port Status/Control Register. If "hold on trigger" is selected, then an interrupt is generated when a data change occurs. Once an interrupt occurs, the interrupt is released by resetting (i.e., writing binary 0) to the HMODE in the Port Status/Control Register. The servicing process is flow charted in Figure 12.

The interrupt level and interrupt vector/logical address are programmed by writing to the Interrupt Control Register (Base +$0A) as detailed in Figure 9. Interrupts can be completely disabled by setting the interrupt level to 000. The level and vector are used for all interrupts generated by the module to the VXI bus. For VXI compliant interrupts, the interrupt



4.0 OPERATING INSTRUCTIONS

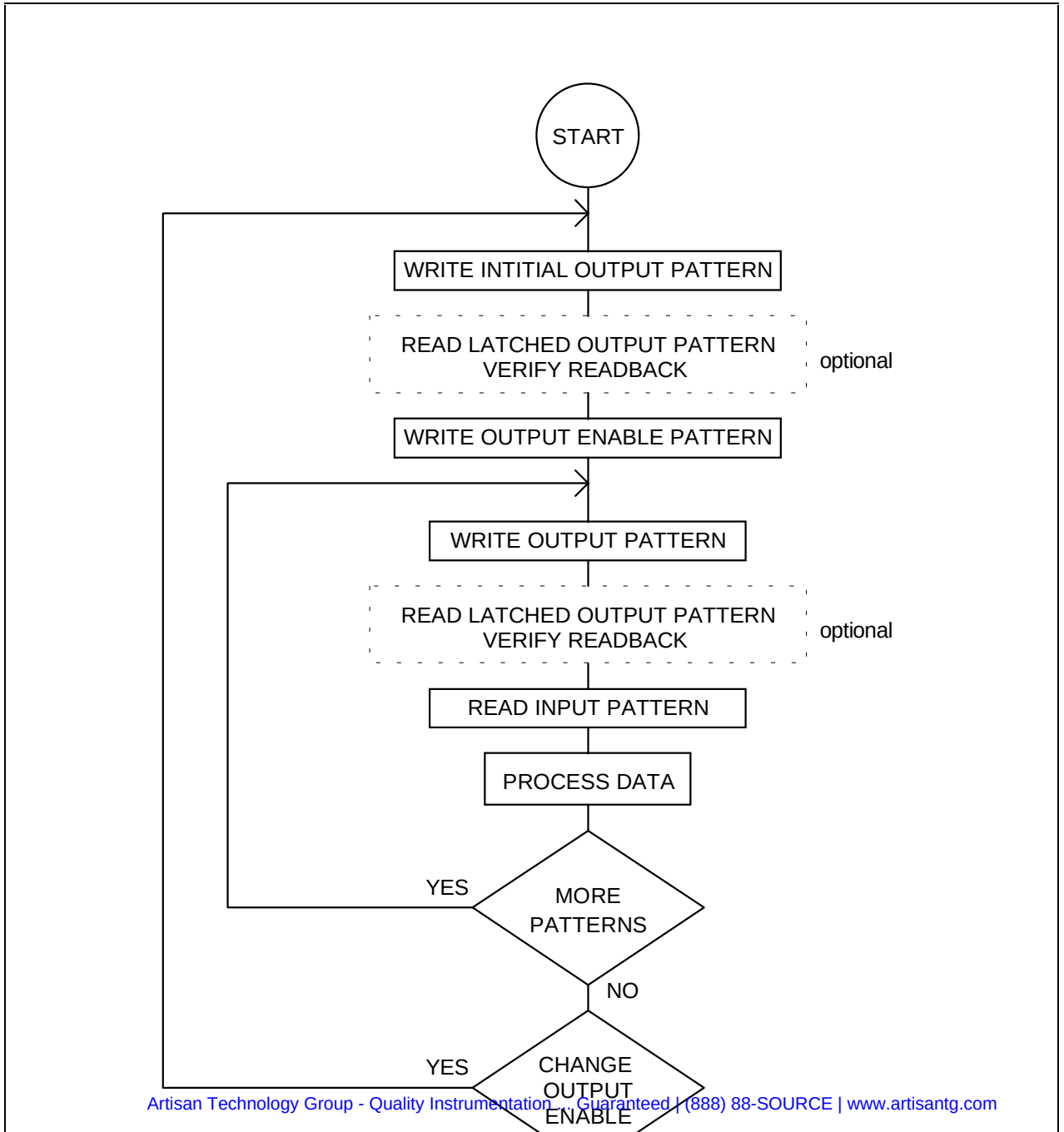
Prior to installation, the module's logical address must be set. The logical address has a range of 0 to 255. Any value within this range is valid, but care should be taken not to set the logical address the same as another module in the system. Position 1 on the switch (marked 128 on the shield) is the most significant bit and has a weighted value of 128 when the switch is in the off position (marked 1 on shield). Position 8 on the switch (marked 1 on the shield) is the least significant bit and has a weighted value of 1 when the switch is in the off position. The sum of the weighted values of all the switches in the off position (marked 1 on the shield) is the module's logical address. The VXI secondary address is the logical address divided by 8.

The default setting for the delay count reference clock period is 1 µs. This setting allows a programmable trigger delay of 1 to 15 µs. If a shorter delay is desired, remove the shield and position the jumper links according to Table **Error! Bookmark not defined.**.

After installation and power-up, configure the General Status/Control Register to the desired trigger and comparison operation and the Port Status/Control Register to the desired latch, hold, trigger, and interrupt modes. An example of accessing the various registers is shown below. The VXI Configuration Registers do not require any setup. The module is now ready for normal input/output operations. The typical program flow is shown in Figure 13.

C / LabWindows Register Access Example

```
static int  port0,cont,ad;

main()
{
int     ad;
int     stat_sel,data_sel,fb_sel,en_sel;
int     statin,datain,fbin,enin;

        ad          = 2;  /*  board Logical Address        */
        port0       = 12; /*  port register                */
        cont        = 8;  /*  general status/control       */
        stat_sel    = 7;  /*  port status/control function */
        data_sel    = 0;  /*  port data function           */
        fb_sel      = 1;  /*  port readback function       */
        en_sel      = 2;  /*  port enable/disable function */

        InitVXIlibrary ();

    /*  Set general control register to port status/control.  */
    /*  Write control and read status port registers.         */
        VXIoutReg (ad, cont, stat_sel);
        VXIoutReg (ad, port0, 0x0000);
        VXIinReg (ad, port0, &statin);

    /*  Set general control register to port enable register. */
    /*  Write and read the enable register.                   */
        VXIoutReg (ad, cont, en_sel);
        VXIoutReg (ad, port0, 0xFF00);
        VXIinReg (ad, port0, &enin);

    /*  Set general control register to port write data and   */
    /*  read feedback registers.                              */
    /*  Write and read the data register.                     */
        VXIoutReg (ad, cont, fb_sel);
        VXIoutReg (ad, port0, 0xAA00);
        VXIinReg (ad, port0, &fbin);

    /*  Set general control register to port write data and   */
    /*  read data registers.                                  */
```



5.0 MAINTENANCE

5.1 BUILT IN TEST AND DIAGNOSTICS

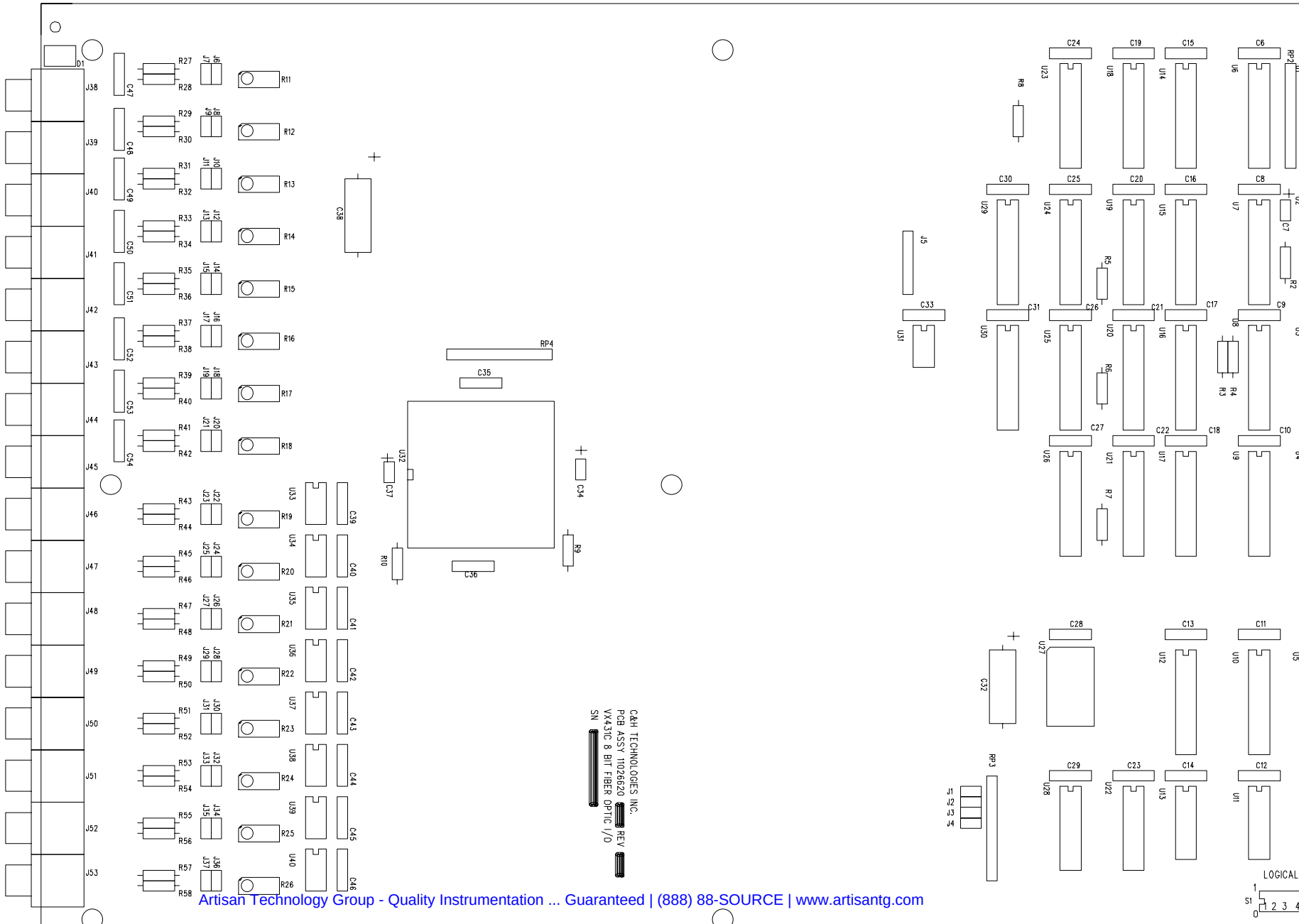
A simple diagnostic routine can be written that uses the read back capability of the modules to insure proper operation up to the driver devices.

5.2 TROUBLE ANALYSIS GUIDE

If a bus error or bus time-out error occurs, verify that the address and mode switch settings are properly set for the system access type. Verify correct program addressing and word size and check the system memory mapping strategy.

If bit errors occur, utilize the modules read back capability to verify the module's internal states. When diagnosing output problems, isolate the module from external loads by removing the connectors.

APPENDIX A - BOARD LAYOUT



APPENDIX B - CONNECTORS

PIN	C	B	A
1	D08	-	D00
2	D09	-	D01
3	D10	-	D02
4	D11	BG0IN*	D03
5	D12	BG0OUT*	D04
6	D13	BG1IN*	D05
7	D14	BG10UT*	D06
8	D15	BG2IN*	D07
9	GND	BG20UT*	GND
10	-	BG3IN*	-
11	-	BG3OUT*	-
12	SYSRESET*	-	DS1*
13	LWORD*	-	DS0*
14	AM5	-	WRITE*
15	-	-	-
16	-	AM0	DTACK*
17	-	AM1	-
18	-	AM2	-
19	-	AM3	-
20	-	GND	IACK*
21	-	-	IACKIN*
22	-	-	IACKOUT*
23	A15	GND	AM4
24	A14	IRQ7*	A07
25	A13	IRQ6*	A06
26	A12	IRQ5*	A05
27	A11	IRQ4*	A04
28	A10	IRQ3*	A03
29	A09	IRQ2*	A02
30	A08	IRQ1*	A01
31	+12 V	-	-12 V
32	+5 V	+5 V	+5 V

PIN	C	B	A
1	-	+5V	-
2	-	GND	-
3	-	-	-
4	-	-	GND
5	-	-	-
6	-	-	-
7	GND	-	-
8	-	-	-
9	-	-	-
10	GND	-	GND
11	-	-	-
12	-	GND	-
13	-	+5V	-
14	-	-	-
15	0	-	-
16	GND	-	GND
17	-	-	-
18	-	-	-
19	-	-	-
20	-	-	-
21	-	-	-
22	GND	GND	GND
23	TTLTRG1*	-	TTLTRG0*
24	TTLTRG3*	-	TTLTRG2*
25	GND	-	+5V
26	TTLTRG5*	-	TTLTRG4*
27	TTLTRG6*	-	TTLTRG6*
28	GND	-	GND
29	-	-	-
30	GND	-	MODID
31	-	GND	GND
32	-	+5V	-

Figure B-2. P2 Pin Configuration

NOTES

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