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SVME/DMV-179
Single Board Computer

Getting Started Manual

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Revision History

Rev	By	Date	Description
-	BJ	December 1999	First release. This document is associated with SVME/DMV-179 products manufactured using PWB # 310939-003 or later.
A	BJ	July 2000	Changed “Support for DY 4 Common Features” on page 1-5 and “Initiating the Power-Up Sequence” on page 3-21 because BI-mode is no longer supported. Corrected Table 2.5 on page 2-9. Changed “About Card Insertion Force” on page 3-3. Added Note and Table 3.8 on page 3-11. Corrected Table 4.2 on page 4-9. Corrected Figure A.1 on page A-4.
B	BJ	June 2001	Modified “Power Requirements” on page 2-9. Modified “Cable Requirements” on page 2-10 to include information on CBL-SBC-FP-000. Updated Chapter 3. Added more information to Chapter 4. Corrected “Changing the Card’s Base Address” on page 4-7. Corrected “Communicating over the VMEbus” on page 4-12. Removed Appendix A. See Chapter 2 of the Hardware User’s Manual for pinout information.
C	JP	February 2002	Updated “Configuring Jumpers” on page 2-3 with changes stemming from new board layout 310939-004, in particular the addition of E Jumpers E48 and E49 to control selection of the Permanent Alternate Boot Site (PABS) as the bootup source. Also added material describing operation of JTAG E Jumpers E55 and E56 to Table 2.1 on page 2-4.
D	BJ	January 2003	Added cross-reference to “Install the PMC Modules on the Basecard” on page 3-4. Updated DMV-179 Installation “Insert the Basecard in the Chassis” on page 3-5. Added note to “CBL-179-003 J2 (SCSI) Connector Pinouts” on page 3-12. Updated “Controlling the Power-Up Sequence” on page 3-20.

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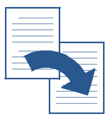
Preface

Purpose

This manual provides an overview of the many features of the SVME/DMV-179 Single Board Computer. After explaining the capabilities of the SVME/DMV-179, the manual provides the procedure for correctly installing and checking out the card's operation.

This manual is intended for the reader who has a technical understanding of hardware engineering fundamentals and a basic understanding of the VMEbus architecture.



Cross Reference

More in-depth technical information about the SVME/DMV-179 hardware is provided in the *SVME/DMV-179 Hardware User's Manual*, document number 809606, which is included in the documentation package.

Scope

This document contains the following chapters:

Chapter 1 - Product Overview. Provides general information about the features and functions of the SVME/DMV-179.

Chapter 2 - Pre-Installation Tasks. Discusses tasks that must be performed prior to installing the SVME/DMV-179 in a chassis. Provides information on jumper configurations, cabling, and power requirements.

Chapter 3 - Hardware Installation. Explains how to install the SVME/DMV-179 in a chassis and verify that it is operating correctly.

Chapter 4 - Card Communications. Explains how to determine the hardware and Foundation Firmware configuration of the card, how to run diagnostics, how to restore the SEEPROM and Foundation Firmware. Explains how to change the SVME/DMV-179's VME base address and how to communicate with other cards over the VMEbus.

Conventions used in the Documentation Package

This document and the accompanying documents in the documentation package use various icon conventions and abbreviations in order to make the documents clearer and easier to read. These conventions cover typography for such elements as sample software code and keystrokes, signal meanings, and graphical elements for important information such as warnings or cautions.

Typographic Conventions

Table 1 lists the typographical conventions used in the documentation package.

Table 1: Typographical Conventions

Item	Convention	Example
Keystrokes	Keys are listed as they appear on most keyboards, surrounded by < > marks. Combinations of keystrokes appear within a single set of < > brackets.	Type < Ctrl-Alt-C > to return to the previous menu. Type < Esc > to exit.
Filenames	Filenames are italicized.	Open the *es.h* file.
Directory names	Directory names show the full directory-path. The last directory in the path does not have a backslash following it.	Go to the c:\windows\temp\backup directory.
Monitor displays	Prompts and other monitor displays appear in a bold monospace font.	**`% mpp MC68040gnu >`**
Firmware Code	Firmware code, and any information you need to type in response to a prompt, appears in monospace font.	`% make -f Makefile.MC68040gnu`

Signal Conventions

Table 2 shows symbols which can follow a signal name. For example, the asterisk (*) is used with a VMEbus signal name, such as BERR*.

Table 2: Signal Conventions

Symbol	Description
*	The signal is active LOW and is connected to the VMEbus.
/	The signal is active LOW and is connected to the local bus only, and not directly to the VMEbus.
[no symbol]	The signal is active HIGH (with no indication as to whether the signal is connected to the VMEbus or local bus).
#	The signal is active LOW and is connected to the PCI bus.

Abbreviations

Table 3 lists the abbreviations used when describing the size of a memory device or a range of addresses.

Table 3: Abbreviations

Abbreviations	Description
1 Kbyte	1,024 bytes
1 Mbyte	1,024 Kbytes
1 Gbyte	1,024 Mbytes

Memory Addresses

Unless stated otherwise, all memory addresses are shown in hexadecimal notation.

Icons

The following icons are used throughout the documentation package:

Warning

The warning icon indicates procedures in the manual that, if not carried out, or if carried out incorrectly, could result in physical injury, cause electrical damage to equipment, or cause a non-recoverable corruption of data. Warnings include instructions on how to prevent such damage. Please observe warning icons and read the accompanying text completely before carrying out the procedure.

Caution

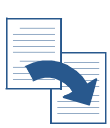
The caution icon indicates non-catastrophic incidents, complex practices or procedures which, if not observed, could result in damage to the hardware. Cautions include specific instructions for avoiding or minimizing these incidents.

Note

The note icon highlights exceptions and special information.

Tip

Tips provide extra information on the subject matter. This could include hints on how to use your current DY 4 card to its maximum potential.



Cross Reference

Cross references to other documents are used when discussing a subject that is fully addressed by another, more authoritative document. Cross references are also used for document chapters and sections.

Reference Documentation

Please refer to the CD-ROM included in the documentation package for additional reference information, supplied in Adobe® Acrobat®-readable format. Included on the CD-ROM are documents relating to the standard Foundation Firmware, a user's manual for the Universe PCI to VMEbus interface, and a helpful guide to using the VMEbus (among other things).

You'll also find copies of the relevant schematics and cable assembly drawings there.

Note

The CD-ROM provides a copy of the Adobe® Acrobat® 4.0 reader software, including the Acrobat® Search plug-in, to enable you to get the most out of your CD-ROM by enabling full-text searches of the information.

In addition, the *SVME/DMV-179 Hardware User's Manual*, document number 809606 (included in hard copy format in the documentation package binder), provides additional technical detail about the SVME/DMV-179.

Chapter 1

Product Overview

In this chapter...

This chapter discusses the following topics related to the SVME/DMV-179 Single Board Computer:

- ❑ general description;
- ❑ block diagram;
- ❑ Dy 4 common features supported;
- ❑ available ruggedization levels;
- ❑ environmental requirements;
- ❑ overview of supplied firmware;
- ❑ physical characteristics.

General Description

The SVME/DMV-179 continues the evolution of DY 4's industry-leading MIL/rugged line of PowerPC-based Single Board Computers (SBCs). Packed with features to satisfy the real-world requirements of defense/aerospace systems integrators, the SVME/DMV-179 is designed with performance, reliability, and ease of use in mind.

The SVME/DMV-179 introduces a full 64-bit architecture, a ground-breaking 48 Mbytes of direct memory-mapped, 64-bit wide Flash, and the DSP capabilities of AltiVec™ technology, all at a low power dissipation of only 17 Watts (typical). Providing high-performance synchronous DRAM combined with the high system integrity of Error Detection and Correction (EDAC), the SVME/DMV-179 is ready for the challenges of avionics, tactical ground vehicle, and rugged naval applications.

For retrofit and technology insertion applications, the SVME/DMV-179 offers a common I/O feature set and the option of pinout compatibility to earlier generations of DY 4 PowerPC SBCs. As a member of DY 4's continuously evolving stream of PowerPC SBCs, the SVME/DMV-179 supports the life-cycle model of successive technology insertions throughout a platform's life time.

Figure 1.1 illustrates the SVME/DMV-179 architecture.

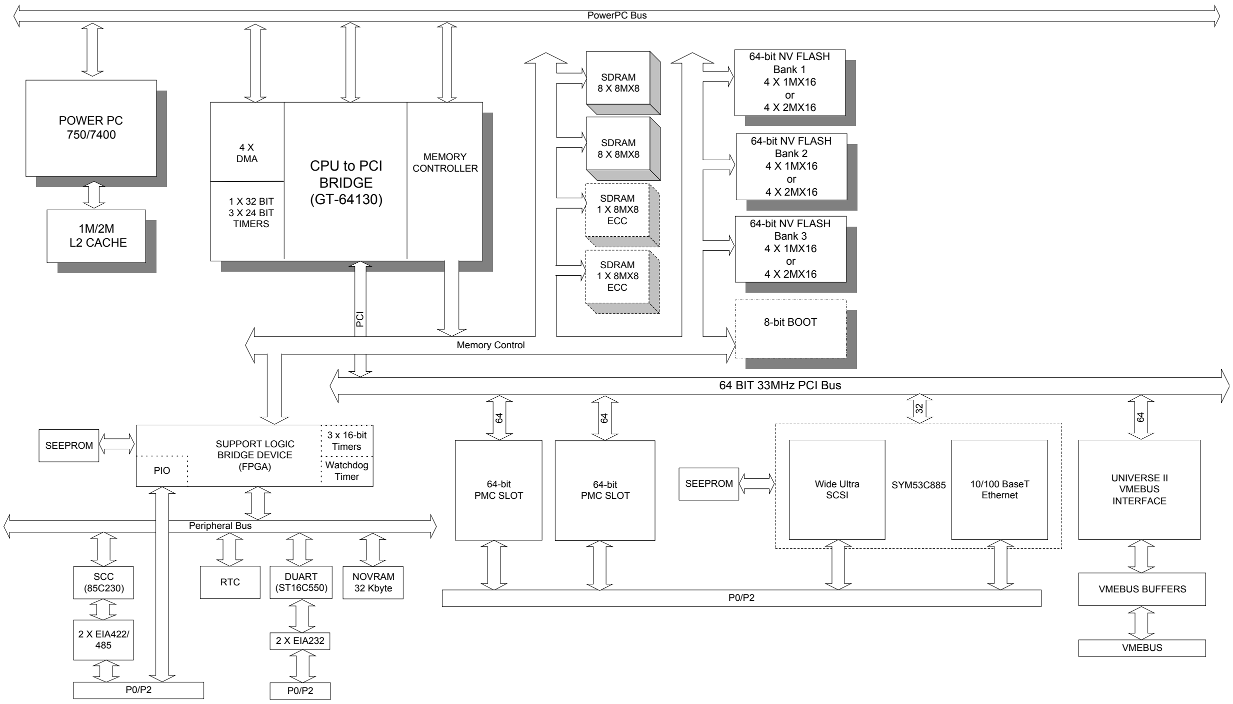


Figure 1.1 SVME/DMV-179 Functional Block Diagram

Cross Reference

Please refer to Chapter 1 of the *SVME/DMV-179 Hardware User's Manual,* document number 809606, for a detailed description of each of the functional blocks in the above diagram.

The SVME/DMV-179 provides a highly integrated, powerful PowerPC architecture in a single-slot solution with high processing performance, industry standard I/O, and the flexibility of user-specific I/O which traditionally required multiple cards.

The SVME/DMV-179's design features address the real-time, mission-critical demands of military and aerospace systems integrators with increased computing performance, self-test coverage and high functional density.

About PMC

PMC, an open industry-standard mezzanine module with a PCI interface, allows system designers to increase the SVME/DMV-179's functionality by utilizing standard DY 4 PMCs, available third party PMC products, or by developing their own PMC-based modules.

Support for DY 4 Common Features

The SVME/DMV-179 supports DY 4 Systems' common architecture feature set, including the capability of a compatible pinout with previous SVME/DMV-17X PowerPC products, a feature-rich VME64 VMEbus interface with Built-In-Test (BIT), read/write FIFOs, and Auto-ID. These features bring benefits in performance as well as supporting technology insertion, reducing program logistics and maintenance costs.

Tundra's Universe II interface chip provides a PCI to VMEbus bridge which implements all VMEbus interface functions with software-programmable features. Based on the popular SCV64, the Universe II device combines low-latency access to the VMEbus with high sustained throughputs. Additional Built-In-Test (BIT) hardware features verify correct operation to a high confidence level.

The Universe II internal FIFOs support write posting, enabling efficient interprocessor messaging thereby minimizing overhead in real-time software. Auto-ID allows the SVME/DMV-179 to be self-configuring, based on its slot position in the VME chassis. Geographical address inputs available as part of the VME64 extensions can be used for VMEbus base address configuration. These features allow users to:

- build high-performance multi-processor systems
- detect and isolate faults during operation
- minimize field maintenance and sparing logistics.

Physical Characteristics

Figure 1.2 shows the location of the major components and the mating connectors on the component side of the SVME/DMV-179 PWB.

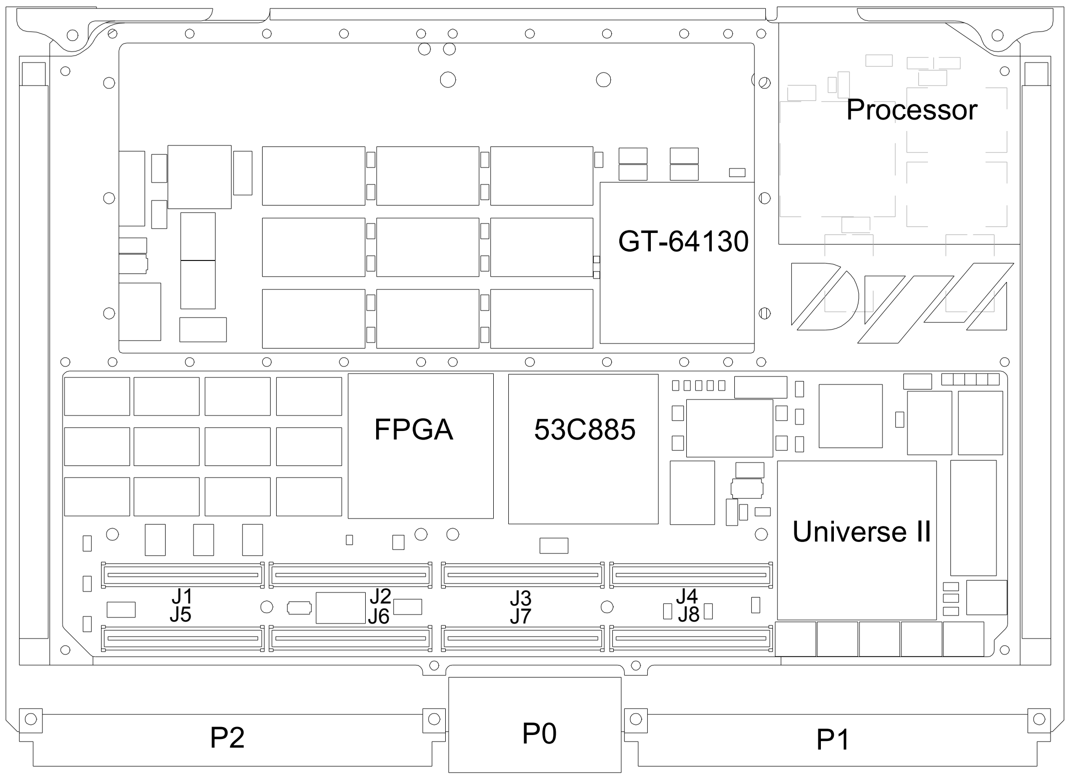


Figure 1.2 **SVME/DMV-179 Component Side Layout**

Figure 1.3 shows the location of the PMC slots.

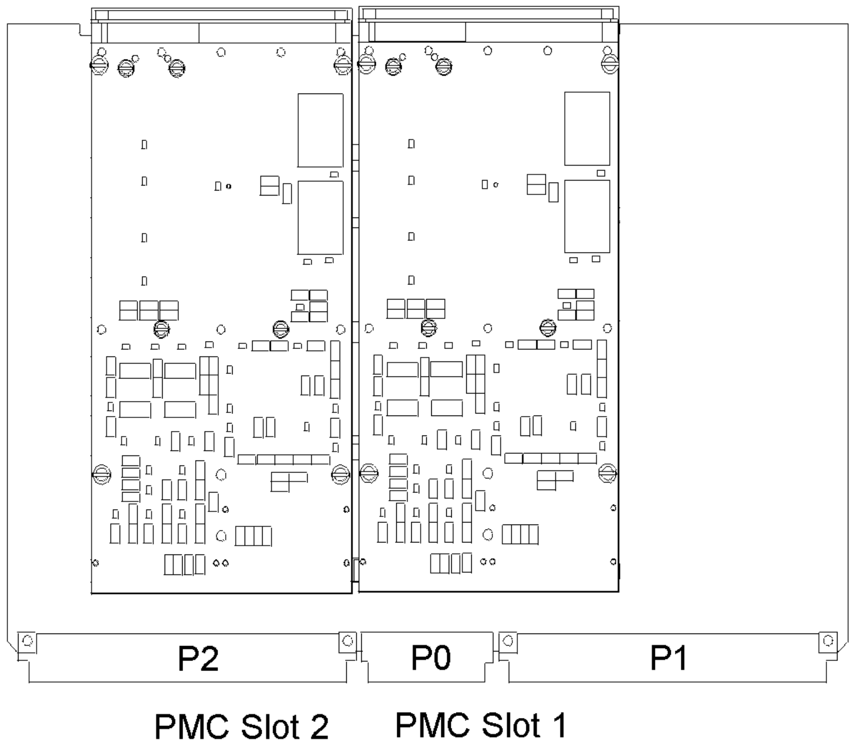


Figure 1.3 **Location of PMC Modules**

Dimensions

The SVME/DMV-179 is built on a VMEbus-compatible double-height (6U) Printed Wiring Board (PWB). Table 1.1 lists the dimensions of the SVME/DMV-179.

Table 1.1: **Dimensions of the SVME/DMV-179**

Parameter	Dimensions
Height	233.4 mm (9.2 in.)
Depth	160 mm (6.3 in.)
Thickness	20.0 mm (0.8 in.)

Weight

The maximum weight of the SVME/DMV-179 is specified in Table 1.2.

Table 1.2: **Maximum Card Weight**

Card Type	Weight (without PMC modules)
SVME-179 (no PMC modules present)	550 g
DMV-179 (no PMC modules present)	600 g

Mating Connectors

Table 1.3 summarizes these connectors, providing a brief description and an indication of what functions/interfaces are supported by each.

Table 1.3: Summary of SVME/DMV-179 Connectors, Functions Supported

Connector Designation	Description	Supported I/O Configurations
J9	31-pin front panel connector (SVME-179 only) compatible with DY 4 front panel cable, CBL-179-001 and CBL-SBC-FP-000.	EIA-232 serial Channels 1 and 2, Ethernet interface, COP/JTAG interface, card reset
J1, J2, J5, J6	connectors for PMC module site 2, compliant with IEEE P1386.	Connectors used for interconnection with optional 32-bit or 64-bit PMC module. All 64 PMC module site 2 I/O signals are accessible via the basecard P2 connector, rows A and C.
J3, J4, J7, J8	connectors for PMC module site 1, compliant with IEEE P1386.	Connectors used for interconnection with optional 32-bit or 64-bit PMC module. All 64 PMC module site 1 I/O signals are accessible via the basecard P0 connector.
P2 (see Note)	160-pin (5 x 32) right-angle DIN connector, row B pin assignments in accordance with the ANSI/ VITA 1-1994 VME64 VMEbus specification, remaining rows employed for user I/O.	VMEbus interface, EIA-232 interfaces (Channels 1 and 2), EIA-422/485 interfaces (Channels 3 and 4), SCSI interface, Ethernet 10Base-T or 100Base-T interface, PMC Site 2 I/O signals (standard factory configuration).
P0 (see Note)	95-pin (5 x 19) AMP connector, part number 98-3165-105-01.	JTAG interface, Discrete Digital I/O interface, Ethernet 10Base-T or 100Base-T interface (see Note), SCSI interface, EIA-232 interfaces (Channels 1 and 2), EIA-422/485 interfaces (Channels 3 and 4), PMC Site 1 I/O signals (standard factory configuration).

Note

The specific interface functions provided via the P0 and P2 interfaces are determined via factory configuration and are largely dependent on the type and number of PMC modules installed on the basecard. The SVME/DMV-179 supports an Ethernet interface via the P0 connector on a special order basis. Please contact the factory if you require this option.

Cross Reference

The standard SVME/DMV-179 factory configuration is mostly P0 and P2 I/O-compatible with the SVME/DMV-178. The SVME/DMV-179 is also factory configurable for SVME/DMV-176/177 P0 and P2 I/O compatibility. See the application note *Migrating from the SVME/DMV-178 to the SVME/DMV-179*, document number 808630 for more information.

Cross Reference

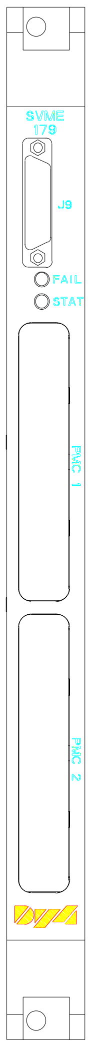
For complete descriptions of all the basecard mating connectors, including detailed pinout listings and electrical characteristics of signals, refer to Chapter 2 of the *SVME/DMV-179 Hardware User's Manual*, document number 809606.

You should consult the *Product Release Notes* for your particular card variant, which contains information describing any variant-specific alterations to the interface configuration of your card, if any have been implemented.

Tip

The Technical Documentation CD-ROM includes a pinout configurator utility. This 32-bit Windows utility calculates the P0 and P2 pinouts based on the I/O mode of the SVME/DMV-179 and the PMC modules installed on it.

SVME-179 Front Panel



J9 Connector: Used in conjunction with the front panel cable, CBL-179-001 or CBL-SBC-FP-000, the J9 connector provides connections for two serial channels, Ethernet, the PowerPC COP port, and a card reset input.

All four serial communications channels (Channels 1 through 4) on both the SVME and DMV-179 can also be made available on the P0 or P2 connectors. The PowerPC COP/JTAG signals are only available on the J9 connector on the SVME-179.

Two Light Emitting Diode (LED) indicators are present on the SVME/DMV-179: the red FAIL LED and the green STAT LED. Both LEDs will turn on after an internal RESET during the power-on sequence or after a System Reset.

Red FAIL LED: The red FAIL LED indicates that the SVME/DMV-179 is driving the SYSFAIL* signal on the VMEbus. The SYSFAIL* signal is controlled by the Universe II device. For further details on the SYSFAIL* signal, refer to the *Universe II User's Manual*, provided on the SVME/DMV-179 Technical Documentation CD-ROM.

Green STAT LED: The green STAT LED indicates the state of the Lower Status LED (STATLED) signal in bit 3 of the E2PROM General Control Register. If the STATLED control bit is 0, then the LED is on. If the STATLED control bit is 1, the LED is off. For further details on the STATLED control bit, refer to the *SVME/DMV-179 Hardware User's Manual*, document number 809606, provided in this documentation package.

PMC Slots: Two openings are provided on the SVME-179 front panel to provide access to connectors that may be incorporated on optional PMC modules that may be installed on the basecard PWB.

Overview of Supplied Firmware

Foundation Firmware

The SVME/DMV-179 is programmed with the following Foundation Firmware (FFW) modules:

- *General Purpose Monitor (GPM)*: provides comprehensive monitoring and debug functions, which can be accessed from a terminal connected to the SVME/DMV-179 serial channel 1 interface
- *Card Level Diagnostics (CLD)*: provides diagnostic routines which work with your card's Built-In-Test functions
- *Card Support Services (CSS)*: provides a software interface to your card's hardware
- *Execution Sequencer (ES)*: controls the execution sequence of software during a card's boot-up
- *Non-Volatile Memory Programmer (NVMP)*: provides for in-circuit programming of Flash memory.

Cross Reference

Refer to the *V8 FFW User's Manual* (included on the and the SVME/DMV-179 Technical Documentation CD-ROM) and the *FFW Programmer's Reference (*included in the documentation package binder and the CD-ROM) for additional information.

Note

DY 4 Systems has also developed a Windows-based application called FlashProg for programming the Flash memory. FlashProg Version 2.4.1 or later is required for the SVME/DMV-179.

A multimedia demonstration of FlashProg is included on your SVME/DMV-179 Technical Documentation CD-ROM.

Contact your DY 4 representative for more information about FlashProg.

Board Support Packages, Drivers

Support is provided for the VxWorks operating system. The VxWorks boot loader is pre-loaded on the SVME/DMV-179 hardware. The VxWorks Board Support Package (BSP) is provided on CD-ROM. A Board Support Package is also available for the LynxOS operating system.

Cross Reference

Refer to the *Release Notes* and the *BSP Software User's Manual* provided on the SVME/DMV-179 BSP CD-ROM for additional information.

Sample Code

Sample code software is supplied on the Technical Documentation CD-ROM to facilitate your initial testing of the installed hardware and help you explore the product functions and capabilities.

Chapter 2

Pre-Installation Tasks

In this chapter...

This chapter explains how to configure the SVME/DMV-179 before it is installed in a VME chassis. Specifically, this chapter provides the following information:

- ❑ unpacking the card;
- ❑ modifying the SVME/DMV-179 jumper settings; and
- ❑ checking cable and power requirements.

Unpacking the Card

Warning

This card uses components that are sensitive to electrostatic discharges. It must be kept in its conductive package until just before the installation begins. Remove the card from its protective package only at a grounded workstation while wearing an approved grounding wrist strap. Avoid touching any metal contacts on the card; static discharge can damage integrated circuits. To avoid damage to the card or to avoid any personal injury, remove the power from the chassis prior to removing or installing cards.

To unpack the card from its protective package, follow these steps:

1. Unpack the card from the shipping carton in a suitable work area. If the shipping carton appears to be damaged, request that an agent of the shipper or carrier be present during unpacking and inspection.
2. Find the packing list. Verify that all the items on the list are present.
3. Save the packing material for storing or reshipping the card.
4. Ensure that any supplied PMC module is mechanically fastened to the SVME/DMV-179 basecard.

Configuring Jumpers

Cross Reference

Depending on your application, it may be necessary to modify the default jumper settings on your SVME/DMV-179. For specific information about your SVME/DMV-179's default settings, refer to the *Product Release Note*.

Note

Factory configurations are performed via the installation/removal of configuration resistors. Please contact the factory if you require information about factory configured options. Under normal circumstances, you should not need to alter any of the factory-configured options.

Table 2.1 lists user-configurable basecard E-jumper settings. More in-depth descriptions of these jumper settings are provided later in this chapter.

Table 2.1: Basecard Jumper Settings Summary

Option	Jumper Setting
Change the Execution Sequence: (see page page 3-20 for more information)	Connect E2-E4 to connect User Link or Software Switch (SW0) signal to ground. Open E2-E4 to pull up User Link or Software Switch (SW0).
Watchdog Timer Power-up Behaviour Selection: Watchdog timer is disabled following power-up. Watchdog timer is enabled following power-up and generates reset on timeout.	Connect E3-E5 Open E3-E5
Choosing Card Bootup Source: Boot from 64-bit Flash. Boot from 8-bit Permanent Alternate Boot Site (PABS). Boot from 8-bit debug Flash site (boot PROM). (Used for “dead” card programming.)	Open E6-E7, disconnect P0 pin A10 Connect P0 pin A10 to ground or connect E48-E49 (E48-E49 present only on SVME/DMV-179 PWBs identified 310939-004 or higher - see **Caution** below). Connect E6-E7, disconnect P0 pin A10 and disconnect E48-E49 (if present).
Permanent Alternate Boot Write Enable: Program permanent alternate boot bank. Do not program permanent alternate boot bank.	Connect E27-E28 (for factory use only) Open E27-E28 (normal configuration)
JTAG Test Chain: (refer to the SVME/DMV-179 Hardware User’s Manual for a detailed description of the JTAG Test Chain) Test CPU only. Test complete JTAG chain.	 Open E55-E56 Connect E55-E56

Caution

When choosing to boot from the Permanent Alternate Boot Site on SVME/DMV-179 cards based upon the 310939-004 (or higher) PWB, do not connect E48-E49 if you have also connected P0 pin A10 to ground... use one or the other method, not both.

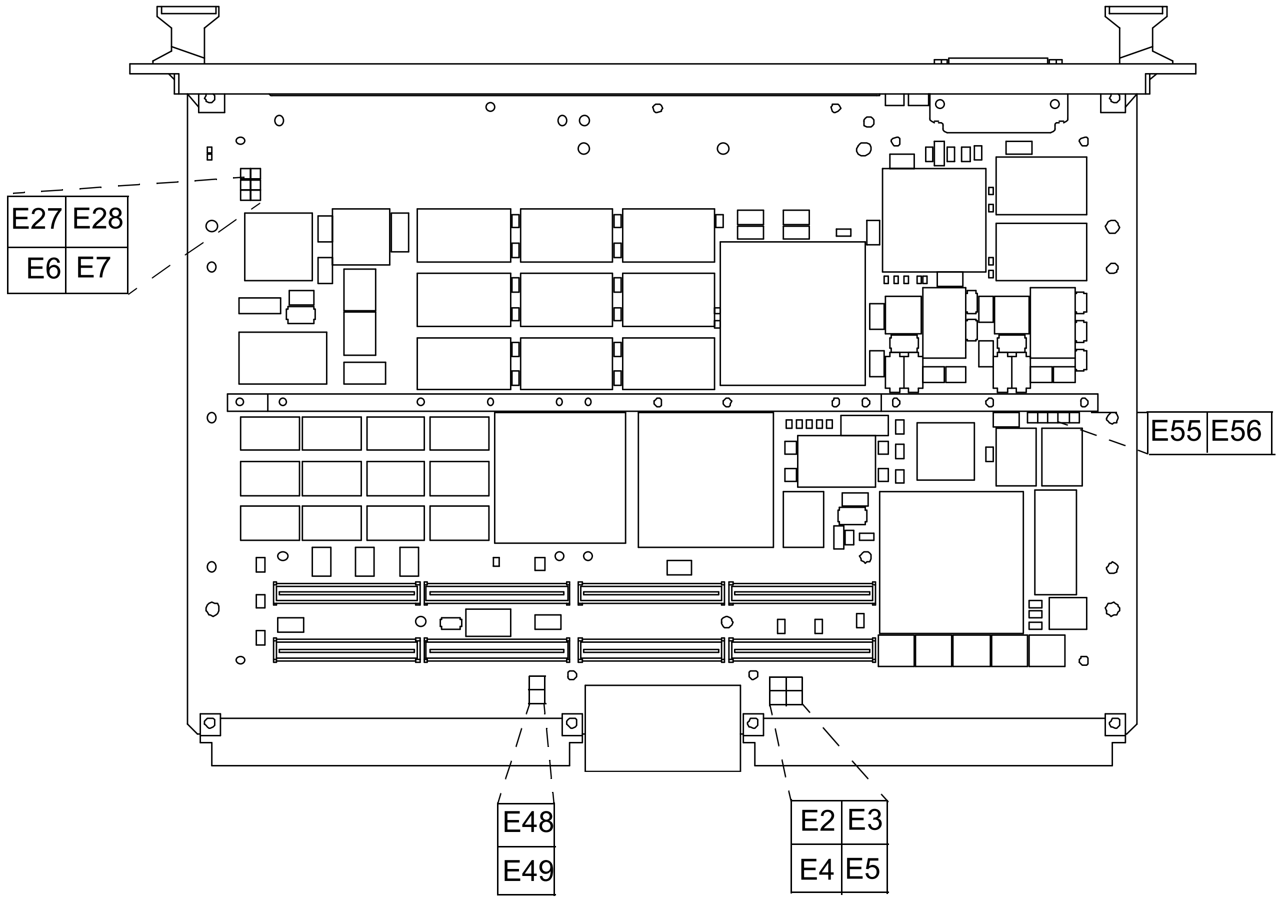


Figure 2.1 **SVME/DMV-179 Jumper Locations**

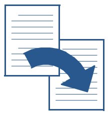
Note

All remaining “E” terminals are reserved for factory use or configuration only.

Execution Sequence Control Jumper

The SVME/DMV-179 has a software-readable E-Jumper located at E2-E4, known as the User Link or Software Switch, used to control the power-up sequence for the Foundation Firmware.

The onboard Foundation Firmware checks the state (connected or open) of the User Link on power-up and uses this along with the serial channel 1 DSR input to select one of four possible execution sequences. See page 3-20.



Cross Reference

For information on the code executed, refer to the *Programmer's Reference Manual*, document number 809016.

Table 2.2: User Link Configuration

Option	Jumper Setting
Execution sequencer control (see page 3-20)	Connect E2-E4 (PCI Control and Status Register bit SW0=0).
Execution sequencer control (see page 3-20)	Open E2-E4 (PCI Control and Status Register bit SW0=1).

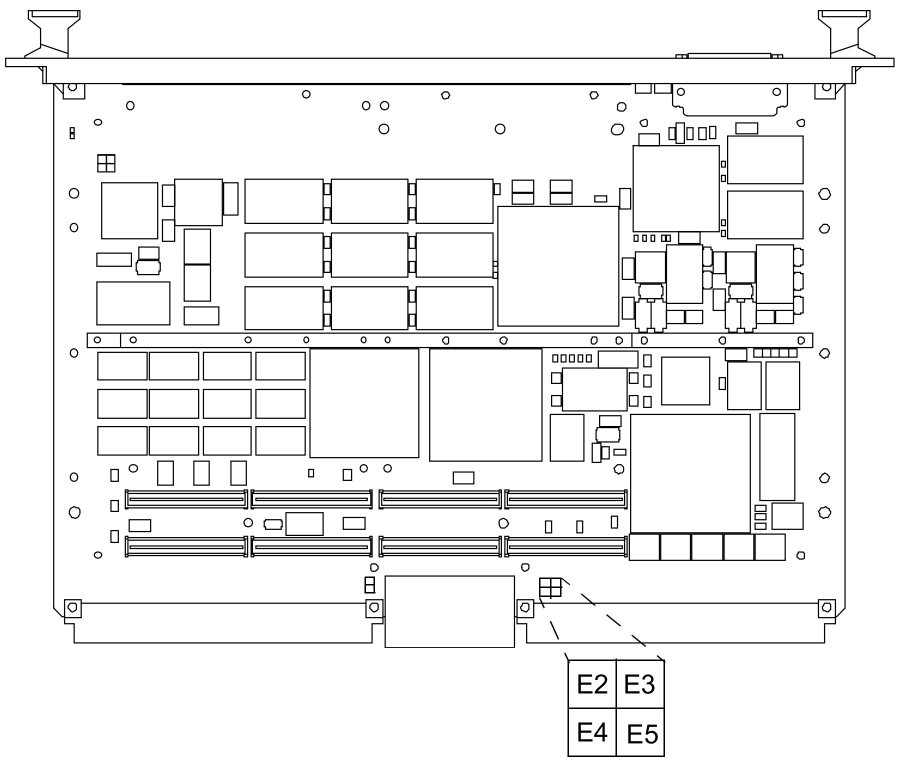


Figure 2.2 User Link Location

Watchdog Timer Power-up Reset Behaviour Selection

The SVME/DMV-179 offers the capability of enabling the watchdog timer immediately following reset without the need for software programming or initialization. This mode of operation is selected by leaving E3-E5 open. The watchdog timer will generate a card reset if left to expire.

With the E3-E5 jumper installed, the watchdog timer is disabled following power-up reset; however, it can be enabled by application software.

Table 2.3: Watchdog Timer Power-up Behaviour

Option	Jumper Settings
Watchdog timer is disabled following power-up.	Connect E3-E5
Watchdog timer is enabled following power-up and generates reset on timeout.	Open E3-E5

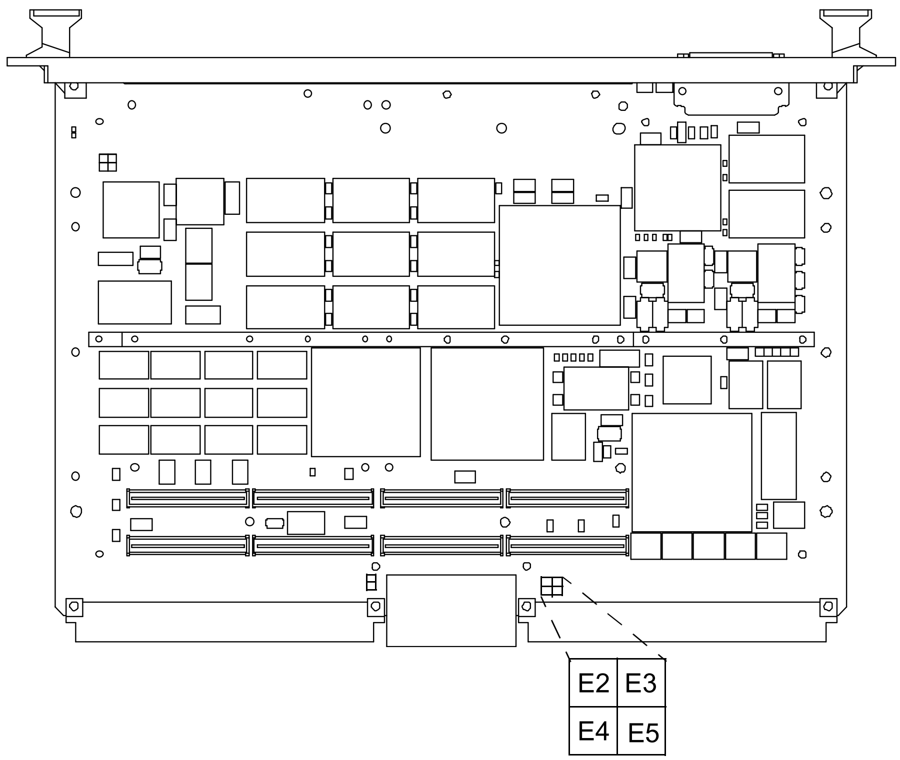


Figure 2.3 Watchdog Timer Power-up Behaviour

Booting

The SVME/DMV-179 includes a 64-bit Flash bank, a Permanently mounted Alternate Boot Site (PABS), and a "debug Flash bank". You may boot the SVME/DMV-179 from any of these three sources. Normally, the SVME/DMV-179 boots from 64-bit Flash. However, if the Foundation Firmware in the 64-bit Flash is corrupted, you may boot from the Permanent Alternate Boot Site. In the case where both the 64-bit Flash and the Permanent Alternate Boot Site are corrupted, you may boot from the "debug Flash bank". Once you have booted the card you may use FlashProg or NVMP to reprogram the 64-bit Flash. You can then power off the card and the remove the jumper to allow local booting.

If the Permanent Alternate Boot Site is blank, it is automatically restored when the card is booted from the debug Flash bank.

Use the jumper settings described in Table 2.4 to select the bank used for booting.

Tip

The SVME/DMV-179 Technical Documentation CD-ROM contains a multimedia demo showing how to use the FlashProg utility.

Caution

To boot from the debug Flash bank, power down the card and install the 8-bit boot device in the 32-pin JEDEC socket (U111) on the solder side of the card, paying careful attention to the device orientation and the keying mechanism associated with pin 31 of the socket site. You must modify 8-bit boot devices by cutting or lifting pin 31 in order to be compatible with the keyed site. Connect E6-E7 and power up the card.

Tip

The PROM image for the debug Flash bank is provided on the SVME/DMV-179 Technical Documentation CD-ROM.

Table 2.4: Booting Configuration

Option	Jumper Settings
Boot SVME/DMV-179 from 64-bit Flash (normal mode)	Open E6-E7 Disconnect P0 pin A10
Boot SVME/DMV-179 from 8-bit Permanent Alternate Boot Site	Connect P0 pin A10 to ground or connect E48-E49 (E48-E49 present only on SVME/DMV-179 PWBs identified 310939-004 or higher - see Caution below).
Boot SVME/DMV-179 from 8-bit Debug Flash Bank (bootPROM)	Connect E6-E7, disconnect P0 pin A10, and disconnect E48-E49 (if present).

Caution

When choosing to boot from the Permanent Alternate Boot Site on SVME/DMV-179 cards based upon the 310939-004 (or higher) PWB, do not connect E48-E49 if you have also connected P0 pin A10 to ground... use one or the other method, not both.

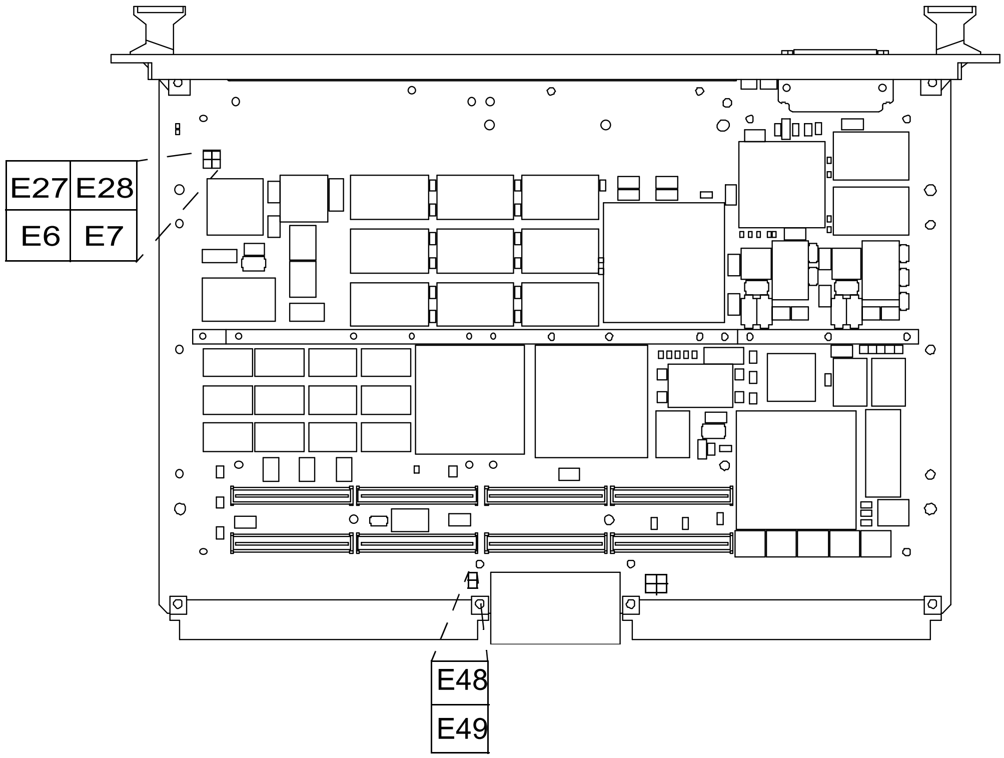


Figure 2.4 **Boot Jumper Locations**

Checking Hardware Requirements

Ensure that the following requirements have been met prior to installation:

Chassis Requirements

The SVME-179 is designed to be installed in a standard VMEbus chassis and backplane which operates in a free-air or forced-air cooling environment. The DMV-179 is conduction-cooled, and is therefore designed to be installed in a VME conduction-cooled chassis.

Power Requirements

Table 2.5 shows the power requirements for the SVME/DMV-179 equipped with a 400 MHz PowerPC 7400 or 750 CPU, 128 or 256 Mbyte DRAM memory and no PMC modules. For proper operation, the +5 V supply must be in the range 4.75 V to 5.25 V.

Table 2.5: **Power Requirements**

Processor	Voltage	Maximum Current	Typical Current
PowerPC 750	+5 VDC	4.2 A	3.4 A
PowerPC 7400	+5 VDC	5.5 A	4.0 A

Note

The SVME/DMV-179 uses on-card voltage regulators to provide the required low voltages to devices on the SVME/DMV-179. If PMC modules requiring 3.3 V are to be used on the SVME/DMV-179, the backplane into which the SVME/DMV-179 is installed must be properly configured to provide 3.3 V power at the P1 connector.

Cable Requirements

The following cables are used during the installation procedure described in this manual. They are available from DY 4 Systems by ordering part numbers listed in Table 2.6. You can also make your own cables using the SVME/DMV-179 connector pin assignments documented in Chapter 2 of the Hardware User’s Manual.

Table 2.6: Cable Part Numbers

Part Number	Identification
CBL-179-001	Cable Assembly, SVME/DMV-179 Front Panel I/O
CBL-SBC-FP-000	Cable Assembly, SVME/DMV-179, SVME/DMV-181, Front Panel I/O
CBL-179-003	Cable Assembly, SVME/DMV-179 P2 I/O
CBL-179-002	Cable Assembly, SVME/DMV-179 P0 I/O

Cabling Considerations

Tip

If the P2 and P0 I/O cables must both be plugged directly into backplane, the strain-relief shroud on the P2 I/O cable can be removed.

Cross Reference

See the section of this manual called *Connecting a Terminal* on page 3-5 for information about how to use the cables available for the SVME/DMV-179.

Chapter 3

Hardware Installation

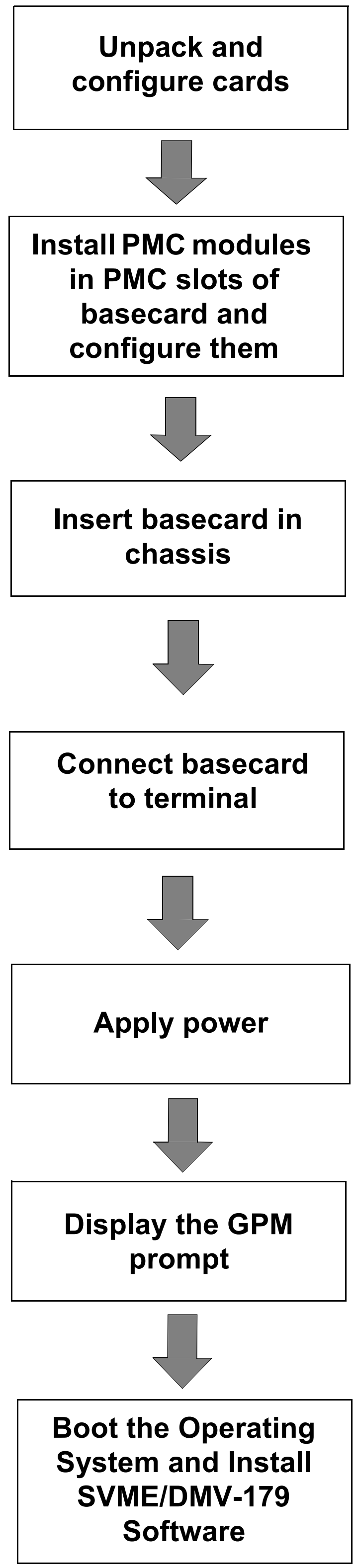
In this chapter...

This chapter explains how to install the SVME/DMV-179 in a VME chassis. Specifically this chapter describes the following procedures:

- ❑ inserting the card into a chassis;
- ❑ connecting a terminal to the card via a serial communications cable;
- ❑ turning on the power and confirming that the Power-up Built-In-Test (PBIT) has completed successfully;
- ❑ displaying the initial screen message and establishing the card’s VME base address; and
- ❑ troubleshooting installation problems.

Installation Procedure Summary

Below is a summary of the installation procedure described in this chapter. If you are experienced, you may wish to use it as a quick installation procedure.



Installation Procedure

Before You Begin...

Warning

This card uses components that are sensitive to electrostatic discharges. It must be kept in its conductive package until just before the installation begins. Remove the card from its protective package only at a grounded workstation while wearing an approved grounding wrist strap. Avoid touching any metal contacts on the card; static discharge can damage integrated circuits.

Turn the power off before inserting or removing cards from the VME chassis. Failure to do so could damage the card circuitry or cause personal injury.

Unpack and Configure the Cards

Before installing the card into a chassis, ensure that you complete the pre-installation tasks described in Chapter 2 of this manual and the pre-installation tasks described in the User's Manuals for the PMC modules.

Install the PMC Modules on the Basecard

If the PMC modules are not already installed on the basecard, install them in a PMC slot of your basecard using the appropriate Dy 4 mounting kits.

Cross Reference

See the SVME/DMV-179 Generic Drawing or the User's Manual for your PMC module for instructions. These documents are included on the Technical Documentation CD-ROM.

When the PMC module is mounted in slot 1 (at the centre of the basecard), its I/O signals are available on the backplane P0 connector. When the PMC module is mounted in slot 2 (near the P2 connector), its I/O signals are available on the backplane P2 connector.

Choose a VME Slot Location

Select Slot 1, the left-most slot in the VME chassis, if you want the basecard to be the System Controller (SYSCON). If you intend to use another card as the SYSCON, select the left-most unoccupied slot. All VME cards should be installed in adjacent slots; leaving empty slots may cause problems with interrupts and Bus Grant signals.

Insert the Basecard in the Chassis

Ensure that the chassis power is turned off before inserting the card.

SVME-179

An SVME basecard is equipped with a faceplate compliant with IEEE 1101.10. The large ejectors on this faceplate facilitate insertion of the basecard into the 160-contact, 5-row connectors for P1 and P2.

If the faceplate is not compatible with your chassis, you can purchase an alternate faceplate from DY 4 (FPL-179-000). Use the basecard generic drawing (included on the SVME/DMV-179 Technical Documentation CD-ROM) to determine how to mount the faceplate on the card.

With the alternate faceplate, you must use a significant amount of insertion force to mate the backplane connectors with the VME backplane. Use extra care when aligning and inserting your basecard into your chassis, to ensure that a secure mechanical and electrical connection is made between the card and the backplane mating connectors.

Once the basecard is inserted in the chassis, secure it by tightening the screws at the top and bottom of the faceplate.

DMV-179

With DMV basecards, you must use a significant amount of insertion force to mate the backplane connectors with the VME backplane. Use extra care when aligning and inserting your basecard into your chassis, to ensure that a secure mechanical and electrical connection is made between the card and the backplane mating connectors.

Once the basecard is inserted in the chassis, use a torque driver/wrench to tighten the wedgelocks at the top and bottom of the card. The required torque is 6 in-lbs.

Connecting a Terminal

In order to access the features available within the embedded firmware on the SVME/DMV-179, you'll need to attach a terminal or PC-emulated equivalent to the Serial Channel 1 interface on the card. You can connect a terminal to the SVME/DMV-179 in one of the following ways:

- via the front panel serial port J9 connector using a serial cable such as CBL-179-001 (for the SVME-179 version product only);
- via the P2 connector using a P2 interface cable such as CBL-179-003, available from DY 4 Systems (for both SVME and DMV-179 version products);
- via the P0 connector using a P0 interface cable such as the CBL-179-002, (for both SVME and DMV-179 version products).

Tip

Default serial communication parameters are 9600 N, 8, 1 (9600 baud, no parity, 8 bits, 1 stop bit).

Ordering Cables

The cable assemblies described in Table 2.6 on page 2-10 are available from DY 4 Systems by ordering individual cables by their part numbers. Should you need to develop your own cabling solution, please refer to Chapter 2 of the Hardware User's Manual for complete interface pinout listings for the J9, P0, and P2 interfaces.

Serial Communications via the Front Panel J9 Connector

The SVME-179 has a single 31-pin connector on the front panel that provides access to two EIA-232 serial channels (1 and 2), an Ethernet 10BaseT or 100BaseT interface, plus a COP/JTAG interface for debugging purposes. The front panel cable (CBL-179-001 or CBL-SBC-FP-000) routes the different interfaces to separate connectors.

Note

CBL-SBC-FP-000 is compatible with both the SVME-179 and the SVME-181. It includes a USB connector (P6) for use with the SVME-181. The USB connector (P6) should **not** be used with the SVME-179 as the USB interface is not present on the SVME-179.

The signal mapping for the cables is shown in Tables 3.1 to 3.4. Figure 3.1 illustrates the CBL-179-001 front panel and cable.

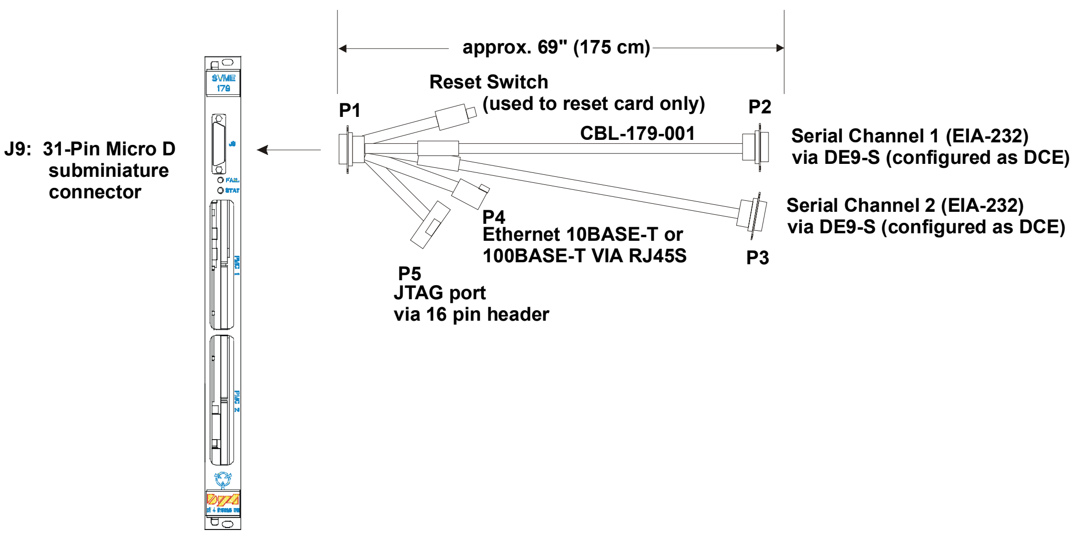


Figure 3.1 **SVME-179 Front Panel I/O Cable (CBL-179-001)**

Table 3.1: Front Panel Cable P1 to P2 and P3 Signal Mapping

Signal Name	SVME/DMV-179 J9 Connector	Cable P1 Connector	Serial Channel 1 P2 Connector	Serial Channel 2 P3 Connector
GND	J9-8	P1-8	P2-5	P3-5
CH2RTS	J9-9	P1-9		P3-7
CH2CTS	J9-10	P1-10		P3-8
CH2RXD	J9-11	P1-11		P3-3
CH2TXD	J9-12	P1-12		P3-2
CH1DSR	J9-13	P1-13	P2-4	
CH1RXD	J9-14	P1-14	P2-3	
CH1DCD	J9-15	P1-15	P2-1	
CH1TXD	J9-16	P1-16	P2-2	

Note

As a minimum, three EIA-232 pins (TXDA, RXDA and GND) must be connected if software handshaking (XON, XOFF) is used. If software handshaking is not used, CTS and RTS must be connected.

Cross Reference

The CH1DSR signal is used to control the power-up sequence. See "Controlling the Power-Up Sequence" on page 3-20 for more information.

Table 3.2: Front Panel Cable P1 to P4 Signal Mapping

Signal Name	SVME/DMV-179 J9 Connector	Cable P1 Connector	Ethernet P4 Connector
ENET_RXD-	J9-17	P1-17	P4-6
ENET_RXD+	J9-18	P1-18	P4-3
ENET_TXD+	J9-19	P1-19	P4-1
ENET_TXD-	J9-20	P1-20	P4-2
ENET_UTP2	J9-21	P1-21	P4-7, P4-8
ENET_UTP1	J9-22	P1-22	P4-4, P4-5

Table 3.3: Front Panel Cable P1 to P5 Signal Mapping

Signal Name	SVME/DMV-179 J9 Connector	Front Panel P1 Connector	COP/JTAG P5 Connector
COPS_TDI	J9-1	P1-1	P5-3
COPS_TMS	J9-2	P1-2	P5-9
COPS_TCK	J9-3	P1-3	P5-7
COPS_CKSTP-	J9-4	P1-4	P5-15
COPS_SRST-	J9-5	P1-5	P5-11
COPS_JTRST	J9-6	P1-6	P5-4
COPS_HRST-	J9-7	P1-7	P5-13
GND	J9-8	P1-8	P5-12,16
COPS_PWR	J9-29	P1-29	P5-6
COPS_TDO	J9-31	P1-31	P5-1
COPS_CPU_QACK	J9-23	P1-23	P5-2

Table 3.4: Front Panel Cable P1 to PB1 Signal Mapping

Signal Name	Front Panel P1 Connector	Reset Pushbutton PB1 Switch
GND	P1-8	PB1-1
FP_RST-	P1-24	PB1-2

Serial Communications via the P2 Connector

Connection from the SVME/DMV-179 P2 interface to the terminal is provided by the 179 P2 I/O cable assembly, CBL-179-003.

Install the 179 P2 I/O cable assembly by carefully pressing the cable P1 connector onto the P2 backplane connector stakes. The cable J4 connector is used to attach to a terminal. Other SVME/DMV-179 basecard-related functions are available via this cable, as described below in Figure 3.2.

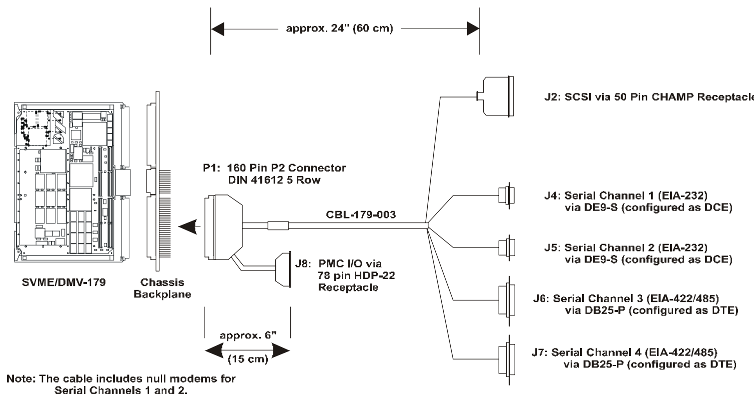


Figure 3.2 **SVME/DMV-179 P2 Cable Connections**

Table 3.5: CBL-179-003 P2 I/O Cable Connector Information

Connector	Manufacturer's Part Number	Description
P1	ERNI 024070	Conn., DIN 41612, 5 row
J2	AMP 2-552476-1	Conn., Recept, CHAMP, 50 way
J4, J5	AMP 205203-1	Conn., D-Sub Receptacle DE9-S
J6, J7	AMP 205208-1	Conn., D-Sub Plug DB25-P
J8	AMP 78569-1	Conn., Receptacle HDP-22

CBL-179-003 J4, J5 (Serial Channels 1, 2) Connector Pinouts

The mapping of Serial Channels 1 and 2 EIA-232 signals from the CBL-179-003 P1 connector to the DE9-S connectors (CBL-179-003 J4, J5) is shown in Table 3.6.

Table 3.6: CBL-179-003 P1 to J4, J5 (Serial Channels 1 and 2) Signal Mapping

P1 Pin (From)	J4, J5 Pin (To)	P1 Signal Name	Comments
P1-D17	J4-2	CH1TXD	EIA-232
P1-D18	J4-3	CH1RXD	EIA-232
P1-D19	J4-4	CH1DSR	EIA-232
P1-B31	J4-5	GND	Signal Ground
P1-D30	J5-2	CH2TXD	EIA-232
P1-Z19	J5-3	CH2RXD	EIA-232
P1-B31	J5-5	GND	Signal Ground

CBL-179-003 J6, J7 (Serial Channels 3, 4) Connector Pinouts

The mapping of Serial Channels 3 and 4 EIA-422 signals from the CBL-179-003 P1 connector to the DB25-P connectors (CBL-179-003 J6, J7) is shown in Table 3.7.

Table 3.7: CBL-179-003 P1 to J6, J7 (Serial Channels 3 and 4) Signal Mapping

P1 Pin (From)	J6, J7 Pin (To)	P1 Signal Name	Comments
P1-D11	J6-2	CH3TXD_A	EIA-422
P1-D12	J6-14	CH3TXD_B	EIA-422
P1-D14	J6-3	CH3RXD_A'	EIA-422
P1-D13	J6-16	CH3RXD_B'	EIA-422
P1-D15	J6-15	CH3TXCOUT_A	EIA-422
P1-D16	J6-24	CH3TXCOUT_B	EIA-422
P1-Z21	J6-17	CH3RXC_A'	EIA-422
P1-Z23	J6-25	CH3RXC_B'	EIA-422
P1-B12	J6-7	GND	Signal Ground
P1-D26	J7-2	CH4TXD_A	EIA-422
P1-D27	J7-14	CH4TXD_B	EIA-422
P1-D21	J7-3	CH4RXD_A'	EIA-422
P1-D20	J7-16	CH4RXD_B'	EIA-422
P1-D22	J7-15	CH4TXCOUT_A	EIA-422
P1-D23	J7-24	CH4TXCOUT_B	EIA-422
P1-D25	J7-17	CH4RXC_A'	EIA-422
P1-D24	J7-25	CH4RXC_B'	EIA-422
P1-B22	J7-7	GND	Signal Ground

Note

The EIA-422 TXD and RXD signals on the cable J6 and J7 connectors are **not** on the pins specified by the EIA-530 standard. If you require connectors compliant with EIA-530, build a cable adapter using the information in Table 3.8.

Table 3.8: Signal Mapping from Cable J6 or J7 Connector to EIA-530

Signal Name	Cable J6 or J7 Connector	EIA-530 Standard Connector (without null modem)	EIA-530 Standard Connector (with null modem)
TXD_A	2	2	5
TXD_B	14	14	17
RXD_A'	3	5	2
RXD_B'	16	17	14
GND	7	7	7

CBL-179-003 J2 (SCSI) Connector Pinouts

The mapping of SCSI signals from the CBL-179-003 P1 connector to the 50 Pin CHAMP Receptacle (CBL-179-003 J2 Connector) is shown in Table 3.9:

Table 3.9: CBL-179-003 P1 to J2 (SCSI 50-Pin CHAMP) Signal Mapping

P1 Pin (From)	J2 Pin (To)	Signal Name	P1 Pin (From)	J2 Pin (To)	Signal Name
P1-B2	J2-1	GND	P1-Z1	J2-26	-DB(0)
P1-B2	J2-2	GND	P1-Z3	J2-27	-DB(1)
P1-B2	J2-3	GND	P1-Z5	J2-28	-DB(2)
P1-B2	J2-4	GND	P1-Z7	J2-29	-DB(3)
P1-B2	J2-5	GND	P1-Z9	J2-30	-DB(4)
P1-B2	J2-6	GND	P1-Z11	J2-31	-DB(5)
P1-B2	J2-7	GND	P1-Z13	J2-32	-DB(6)
P1-B2	J2-8	GND	P1-Z15	J2-33	-DB(7)
P1-B2	J2-9	GND	P1-Z17	J2-34	-DB(P)
P1-B2	J2-10	GND	P1-B22	J2-35	GND
P1-B12	J2-11	GND	P1-B22	J2-36	GND
P1-B12	J2-12	RESERVED	P1-B22	J2-37	GND
P1-B12	J2-13	OPEN	P1-D10	J2-38	TERMPWR (fused +5V)
P1-B12	J2-14	RESERVED	P1-B22	J2-39	GND
P1-B12	J2-15	GND	P1-B22	J2-40	GND
P1-B12	J2-16	GND	P1-D1	J2-41	-ATN
P1-B12	J2-17	GND	P1-B22	J2-42	GND
P1-B12	J2-18	GND	P1-D2	J2-43	-BSY
P1-B12	J2-19	GND	P1-D3	J2-44	-ACK
P1-B12	J2-20	GND	P1-D4	J2-45	-RST
P1-B22	J2-21	GND	P1-D5	J2-46	-MSG
P1-B22	J2-22	GND	P1-D6	J2-47	-SEL
P1-B22	J2-23	GND	P1-D7	J2-48	-C/D
P1-B22	J2-24	GND	P1-D8	J2-49	-REQ
P1-B22	J2-25	GND	P1-D9	J2-50	-I/O

Note

The SVME/DMV-179 provides TERMPWR as specified in SCSI-2.

When connecting a SCSI peripheral, make sure to configure the peripheral to accept TERMPWR from the SCSI bus. This is a jumper setting on the SCSI peripheral.

CBL-179-003 J8 (PMC Site 2 I/O) Connector Pinouts

The mapping of PMC I/O signals from the CBL-179-003 P1 connector to the 78 contact HDP-22 receptacle (CBL-179-003 J8) is shown in Table 3.10.

Table 3.10: CBL-179-003 P1 to J8 (PMC I/O) Signal Mapping

P1 Pin (From)	J8 Pin (To)	Signal Name
P1-C1	J8-9	PMC_01
P1-A1	J8-16	PMC_02
P1-C2	J8-31	PMC_03
P1-A2	J8-17	PMC_04
P1-C3	J8-10	PMC_05
P1-A3	J8-18	PMC_06
P1-C4	J8-3	PMC_07
P1-A4	J8-19	PMC_08
P1-C5	J8-11	PMC_09
P1-A5	J8-20	PMC_10
P1-C6	J8-6	PMC_11
P1-A6	J8-36	PMC_12
P1-C7	J8-12	PMC_13
P1-A7	J8-37	PMC_14
P1-C8	J8-13	PMC_15
P1-A8	J8-1	PMC_16
P1-C9	J8-29	PMC_17
P1-A9	J8-2	PMC_18
P1-C10	J8-14	PMC_19
P1-A10	J8-4	PMC_20
P1-C11	J8-30	PMC_21
P1-A11	J8-21	PMC_22
P1-C12	J8-42	PMC_23
P1-A12	J8-22	PMC_24
P1-C13	J8-77	PMC_25
P1-A13	J8-5	PMC_26
P1-C14	J8-23	PMC_27
P1-A14	J8-24	PMC_28
P1-C15	J8-69	PMC_29
P1-A15	J8-43	PMC_30
P1-C16	J8-45	PMC_31
P1-A16	J8-62	PMC_32
P1-C17	J8-71	PMC_33

Table 3.10: CBL-179-003 P1 to J8 (PMC I/O) Signal Mapping (Continued)

P1 Pin (From)	J8 Pin (To)	Signal Name
P1-A17	J8-38	PMC_34
P1-C18	J8-48	PMC_35
P1-A18	J8-60	PMC_36
P1-C19	J8-70	PMC_37
P1-A19	J8-61	PMC_38
P1-C20	J8-49	PMC_39
P1-A20	J8-44	PMC_40
P1-C21	J8-15	PMC_41
P1-A21	J8-39	PMC_42
P1-C22	J8-50	PMC_43
P1-A22	J8-55	PMC_44
P1-C23	J8-32	PMC_45
P1-A23	J8-56	PMC_46
P1-C24	J8-51	PMC_47
P1-A24	J8-57	PMC_48
P1-C25	J8-74	PMC_49
P1-A25	J8-40	PMC_50
P1-C26	J8-68	PMC_51
P1-A26	J8-41	PMC_52
P1-C27	J8-33	PMC_53
P1-A27	J8-58	PMC_54
P1-C28	J8-78	PMC_55
P1-A28	J8-59	PMC_56
P1-C29	J8-73	PMC_57
P1-A29	J8-75	PMC_58
P1-C30	J8-63	PMC_59
P1-A30	J8-76	PMC_60
P1-C31	J8-64	PMC_61
P1-A31	J8-65	PMC_62
P1-C32	J8-66	PMC_63
P1-A32	J8-67	PMC_64

Expanded I/O via the P0 Connector

Connection with the SVME/DMV-179 P0 interface is provided by the 179 P0 I/O cable assembly, CBL-179-002, DY 4 part number 901434-000.

Install the 179 P0 I/O cable assembly by carefully pressing the cable P1 connector onto the P0 backplane connector stakes. The cable J3 connector is used to attach to a terminal. Other SVME/DMV-179 basecard-related functions are available via this cable, as described below in Figure 3.2.

Warning

Exercise care when inserting and extracting the P0 I/O cable as the P0 backplane pins can be easily bent if the cable connector is not properly aligned.

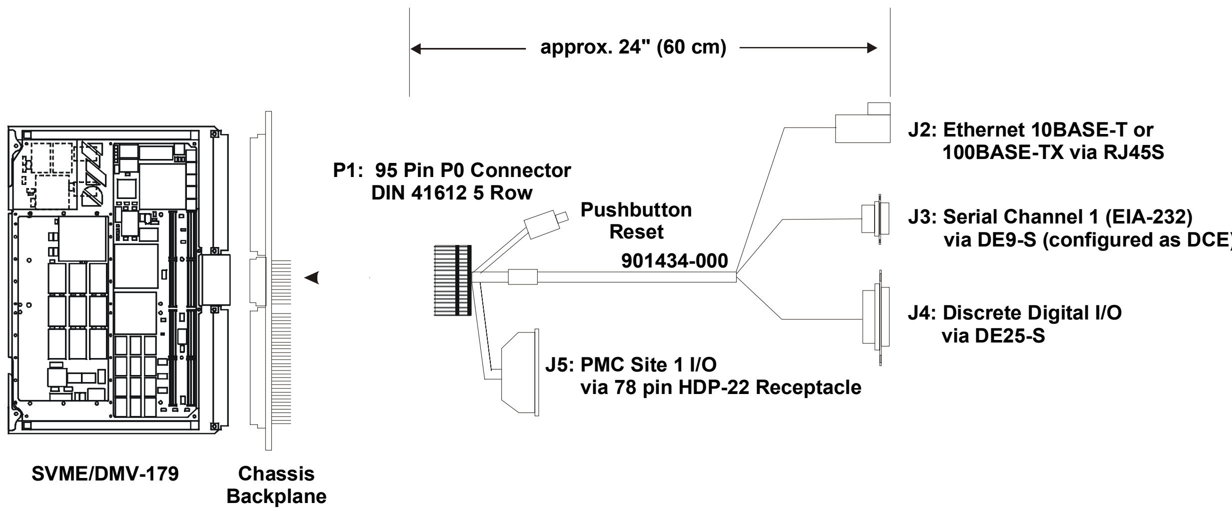


Figure 3.3 Expanded I/O via P0

Table 3.11: CBL-179-002 P0 I/O Cable Connector Information

Connector	Manufacturer's Part Number	Description
P1	AMP 98-3165-087-1	Conn., DIN 41612, 5 row
J2	Panduit CJ5581W	Conn., RJ45S
J3	AMP 205203-1	Conn., D-Sub Receptacle DE9-S
J4	AMP 205207-1	Conn., D-Sub Receptacle DB25-S
J5	AMP 78569-1	Conn., HDP-22 Receptacle 78 pins

CBL-179-002 J2 (Ethernet) Connector Pinout

The mapping of Ethernet signals from the CBL-179-002 P1 connector to the RJ45S connector (CBL-179-002 J2) is shown in Table 3.12.

Note

Note that while the CBL-179-002 cable includes a branch for the Ethernet signals, Ethernet via the P0 connector is not a standard feature of the SVME/DMV-179, and is only provided on a special order basis. Please consult the Product Release Note for your version of the SVME/DMV-179 for further information.

Table 3.12: CBL-179-002 P1 to J2 (Ethernet RJ45S) Signal Mapping

P1 Pin (From)	J2 Pin (To)	Signal Name	Comments
P1-B2	J2-1	ENET_TXD+	Ethernet (IEEE 802.3)
P1-A2	J2-2	ENET_TXD-	Ethernet (IEEE 802.3)
P1-B3	J2-3	ENET_RXD+	Ethernet (IEEE 802.3)
P1-A3	J2-6	ENET_RXD-	Ethernet (IEEE 802.3)
P1-A1	J2-4, 5	ENET_UPT2	Ethernet (IEEE 802.3)
P1-B1	J2-7, 8	ENET_UPT1	Ethernet (IEEE 802.3)

CBL-179-002 J3 (Serial Channel 1) Connector Pinout

The mapping of Serial Channel 1 EIA-232 signals from the CBL-179-002 P1 connector to the DE9-S connector (CBL-179-002 J3) is shown in Table 3.13.

Table 3.13: CBL-179-002 P1 to J3 (Serial Channel 1) Signal Mapping

P1 Pin (From)	J3 Pin (To)	Signal Name	Comments
P1-C1	J3-2	CH1TXD	EIA-232
P1-D1	J3-3	CH1RXD	EIA-232
P1-E1	J3-4	CH1DSR	EIA-232
P1-C2	J3-5	GND	Signal Ground

CBL-179-002 J4 (Parallel I/O) Connector Pinout

The mapping of parallel I/O signals from the CBL-179-002 P1 connector to the DB25-s connector (CBL-179-002 J4) is shown in Table 3.14.

Table 3.14: CBL-179-002 P1 to J4 (Parallel I/O) Signal Mapping

P1 Pin (From)	J4 Pin (To)	Signal Name
P1-A9	J4-1	PIO(0)
P1-B9	J4-3	PIO(1)
P1-B10	J4-5	PIO(2)
P1-C9	J4-7	PIO(3)
P1-C10	J4-9	PIO(4)
P1-D9	J4-11	PIO(5)
P1-D10	J4-13	PIO(6)
P1-E9	J4-14	PIO(7)
P1-E10	J4-16	PIO(8)
P1-E2	J4-18	PIO(9)
P1-E3	J4-20	PIO(10)
P1-A19	J4-22	PIO(11)
P1-C2	J4-2, 6, 10, 17, 21	GND

CBL-179-002 J5 (PMC Site 1 I/O) Connector Pinout

The mapping of PMC Site 1 I/O signals from the CBL-179-002 P1 connector to the 78-pin PMC Site 1 I/O connector (CBL-179-002 J5) is shown in Table 3.15.

Table 3.15: CBL-179-002 P1 to J5 (PMC Site 1 I/O) Signal Mapping

P1 Pin (From)	J5 Pin (To)	Signal Name
P1-E4	J5-9	PMC_01
P1-D4	J5-16	PMC_02
P1-C4	J5-31	PMC_03
P1-B4	J5-17	PMC_04
P1-A4	J5-10	PMC_05
P1-E5	J5-18	PMC_06
P1-D5	J5-3	PMC_07
P1-C5	J5-19	PMC_08
P1-B5	J5-11	PMC_09
P1-A5	J5-20	PMC_10
P1-E6	J5-6	PMC_11
P1-D6	J5-36	PMC_12
P1-C6	J5-12	PMC_13

Table 3.15: CBL-179-002 P1 to J5 (PMC Site 1 I/O) Signal Mapping (Continued)

P1 Pin (From)	J5 Pin (To)	Signal Name
P1-B6	J5-37	PMC_14
P1-A6	J5-13	PMC_15
P1-E7	J5-1	PMC_16
P1-D7	J5-29	PMC_17
P1-C7	J5-2	PMC_18
P1-B7	J5-14	PMC_19
P1-A7	J5-4	PMC_20
P1-E8	J5-30	PMC_21
P1-D8	J5-21	PMC_22
P1-C8	J5-42	PMC_23
P1-B8	J5-22	PMC_24
P1-A8	J5-77	PMC_25
P1-E12	J5-5	PMC_26
P1-D12	J5-23	PMC_27
P1-C12	J5-24	PMC_28
P1-B12	J5-69	PMC_29
P1-A12	J5-43	PMC_30
P1-E13	J5-45	PMC_31
P1-D13	J5-62	PMC_32
P1-C13	J5-71	PMC_33
P1-B13	J5-38	PMC_34
P1-A13	J5-48	PMC_35
P1-E14	J5-60	PMC_36
P1-D14	J5-70	PMC_37
P1-C14	J5-61	PMC_38
P1-B14	J5-49	PMC_39
P1-A14	J5-44	PMC_40
P1-E15	J5-15	PMC_41
P1-D15	J5-39	PMC_42
P1-C15	J5-50	PMC_43
P1-B15	J5-55	PMC_44
P1-A15	J5-32	PMC_45
P1-E16	J5-56	PMC_46
P1-D16	J5-51	PMC_47
P1-C16	J5-57	PMC_48
P1-B16	J5-74	PMC_49
P1-A16	J5-40	PMC_50
P1-E17	J5-68	PMC_51

Table 3.15: CBL-179-002 P1 to J5 (PMC Site 1 I/O) Signal Mapping (Continued)

P1 Pin (From)	J5 Pin (To)	Signal Name
P1-D17	J5-41	PMC_52
P1-C17	J5-33	PMC_53
P1-B17	J5-58	PMC_54
P1-A17	J5-78	PMC_55
P1-E18	J5-59	PMC_56
P1-D18	J5-73	PMC_57
P1-C18	J5-75	PMC_58
P1-B18	J5-63	PMC_59
P1-A18	J5-76	PMC_60
P1-E19	J5-64	PMC_61
P1-D19	J5-65	PMC_62
P1-C19	J5-66	PMC_63
P1-B19	J5-67	PMC_64

Controlling the Power-Up Sequence

The power-up sequence for the Foundation Firmware depends on the settings of the User Link, the state of the Serial Channel 1 DSR line, and the version of Foundation Firmware installed. The possible power-up sequences are shown in Table 3.16.

Tip

Use the GPM CIT command to determine the version of Foundation Firmware installed.

Table 3.16: Foundation Firmware Execution Sequence

Condition	Execution Sequence
User Link (E2 - E4) off DSR negated (cable out)	PBIT → Default Application → GPM When the SVME/DMV-179 boots, it executes PBIT and then calls the default application. If the default application returns, it returns to GPM.
User Link (E2 - E4) off DSR asserted (terminal connected to SVME/DMV-179 Serial Channel 1)	PBIT → GPM → Default Application → GPM When the SVME/DMV-179 boots, it executes PBIT and then GPM. Type “rts” at the GPM prompt to call the default application. If the default application returns, it returns to GPM.
User Link (E2 - E4) on DSR negated (cable out)	Default Application → GPM When the SVME/DMV-179 boots, it calls the default application immediately. If the default application returns, it returns to GPM.
User Link (E2 - E4) on DSR asserted (terminal connected to SVME/DMV-179 Serial Channel 1)	**For FF/W 601942-106 or earlier:** PBIT → Default Application→ GPM When the SVME/DMV-179 boots, it executes PBIT and then calls the default application. If the default application returns, it returns to GPM. **For FF/W 602406-100 or later:** Recovery Mode (CBOOT parameters are not used) The card uses Foundation Firmware default parameters instead of the CBOOT parameters set in the Configuration Boot Manager (CBM). GPM When the SVME/DMV-179 boots, it executes GPM.

Cross Reference

Power-up Built-In-Test (PBIT) is an application that is run at power-up to execute a preconfigured list of Card Level Diagnostics (CLD). For more information about PBIT, see the *V8 Foundation Firmware User's Manual (808006),* included on the Technical Documentation CD-ROM.

Foundation Firmware Used During Power-Up

The card can run the following programs during power-up:

- **Power-up Built-In Test (PBIT)**: PBIT tests all major subsystems on the card. Test results are placed in the Diagnostic Results Table (DRT).
- **General Purpose Monitor (GPM)**: The GPM is the standard DY 4 monitor shipped with most SBCs. This allows users to examine memory, download and execute programs and communicate with other boards in the VME system.
- **Default Application**: This is any user application programmed into the on-board Flash. The VxWorks boot loader is initially programmed as the default application.

Initiating the Power-Up Sequence

This section describes the normal power-up behaviour of the SVME/DMV-179.

Power-Up

Switch the VME chassis on.

Initial LED Activity

Immediately on power-up, both the red FAIL LED and green STATUS LED will light up.

Once the card passes its initial diagnostics, PBIT turns the red FAIL LED off. If a diagnostic fails, the red FAIL LED remains lit. In either case, the green STATUS LED remains lit.

Cross Reference

If the red FAIL LED stays on after power-up, then PBIT has found one or more problems or the selected execution sequence did not include PBIT. Refer to the Troubleshooting section on page 3-22 for information on locating the problem.

Displaying the Initial Screen Message

After control is transferred to the GPM, pressing any key on the keyboard will inform the GPM that I/O data is being received from the serial data port. The GPM will then display a sign-on message similar to the following:

```
SVME-179 PowerPC 750 General Purpose Monitor, Version 8.0
(c) DY 4 Systems Inc.
Type ? for help
40000000*
```

The last line is the initial prompt which shows the VMEbus base address of the card. In this example the base address is 4000 0000_{H}.

Cross Reference

Type '?' at the prompt to display the help screen for the GPM. For more detailed information on using the GPM, refer to the *V8 Foundation Firmware User's Manual (808006)*.

Troubleshooting

Verify Insertion in Chassis

Power down the chassis. Make sure that the card is properly seated in the VME chassis. Because of the five-row backplane, a considerable amount of insertion force is required.

Verify that PMC Module Has 3.3 V Power

If there is a PMC module mounted on the SVME/DMV-179, it will cause unpredictable behaviour if it is not properly powered. Many PMC modules require 3.3 V power. If this is the case, ensure that 3.3 V is present on the P1 connector of the backplane. PMC 3.3 V power is obtained from the backplane, **not** the basecard.

FAIL LED Stays Lit

If the red FAIL LED stays lit after power-up, then PBIT found one or more problems or PBIT was not run. The ASCII Diagnostic Results Table (DRT) lists the results of all CLD tests run during PBIT. Each line of the displayed DRT describes a test and its overall result. Use the GPM *Dump* command to display the DRT by entering this command at the prompt:

    D 3700 A <CR>

where:

D is the memory Dump command
3700 is the address of the DRT
A means to print out the table in ASCII format for readability.

Type the *Dump* command without an address to display the next screen full of DRT data, as shown below:

    D <CR>

If the red FAIL LED is off, the DRT will confirm that all its tests passed. Refer to the *V8 Foundation Firmware User's Manual* and the *Product Release Note* for more information on the CLD routines.

Cross Reference

If the CLD does not report any results, check the power-up sequence being run. See page 3-20.

Sign-on Message Garbled

If the sign-on message is garbled, check that your terminal settings match 9600 8, N, 1 (9600 baud, 8 data bits, no parity, 1 stop bit). Also, ensure that you are using a cable compatible with the ones listed in Table 2.6 on page 2-10.

Additional Information

Cross Reference

Additional troubleshooting information (for example how to run Card Level Diagnostics to isolate problems) is available in Chapter 4 of this manual. Refer also to the FAQ database in the Support area of the DY 4 web site (www.dy4.com).

The Next Step

Cross Reference

Once the hardware is correctly configured and installed in the chassis, the next step is to install the board support package software. See the section “BSP Installation Procedure,” in Chapter 1 of your *BSP Software User’s Manual*, which is included in Acrobat pdf format on your BSP CD-ROM.

Chapter 4

Card Communications

In this chapter...

This chapter provides the following information about using the SVME/DMV-179's General Purpose Monitor (GPM):

- ❑ determining the version of Foundation Firmware on the card;
- ❑ determining the configuration of the card;
- ❑ running diagnostics;
- ❑ restoring the SEEPROM;
- ❑ restoring Foundation Firmware;
- ❑ changing the VME base address of the card;
- ❑ communicating with other cards over the VMEbus;
- ❑ Ethernet address.

Determining the Foundation Firmware Version

To determine the version of Foundation Firmware programmed on your card, type

```
cit
```

at the GPM prompt. This will display the CSCI information table as shown in Figure 4.1. The second line gives the Foundation Firmware Image #.

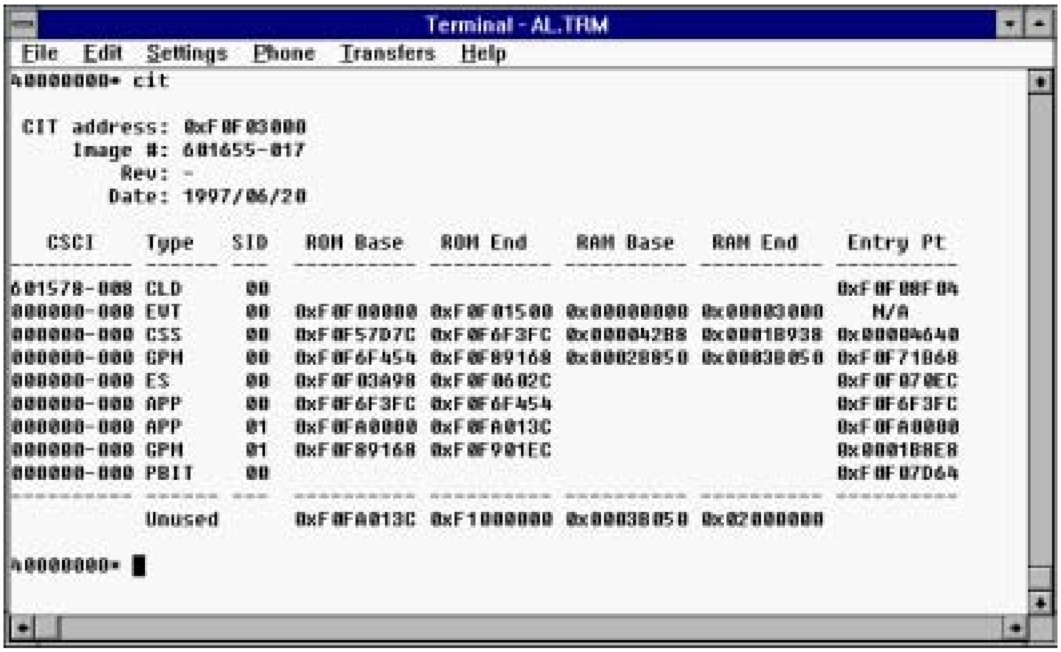


Figure 4.1 **CIT Command**

Determine the Configuration of the Card

To determine the hardware map of the card, type

```
map
```

at the GPM prompt. This will display a hardware map of the card and its PMC modules as shown in Figure 4.2.

```
40000000* map

                   Hardware map for the SVME/DMV-179

                   Base Addr.     Size      LM Addr.
                   ----------  ----------  ----------
             A24:  0x00400000  0x00080000  0x00000000
             A32:  0x40000000  0x07FFF000  0x00000000
                   ----------  ----------  ----------
       BOOT PROM:  0xFFF00000  0x00080000
      CFI1-4Mx16:  0xFE000000  0x01000000
      CFI1-4Mx16:  0xFD000000  0x01000000
            DRAM:  0x00000000  0x08000000
          NOVRAM:  0xF4008000  0x00008000
                   ----------  ----------  ----------
                   ----------  ----------  ----------

             Vendor Device HDR    Config        Memory Space Allocation
 Device name   ID     ID   TYPE Base Addr   BAR  PCI Base      Size       Type
 ----------- ------ ------ ---- ----------  --- ---------- ---------- -------
 GT-64130    0x11AB 0x6320 0x00 0x80000000
 Universe    0x10E3 0x0000 0x00 0x80003000   0  0xD0001000 0x00001000 Memory
                                             1  0xE0001000 0x00001000 I/O
 SYM53C885SC 0x1000 0x000D 0x80 0x80004000   0  0xE0000100 0x00000100 I/O
                                             1  0xD0000100 0x00000100 Memory
                                             2  0xD0002000 0x00001000 Memory
 SYM53C885ET 0x1000 0x0701 0x80 0x80004100   0  0xE0000000 0x00000100 I/O
                                             1  0xD0000000 0x00000100 Memory
 Unknown     0x1011 0x0024 0x01 0x80005000
 Unknown     0x1011 0x0019 0x00 0x80012000   0  0xE0002000 0x00000080 I/O
                                             1  0xD0100000 0x00000400 Memory
 Unknown     0x1011 0x0019 0x00 0x80012800   0  0xE0002080 0x00000080 I/O
                                             1  0xD0100400 0x00000400 Memory
 PMC642-BRDG 0x8086 0x0964 0x81 0x80005800
 PMC642      0x13F4 0x4101 0x80 0x80005900   0  0xD4000000 0x04000000 Memory

40000000*
```

Figure 4.2 **GPM MAP Command**

Running Diagnostics

If the red Fail LED on the front panel remains lit, type

```
cld
```

at the GPM prompt. This will run Card Level Diagnostics and display the results as shown in Figure 4.3.

```
50000000* cld

CLD complete: 16 diagnostics were executed

Summary;: Pass
Pass: Pass
Cpu Space Decode; : Pass
EPROM transfer: Pass
RAM data convergence: Pass
RAM address convergence: (0x0004461C-0x000455B8) Pass
RAM misaligned transfer: Pass
RAM read/write: (0x0004461C-0x000455B8) Pass
UART Loopback: Pass
UART Loopback: Pass
Universe Controllable bits: Pass
Universe Int: Pass
Universe Register Test: Pass
Universe Data Convergence 64: Pass
SCC: Data Convergence: Pass
SCC: Ch A Poll Mode, :Pass
SCC: Ch A Interrupt Mode, :Pass
SCC: Ch B Poll Mode, :Pass
SCC: Ch B Interrupt Mode, :Pass
Base Card CSR Controllable bits: Pass
RAM data convergence: Pass
RAM misaligned transfer: Pass
RAM read/write: (0xF4008000-0xF400FFFC) Pass
Partition checksum: Pass
SCSI Reg Test: Pass
SCSI Controllable bits: Pass
SCSI Data Convergence: Pass
SCSI Interrupt: Pass
SCSI LoopBack: Pass
Ethernet Reg Test: Pass
Ethernet Controllable bits: Pass
Ethernet Loopback: Pass
L2 RAM Data Test: Pass
L2 RAM Address Test: Pass
L2 Cache Miss Test: Pass
PCI-N-Bridge Reg Test: Pass
ECC Polled: Pass
ECC Interrupt: Pass
50000000*
```

Figure 4.3 CLD Results

Restoring the SEEPROM

If the CLD results indicate that the SEEPROM has failed, the simplest method of restoring it is to wipe the contents. The card Foundation Firmware will re-initialize it when it next resets.

The process to re-initialize the SEEPROM contents is:

1. From GPM, fill an area of RAM with FF:

   ```
   fil 100000 100 ff
   ```

2. Then move this into SEEPROM, thereby erasing the entire DY 4 section of the ROM:

   ```
   emv 100000 0 100
   ```

Note

This will erase all contents including VxWorks boot parameters. See the BSP Target Document (included in your BSP tree) for instructions on setting up the boot parameters.

On the first reset, the card will indicate a checksum failure and then re-initialize the SEEPROM. When the card is reset a second time, the checksum test will pass since the contents are now correct.

Restoring Foundation Firmware

Tip

If the GPM prompt is not displayed, or if you need to upgrade the Foundation Firmware, use FlashProg to reprogram the card. See the FlashProg demo on your Technical Documentation CD-ROM for detailed instructions.

Changing the Card's Base Address

Auto-ID

The Auto-ID function automatically assigns the base address of the card. Each card in the chassis participating in the Auto-ID scheme generates a unique ID code. The SVME/DMV-179 calculates its base address using this ID code and a table in its on-board serial EEPROM. See Table 4.2 on page 4-9.

The system requires an Auto-ID capable SYSCON in the left-hand slot (Slot 1). The SVME/DMV-179 can act as the SYSCON, if it is installed in Slot 1. Cards that have Auto-ID functionality should be installed in the left-hand side of the chassis in adjacent slots.

Cross Reference

To ensure reliable Auto-ID operation, VME cards which are not Auto-ID capable should be installed to the right of all Auto-ID capable cards. If your configuration includes cards which cannot support the Auto-ID function, refer to the *V8 Foundation Firmware Software User's Manual* for information on avoiding conflicts. Most DY 4 cards support the Auto-ID function.

Geographical Addressing

The SVME/DMV-179 supports the geographical addressing method for determining the VMEbus slot ID when used in VMEbus backplanes supporting this feature. When selected for geographical addressing, the SVME/DMV-179 firmware reads the geographical address and generates a unique ID code. The SVME/DMV-179 calculates its base address using this ID code and a table in its on-board serial EEPROM. See Table 4.2 on page 4-9.

Refer to "Changing the Base Address" on page 4-10 for information on how to select this feature and Table 4.1 for the standard P1 backplane configuration.

Table 4.1: Geographical Address Pin Assignments

Slot Index (Hex)	GAP* Pin P1 pin d9	GA4* Pin P1 pin d17	GA3* Pin P1 pin d15	GA2* Pin P1 pin d13	GA1* Pin P1 pin d11	GA0* Pin P1 pin d10
1	Open	Open	Open	Open	Open	GND
2	Open	Open	Open	Open	GND	Open
3	GND	Open	Open	Open	GND	GND
4	Open	Open	Open	GND	Open	Open
5	GND	Open	Open	GND	Open	GND
6	GND	Open	Open	GND	GND	Open
7	Open	Open	Open	GND	GND	GND
8	Open	Open	GND	Open	Open	Open
9	GND	Open	GND	Open	Open	GND
A	GND	Open	GND	Open	GND	Open
B	Open	Open	GND	Open	GND	GND
C	GND	Open	GND	GND	Open	Open
D	Open	Open	GND	GND	Open	GND
E	Open	Open	GND	GND	GND	Open
F	GND	Open	GND	GND	GND	GND
10	Open	GND	Open	Open	Open	Open
11	GND	GND	Open	Open	Open	GND
12	GND	GND	Open	Open	GND	Open
13	Open	GND	Open	Open	GND	GND
14	GND	GND	Open	GND	Open	Open
15	Open	GND	Open	GND	Open	GND

VME Base Addresses

The default VME 24-bit and 32-bit base addresses for each slot index are shown in hexadecimal format in Table 4.2.

Table 4.2: VMEbus Base Addresses

Slot Index (Hex)	Extended Address (A32)	Standard Address (A24)
00	Reserved	Reserved
01	4000 0000	40 0000
02	4800 0000	48 0000
03	5000 0000	50 0000
04	5800 0000	58 0000
05	6000 0000	60 0000
06	6800 0000	68 0000
07	7000 0000	70 0000
08	7800 0000	78 0000
09	8000 0000	80 0000
0A	8800 0000	88 0000
0B	9000 0000	90 0000
0C	9800 0000	98 0000
0D	A000 0000	A0 0000
0E	A800 0000	A8 0000
0F	B000 0000	B0 0000
10	B800 0000	B8 0000
11	C000 0000	C0 0000
12	C800 0000	C8 0000
13	D000 0000	D0 0000
14	D800 0000	D8 0000
15	E000 0000	E0 0000
16	E800 0000	E8 0000
17	F000 0000	F0 0000

Changing the Base Address

In some cases, you may need to bypass the Auto-ID function and use the geographical address or assign a specific VME base address. The SVME/DMV-179 card has an Auto-ID bypass byte at offset $0D_H$ in the Foundation Firmware partition of the serial EEPROM.

If the value of the Auto-ID bypass byte is FF_H, the Auto-ID value is used. If the value of this byte is FE_H, the geographical address is used. If the value of this byte is anything else, this value is used as the first five bits of the base address. See Table 4.3 on page 4-11. To modify the contents of the serial EEPROM, use the partition command as shown below.

Assume you want to assign a base address of $7800\ 0000_H$, corresponding to and Auto-ID bypass byte of $0F_H$. Follow these steps:

1. Retrieve the partition from the SEEPROM (device 0) and copy it into memory. At the GPM prompt, type:

   ```
   PART r 0 1 100000 10000<CR>
   ```

   The first four bytes of the partition contain the checksum and the size.

2. Modify the Auto-ID bypass byte in memory (at offset $0D_H + 04_H = 11_H$).

   ```
   MM 100011 b<CR>
   ```

   Type the new Auto-ID bypass byte, followed by a carriage return as follows:

   ```
   0F<CR>
   ```

3. Copy the partition back into the SEEPROM. The first four bytes of the partition are checksum and size and are set automatically. The size of the partition is 88_H.

   ```
   PART w 0 1 100004 88<CR>
   ```

4. Reset the chassis.

This procedure changes the default ID in the configuration serial EEPROM. The change will take effect on the next card reset or reboot and will remain in effect until the byte is changed again in the serial EEPROM.

Cross Reference

The simplest way of determining the card's VME base address is to connect a computer terminal directly to it and check the GPM starting message. The initial prompt always displays the VMEbus A32 base address of the card. Refer to the *V8 Foundation Firmware User's Manual* for more information.

Table 4.3: Auto-ID Bypass Byte and VME Address

Auto-ID Bypass Byte	Extended Address (A32)	Standard Address (A24)
00	Reserved	Reserved
01	0800 0000	08 0000
02	1000 0000	10 0000
03	1800 0000	18 0000
04	2000 0000	20 0000
05	2800 0000	28 0000
06	3000 0000	30 0000
07	3800 0000	38 0000
08	4000 0000	40 0000
09	4800 0000	48 0000
0A	5000 0000	50 0000
0B	5800 0000	58 0000
0C	6000 0000	60 0000
0D	6800 0000	68 0000
0E	7000 0000	70 0000
0F	7800 0000	78 0000
10	8000 0000	80 0000
11	8800 0000	88 0000
12	9000 0000	90 0000
13	9800 0000	98 0000
14	A000 0000	A0 0000
15	A800 0000	A8 0000
16	B000 0000	B0 0000
17	B800 0000	B8 0000
18	C000 0000	C0 0000
19	C800 0000	C8 0000
1A	D000 0000	D0 0000
1B	D800 0000	D8 0000
1C	E000 0000	E0 0000
1D	E800 0000	E8 0000
1E	F000 0000	F0 0000
1F	Not Valid	Not Valid
FE	Use Geographical Address	
FF	Use Auto-ID Value	

Communicating over the VMEbus

The SVME/DMV-179 can communicate serial data over the VMEbus with any DY 4 card that is running GPM.

Note

Both cards **must** be executing GPM for this to work. If either card is running a default application (such as VxWorks), this will not work.

Set up the cards as follows:

- On the primary card, make sure that the user link (E2 - E4) is not connected. Connect a terminal to Serial Channel 1.
- On the secondary card, make sure that the user link (E2 - E4) is not connected and that the CH1DSR signal is connected to ground. CH1DSR is accessible at P0-E1 and P2-D19. (You may connect a terminal to Serial Channel 1 instead of connecting CH1DSR to ground.)
- Reset the chassis.
- If there is a terminal connected to the secondary card, **do not** press a key after resetting the card.

Figure 4.4 shows how to establish a serial connection over the VMEbus to another card. The computer terminal establishes a serial data connection through the primary card to the VMEbus and into the GPM through the secondary card. In this way, you can connect to any DY 4 card in the system from a host computer terminal.

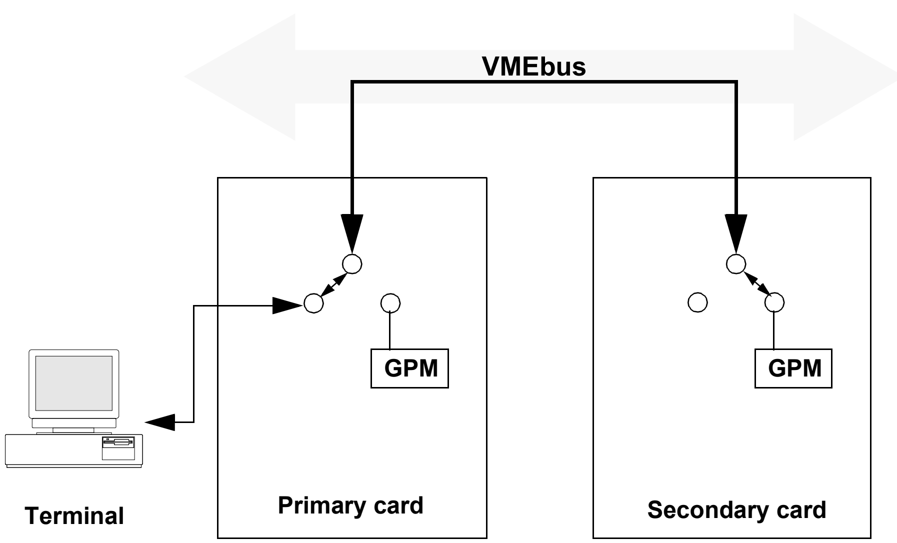


Figure 4.4 Serial Data Communications over the VMEbus

Establishing the Link

To establish serial data communications over the VMEbus, use the GPM Communicate command. The command syntax is as follows:

```
XX000000* C YY000000 <cr><cr>
```

where:

XX000000 is the monitor prompt which displays the Primary card's base address
C is Connect Command
YY000000 is the Secondary card's base address.

The second <cr> could be any character on the keyboard. It lets the secondary card's GPM know that I/O data is being transmitted from the VMEbus (from a card attached to a computer terminal).

The GPM on the secondary card then responds with its sign-on message and prompt with its base address. The following is an example:

```
SVME/DMV-179 750 General Purpose Monitor Version 8.0
(c) DY 4 Systems Inc.
Type ? for help
58000000*
```

Terminating the Link

There are two methods of terminating communication link:

- Typing the **Disconnect** <Ctrl-K> character shuts down the communications link but leaves the remote card running
- Typing the **Abort** <Ctrl-\> character terminates the communication and aborts the remote card.

Cross Reference

Refer to the *V8 Foundation Firmware User's Manual*, included in the documentation package CD-ROM, for more details on the Communicate command.

Ethernet Address

Each SVME/DMV-179 card is pre-programmed with a unique Ethernet address. The three high bytes are 00_H, 80_H, $7F_H$ and the lower three bytes are a unique number.

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