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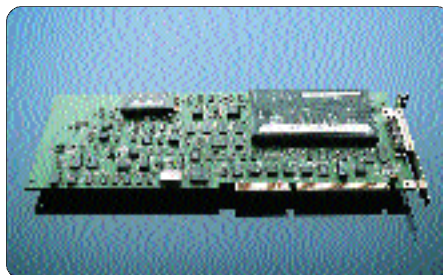
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## DT2831 Series

### “Hands-Off” Analog and Digital I/O

The DT2831 Series is a family of high-speed, dual-DMA analog and digital I/O boards for IBM PC AT compatibles. Fully software-controlled, all DT2831 Series configuration and calibration is accomplished using software. High speed Continuous Performance (gap-free) A/D or D/A transfers are provided by two DMA channels—you'll never lose another data point. For phase coherence between samples (sampling all channels within  $\pm 5\text{ns}$ ), Simultaneous Sample and Hold (SS&H) inputs are available. SS&H models also feature high throughput (160 kS/s or 250 kS/s), 12- or 16-bit resolution, and patented Real-Time Error Prevention™ circuitry. All DT2831 Series boards feature two high-speed analog outputs, eight digital I/O, and two user counter/timers.



M-5285

- “Hands-Off” design means all operating parameters are software-selectable and can be fully calibrated by the software
- Dual-DMA design allows high-speed continuous performance (no lost samples)
- Steel-encased A/D converter module, shielded I/O connectors, and careful analog circuit design reduce noise pickup errors
- Simultaneous Sample and Hold models feature throughputs of 160 kS/s or 250 kS/s, 12- or 16-bit resolution, and Real-Time Error Prevention™ circuitry

### Summary

**A/D:** 12 or 16 bits; 33 to 250 kS/s throughput; gains to 500; SSH available

**D/A:** 2 DACs; 12 or 16 bits; 100 or 130 kS/s throughput per DAC

**Digital I/O:** 8 lines

**Clocks:** Two programmable clocks

**Counter/Timers:** Two 16-bit counter/timers

**Interface:** Dual-channel DMA, or programmed I/O; one interrupt

### Analog Inputs

	Resolution (bits)	Throughput (kS/s)	Input Channels	Gain	Ranges (V)	System Error (% of FSR)	Total Harmonic Distortion (dB)**	Conversion Time ( $\mu\text{s}$ )	CMRR (dB @ 60 Hz)	Channel-to-Channel Aperture Uncertainty (ns)	Max. Input Volt Protection (On/Off)
DT2831	12 (.024% FSR)	50	16SE/8DI*	1,2,4,8	0–1.25, 2.5, 5, 10 $\pm 1.25, 2.5, 5, 10$	.03, G=1 .05, G=8	–80 @11 kS/s	11	80	—	$\pm 35/\pm 20$
DT2831-G	12 (.024% FSR)	250	16SE/8DI	1,2,4,8	0–1.25, 2.5, 5, 10 $\pm 1.25, 2.5, 5, 10$	.03, G=1 .05, G=8	–82 @41 kS/s	2	80	—	$\pm 27/\pm 12$
DT2833	12 (.024% FSR)	250	8DI, SS&H	1	0–10 $\pm 10$	.04	–77 @40 kS/s	3.5	76	$\pm 5$	$\pm 25/\pm 12$
DT2835	12 (.024% FSR)	50, G 10 2.5, G 100	16SE/8DI*	1,10,100, 500	0–.02, .1, 1, 10 $\pm .02, .1, 1, 10$	.03, G=1 .10, G=500	–80 @11 kS/s	11	80	—	$\pm 35/\pm 20$
DT2836	16 (.0015% FSR)	33	16SE/8DI*	1,2,4,8	0–1.25, 2.5, 5, 10 $\pm 1.25, 2.5, 5, 10$	.0024, G=1 .0140, G=8	–96 @1 kS/s	25	80	—	$\pm 35/\pm 20$
DT2837	16 (.0015% FSR)	33, G 10 2.6, G 100	16SE/8DI*	1,10,100, 500	0–.02, .1, 1, 10 $\pm .02, .1, 1, 10$	.0024, G=1 .0479, G=500	–96 @1 kS/s	25	80	—	$\pm 35/\pm 20$
DT2838	16 (.0015% FSR)	160	8DI, SS&H	1	0–10 $\pm 10$	.024	–90 @1.1 kS/s	6.25	80	$\pm 5$	$\pm 35/\pm 20$

\*With multiple DT727 panels, up to 256SE/128DI.

\*\*Total harmonic distortion is measured at a gain of one, sampling at maximum board throughput.

### Analog Outputs

	DACs	Resolution (bits)	Throughput (kS/s)	Ranges (V @ $\pm 5$ mA min)	Settling Time ( $\mu\text{s}$ )	Error (% of FSR)	Drift (ppm of FSR/°C)
DT2831, DT2833, DT2835, DT2831-G	2	12 (.024% FSR)	130/DAC	0–10, $\pm 10$	5	$\pm .012$	$\pm 10$ , Zero $\pm 30$ , Gain
DT2836, DT2837, DT2838	2	16 (.0015% FSR)	100/DAC	0–10, $\pm 10$	9	$\pm .012$	$\pm 2$ , Zero $\pm 2$ , Gain

## DT2831 Series

**BUS: ISA**

**Type: Hands Off**

## Ordering Summary

All Data Translation products are covered by a 1-year warranty. For pricing information, see a current price list, visit our web site, or contact your local reseller.

Each DT2831 Series board ships with a DT-Open Layers device driver for Windows 95/98, diagnostics, and a comprehensive user manual.

- DT2831—50 kS/s, 12-bit, autocal A/D, PGH
- DT2831-G—250 kS/s, 12-bit A/D, PGH
- DT2833-SSH, 250 kS/s, 12-bit A/D
- DT2835—Low-level, 12-bit, autocal A/D, PGL
- DT2836—16-bit A/D, PGH; 16-bit D/A
- DT2837—16-bit A/D, PGL; 16-bit D/A
- DT2838-SSH, 16-bit A/D; 16-bit D/A

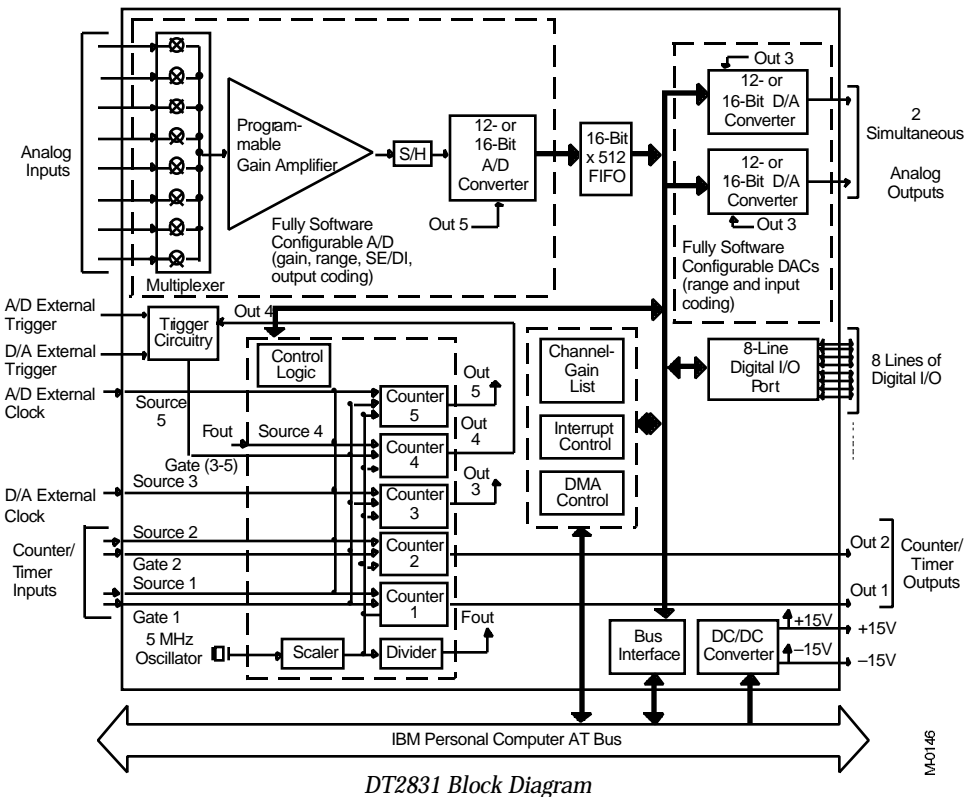
### Accessories

- DT717—Screw terminal panel
- DT717-T—Panel for thermocouples
- DT727—Channel expansion panel and cable
- EP226—95 m (3.2 ft.) unshielded cable
- EP227—95 m (3.2 ft.) shielded cable
- EP227-3—3 m (10 ft.) version of EP227
- EP229—Enclosure for DT717 or DT717-T

### Software

The following products include a copy of the software, a single-user license, and a user manual. All software is supplied on CD-ROM, except as noted.

- HP VEE with DT VPI visual programming software Version 5.0 for Windows 95/98 SP1950-CD
- HP VEE Lab with DT VPI visual programming software version 5.0 for Windows 95/98 SP1950-CD
- TestPoint software for designing test, measurement and D/A applications for Windows 95/98 SPTPX-CD (see page 32 for details)
- DTx-EZ visual programming tools for Visual Basic and Visual C++ for Windows 95/98 SP0970-CD
- DataAcq SDK Software Development Kit for Windows 95/98 SP0945-CD
- DT-LV Link data acquisition connection to LabVIEW for Windows 95/98, on 3.5 in. 1.4 MB disk SP0810-CL



DT2831 Block Diagram

MA0146

## Specifications

All specifications are typical at 25° C and rated voltage, unless otherwise specified.



### DIGITAL I/O

**Number of Lines**  
8, organized as a single port that can be set for input or output

**Fanout**  
15 ALSTTL loads

**Input Load**  
1 ALSTTL load; unused inputs float

### PACER CLOCK

**Function**  
Independent A/D and D/A pacer clocks initiate A/D or D/A conversions; clocks are started by software trigger or external trigger.

**Usable Range**  
From 4µs (250 kS/s) to 14 min, 19 s (.001 Hz)

**Description**  
Each pacer clock consists of a 16-bit counter plus an external (4 MHz, TTL levels) or onboard frequency source; the onboard frequency source consists of a 5 MHz (.2 µs increments)

oscillator plus a scaler (divides by 1, 10, 16, 100, 256, 1,000, 4,096, 10,000, or 65,536).

### COUNTER/TIMERS

Two 16-bit counter/timers; built-in 5 MHz oscillator

### OPERATING MODES

**A/D**  
Channel/Gain Selection—512-element channel-gain list  
**Operation**—single scan (once through channel-gain list); continuous scan (continuous through channel-gain list); triggered scan (single scans initiated by onboard clock; interval between scans is programmable)  
**Data Transfer**—programmed I/O; single-channel DMA; dual-channel (Continuous Performance) DMA

### D/A

**Channel Selection**—either channel singly or both channels simultaneously

**Data Transfer**—programmed I/O; single-channel DMA; dual-channel (Continuous Performance) DMA

Simultaneous A/D, D/A  
A/D and D/A single-channel DMA transfers can be performed simultaneously

### GENERAL

**Interface**  
IBM PC AT bus or EISA bus; I/O mapped, 10-bit I/O address; 16-bit data path; one or two DMA channels

**Interrupt**—one line, software-selected level; source: A/D, D/A done; A/D, D/A DMA done; A/D, D/A error; A/D scan done; counter/timer 1, counter/timer 2 terminal count

### Power

**Requirements**  
+5 V @ 2.8 A typical; low-noise ±15 V generated by onboard DC/DC converter

**Physical/Environmental**  
**Dimensions**—full-size PC AT board mechanically compatible with ISA system slots only; 11.4 x 33.6 x 1.9 cm (4.5 in. x 13.25 in. x .75 in.)

**Temperature**—operating: 0 to 70° C; storage: -25 to 70° C

**Relative Humidity**—to 95%, non-condensing

**EMI Compliance**—all models are FCC Class A verified; will not compromise FCC compliance of host computer



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