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VMIVME-7589

Single Board Pentium® Processor-Based VMEbus CPU

Product Manual

12090 South Memorial Parkway
Huntsville, Alabama 35803-3308, USA
(256) 880-0444 ◆ (800) 322-3616 ◆ Fax: (256) 882-0859

500-007589-000 Rev. B
11-May-1998

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Overview

Introduction

VMIC's VMIVME-7589 is a complete IBM PC / AT-compatible Pentium® processor-based computer with the additional benefits of single Eurocard construction and full compatibility with the VMEbus Specification Rev. C.1. The VMIVME-7589 with advanced VMEbus interface and RAM that is dual-ported to the VMEbus, is ideal for multiprocessor applications.

The single CPU board functions as a standard PC / AT, executing a PC / AT-type power-on self-test, then boots up MS-DOS®, Windows® 3.11, Windows 95, Windows NT®, or any other PC / AT-compatible operating system. The PC / AT mode of the VMIVME-7589 is discussed in Chapter 3 of this manual.

The VMIVME-7589 also operates as a VMEbus controller and interacts with other VMEbus modules by adding the optional PCI-to-VMEbus bridge mezzanine.

The VMIVME-7589 may be accessed as a VMEbus slave board. The VMEbus functions are available by programming the VMIVME-7589's PCI-to-VMEbus bridge according to the references defined in this volume and / or in the second volume dedicated to the optional PCI-to-VMEbus interface board titled: *VMIVME-7589 Tundra Universe™-Based VMEbus Interface Option Product Manual (document No. 500-7589000-001 Rev. 1.1).*

The VMIVME-7589 programmer may quickly and easily control all the VMEbus functions simply by linking to a library of VMEbus interrupt and control functions. This library is available with VMIC's VMISFT-9420 IOWorks Access software for Windows NT users.

The VMIVME-7589 also provides capabilities beyond the features of a typical IBM PC / AT compatible CPU including general-purpose timers, a programmable watchdog timer, a bootable Flash Disk system, and nonvolatile, battery-backed SRAM. These features make the unit ideal for embedded applications. These nonstandard PC / AT functions are discussed in Chapter 4 of this manual.

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Organization of the Manual

This manual is composed of the following chapters and appendices:

Chapter 1 - VMIVME-7589 Features and Options describes the features of the base unit followed by descriptions of the associated features of the unit in operation on a VMEbus. The interface configuration includes the option to attach a VMEbus interface.

Chapter 2 - Installation and Setup describes unpacking, inspection, hardware jumper settings, connector definitions, installation, system setup, and operation of the VMIVME-7589.

Chapter 3 - PC/AT Functions describes the unit design in terms of the standard PC memory and I/O maps, along with the standard interrupt architecture.

Chapter 4 - Embedded PC/RTOS Features describes the unit features that are beyond standard PC/AT functions.

Chapter 5 - Maintenance provides information relative to the care and maintenance of the unit.

Appendix A - Connector Pinouts illustrates and defines the connectors included in the unit's I/O ports.

Appendix B - System Drive Software includes detailed instructions for the installation of the drivers during installation of Windows for Workgroups Version 3.11, Windows 95, or Windows NT (Versions 3.5x and 4.0) operating systems.

Appendix C - Basic Input/Output System describes the menus and options associated with the AMI (system) BIOS.

Appendix D - Device Configuration: I/O and Interrupt Control provides the user with the information needed to develop custom applications such as the revision of the current BIOS configuration to a user-specific configuration.

Appendix E - Sample C Software provides a library of sample code the programmers may utilize to build the required application software for their system.

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References

For the most up-to-date specifications for the VMIVME-7589, please refer to:

VMIC specification number 800-007589-000

The following books refer to the Tundra Universe-based interface option available in the VMIVME-7589:

VMIVME-7589, Tundra Universe™-Based VMEbus Interface Option Product Manual
VMIC Doc. No. 500-007589-001

VMEbus Interface Components Manual
Tundra Semiconductor Corporation
603 March Rd.
Kanata, Ontario
Canada, K2K 2M5
(613) 592-0714 FAX (613) 592-1320
www.tundra.com

PCI bus Interface and Clock Distribution Chips
PLX Technology, Inc.
625 Clyde Avenue
Mountain View, CA 94043
(415) 694-2800 (415) 960-0479
www.plxtech.com

Some reference sources helpful in using or programming the VMIVME-7589 include:

Pentium® and Pentium Pro Processors and Related Products
Intel Literature Sales
P.O. Box 7641
Mt. Prospect, IL 60056-7641
(800) 548-4752
www.intel.com

Pentium® Processor at 150 MHz, 166 MHz, and 200 MHz
February 1996, Order Number 242769-003
Intel Corporation
2200 Mission College Blvd.
P.O. Box 58119
Santa Clara, CA 95052-8119
(408) 765-8080
www.intel.com

Programmer's Guide to the AMIBIOS
American Megatrends, Inc.
6145-F Northbelt Parkway
Norcross, GA 30071
www.megatrends.com

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Award BIOS

Award Software International, Inc.
777 East Middle Field Road
Mountain View, CA 94043-4023
(650) 237-6800 FAX: (650) 968-0274 BBS: (650) 968-0249
www.award.com

Pentium® Processor with MMX™ Technology

January 1997, Order Number 243185-001
Intel Corporation
2200 Mission College Blvd.
P.O. Box 58119
Santa Clara, CA 95052-8119
(408) 765-8080
www.intel.com

Intel 430TX PCIset

82441FX PCI and Memory Controller (PMC)
82442FX Data Bus Accelerator (DBX)
May 1996, Order Number 290549-001
Intel Corporation
2200 Mission College Blvd.
P.O. Box 58119
Santa Clara, CA 95052-8119
(408) 765-8080
www.intel.com

PCI Special Interest Group

P.O. Box 14070
Portland, OR 97214
(800) 433-5177 (U.S.) (503) 797-4207 (International)
FAX (503) 234-6762
www.pcisig.com

The VMEbus interrupt and control software library references included for Windows NT:

VMISFT-9420 IOWorks Access User's Guide

Doc. No. 520-009420-910
VMIC
12090 South Memorial Parkway
Huntsville, AL 35803-3308
(800) 322-3616 FAX: (205) 882-0859
www.vmic.com

For a detailed description and specification of the VMEbus, please refer to:

VMEbus Specification Rev. C. and The VMEbus Handbook

VMEbus International Trade Association (VITA)
7825 East Gelding Drive
Suite No. 104
Scottsdale, AZ 85260
(602) 951-8866 FAX: (602) 951-0720
www.vita.com

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Safety Summary

The following general safety precautions must be observed during all phases of the operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of this product.

VME Microsystems International Corporation assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VME Microsystems International Corporation for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this system. Use extreme caution when handling, testing, and adjusting.

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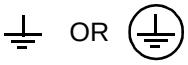
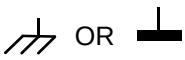
Safety Symbols Used in This Manual

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 V are so marked).



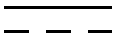
Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.



Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

Alternating current (power line).



Direct current (power line).

Alternating or direct current (power line).

The STOP symbol informs the operator the that a practice or procedure should not be performed. Actions could result in injury or death to personnel, or could result in damage to or destruction of part or all of the system.

The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, which, if not correctly performed or adhered to, could result in injury or death to personnel.

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, a practice, or a condition, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

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Notation and Terminology

This product bridges the traditionally divergent worlds of Intel-based PC's and Motorola-based VMEbus controllers; therefore, some confusion over "conventional" notation and terminology may exist. Every effort has been made to make this manual consistent by adhering to conventions typical for the Motorola/VMEbus world; nevertheless, users in both camps should review the following notes:

- Hexadecimal numbers are listed Motorola-style, prefixed with a dollar sign: $F79, for example. By contrast, this same number would be signified 0F79H according to the Intel convention, or 0xF79 by many programmers. Less common are forms such as $F79_h$ or the mathematician's $F79_{16}$.
- An 8-bit quantity is termed a "byte," a 16-bit quantity is termed a "word," and a 32-bit quantity is termed a "longword." The Intel convention is similar, although their 32-bit quantity is more often called a "doubleword."
- Motorola programmers should note that Intel processors have an I/O bus that is completely independent from the memory bus. Every effort has been made in the manual to clarify this by referring to registers and logical entities in I/O space by prefixing I/O addresses as such. Thus, a register at "I/O $140" is not the same as a register at "$140," since the latter is on the memory bus while the former is on the I/O bus.
- Intel programmers should note that addresses are listed in this manual using a linear, "flat-memory" model rather than the old segment:offset model associated with Intel Real Mode programming. Thus, a ROM chip at a segment:offset address of C000:0 will be listed in this manual as being at address $C0000. For reference, here are some quick conversion formulas:

Segment:Offset to Linear Address

Linear Address = (Segment × 16) + Offset

Linear Address to Segment:Offset

Segment = ((Linear Address ÷ 65536) – *remainder*) × 4096

Offset = *remainder* × 65536

Where *remainder* = the fractional part of (Linear Address ÷ 65536)

Note that there are many possible segment:offset addresses for a single location. The formula above will provide a unique segment:offset address by forcing the segment to an even 64 Kbyte boundary, for example, $C000, $E000, etc. When using this formula, make sure to round the offset calculation properly!

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CHAPTER 1

VMIVME-7589 Features and Options

Contents

Introduction

The VMIVME-7589 performs all the functions of a standard IBM PC / AT motherboard with the following features:

- Single-slot VMEbus 6U size
- Includes a current high-performance Intel Pentium® processor
- Low-power split voltage-based design
- Up to 128 Mbyte of Synchronous DRAM
- 64-bit PCI SVGA video graphics accelerator
  - 2 Mbyte SGRAM Video Memory
  - Resolutions up to 1280 x 1024 x 256 colors, 1500 x 1200 x 256 colors, or 800 x 600 x 16 M colors
- Battery-backed clock / calendar
- Front panel reset switch and miniature speaker
- On-board ports for keyboard and mouse, Ultra-IDE hard drive, floppy drive, Ethernet, video, serial, and parallel I / O
- Front panel “vital sign” indicators (power, Ultra-IDE hard drive activity, VMEbus SYSFAIL, and Ethernet status)
- Three general-purpose programmable 16-bit timers
- Software-controlled watchdog timer
- 8 Mbyte of bootable flash on secondary IDE
- 32 Kbyte of battery-backed SRAM

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The VMIVME-7589 supports standard PC / AT I / O features such as those listed in Table 1-1. Figure 1-1 on page 25 shows a block diagram of the VMIVME-7589 emphasizing the I / O features, including the optional PCI-to-VMEbus bridge option.

Table 1-1 PC/AT I/O Features

I/O FEATURE	IDENTIFIER	PHYSICAL ACCESS
Two Serial Ports (16550-Compatible RS-232C)	COM1, COM2	Front Panel, Micro-D 9-Pin
One Enhanced Parallel Port, Supports ECP / EPP Modes	Parallel	Front Panel Micro-D 25-Pin
AT-Style Keyboard Controller with PS / 2-Style Adapter	KYB	Front Panel PS / 2-Style Connector, Mini-DIN Circular (female)
PS / 2 Mouse	MSE	Front Panel PS / 2-Style Connector, Mini-DIN Circular (female)
Real-Time Clock / Calendar with Battery and Watchdog Timer	Date, Time	
Super VGA Video Controller with 2 Mbyte DRAM	SVGA	Front Panel DB15HD High Density (female)
Ethernet, 10BaseT, 100BaseTx, Novell NE-2000 Compatible	LAN	Front Panel RJ45
Floppy Disk Controller (two drives maximum)	Drives A, B	34-pin Header Flat Cable Type
Ultra IDE Fixed Disk Controller (two drives maximum)	Drives C, D	40-pin Header Flat Cable Type
Hardware Reset	RST	Front Panel Push-Button
IBM / PC Sound	Beep	Front Panel Speaker Port
Power Status, Hard Drive Activity, and Ethernet Status	LED Indicators	Front Panel

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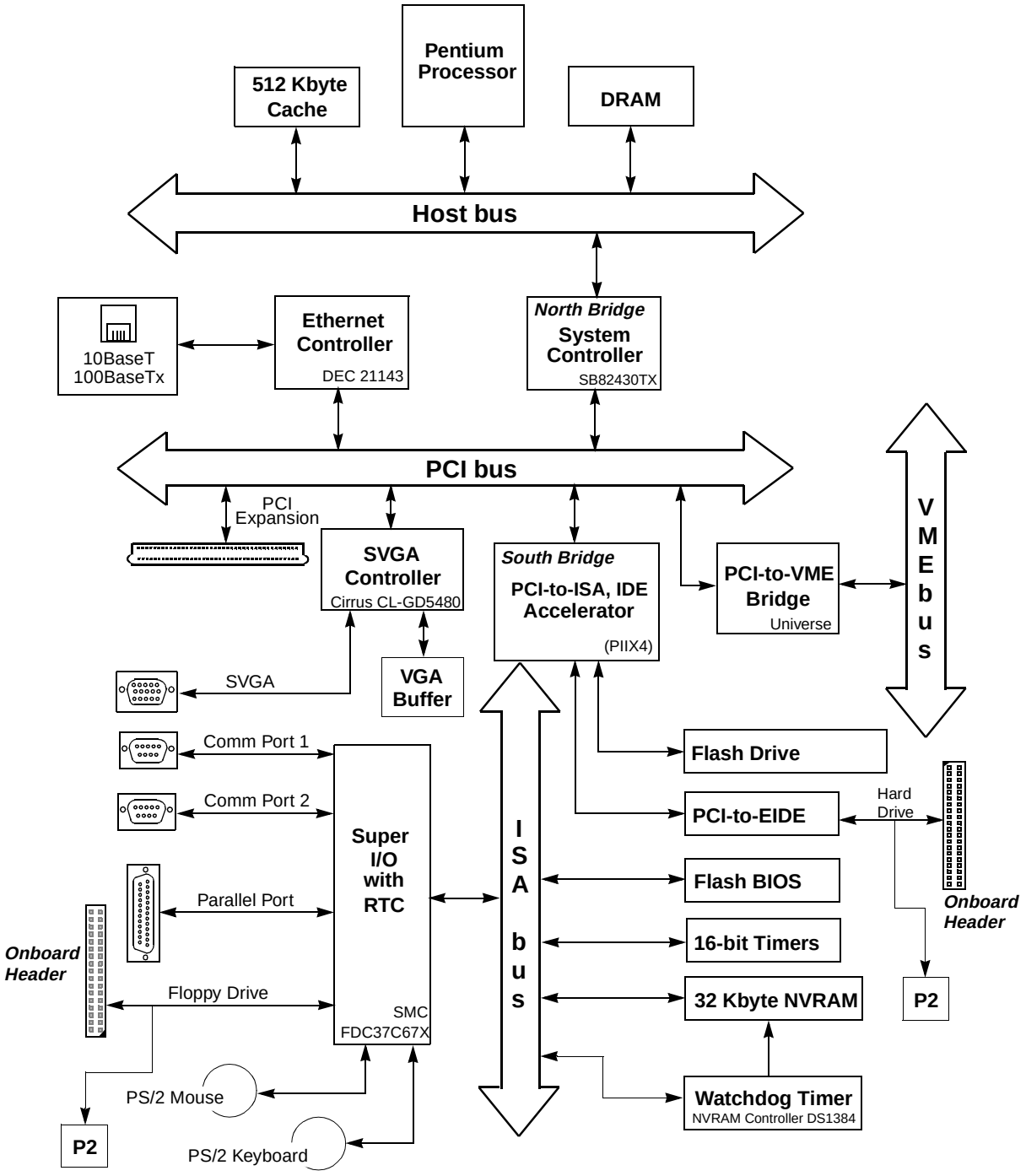

Figure 1-1 VMIVME-7589 Block Diagram

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VMEbus Features

In addition to its PC / AT functions, the VMIVME-7589 has the following VMEbus features when purchased with the Universe-based bridge option:

- Single-slot, 6U height VMEbus board
- Complete six-line Address Modifier (AM-Code) programmability
- VME data interface with separate hardware byte / word swapping for master and slave accesses
- Support for VME64 multiplexed MBLT 64-bit VMEbus block transfers
- User-configured interrupter
- User-configured interrupt handler
- System Controller mode with programmable VMEbus arbiter (PRI, SGL, and RRS modes are supported)
- VMEbus BERR* bus error timer (software programmable)
- Slave access from the VMEbus to local RAM and mailbox registers
- Full-featured programmable VMEbus requester (ROR, RWD, and BCAP modes are supported)
- System Controller autodetection
- Complete VMEbus master access through five separate Protected-mode memory windows

Figure 1-2 illustrates the VMIVME-7589 functions in a typical VMEbus system. The VMIVME-7589 is a versatile single-board solution for VMEbus control with familiar PC / AT operation.

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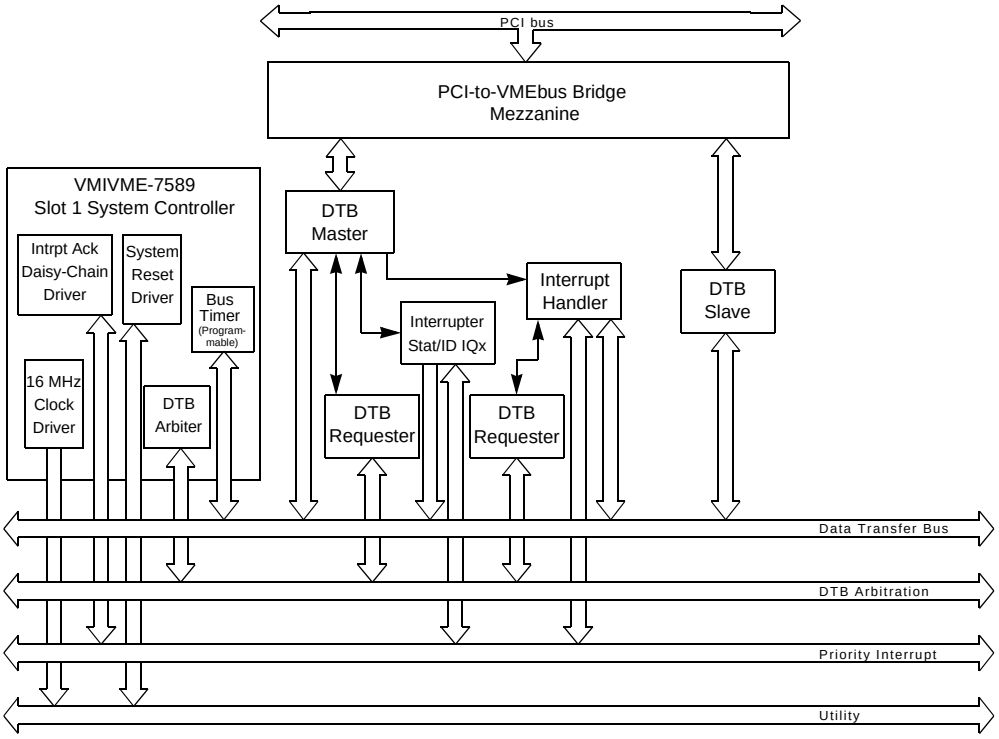

Figure 1-2 VMIVME-7589 VMEbus Functions

VMIVME-7589 Product Options

VMIC's VMIVME-7589 is built around three fundamental hardware configurations. These involve processor power, RAM memory, and the user interface. *These options are subject to change based on emerging technologies and availability of vendor configurations.*

The options and current details available with the VMIVME-7589 are defined in the device specification sheet available from your VMIC representative.

The VMIVME-7589 VMEbus interface is provided by the PCI-to-VMEbus bridge mezzanine built around the Tundra Semiconductor Corporation Universe VMEbus interface chip. The Universe provides a reliable high-performance 64-bit VMEbus-to-PCI interface in one design. The functions and programming of the Universe-based VMEbus are addressed in detail in a separate associated manual to this product. The manual titled: The *VMIVME-7589 Tundra Universe™ Based VMEbus Interface Option Product Manual* is provided with the purchase of the PCI-to-VMEbus bridge option.

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CHAPTER
2

Installation and Setup

Contents

Introduction

This chapter describes the hardware jumper settings, connector definitions, installation, system setup, and operation of the VMIVME-7589. The PCI-to-VMEbus bridge option and the Tundra Universe-based interface are also included.

Unpacking Procedures

Any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC Customer Service together with a request for advice concerning the disposition of the damaged item(s).

Some of the components assembled on VMIC's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high energy electrostatic field. When the board is placed on a bench for configuring, etc., it is suggested that conductive material be placed under the board to provide a conductive shunt. Unused boards should be stored in the same protective boxes in which they were shipped.

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Hardware Setup

The VMIVME-7589 is factory populated with user-specified options as part of the VMIVME-7589 ordering information. The CPU speed and RAM size are not user-upgradable. To change CPU speeds or RAM size, contact customer service to receive a Return Material Authorization (RMA).

VMIC Customer Service is available at: 1-800-240-7782.

The VMIVME-7589 is tested for system operation and shipped with factory-installed header jumpers. The physical location of the jumpers and connectors for the single board CPU are illustrated in Figure 2-1 on page 31. The definitions of the CPU board jumpers and connectors are included in Table 2-1 through Table 2-13. The Tundra Universe-based PCI-to-VMEbus Bridge jumper configuration is discussed in a following section.

All jumpers are factory configured and should not be modified by the user. There are four exceptions: the Programmable Timer Clock Select (J36), the IDE Routing Option (J12), the Password Clear (J33), and the Watchdog Timer (J30).

Modifying any other jumper will void the Warranty and may damage the unit. The default jumper condition of the VMIVME-7589 is expressed in Table 2-1 through Table 2-9 with **bold text** in the table cells.

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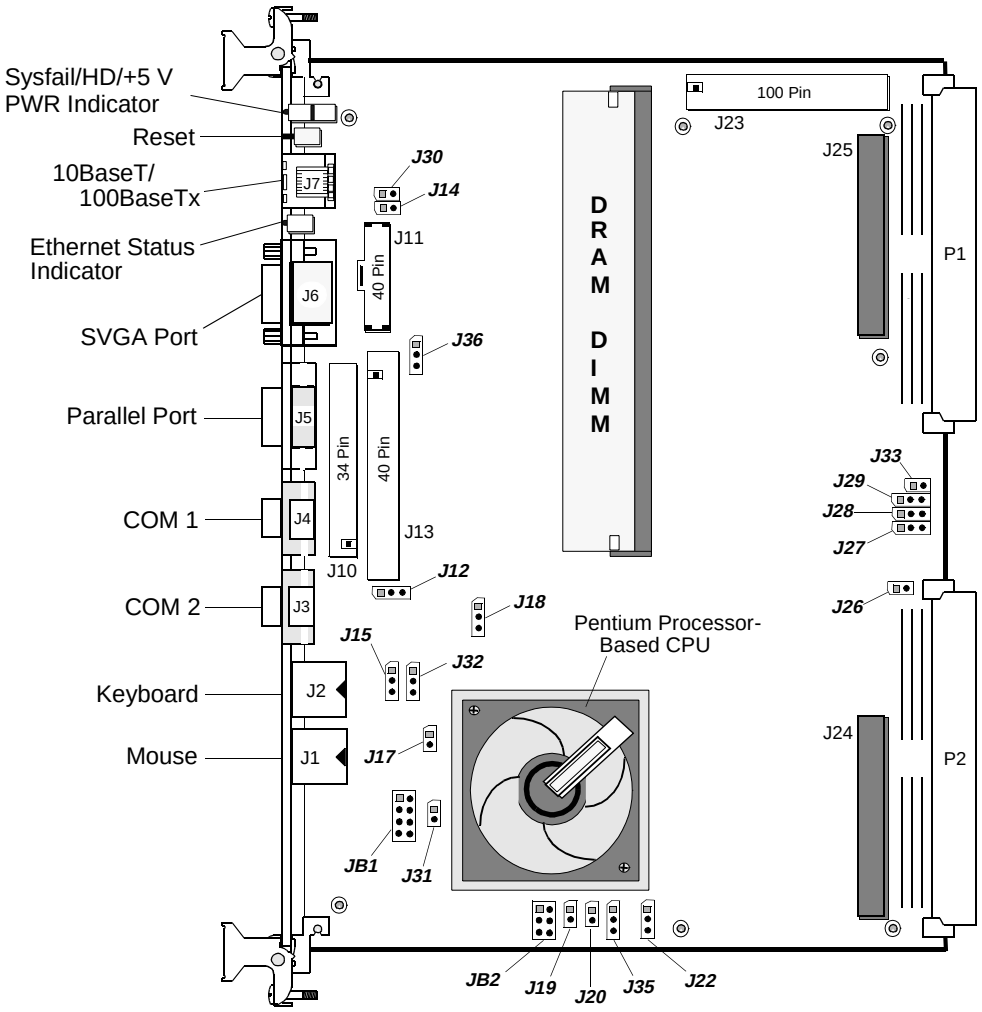

Figure 2-1 VMIVME-7589 CPU Board, I/O Port, and Jumper Locations

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Table 2-1 CPU Board Connectors

Connector	Function
J1	Mouse Connector
J2	PS/2 Keyboard Connector
J3	COM2
J4	COM1
J5	Parallel Port Connector
J6	Video Connector
J7	Ethernet Connector
J10	Floppy Interface Connector
J11	Port 80 Test Interface
J13	EIDE Connector
J18	Fan Connector
J23	PCI Expansion Connector
J24, J25	PCI/VME Connectors
P1, P2	VME Connectors

Table 2-2 CPU Bus Frequency Select - Jumpers (J27, J28, and J42)

CPU Bus Frequency (MHz)	PCI Bus Frequency (MHz)	J27 Position	J28 Position	J29 Position
60	30	2-3	2-3	2-3
66.6	33.3	2-3	2-3	1-2
50	25	2-3	1-2	2-3
55	27.5	2-3	1-2	1-2
Reserved	Reserved	1-2	2-3	2-3
83.3	33.3	1-2	2-3	1-2

Table 2-3 Programmable Timer Clock Select (**User Configurable**) - Jumper (J36)

Select	Jumper Position
2 MHz	1-2
1 MHz	***2-3***

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Table 2-4 CPU Selection - Jumpers (J19 and J20)

Jumper	M1	*Others*
J19	Out	***In***
J20	Out	***In***

Table 2-5 Fan Connector Option - Jumper (J18)

Select	Jumper Position
+5 V	***1-2***
+12 V	2-3

Table 2-6 CPU Power Supply Option - Jumpers (J15, J17, J31, J32, and JB1)

Select	J15	J17	J31	J32	JB1
VIO=3.3 V, VCORE=3.3 V	2-3	Out	1-2	1-2	In
VIO=3.3 V, VCORE=2.8 V	2-3	In	1-2	1-2	Out
VIO=3.3 V, VCORE=2.9 V	2-3	In	1-2	2-3	Out
VIO=3.3 V, VCORE=3.2 V	2-3	Out	2-3	1-2	In
VIO=3.3 V, VCORE=2.5 V	2-3	Out	1-2	1-2	Out
VCORE=VRE	1-2	X	1-2	X	X

Table 2-7 CPU Clock/Bus Multiple - Jumper Blocks (J35 and JB2)

Core/Bus Speed Ratio	Intel Based		Other (Non-Intel) Based	
	J35	JB2	J35	JB2
1X	NA	OUT	OUT	OUT
2X	NA	3-5, 2-4	Out	3-5, 2-4
5/2X	NA	3-5, 4-6	Out	3-5, 4-6
3X	NA	1-3, 4-6	Out	1-3, 4-6
7/2X	NA	1-3, 2-4	Out	1-3, 2-4

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Table 2-7 CPU Clock/Bus Multiple - Jumper Blocks (J35 and JB2)

Core/Bus Speed Ratio	Intel Based		Other (Non-Intel) Based	
	J35	JB2	J35	JB2
4X	NA	NA	In	3-5, 2-4
9/2X	NA	NA	In	3-5, 4-6
5X	NA	NA	In	1-3, 4-6
11/2X	NA	NA	In	1-3, 2-4

Table 2-8 EIDE Routing Option (**User Configurable**) - Jumper (J12)

Select	Jumper Position
Ultra IDE Onboard Header	***1-2***
P2	2-3

Note

The default jumper position of 1-2 on J12 enables the utilization of the onboard headers J10 for the floppy drive interface and J13 for an IDE harddrive interface. If the user is configuring the VMIVME-7589 for using a VMIVME-7452 with a P2 option, J12 should be placed in the 2-3 position.

Table 2-9 PCI/VME Mezzanine Option - Jumper (J26)

Select	Jumper Position
Mezzanine Installed	Out
Mezzanine Not Installed	In

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Table 2-10 BIOS Mode Option - Jumper (J14)

Select	Jumper Position
Boot Block Programming	In
No Program	***Out***

Table 2-11 430TX Clock Select - Jumper (J22)

CPU Clock	Jumper Position
66 MHz	1-2
60 MHz	2-3

Table 2-12 Watchdog Timer (**User Configurable**) - Jumper (J30)

Select	Jumper Position
RTCRESET	In
No RTCRESET	***Out***

Table 2-13 Password Clear (**User Configurable**) - Jumper (J33)

	Jumper Position
Normal	***Out***
Clear NVRAM/CMOS/ Password	In

Note

The VMIVME-7589's BIOS has the capability (not currently enabled) of password protecting casual access to the unit's CMOS set-up screens. The Password Clear jumper (J33) allows for a means to clear the password feature, as might be necessary to do in the case of a forgotten password.

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To clear the CMOS:

1. Turn off power to the unit
2. Install a jumper at J33
3. Power up the unit
4. Turn off the power to the unit and remove the jumper from J33

When power is reapplied to the unit, the CMOS will be cleared.

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VMIVME-7589, Tundra Universe™-Based PCI-to-VMEbus Bridge

The optional Tundra Universe-based PCI-to-VMEbus bridge is tested for system operation and shipped with factory-installed header jumpers. The bridge is shipped with the unit as part of the VMIVME-7589. Figure 2-2 illustrates the physical location of the user-configurable jumpers and connectors on the bridge option. Table 2-14 lists each jumper designator, its function, and the factory-installed default configuration.

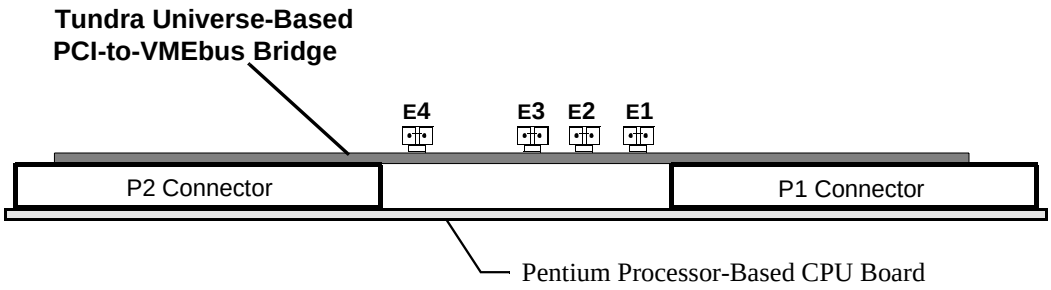

Figure 2-2 Jumper Locations on the Universe-Based PCI-to-VMEbus Bridge (Rear View)

Table 2-14 Universe-Based PCI-to-VMEbus Bridge Jumper Functions and Factory Settings

JUMPER	FUNCTION	FACTORY SETTING
E1	Installed - Universe memory-mapped Removed - Universe I/O-mapped	Installed **(Should Not be Removed)**
E2	Installed - Receives VMEbus SYSRESET Removed - Does Not Receive	Installed
E3	Installed - Drives VMEbus SYSRESET Removed - Does Not Drive	Installed
E4	Installed - SYSFAIL Not asserted upon reset Removed - SYSFAIL Asserted upon reset	Installed

Note

Any other jumper locations are reserved for VMIC use only and should not be altered from the factory default settings.

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Installation

The VMIVME-7589 conforms to the VMEbus physical specification for a 6U dual Eurocard (dual height). It can be plugged directly into any standard chassis accepting this type of board.

Do not install or remove the board while power is applied.

The following steps describe the VMIC recommended method for VMIVME-7589 installation and powerup:

1. Make sure power to the equipment is off.
2. If a drive module or other expansion module such as VMIC's VMIVME-7452, VMIVME-7453, or VMIVME-7454 VMEbus Floppy / Hard Disk Module is to be used, connect it to the controller prior to board installation. Refer to the disk module manual.
3. Choose chassis slot. The VMIVME-7589 ***must*** be attached to a dual P1 / P2 VMEbus backplane.

   If the VMIVME-7589 with the Universe-based PCI-to-VMEbus bridge is to be the VMEbus system controller, choose the first VMEbus slot. If some other board is the VMEbus system controller, choose any slot ***except*** slot one. The Universe-based bridge requires no jumpers for enabling / disabling the system controller function.

The VMIVME-7589 requires forced air cooling. It is advisable to install blank panels over any exposed VMEbus slots. This will allow for better air flow over the VMIVME-7589 board. For 20-slot VME configurations, three 100 CFM fans are recommended.

4. Insert the VMIVME-7589 and its attached expansion modules into the chosen VMEbus chassis slot (expansion modules should fill the slots immediately adjacent to the VMIVME-7589). While ensuring that the boards are properly aligned and oriented in the supporting board guides, slide the boards smoothly forward against the mating connector until firmly seated.
5. Connect all needed peripherals to the front panel. Each connector is clearly labeled on the front panel, and detailed pinouts are in Appendix A. Minimally, a keyboard and a monitor are required if the user has not previously configured the system.
6. Apply power to the system. Several messages are displayed on the screen, including names, versions, and copyright dates for the various BIOS modules on the VMIVME-7589.

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7. The VMIVME-7589 features a Flash Disk resident on the board. Refer to Chapter 4 for set up details.
8. If an external drive module is installed, the BIOS Setup program must be run to configure the drive types. See Appendix C to properly configure the system.
9. If a drive module is present, install the operating system according to the manufacturer's instructions.

See Appendix B for instructions on installing VMIVME-7589 peripheral driver software during operating system installation.

BIOS Setup

The VMIVME-7589 has an on-board BIOS Setup program that controls many configuration options. These options are saved in a special nonvolatile, battery-backed memory chip and are collectively referred to as the board's "CMOS configuration." The CMOS configuration controls many details concerning the behavior of the hardware from the moment power is applied.

The VMIVME-7589 is shipped from the factory with no hard drives configured in CMOS. The BIOS Setup program must be run to configure the specific drives attached.

Details of the VMIVME-7589 BIOS setup program are included in Appendix C.

Front Panel Connectors

The front panel connections, including connector pinouts and orientation, for the VMIVME-7589 are defined in detail in Appendix A.

PCI Expansion Site Connector

The VMIVME-7589 supplies a PCI expansion site connector for adding a VMIVME-7434 PMC expansion board. This expansion capability allows third-party devices to be used with the VMIVME-7589, as shown in Figure 2-3.

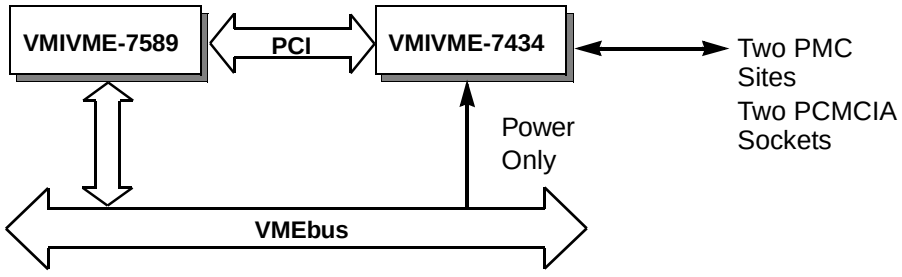

Figure 2-3 PCI Expansion Site

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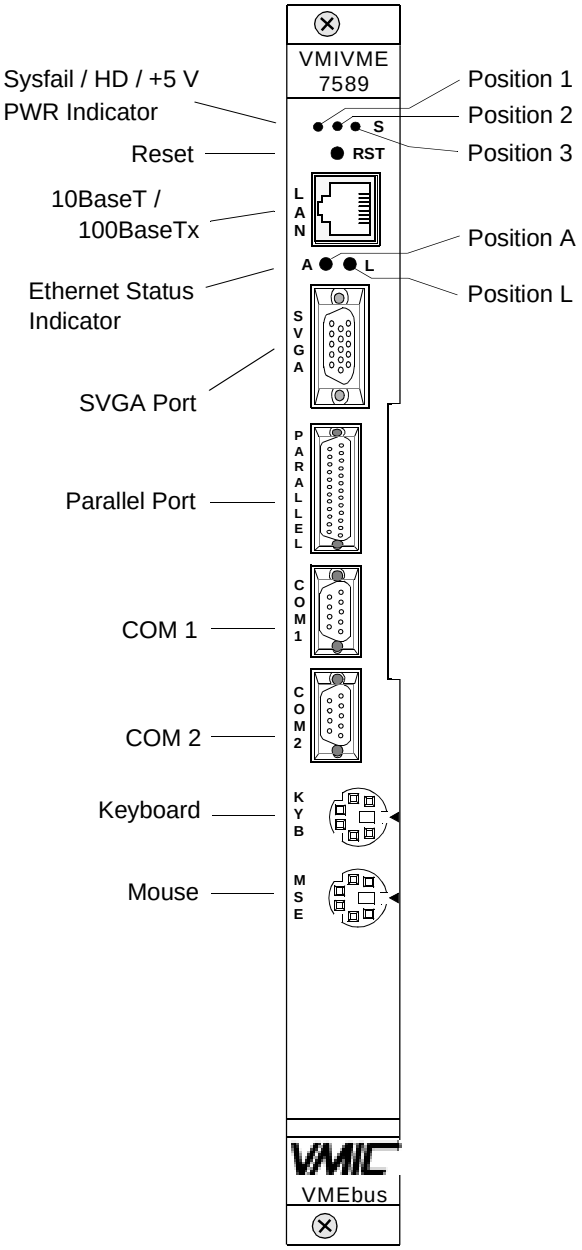
LED Definition



Position 1 *Power* - Indicates when power is applied to the board.

Position 2 *Hard Drive Indicator* - Indicates when hard drive activity is occurring.

Position 3 *SYSFAIL* - Indicates when a VMEbus SYSFAIL is asserted.

Position A *Ethernet Active* - Indicates when the Ethernet is transmitting or receiving data.

Position L *Ethernet Link* - *Yellow* indicates when the Ethernet is linked in 10BaseT mode. *Green* indicates when the Ethernet is linked in 100BaseTx mode.

Figure 2-4 LED Position on the Front Panel

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CHAPTER

3

PC/AT Functions

Contents

Introduction

The VMIVME-7589 provides a complete IBM PC / AT-compatible Pentium® processor-based computer. The design includes a high-speed microprocessor with current technology memory. Reference the VMIC product specifications for available component options.

Because the design is PC / AT compatible, it retains standard PC memory and I / O maps along with standard interrupt architecture. Furthermore, the VMIVME-7589 includes a PCI-compatible video adapter and Ethernet controller.

The following sections describe in detail the PC / AT functions of the VMIVME-7589.

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CPU Socket

The VMIVME-7589 CPU socket is factory populated with a current, high-speed Pentium processor. The CPU speed and RAM size are user-specified as part of the VMIVME-7589 ordering information. The CPU speed is not user-upgradable.

To change CPU speeds or RAM size, contact customer service to receive a Return Material Authorization (RMA).

VMIC Customer Service is available at: 1-800-240-7782.

Physical Memory

The VMIVME-7589 provides Synchronous DRAM (SDRAM) as on-board system memory. Memory can be accessed as bytes, words, or longwords.

All RAM on the VMIVME-7589 is dual-ported to the VMEbus through the PCI-to-VME bridge. The memory is addressable by the local processor, as well as the VMEbus slave interface by another VMEbus master. Caution must be used when sharing memory between the local processor and the VMEbus to prevent a VMEbus master from overwriting the local processor's operating system.

When using the Configure utility of I/O Works Access with Windows NT 4.0 to configure RAM, do not request more than 25 percent of the physical RAM. Exceeding the 25 percent limit may result in a known Windows NT bug causing unpredictable behavior during the Windows NT boot sequence and require the use of an emergency repair disk to restore the computer. The bug is present in Windows NT 4.0 service pack level 3. It is recommended that an emergency repair disk be kept up-to-date and easily accessible.

The VMIVME-7589 includes both the system and video BIOS in a single 256 K x 8 FLASH memory device.

The VMIVME-7589 memory includes 32 Kbyte of battery-backed SRAM addressed at $D800E to $DFFF. All but the first 14 bytes are accessable. Bytes $D8000 - $D800D are used by the SRAM controller. The battery-backed SRAM can be accessed by the CPU at anytime, and can be used to store system data that must not be lost during power-off conditions.

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Memory and Port Maps

Memory Map - Tundra Universe-Based PCI-to-VMEbus Bridge

The memory map for the Tundra Universe-based interface VMIVME-7589 is shown in Table 3-1. All systems share this same memory map, although a VMIVME-7589 with less than the full 64 Mbyte of DRAM does not fill the entire space reserved for On-Board Extended Memory.

Table 3-1 VMIVME-7589, Universe-Based Interface Memory Address Map

MODE	MEMORY ADDRESS RANGE	SIZE	DESCRIPTION
PROTECTED MODE	$FFFF 0000 - $FFFF FFFF	64 Kbyte	ROM BIOS Image
	$0400 0000 - $FFFE FFFF	3.9 Gbyte	Unused *
	$0010 0000 - $03FF FFFF	63 Mbyte	Reserved for ** On-Board Extended Memory (not filled on all systems)
REAL MODE	$E0000 - $FFFFF	128 Kbyte	ROM BIOS
	$D8000 - $D800D	14 bytes	RTC / Watchdog Timer Control Registers
	$D800E - $DFFFF	32 Kbyte	Battery-Backed SRAM and Watchdog Timer
	$D0000 - $D7FFF	32 Kbyte	Unused
	$C8000 - $CFFFF	32 Kbyte	Reserved
	$C0000 - $C7FFF	32 Kbyte	Video ROM
	$A0000 - $BFFFF	128 Kbyte	Video RAM
	$00000 - $9FFFF	640 Kbyte	User RAM / DOS RAM

* This space can be used to set up protected mode PCI-to-VMEbus windows (also referred to as PCI slave images).
** This space can be allocated as shared memory (for example, between the Pentium processor-based CPU and VMEbus Master. Note, that if a PMC board is loaded, the expansion BIOS may be placed in this area.

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I/O Port Map

The Pentium processor-based CPU includes special input/output instructions that access I/O peripherals residing in I/O addressing space (separate and distinct from memory addressing space). Locations in I/O address space are referred to as *ports*. When the CPU decodes and executes an I/O instruction, it produces a 16-bit I/O address on lines A00 to A15 and identifies the I/O cycle with the M/I/O control line. Thus, the CPU includes an independent 64Kbyte I/O address space which is accessible as bytes, words, or longwords.

Standard PC/AT hardware circuitry reserves only 1,024 byte of I/O addressing space from I/O $000 to $3FF for peripherals. All standard PC I/O peripherals such as serial and parallel ports, hard and floppy drive controllers, video system, real-time clock, system timers, and interrupt controllers are addressed in this region of I/O space. The BIOS initializes and configures all these registers properly; adjusting these I/O ports directly is not normally necessary.

The assigned and user-available I/O addresses are summarized in the I/O Address Map, Table 3-2.

Table 3-2 VMIVME-7589 I/O Address Map

I/O ADDRESS RANGE	SIZE IN BYTES	HW DEVICE	PC/AT FUNCTION
$000 - $00F	16		DMA Controller 1 (Intel 8237A Compatible)
$010 - $01F	16		Reserved
$020 - $021	2		Master Interrupt Controller (Intel 8259A Compatible)
$022 - $03F	30		Reserved
$040 - $043	4		Programmable Timer (Intel 8254 Compatible)
$044 - $05F	30		Reserved
$060 - $064	5		Keyboard, Speaker, Eqpt. Configuration (Intel 8042 Compatible)
$065 - $06F	11		Reserved
$070 - $071	2		Real-Time Clock, NMI Mask
$072 - $07F	14		Reserved
$080 - $08F	16		DMA Page Registers
$090 - $091	2		Reserved
$092	1		Alt. Gate A20/Fast Reset Register
$093	1		Reserved

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Table 3-2 VMIVME-7589 I/O Address Map (Continued)

I/O ADDRESS RANGE	SIZE IN BYTES	HW DEVICE	PC/AT FUNCTION
$094	1	Super VGA Chip	POS102 Access Control Register
$095 - $09F	11		Reserved
$0A0 - $0A1	2		Slave Interrupt Controller (Intel 8259A Compatible)
$0A2 - $0BF	30		Reserved
$0C0 - $0DF	32		DMA Controller 2 (Intel 8237A Compatible)
$0E0 - $16F	142		Reserved
$170 - $177	8	PIIX4	Secondary Hard Disk Controller
$178 - $1EF	120		User I/O
$1F0 - $1F7	8	PIIX4	Primary Hard Disk Controller
$1F8 - $277	128		User I/O
$278 - $27F	8	I/O Chip*	LPT2 Parallel I/O*
$280 - $2E7	104		Reserved
$2E8 - $2EE	7	UART*	COM4 Serial I/O*
$2EF - $2F7	9		User I/O
$2F8 - $2FE	7	Super-I/O Chip	COM2 Serial I/O (16550 Compatible)
$2FF - $36F	113		Reserved
$370 - $377	8	Super-I/O Chip	Secondary Floppy Disk Controller
$378 - $37F	8	Super-I/O Chip	LPT1 Parallel I/O
$380 - $3E7	108		Reserved
$3E8 - $3EE	7	UART*	COM3 Serial I/O*
$3F0 - $3F7	8	Super-I/O Chip	Primary Floppy Disk Controller
$3F8 - $3FE	7	Super-I/O Chip	COM1 Serial I/O (16550 Compatible)
$3FF - $CFF			Reserved
$500 - $503	4	82C54 Timer	Programmable Internal Timer

* While these I/O ports are reserved for the listed functions, they are not implemented on the VMIVME-7589. They are listed here to make the user aware of the standard PC/AT usage of these ports.

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PC/AT Interrupts

In addition to an I/O port address, an I/O device has a separate hardware interrupt line assignment. Assigned to each interrupt line is a corresponding interrupt vector in the 256-vector interrupt table at $00000 to $003FF in memory. The 16 maskable interrupts and the single Non-Maskable Interrupt (NMI) are listed in Table 3-3 along with their functions. Table 3-4 on page 47 details the vectors in the interrupt vector table. The interrupt number in HEX and decimal are also defined for real and protected mode in Table 3-4.

The interrupt hardware implementation on the VMIVME-7589 is standard for computers built around the PC/AT architecture, which evolved from the IBM PC/XT. In the IBM PC/XT computers, only eight interrupt request lines exist, numbered from IRQ0 to IRQ7 at the PIC. The IBM PC/AT computer added eight more IRQx lines, numbered IRQ8 to IRQ15, by cascading a second slave PIC into the original master PIC. IRQ2 at the master PIC was committed as the cascade input from the slave PIC. This architecture is represented in Figure 3-1 on page 52.

To maintain backward compatibility with PC/XT systems, IBM chose to use the new IRQ9 input on the slave PIC to operate as the old IRQ2 interrupt line on the PC/XT Expansion Bus. Thus, in AT systems, the IRQ9 interrupt line connects to the old IRQ2 pin (pin B4) on the AT Expansion Bus (or ISA bus).

Table 3-3 PC/AT Hardware Interrupt Line Assignments

IRQ	AT FUNCTION	COMMENTS
NMI	Parity Errors (Must be enabled in BIOS Setup)	Used by VMIVME-7589 VMEbus Interface
0	System Timer	Set by BIOS Setup
1	Keyboard	Set by BIOS Setup
2	Duplexed to IRQ9	
3	COM2/COM4	
4	COM1/COM3	
5	Timer	Assigned to On-Board Timer
6	Floppy Controller	
7	LPT1	
8	Real-Time Clock	
9	Old IRQ2	SVGA or Network I/O

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Table 3-3 PC/AT Hardware Interrupt Line Assignments

IRQ	AT FUNCTION	COMMENTS
10	Not Assigned	Determined by BIOS
11	Not Assigned	Determined by BIOS
12	Mouse	
13	Math Coprocessor	
14	AT Hard Drive	
15	Flash Drive	

Table 3-4 PC/AT Interrupt Vector Table

INTERRUPT NO.		IRQ LINE	REAL MODE	PROTECTED MODE
HEX	DEC			
00	0		Divide Error	Same as Real Mode
01	1		Debug Single Step	Same as Real Mode
02	2	NMI	Memory Parity Error, VMEbus Interrupts	Same as Real Mode (Must be enabled in BIOS Setup)
03	3		Debug Breakpoint	Same as Real Mode
04	4		ALU Overflow	Same as Real Mode
05	5		Print Screen	Array Bounds Check
06	6			Invalid OpCode
07	7			Device Not Available
08	8	IRQ0	Timer Tick	Double Exception Detected
09	9	IRQ1	Keyboard Input	Coprocessor Segment Overrun
0A	10	IRQ2	BIOS Reserved	Invalid Task State Segment
0B	11	IRQ3	COM2 Serial I/O	Segment Not Present
0C	12	IRQ4	COM1 Serial I/O	Stack Segment Overrun
0D	13	IRQ5	Timer	Same as Real Mode
0E	14	IRQ6	Floppy Disk Controller	Page Fault
0F	15	IRQ7	LPT1 Parallel I/O	Unassigned

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Table 3-4 PC/AT Interrupt Vector Table (Continued)

INTERRUPT NO.		IRQ LINE	REAL MODE	PROTECTED MODE
HEX	DEC			
10	16		BIOS Video I/O	Coprocessor Error
11	17		Eqpt Configuration Check	Same as Real Mode
12	18		Memory Size Check	Same as Real Mode
13	19		XT Floppy/Hard Drive	Same as Real Mode
14	20		BIOS Comm I/O	Same as Real Mode
15	21		BIOS Cassette Tape I/O	Same as Real Mode
16	22		BIOS Keyboard I/O	Same as Real Mode
17	23		BIOS Printer I/O	Same as Real Mode
18	24		ROM BASIC Entry Point	Same as Real Mode
19	25		Bootstrap Loader	Same as Real Mode
1A	26	IRQ8	Real-Time Clock	Same as Real Mode
1B	27		Control/Break Handler	Same as Real Mode
1C	28		Timer Control	Same as Real Mode
1D	29		Video Parameter Table Pntr	Same as Real Mode
1E	30		Floppy Parm Table Pntr	Same as Real Mode
1F	31		Video Graphics Table Pntr	Same as Real Mode
20	32		DOS Terminate Program	Same as Real Mode
21	33		DOS Function Entry Point	Same as Real Mode
22	34		DOS Terminate Handler	Same as Real Mode
23	35		DOS Control/Break Handler	Same as Real Mode
24	36		DOS Critical Error Handler	Same as Real Mode
25	37		DOS Absolute Disk Read	Same as Real Mode
26	38		DOS Absolute Disk Write	Same as Real Mode
27	39		DOS Program Terminate, Stay Resident	Same as Real Mode
28	40		DOS Keyboard Idle Loop	Same as Real Mode
29	41		DOS CON Dev. Raw Output	Same as Real Mode

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Table 3-4 PC/AT Interrupt Vector Table (Continued)

INTERRUPT NO.		IRQ LINE	REAL MODE	PROTECTED MODE
HEX	DEC			
2A	42		DOS 3.x+ Network Comm	Same as Real Mode
2B	43		DOS Internal Use	Same as Real Mode
2C	44		DOS Internal Use	Same as Real Mode
2D	45		DOS Internal Use	Same as Real Mode
2E	46		DOS Internal Use	Same as Real Mode
2F	47		DOS Print Spooler Driver	Same as Real Mode
30-60	48-96		Reserved by DOS	Same as Real Mode
61-66	97-102		User Available	Same as Real Mode
67-71	103-113		Reserved by DOS	Same as Real Mode
72	114	IRQ10	Not Assigned	
73	115	IRQ11	Not Assigned	
74	116	IRQ12	Mouse	
75	117	IRQ13	Math Coprocessor	
76	118	IRQ14	AT Hard Drive	
77	119	IRQ15	Flash Drive	
78-7F	120-127		Reserved by DOS	Same as Real Mode
80-F0	128-240		Reserved for BASIC	Same as Real Mode
F1-FF	241-255		Reserved by DOS	Same as Real Mode

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PCI Interrupts

Interrupts on Peripheral Component Interconnect (PCI) Local Bus are optional and defined as “level sensitive,” asserted low (negative true), using open drain output drivers. The assertion and de-assertion of an interrupt line, INTx#, is asynchronous to CLK. A device asserts its INTx# line when requesting attention from its device driver. Once the INTx# signal is asserted, it remains asserted until the device driver clears the pending request. When the request is cleared, the device de-asserts its INTx# signal.

PCI defines one interrupt line for a single function device and up to four interrupt lines for a multifunction device or connector. For a single function device, only INTA# may be used while the other three interrupt lines have no meaning. Figure 3-1 on page 52 depicts the VMIVME-7589 interrupt logic pertaining to VMEbus operations and the PCI expansion site.

Any function on a multifunction device can be connected to any of the INTx# lines. The Interrupt Pin register defines which INTx# line the function uses to request an interrupt. If a device implements a single INTx# line, it is called INTA#; if it implements two lines, they are called INTA# and INTB#; and so forth. For a multifunction device, all functions may use the same INTx# line or each may have its own (up to a maximum of four functions) or any combination thereof. A single function can never generate an interrupt request on more than one INTx# line.

The slave PIC accepts the VMEbus interrupts through lines that are defined by the BIOS. The BIOS defines which interrupt line to utilize depending on which system requires the use of the line.

The PCI-to-VME Bridge has the capability of generating a Non-Maskable Interrupt (NMI) via the PCI SERR# line. Table 3-5 describes the register bits that are used by the NMI. The SERR interrupt is routed through certain logic back to the NMI input line on the CPU. The CPU reads the NMI Status Control register to determine the NMI source (bits set to 1). After the NMI interrupt routine processes the interrupt, software clears the NMI status bits by setting the corresponding enable / disable bit to 1. The NMI Enable and Real-Time Clock register can mask the NMI signal and disable / enable all NMI sources.

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Table 3-5 NMI Register Bit Descriptions

Status Control Register (I/O Address $061, Read/Write, Read Only)	
Bit 7	SERR# NMI Source Status (Read Only) - This bit is set to 1 if a system board agent detects a system board error. It then asserts the PCI SERR# line. To reset the interrupt, set bit 2 to 0 and then set it to 1. When writing to port $061, bit 7 must be 0.
Bit 2	PCI SERR# Enable (Read / Write) - 1 = Clear and Disable, 0 = Enable
Enable and Real-Time Clock Address Register (I/O Address $070, Write Only)	
Bit 7	NMI Enable - 1 = Disable, 0 = Enable

I/O Ports

The VMIVME-7589 incorporates the SMC Super-I / O chip. The SMC chip provides the VMIVME-7589 with a standard floppy drive controller, two 16550 UART-compatible serial ports, and one standard Centronics parallel port. The Ultra-IDE hard drive interface is provided by the Intel 82371SB (PIIX4) PCI ISA IDE Xcelerator chip. All ports are present in their standard PC / AT locations, using default interrupts.

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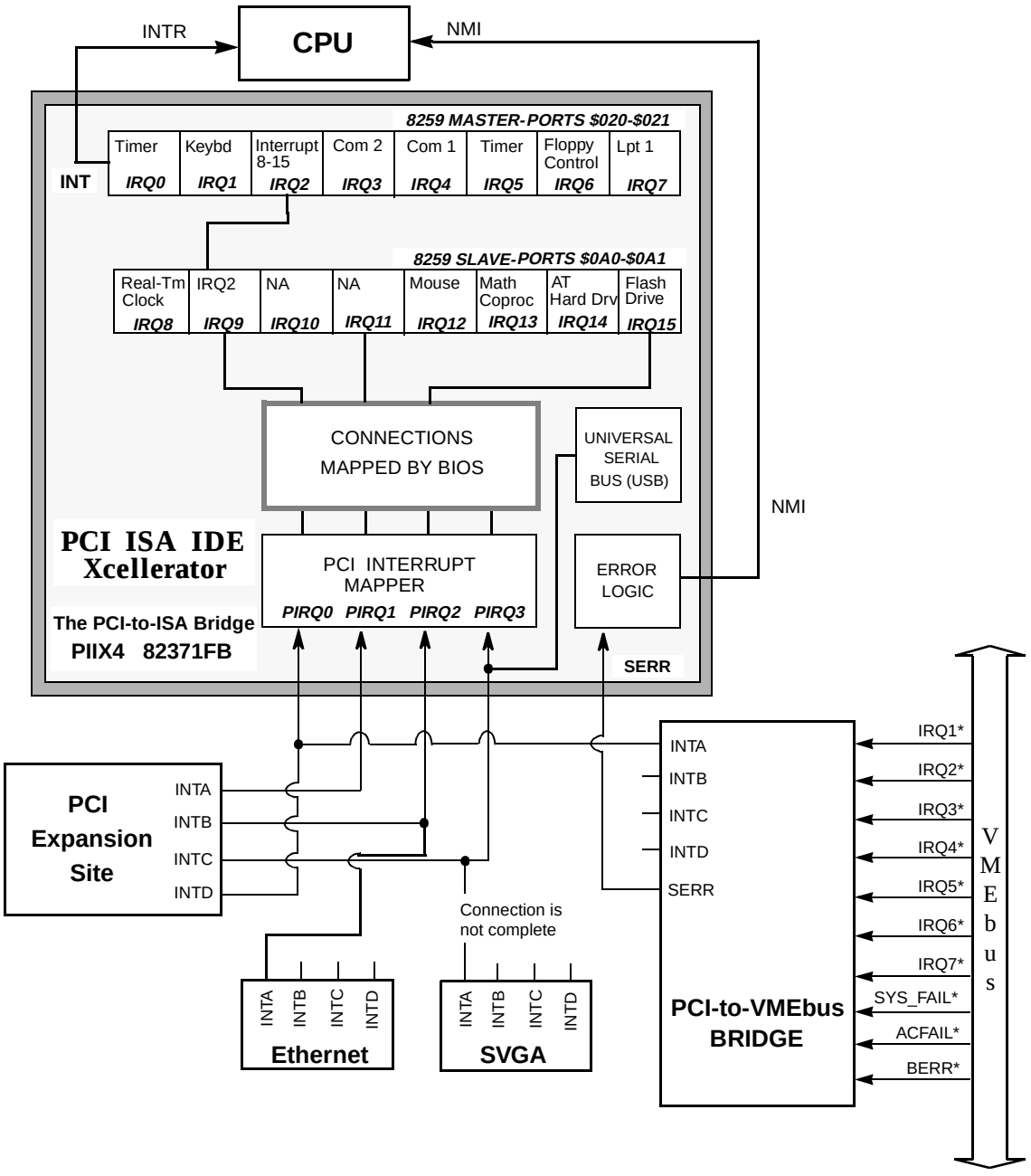

Figure 3-1 Connections for the PC Interrupt Logic Controller

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Video Graphics Adapter

The monitor port on the VMIVME-7589 is controlled by a Cirrus Logic CL-GD 5480 chip with 2 Mbyte video DRAM. The video controller chip is hardware and BIOS compatible with the IBM EGA and SVGA standards and also supports VESA high-resolution and extended video modes. Table 3-6 shows the graphics video modes supported by the Cirrus Logic video chip.

Table 3-6 Supported Graphics Video Resolutions

SCREEN RESOLUTION	MAXIMUM COLORS	REFRESH RATES (Hz)
640 x 480	16 M	100
800 x 600	16 M	100
1,024 x 768 (Interlaced)	64 K	100
1,152 x 864	64 K	100
1,280 x 1,024	256	85
1,500 x 1,200	256	70

Not all SVGA monitors support resolutions and refresh rates beyond 640 x 480 at 60 Hz. Do not attempt to drive a monitor to a resolution or refresh rate beyond its capability.

The VMIVME-7589's processor includes a 32-bit access to video memory with no-wait states. Video I/O registers are accessed using PCI bus. In addition, the Cirrus Logic video controller supports up to a 64 x 64 pixel hardware cursor.

Floppy disks supplied with the VMIVME-7589 also contain video drivers for Windows® and other popular programs and operating systems. Appendix B contains instructions on the incorporation of the video drivers during operating system installation.

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Ethernet Controller

The network capability is provided by the Digital Semiconductor's 21143. This Ethernet controller is PCI bus based and is software configurable. The VMIVME-7589 supports 10BaseT and 100BaseTx Ethernet.

10BaseT

A network based on the 10BaseT standard uses unshielded twisted-pair cables, providing an economical solution to networking by allowing the use of existing telephone wiring and connectors. The RJ-45 connector is used with the 10BaseT standard. 10BaseT has a maximum length of 100 m from the wiring hub to the terminal node.

100BaseTx

The VMIVME-7589 also supports the 100BaseTx Ethernet. A network based on a 100BaseTx standard uses unshielded twisted-pair cables and a RJ-45 connector. The 100BaseTx has a maximum deployment length of 250 m.

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CHAPTER

4

Embedded PC/RTOS Features

Contents

Introduction

VMIC's VMIVME-7589 features additional capabilities beyond those of a typical IBM PC / AT-compatible CPU. The unit provides three software-controlled, general-purpose timers along with a programmable Watchdog timer for synchronizing and controlling multiple events in embedded applications. The VMIVME-7589 also provides a bootable Flash Disk system, and 32 K byte of nonvolatile, battery-backed SRAM. These features make the unit ideal for embedded applications, particularly applications where standard hard drives and floppy disk drives cannot be used.

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Timers

General

The VMIVME-7589 provides a user-programmable 82C54 internal timer / counter. The 82C54 provides three independent, 16-bit timers each operating at 1 or 2 MHz clock speed determined by the configuration of jumper J36; reference Table 2-3 on page 32. These timers are completely available to the user, and are not dedicated to any PC / AT function. These timers may be used to generate system interrupts.

Events can be timed by either polling the timers or generating a system interrupt via circuity external to the 82C54. The external circuity consists of logic which generates the interrupt and a Timer Interrupt Status register which indicates which of the three Timers generated an interrupt.

The 82C54 timers are mapped at I / O address $500. The interrupt used by the Timers is IRQ5. The Timer Interrupt Status register is available via the Power Management I / O address space. The access to this space is explained in the Timer Interrupt Status section.

Timer Interrupt Status

A single interrupt, IRQ5, is used by all three Timers. A Timer Interrupt Status register is provided in order to determine which Timer(s) initiated an interrupt. The interrupt status register is a general-purpose input register located, external to the 82C54, at offset 31h from the Power Management Base I / O address. The interrupt status register address can be found by first determining the PCI Configuration Base address for Device ID 7113h and Vendor ID 8086h. The Power Management Base I / O address can be found by reading offset 40h from this PCI Configuration address. The Timer Interrupt Status register bits are located at offset 31h from the Power Management Base I / O address, bits 5, 6, and 7 (refer to Figure 4-2).

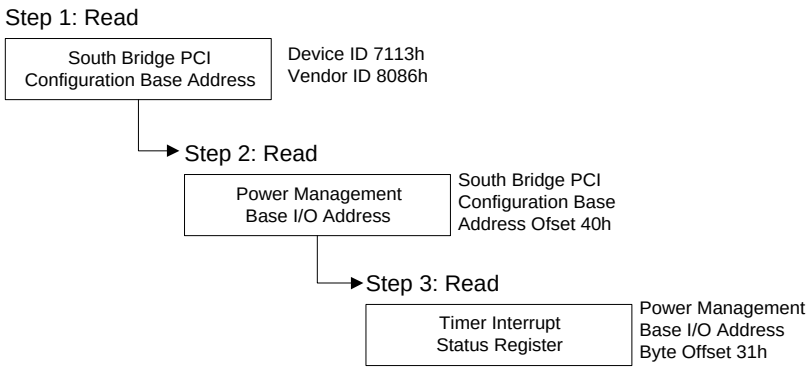

Figure 4-1 Timer Interrupt Status Register Read/Steps

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A byte read of Offset 31h from the Power Management Base I/O address is used to obtain these bits. Bits 5, 6, and 7 correspond to Timers 2, 1, and 0, respectively

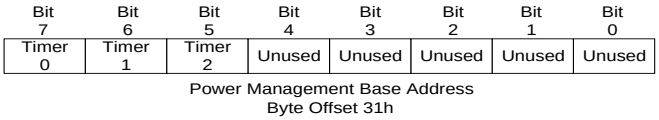

Figure 4-2 Timer Interrupt Status Register

In order to clear the Timer Interrupt Status register, first write zeros (0's) to the general-purpose output register located at offset 37h of the Power Management Base I/O address bits 3, 4, and 6 (Not bits 3, 4 and 5). Then write ones (1's) to these same bits to re-enable the Timer Interrupt Status register. Bits 3, 4, and 6 correspond to Timers 2, 1, and 0, respectively.

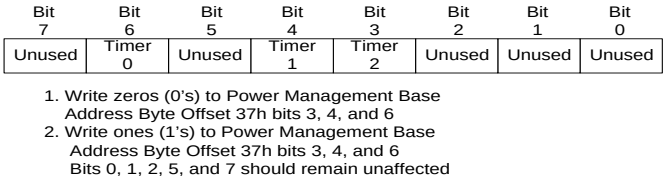

Figure 4-3 Clearing the Timer Interrupt Status Register

Clearing the Interrupt

The Timer Interrupts are cleared using the standard procedure for clearing PC/AT IRQ5. Refer to Appendix D for an example of using the 82C54 timers.

Timer Programming

Architecture

The VMIVME-7589 Timers are mapped in I/O address space starting at $500. See Table 4-1. The Timers, consisting of three 16-bit timers and a Control Word Register (see Figure 4-4) are read from/written to via an 8-bit data bus.

Table 4-1 I/O Address of the Control Word Register and Timers

I/O Address	Select
$500	Timer 0
$501	Timer 1
$502	Timer 2
$503	Control Word Register

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Table 4-1 shows the I/O address's of the Control Word Register and Timers.

The Control Word Register is write only. The Timer status information can be obtained from the Read-Back command (see Reading section on page 61).

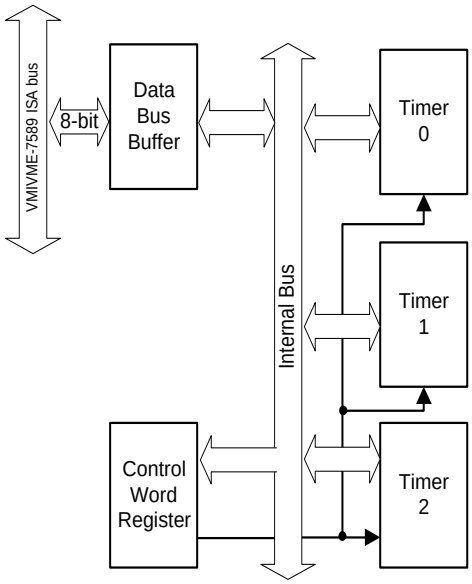

Figure 4-4 82C54 Diagram

The three Timers, Timer 0, 1, and 2, are functionally equivalent. Therefore only a single Timer will be described. Figure 4-5 is a block diagram of a Timer. Each Timer is functionally independent. Although the Control word is shown in the Timer block diagram, it is not a part of the Timer, but its contents directly affect how the Timer functions.

The status register, as shown in Figure 4-5, when latched, contains the present contents of the Control Word Register and the present state of the output and load count flag (The Status Word is available via the Read-Back command, see Reading section on page 61).

The Timer is labelled TE (Timer Element). It is a 16-bit synchronous presettable down counter.

The blocks labelled OL_M and OL_L are 8-bit Output Latches (OL). The subscripts M and L stand for Most Significant byte and Least Significant byte. These latches usually track the TE but when commanded will latch and hold the present count until the CPU reads the count. When the latched count is read, the OL registers will continue to track the TE. When reading the OL registers, two 8-bit accesses must be performed to retrieve the complete 16-bit value of the Timer as only one latch at a time is enabled. The TE cannot be read, the count is read from the OL registers.

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There are two 8-bit registers labeled TR_M and TR_L (Timer Register). The subscripts M and L stand for Most Significant byte and Least Significant byte. When a new count is written to the Timer the count is loaded into the TR and later transferred to the TE. The Control logic lets one 8-bit TR register be written to at a time. Two 8-bit writes must be performed to load a complete 16-bit count value. Both TR bytes are transferred to the TE at the same time. The TE cannot be directly written to by the user, the count is written to the TR registers then latched to the TE.

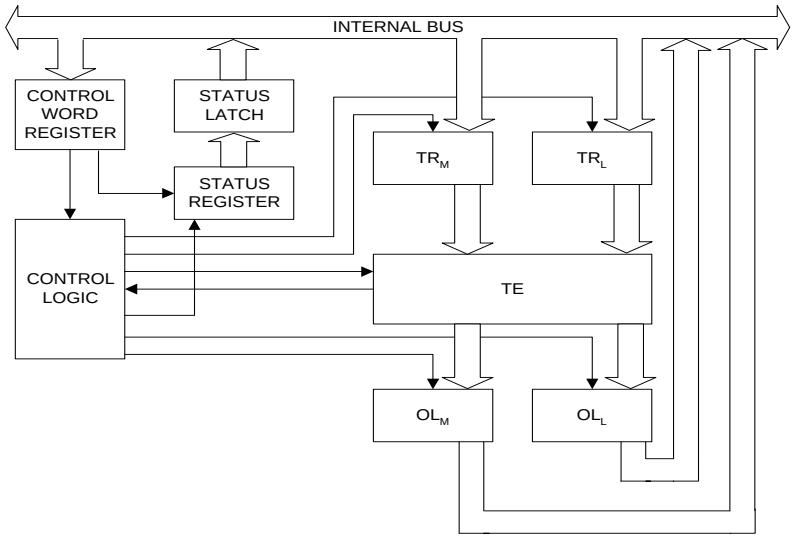

Figure 4-5 Internal Timer Diagram

Writing

The Timers are programmed by first writing a Control Word and then the initial count. The format of the Control Word is shown in Tables 4-2 through 4-6. All Control Words are written into the Control Word Register while the initial counts are written into the individual Timer registers. The format of the initial count is determined by the Control Word.

Table 4-2 Control Word Format

D7	D6	D5	D4	D3	D2	D1	D0
ST1	ST0	RW1	RW0	M2	M1	M0	BCD

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Table 4-3 ST - Select Timer

ST1*	ST0*	Description
0	0	Select Timer 0
0	1	Select Timer 1
1	0	Select Timer 2
1	1	Read-Back Command (See Reading section on page 61)
* The ST bits specify which Timer (0, 1, or 2) the Control word refers to or whether this is a Read-Back command		

.

Table 4-4 RW - Read/Write

RW1*	RW0*	Description
0	0	Timer Latch Command (see Reading section)
0	1	Read / Write least significant byte only
1	0	Read / Write most significant byte only
1	1	Read / Write least significant byte first, then most significant
* The RW bits specify whether this is a Timer Latch command or the byte ordering of the Read / Write transaction.		

Table 4-5 M - Mode

M2*	M1*	M0*	Description
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5
* Only Mode 2 is described in this manual.			

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Table 4-6 BCD

BCD*	Description
0	Binary Timer 16-bits
1	Binary Coded Decimal (BCD) Timer (4 Decades)
* The BCD bit specifies whether the Timer count value is in Binary or BCD.	

When programming the 82C54, only two rules need to be followed.

1. For each Timer, the Control Word must be written first.
2. The initial count must follow the format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte then most significant byte). As long as these rules are adhered to, any programming sequence is acceptable.

Reading

There are two methods for reading the timers: the Timer Latch Command and the Read-Back Command.

Timer Latch Command

The Timer Latch Command allows the reading of a Timer 'on the fly' without affecting the timing in process.

Like a Control Word, the Timer Latch Command is written to the Control Word Register (I/O Address $503, see Table 4-1). The Select Timer bits (ST1, ST0, see Table 4-3) select one of the three timers while the Read/Write bits (RW1,RW0, see Table 4-4) select the Timer Latch Command, RW1 = 0 and RW0 = 0. The selected Timer's count is latched into the 0L registers at the time of the Timer Latch Command. The count is held in the 0L latches until it is read. Multiple Timer Latch Commands can be used to latch more than one Timer. Again, each Timer's count is held latched until it is read.

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Read-Back Command

The Read-Back Command allows the user to view the Timer count, the Timer Mode, the current state of the OUT pin, and the Load Flag of the selected Timer. Like a Control Word, the Read-Back Command is written into the Control Word Register and has the format shown in Tables 4-7 and 4-8. The Command applies to the Timer(s) selected by setting the corresponding bits Cnt2, Cnt1, Cnt0 = 1.

Table 4-7 Read-Back Command Format

D7	D6	D5	D4	D3	D2	D1	D0
1	1	$\overline{\text{Count}}$	$\overline{\text{Status}}$	Cnt2	Cnt1	Cnt0	0

Table 4-8 Read-Back Command Description

Bit	Description
D5: $\overline{\text{Count}}$	Latch count of selected Timer(s)
D4: $\overline{\text{Status}}$	Latch status of selected Timer(s)
D3: Cnt2	Select Timer 2
D2: Cnt1	Select Timer 1
D1: Cnt0	Select Timer 0
D0	Reserved, must be 0

The Read-Back Command can be used to latch several Timer counts by setting the $\overline{\text{Count}}$ bit = 0 and selecting the Timers. This is the same as using multiple Timer Latch Commands. Again each Timer's latched count will be held until it is read.

The Read-Back command can also be used to latch the timer status by setting the $\overline{\text{Status}}$ bit = 0 and selecting the Timers. Status of a Timer is accessed by a read from that Timer (see Table 4-1 on page 57). If more than one Timer Status Read-Back command is issued without reading the status, all but the first is ignored.

The format of the Timer Status byte is shown in Tables 4-9 and 4-10.

Table 4-9 Status Byte

D7	D6	D5	D4	D3	D2	D1	D0
OUT	LOAD	RW1	RW0	M2	M1	M0	BCD

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Table 4-10 Status Byte Description

Bit	Description
D7: OUT	Current state of Timers OUT pin
D6: LOAD	Count loaded into Timer
D5-D0	Timer Programmed Mode

Bit D7 contains the state of the Timers OUT pin. This allows viewing of the Timer's OUT pin via software.

Bit D6 indicates when the count written to the Timer is actually loaded into the Timer register. The exact time of the loading depends on the Mode the Timer is in and is defined in the Mode Definitions section. The count cannot be read from the Timer until it has been loaded. If a count is read before this time, the value read will not be the new count just written. Refer to Table 4-11.

Bits D5 through D0 contain the Timer's programmed mode exactly, bit for bit, like the Timer Control Words bits D5 through D0. See Table 4-2 on page 59.

Table 4-11 LOAD Bit Operation

Action	Causes
1. Write to the Control Word Register [1]	LOAD bit = 1
2. Write count to Timer [2]	LOAD bit = 1
3. New count loaded into Timer	LOAD bit = 0

[1]Only the Timer specified in the Control Word will have its LOAD bit set to 1. LOAD bits of other Timers are not affected.

[2]If the Timer is programmed for two byte counts (least significant then most significant), the LOAD bit will go to 1 when the second byte is written.

Both the count and status of the specified Timer(s) can be latched at the same time by setting both the $\overline{\text{Count}}$ bit (D5) and $\overline{\text{Status}}$ bit (D4) to zero (0) in the Read-Back command. If this technique is used, the first read operation of the Timer will return the status while the next one or two reads (depending on whether the Timer is programmed for one or two bytes) will return the count. Succeeding reads will return unlatched counts.

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Mode Definitions

The VMIVME-7589 utilizes an 82C54 Timer / Counter for its Timers. 82C54 Timer / Counters can be programmed to function in six different modes (numbered Mode 0 through Mode 5). The VMIVME-7589 Timers are hardware configured to operate using Mode 2. Only Mode 2 is defined.

Mode 2 functions as a divide by N counter. Once a Control Word and an initial count are written to the Timer the initial count is loaded on the next Clock cycle. When the count decrements to 1 an interrupt is generated. The Timer then reloads the initial count and the process repeats. This Mode is periodic. For an initial count of N, the sequence repeats every N CLK cycles. An initial count of 1 is illegal.

Writing a new count while the Timer is counting does not affect the current sequence. The new count will be loaded at the end of current sequence.

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Flash Disk

The VMIVME-7589 features an on-board Flash mass storage system that allows the host computer to issue commands to read or write blocks to memory in a Flash memory array. This Flash Disk appears to the user as an intelligent ATA (IDE) disk drive with the same functionality and capabilities as a “rotating media” IDE hard drive.

Configuration

The Flash Disk resides on the VMIVME-7589 as the secondary IDE bus master device (the secondary IDE bus slave device is not assignable). The default setting in the AMIBIOS ‘STANDARD CMOS SETUP’ screen is the ‘AUTO’ setting. In the AMIBIOS ‘PERIPHERAL SETUP’ screen, the secondary PCI IDE interface must be enabled for the Flash Disk to be functional. Refer to Appendix C, AMI-Basic Input / Output System for additional details.

Figure 4-6 maps the configuration possibilities for a typical system consisting of the VMIVME-7589 with a resident Flash Disk, a hard drive attached to the Primary IDE interface, and a floppy drive attached to the floppy interface.

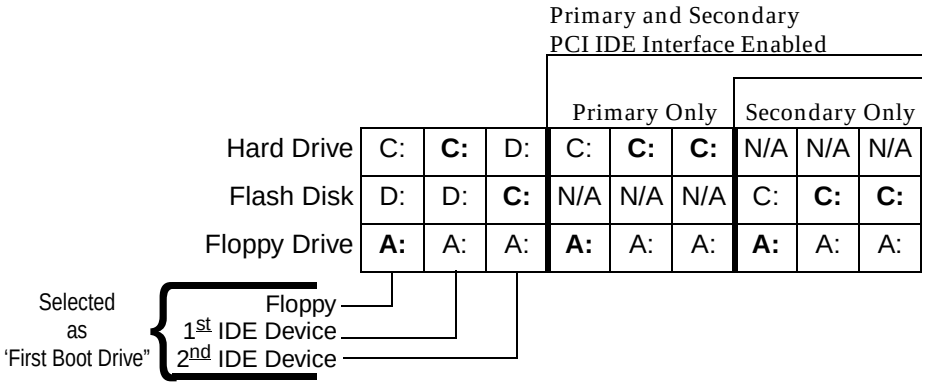

Figure 4-6 Typical System Configuration

The Primary and Secondary PCI IDE Interfaces are controlled (enabled or disabled) in the Peripheral Setup screen of the AMI BIOS. The First Boot Device is selected in the Advanced CMOS Setup screen.

Figure 4-6 identifies the drive letter assigned to each physical device, and indicates in bold lettering the device booted from in each configuration, using devices that were bootable. Bootable being a device on which an operating system has been installed, or formatted as a system disk using MS-DOS.

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Note

If during the configuration efforts a drive device is identified as a USER setting in the Standard CMOS Setup screen, as occurs after using the Auto-Detect Hard Drives function of the BIOS, then disabled (the device's IDE interface disabled) in the Peripheral Setup screen, the following error may occur:

Primary (or Secondary) Master HHD Error
Run Setup
Press <ESC> to Resume

Press the Escape key as directed to resume the boot procedure. The settings should be changed to prevent the reoccurrence of this error condition.

Functionality

The Flash Disk performs identically to a standard IDE hard drive. Reads and writes to the device are performed using the same methods, utilizing DOS command line entries or the file managers resident in the chosen operating system.

Advanced Configuration

The previous discussion is based on using the IDE disk devices formatted as one large partition per device. Some applications may require the use of multiple partitions. The following discussion of these partitions includes the special procedures that must be followed to allow the creation of multiple partitions on the VMIVME-7589 IDE disk devices (including the resident Flash Disk).

Partitions may be either a primary partition or an extended partition. An extended partition may be subdivided farther into logical partitions. Each device may have up to four main partitions, one of which may be an extended partition. However, if multiple primary partitions are created, only one partition may be active at one time. Data in the non-active partitions are not accessible.

Following the creation of the partitioning scheme, the partitions can be formatted to contain the desired file system.

As discussed earlier, a typical system consists of the VMIVME-7589 with its resident Flash Disk configured as the Secondary IDE device, a hard drive attached to the Primary IDE interface, and a floppy drive attached to the floppy interface.

Using this configuration, it may be desirable to have a logical device on either IDE device configured as a bootable device, allowing the selection of the first boot device via the Advanced CMOS Setup screen. Using this capability, a user could have a system configured with multiple operating systems that would then be selectable by assigning the IDE logical device as the boot device.

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The DOS utility FDISK is commonly used to configure the partition structure on a hard drive. Other utility programs are available for performing this task. Partition Magic by PowerQuest is a popular and capable commercially available program. Comments that follow pertain to partitioning efforts using FDISK.

CAUTION: Deleting a partition will erase all the data previously held in that partition.

The Flash Disk will be configured as a single partition device as delivered from the factory. The following sample sequence illustrates a proven method for creating two 4 Megabyte partitions, with one as an active primary partition. Take note of the instructions to exit FDISK. This has been shown to be an important step in a successful partitioning effort.

1. Power up VMIVME-7589, and enter CMOS Set-up.
2. Set Primary Master to “Not Installed”.
3. Set Secondary Master to “Auto”
4. Set boot device to floppy.
5. Boot DOS from the floppy, verify that the System Configuration Screen shows only the Flash Disk.
6. Run FDISK.
7. Delete all current partitions (any data currently stored in the partitions will be lost).
8. Exit FDISK, this will cause a reboot, then run FDISK again.
9. Create a 4 Mbyte primary partition.
10. Create a 4 Mbyte extended partition.
11. Set-up a logical device for the 4 Mbyte extended partition.
12. Set the Primary partition as an active partition.
13. Exit FDISK.
14. Run FORMAT C: (use the /s option if you want the Flash Disk as a bootable DOS device.)
15. Format D:
16. Reset the CPU, and enter the CMOS set-up.
17. Set Primary Master to “AUTO”.
18. Set boot device to desired boot source.

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Drive letter assignments for a simple system were illustrated in Figure 4-6. Understanding the order the operating system assigns drive letters is necessary for these multiple partition configurations. The operating system assigns drive letter C: to the active primary partition on the first hard disk (the boot device). Drive D: is assigned to the first recognized primary partition on the next hard disk. The operating system will continue to assign drive letters to the primary partitions in an alternating fashion between the two drives. Next, logical partitions will be assigned drive letters starting on the first hard drive lettering each logical device sequentially until they are all named, then doing the same sequential lettering of each logical partition on the second hard disk.

Note

Drive letter changes caused by adding a drive or changing the initial partitioning scheme may cause difficulties with an operating system installed prior to the changes. Plan your configuration prior to installing the operating system(s) to minimize difficulties.

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Watchdog Timer

The VMIVME-7589 utilizes a Dallas DS1384 Watchdog Timekeeping Controller as its Watchdog Timer. The device provides a Time of Day feature, a Watchdog Alarm and an Non-Volatile SRAM controller. The Time of Day feature found within the DS1384 device is explained in this section, but is not utilized by the VMIVME-7589. The actual Time of Day registers used by the VMIVME-7589 are located at the standard PC / AT I / O address. The Time of Day feature in the DS1384 Watchdog Timer is available for use by the user at their discretion.

The Non-Volatile SRAM is explained in the Battery Backed SRAM section of this manual.

The Watchdog Timer provides a Watchdog alarm window and interval timing between 0.01 and 99.99 seconds. If enabled, and if jumper J30 is loaded, the Watchdog alarm will reset the CPU to a known state if not accessed during the alarm window.

Figure 4-7 shows a generalized block diagram of how the Watchdog Timer is used in the VMIVME-7589. The Watchdog Timer registers are memory-mapped in the bottom fourteen locations of battery-backed SRAM addresses $D8000 through $D800D. Table 4-12 shows the address, content and the range of each Watchdog Register.

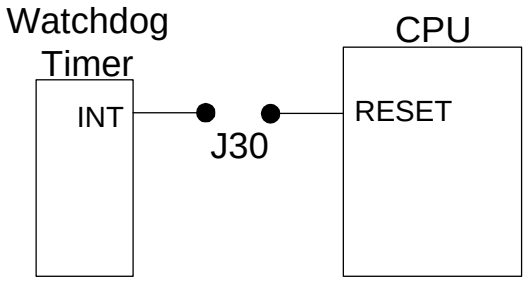

Figure 4-7 Watchdog Alarm Block

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Table 4-12 Watchdog Registers

Register	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Range
0	$D8000	0.1 Seconds (BCD)				0.01 Seconds (BCD)				00 - 99
1	$D8001	10 Seconds (BCD)				Seconds (BCD)				00 - 59
2	$D8002	10 Minutes (BCD)				Minutes (BCD)				00 - 59
3	$D8003	M	10 Minute Alarm (BCD)			Minute Alarm (BCD)				00 - 59
4	$D8004	0	12/24	AM/PM*	10 Hr	Hours (BCD)				
5	$D8005	M	12/24	AM/PM*	10 Hr	Hour Alarm (BCD)				
6	$D8006	0	0	0	0	Days (BCD)				01 - 07
7	$D8007	M	0	0	0	Day Alarm (BCD)				01 - 07
8	$D8008	0	0	10 Date (BCD)		Date (BCD)				01 - 31
9	$D8009	$\overline{\text{Eosc}}$	1**	0	10 Mo	Months (BCD)				01 - 12
A	$D800A	10 Years (BCD)				Years (BCD)				00 - 99
B	$D800B	Te	Ipsw	Ibh/lo	Pu/lvl	Wam	Tdm	Waf	Tdf	
C	$D800C	0.1 Seconds (BCD)				0.01 Seconds (BCD)				00 - 99
D	$D800D	10 Seconds (BCD)				Seconds (BCD)				00 - 99

* In the 12 hour mode Bit 5 determines AM (0) or PM (1). In the 24 hour mode Bit 5 combines with Bit 4 to represent the 10 hour value.
** Bit 6 of Register 9 must be set to a 1. If set to a 0, an unused square wave will be generated in the circuit.

Registers 0 through A are Clock, Calendar, Time of Day Registers.
Register B is the Command Register.
Registers C and D are Watchdog Alarm Registers.

The Watchdog Timer contains 14 registers which are 8-bits wide. These registers contain all of the Time of Day, Alarm, Watchdog, Control, and Data information. The Clock Calendar, Alarm, and Watchdog Registers have both external (user accessible) and internal memory locations containing copies of the data. The external memory locations are independent of the internal functions except that they are updated periodically by the transfer of the incremented internal values. Registers 0, 1, 2, 4, 6, 8, 9, and A contain Time of Day and Data information in Binary Coded Decimal (BCD). Registers 3, 5, and 7 contain the Time of Day Alarm information in BCD. The Command Register (Register B) contains data in binary. The Watchdog Alarm Registers are Registers C and D and information stored in these registers is in BCD.

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Time of Day Registers

Registers 0, 1, 2, 4, 6, 8, 9, and A contain Time of Day data in BCD.

Register 0 contains two Time of Day values. Bits 3 - 0 contain the 0.01 Seconds value with a range of 0 to 9 in BCD while Bits 7 - 4 contain the 0.1 Seconds value with a range of 0 to 9 in BCD. This Register has a total range of 0.00 to 0.99 Seconds.

Register 1 contains two Time of Day values. Bits 3 - 0 contain the 1 Seconds value with a range of 0 to 9 in BCD while Bits 7 - 4 contain the 10 Seconds value with a range of 0 to 5 in BCD. This Register has a total range of 0.0 to 59.0 Seconds. Bit 7 of this register will always be zero regardless of what value is written to it.

Register 2 contains two Time of Day values. Bits 3 - 0 contain the 0.01 Seconds value with a range of 0 to 9 in BCD while Bits 7 - 4 contain the 0.1 Seconds value with a range of 0 to 9 in BCD. This Register has a total range of 0.00 to 0.99 Seconds. Bit 7 of this register will always be zero regardless of what value is written to it.

Register 4 contains the Hours value of the Time of Day. The Hours can be represented in either 12 or 24 hour format depending on the state of Bit 6. When Bit 6 is set to a one (1) the format is 12 hour. When Bit 6 is set to a zero (0) the format is 24 hour. For the 12 hour format Bits 3 - 0 contain the 1 Hour value with a range of 0 to 9 in BCD and Bit 4 contains the 10 Hour value with a range of 0 to 1. In the 12 hour format Bit 5 is used as the AM / PM bit. When AM Bit 5 is a zero (0) and when PM bit 5 is a one (1). The total range of this register in the 12 hour format is 01 AM to 12 AM and 01 PM to 12 PM.

When Register 4 is in 24 hour format (Bit 6 is set to a zero (0)) Bits 3 - 0 contain the 1 Hour value with a range of 0 to 9 in BCD, Bit 5 combines with 4 to represent the 10 Hour value. The 10 Hour range is from 0 to 2. The total range of register 4 in the 24 hour format is 00 to 23 hours. Bit 7 of register 4 will always be zero regardless of what value is written to it and regardless of format (12 or 24 hour).

Register 6 contains the Days value of the Time of Day. Bits 2 - 0 contain the Days value with a range of 1 to 7 in BCD.

Register 8 contains two Time of Day values. Bits 3 - 0 contain the Date value with a range of 0 to 9 in BCD while Bits 5 - 4 contain the 10 Date value with a range of 0 to 3. This Register has a total range of 01 to 31. Bits 7 - 6 of this register will always be zero regardless of what value is written to it.

Register 9 contains two Time of Day values. Bits 3 - 0 contain the Months value with a range of 0 to 9 in BCD while Bits 4 contain the 10 Date value with a range of 0 to 1. This Register has a total range of 01 to 12. Bit 5 will always be zero regardless of what value is written to it. Bit 6 is unused but must be set to a 1. Bit 7, $\overline{\text{Eosc}}$, is the clock oscillator enable bit. When this bit is set to a zero (0) the oscillator is internally enabled. When set to a one (1) the oscillator is internally disabled. The oscillator via this bit is usually turned on once during system initialization but can be toggled on and off at the users discretion.

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There are two techniques for reading the Time of Day from the Watchdog Timer. The first is to halt the external Time of Day registers from tracking the internal Time of Day registers by setting the Te bit (Bit 7 of the Command Register) to a logic zero (0) then reading the contents of the Time of Day registers. Using this technique eliminates the chance of the Time of Day changing while the read is taking place. At the end of the read, the Te bit is set to a logic one (1) allowing the external Time of Day registers to resume tracking the internal Time of Day Registers. No time is lost as the internal Time of Day Registers continue to keep time while the external Time of Day registers are halted. This is the recommended method.

The second technique for reading the Time of Day from the Watchdog Timer is to read the external Time of Day registers without halting the tracking of the internal Registers. This is not recommended as the registers may be updated while the reading is taking place, resulting in erroneous data being read.

Time of Day Alarm Registers

Registers 3, 5, and 7 are the Time of Day Alarm registers and are reformatted similar to Register 2, 4, and 6 respectively. Bit 7 of registers 3, 5, and 7 is a mask bit. The mask bits, when active (logic one (1)), disable the use of the particular Time of Day Alarm register in the determination of the Time of Day Alarm (see Table 4-13). When all the mask bits are low (0) an alarm will occur when Registers 2, 4, and 6 match the values found in registers 3, 5, and 7. When Register 7's mask bit is set to a logic one (1) register 6 will be disregarded in the determination of the Time of Day alarm and an alarm will occur everyday. When registers 7 and 5's mask bit is set to a logic one (1), Register 6 and 4 will be disregarded in the determination of the Time of Day alarm and an alarm will occur every hour. When Registers 7, 5 and 3's mask bit is set to a logic one (1), Register 6, 4, and 2 will be disregarded in the determination of the Time of Day alarm and an alarm will occur every minute (when register 1's seconds step from 59 to 00).

Table 4-13 Time of Day Alarm Registers

Register			Comment
Minutes	Hours	Days	
1	1	1	Alarm once per minute
0	1	1	Alarm when minutes match
0	0	1	Alarm when hours and minutes match
0	0	0	Alarm when hours, minutes, and days match

The Time of Day Alarm registers are read and written to in the same format as the Time of Day registers. The Time of Day alarm flag and interrupt are cleared when the alarm registers are read or written.

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Watchdog Alarm Registers

Register C contains two Watchdog alarm values. Bits 3 - 0 contain the 0.01 Seconds value with a range of 0 to 9 in BCD while Bits 7 - 4 contain the 0.1 Seconds value with a range of 0 to 9 in BCD. This Register has a total range of 0.00 to 0.99 Seconds.

Register D contains two Watchdog Alarm values. Bits 3 - 0 contain the 1 Second value with a range of 0 to 9 in BCD while Bits 7 - 4 contain the 10 Seconds value with a range of 0 to 9 in BCD. This Register has a total range of 00.0 to 99.0 Seconds.

The Watchdog Alarm Registers can be read or written in any order. When a new value is entered or the Watchdog registers are read, the Watchdog Timer will start counting down from the entered value. When zero is reached the Watchdog Interrupt Output will go active. If jumper J30 is loaded, the CPU will reset to a known state Refer to Figure 4-7. The Watchdog Timer count is reinitialized back to the entered value, the Watchdog flag bit is cleared, and the Watchdog interrupt output is cleared every time either of the registers are accessed. Periodic accesses to the Watchdog Timer will prevent the Watchdog Alarm from occurring. If access does not occur, the alarm will be repetitive. The Watchdog Alarm Register always reads the entered value. The actual countdown value is internal and not accessible to the user. Writing zero's to Registers C and D will disable the Watchdog Alarm feature.

Command Register

Register B is the Command Register. Within this register are mask bits, control bits, and flag bits. The following paragraphs describe each bit.

Te - Bit 7 Transfer Enable - This bit enables and disables the tracking of data between the internal and external registers. When set to a logic zero (0), tracking is disabled that is the data in the external register is frozen. When set to a logic one (1), tracking is enabled. This bit must be set to a logic one (1) to allow the external register to be updated.

Ipsw - Bit 6 Interrupt Switch - This bit toggles the Interrupt Output between the Time of Day Alarm and the Watchdog Alarm. When set to a logic zero (0), the Interrupt Output is from the Watchdog Alarm. When set to a logic one (1), the Interrupt Output is from the Time of Day Alarm.

Ibh/lo - Bit 5 Reserved - This bit should be set to a logic low (0).

Pu/lvl - Bit 4 Interrupt Pulse Mode or Level Mode - This bit determines whether the Interrupt Output will output as a pulse or a level. When set to a logic zero (0), Interrupt Output will be a level. When set to a logic one (1), Interrupt Output will be a pulse. In pulse mode the Interrupt Output will sink current for a minimum of 3 ms. This bit should be set to a logic one (1).

Wam - Bit 3 Watchdog Alarm Mask - Enables / Disables the Watchdog Alarm to Interrupt Output when Ipsw (Bit 6, Interrupt Switch) is set to logic zero (0). When set to a logic zero (0), Watchdog Alarm Interrupt Output will be enabled. When set to a logic one (1), Watchdog Alarm Interrupt Output will be disabled.

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Tdm - Bit 2 Time of Day Alarm Mask - Enables / Disables the Time of Day Alarm to Interrupt Output when Ipsw (see Bit 6, Interrupt Switch) is set to logic one (1). When set to a logic zero (0), Time of Day Alarm Interrupt Output will be enabled. When set to a logic one (1), Time of Day Alarm Interrupt Output will be disabled.

Waf - Bit 1 Watchdog Alarm Flag - This is a read-only bit set to a logic one (1) when a Watchdog Alarm Interrupt occurs. This bit is reset when any of the Watchdog Alarm registers are accessed. When the Interrupt Output is set to Pulse Mode (see Bit 4, Interrupt Pulse Mode or Level Mode), the flag will be set to a logic one (1) only when the Interrupt Output is active.

Tdf - Bit 0 Time of Day Alarm Flag - This is a read-only bit set to a logic one (1) when a Time of Day Alarm Interrupt occurs. This bit is reset when any of the Time of Day Alarm registers are accessed. When the Interrupt Output is set to Pulse Mode (see Bit 4, Interrupt Pulse Mode or Level Mode), the flag will be set to a logic one (1) only when the Interrupt Output is active.

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Battery Backed SRAM

The VMIVME-7589 includes 32 K byte of battery-backed SRAM addressed at $D8000 to $DFFFF (the lower 14 bytes, $D8000 to $D800D, are dedicated to Watchdog Timer registers and are unavailable for general use. See the Watchdog Timer section). The battery-backed SRAM can be accessed by the CPU at anytime, and can be used to store system data that must not be lost during power-off conditions.

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CHAPTER 5

Maintenance

If a VMIC product malfunction, please verify the following:

1. Software resident on the product
2. System configuration
3. Electrical connections
4. Jumper or configuration options
5. Boards are fully inserted into their proper connector location
6. Connector pins are clean and free from contamination
7. No components or adjacent boards were disturbed when inserting or removing the board from the chassis
8. Quality of cables and I/O connections

If products must be returned, contact VMIC for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return**.

VMIC Customer Service is available at: 1-800-240-7782.
Or E-mail us at customer.service@vmic.com

Maintenance Prints

User level repairs are not recommended. The drawings and diagrams in this manual are for reference purposes only.

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Appendix

A

Connector Pinouts

Contents

Introduction

The VMIVME-7589 PC / AT-Compatible VMEbus Controller has several connectors for its I / O ports. Figure A-1 shows the locations of the connectors on the VMIVME-7589. Wherever possible, the VMIVME-7589 uses connectors and pinouts typical for any desktop PC. This ensures maximum compatibility with a varity of systems.

Connector diagrams in this appendix are generally shown in a natural orientation with the controller board mounted in a VMEbus chassis.

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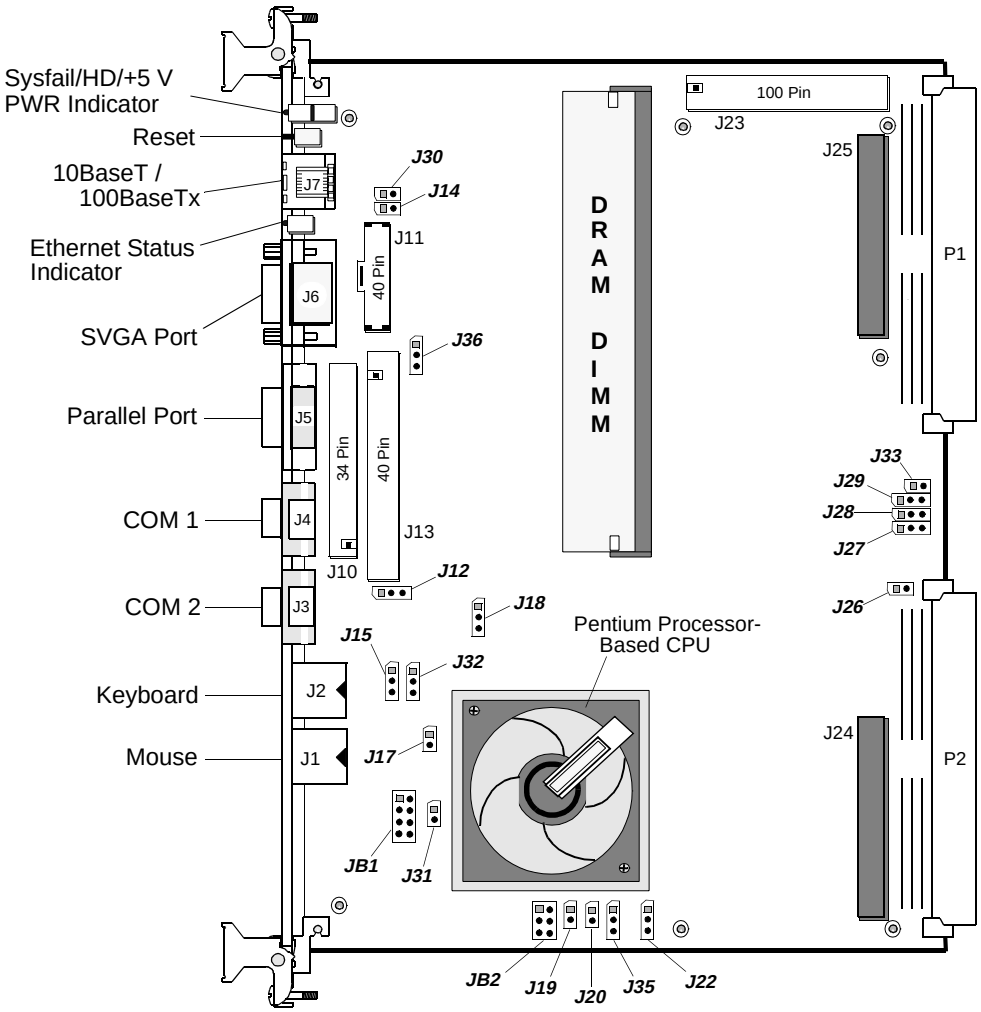

Figure A-1 VMIVME-7589 Connector and Jumper Locations

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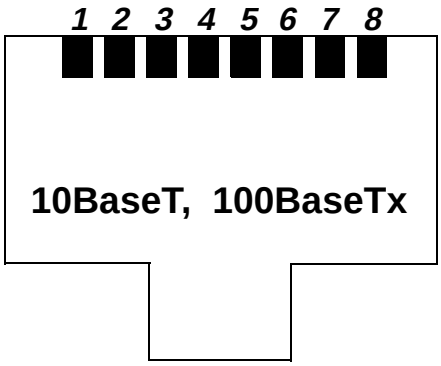
Ethernet Connector Pinout

The pinout diagram for the Ethernet 10BaseT and 100BaseTx connectors are shown in Figure A-2.



ETHERNET CONNECTOR (10BaseT, 100BaseTx)		
PIN	**Signal Name**	
1	TD+	Transmit Data
2	TD-	Transmit Data
3	RD+	Receive Data
4	NC	No Connection
5	NC	No Connection
6	RD-	Receive Data
7	NC	No Connection
8	NC	No Connection

Figure A-2 Ethernet Connector Pinout

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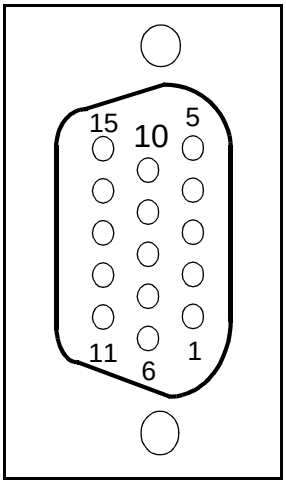
Video Connector Pinout

The video port uses a standard high-density D15 SVGA connector. Figure A-3 illustrates the pinout.



VIDEO CONNECTOR		
PIN	**DIRECTION**	**FUNCTION**
1	Out	Red
2	Out	Green
3	Out	Blue
4		Reserved
5		Ground
6		Ground
7		Ground
8		Ground
9		Reserved
10		Ground
11		Reserved
12		Reserved
13	Out	Horizontal Sync
14	Out	Vertical Sync
15		Reserved
Shield		Chassis Ground

Figure A-3 Video Connector Pinout

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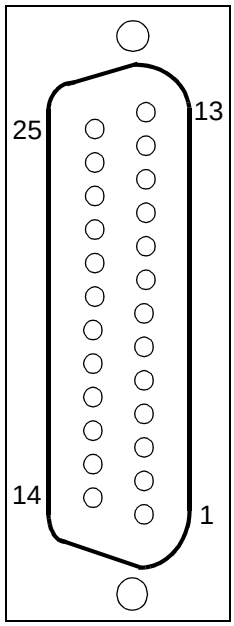
Parallel Port Connector Pinout

The printer port shown in Figure A-4 uses a Microminiature D25 female connector typical of any PC / AT system.



PARALLEL PORT CONNECTOR		
PIN	**DIRECTION**	**FUNCTION**
1	In / Out	Data Strobe
2	In / Out	Bidirectional Data D0
3	In / Out	Bidirectional Data D1
4	In / Out	Bidirectional Data D2
5	In / Out	Bidirectional Data D3
6	In / Out	Bidirectional Data D4
7	In / Out	Bidirectional Data D5
8	In / Out	Bidirectional Data D6
9	In / Out	Bidirectional Data D7
10	In	Acknowledge
11	In	Device Busy
12	In	Out of Paper
13	In	Device Selected
14	Out	Auto Feed
15	In	Error
16	Out	Initialize Device
17	In	Device Ready for Input
18		Signal Ground
19		Signal Ground
20		Signal Ground
21		Signal Ground
22		Signal Ground
23		Signal Ground
24		Signal Ground
25		Signal Ground
Shield		Chassis Ground

Figure A-4 Parallel Port Connector Pinout

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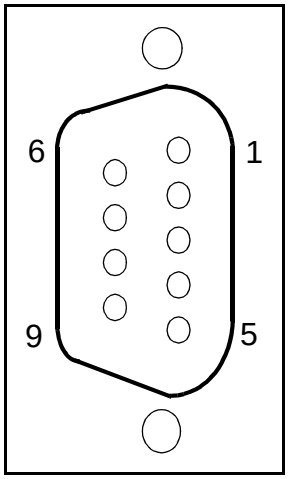
Serial Connector Pinout

Each standard RS-232 serial port connectors is a Microminiature D9 male as shown in the upper drawing in Figure A-5. The boards are supplied with adapters to connect standard D9 serial peripherals.



SERIAL COM PORT CONNECTORS			
D9 PIN	**DIR**	**RS-232 SIGNAL**	**FUNCTION**
1*	In	DCD	Data Carrier Detect
2	In	RX	Receive Data
3	Out	TX	Transmit Data
4	Out	DTR	Data Terminal Ready
5		GND	Signal Ground
6	In	DSR	Data Set Ready
7	Out	RTS	Request to Send
8	In	CTS	Clear to Send
9*	In	RI	Ring Indicator
Shield			Chassis Ground

* RJ45 pin 8 is either assigned to the DCD or the RI signal, depending upon a jumper on the controller board. If the supplied RJ45-to-D9 adapter is being used, D9 pin 9 is not connected and D9 pin 1 is the DCD or RI signal from RJ45 pin 8.

Figure A-5 Serial Connector Pinouts

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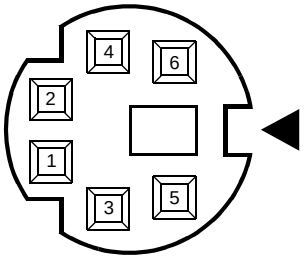
Keyboard Connector Pinout

The keyboard connector is a standard 6-pin female mini-DIN PS/2 connector as shown in Figure A-6.



KEYBOARD CONNECTOR		
PIN	**DIR**	**FUNCTION**
1	In/Out	Data
2		Reserved
3		Ground
4		+5 V
5	Out	Clock
6		Reserved
Shield		Chassis Ground

Figure A-6 Keyboard Connector Pinout

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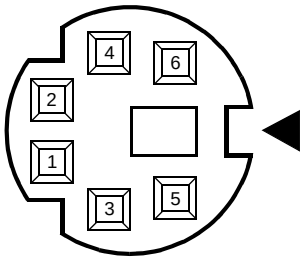
Mouse Connector Pinout

The mouse connector is a standard 6-pin female mini-DIN PS/2 connector as shown in Figure A-7.



MOUSE CONNECTOR		
PIN	**DIR**	**FUNCTION**
1	In/Out	Data
2		Reserved
3		Ground
4		+5 V
5	Out	Clock
6		Reserved
Shield		Chassis Ground

Figure A-7 Mouse Connector Pinout

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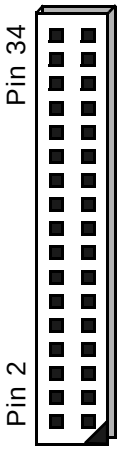
Floppy Interface Connector Pinout

The floppy drive connector is a dual-row 34-pin header connector and is located at site J10 on Figure A-1 on page 80. Pin 1 marks the beginning of the odd-numbered row. Most standard PC-compatible floppy disk drives use this pinout, which is illustrated in Figure A-8. The user should exercise caution when aligning the floppy drive connector and cable.



FLOPPY DRIVE CONNECTOR		
PIN	**DIRECTION**	**FUNCTION**
1		Ground
2	From Controller	Drive Density 0 (not connected on some controllers)
3		Ground
4		Reserved
5		Ground
6	From Controller	Drive Density 1 (not connected on some controllers)
7		Ground
8	From Drive	Index
9		Ground
10	From Controller	Motor Enable A
11		Ground
12	From Controller	Drive Select B
13		Ground
14	From Controller	Drive Select A
15		Ground
16	From Controller	Motor Enable B
17		Ground
18	From Controller	Step Motor Direction
19		Ground
20	From Controller	Step Pulse
21		Ground
22	From Controller	Write Data
23		Ground
24	From Controller	Write Enable
25		Ground
26	From Drive	Track 0
27		Ground
28	From Drive	Write Protect
29		Ground
30	From Drive	Read Data
31		Ground
32	From Controller	Select Head 1
33		Ground
34	From Drive	Disk Change

Figure A-8 Floppy Drive Connector Pinout

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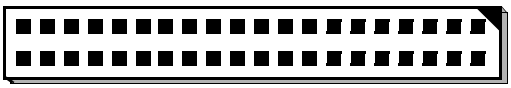
EIDE Hard Drive Connector Pinout

Figure A-9 describes the pin assignment for the 40-pin EIDE / ATA hard drive header connector. The connector is located at the J13 site in Figure A-1 on page 80. Like the floppy header connector it has an odd-numbered row and an even-numbered row. The user should exercise caution to align the hard drive connector and cable.



Pin 40 Pin 2

PIN	DIRECTION	DESCRIPTION	PIN	DIRECTION	DESCRIPTION
1	Out	Reset Drive	2	Out	Signal Ground
3	In / Out	Bidirectional Data 07	4	In / Out	Bidirectional Data 08
5	In / Out	Bidirectional Data 06	6	In / Out	Bidirectional Data 09
7	In / Out	Bidirectional Data 05	8	In / Out	Bidirectional Data 10
9	In / Out	Bidirectional Data 04	10	In / Out	Bidirectional Data 11
11	In / Out	Bidirectional Data 03	12	In / Out	Bidirectional Data 12
13	In / Out	Bidirectional Data 02	14	In / Out	Bidirectional Data 13
15	In / Out	Bidirectional Data 01	16	In / Out	Bidirectional Data 14
17	In / Out	Bidirectional Data 00	18	In / Out	Bidirectional Data 15
19	Out	Signal Ground	20	None	Unused, Keying Position
21		Reserved	22	Out	Signal Ground
23	Out	Write Strobe	24	Out	Signal Ground
25	Out	Read Strobe	26	Out	Signal Ground
27		Reserved	28	Out	Address Latch Enable
29		Reserved	30	Out	Signal Ground
31	In	Interrupt Request #14	32	In	16-bit Data Word Size
33	Out	Address Line #1	34	In	Diagnostic Test Passed
35	Out	Address Line #0	36	Out	Address Line #2
37	Out	Chip Select #0	38	Out	Chip Select #1
39	In	Slave/Activity Status	40	Out	Signal Ground

Figure A-9 EIDE Hard Drive Connector Pinout

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VMEbus Connector Pinout

Figure A-10 shows the location of the VMEbus P1 and P2 connectors and their orientation. Table A-1 shows the pin assignments for the VMEbus connectors. Note that only Row B of connector P2 is used; all other pins on P2 are reserved and should not be connected.

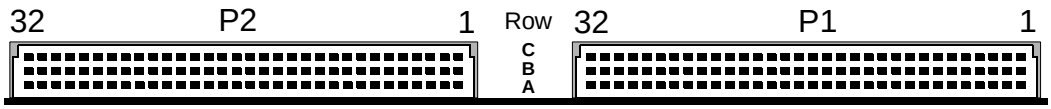

Figure A-10 VMEbus Connector Diagram

Table A-1 VMEbus Connector Pinout

PIN NUMBER	P1 ROW A SIGNAL	P1 ROW B SIGNAL	P1 ROW C SIGNAL	P2 ROW A SIGNAL	P2 ROW B SIGNAL	PC ROW C SIGNAL
1	D00	BBSY	D08	GND	+5 V	IDE RST#
2	D01	BCLR	D09	DDP8	GND	DDP7
3	D02	ACFAIL	D10	DDP9	Reserved	DDP6
4	D03	BG0IN	D11	DDP10	A24	DDP5
5	D04	BG0OUT	D12	DDP11	A25	DDP4
6	D05	BG1IN	D13	DDP12	A26	DDP3
7	D06	BG1OUT	D14	DDP13	A27	DDP2
8	D07	BG2IN	D15	DDP14	A28	DDP1
9	GND	BG2OUT	GND	DDP15	A29	DDP0
10	SYSCLK	BG3IN	SYSFAIL	IDE REQ0	A30	IOCS1.64#
11	GND	BG3OUT	BERR	IDE IOW0 #	A31	GND
12	DS1	BR0	SYSRESET	IDE IOR0 #	GND	GND
13	DS0	BR1	LWORD	IDE IORDY0#	+5 V	GND
14	WRITE	BR2	AM5	HD_ACT #	D16	IDESELA

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Table A-1 VMEbus Connector Pinout (Continued)

PIN NUMBER	P1 ROW A SIGNAL	P1 ROW B SIGNAL	P1 ROW C SIGNAL	P2 ROW A SIGNAL	P2 ROW B SIGNAL	PC ROW C SIGNAL
15	GND	BR3	A23	GND	D17	IDE DACK0#
16	DTACK	AM0	A22	GND	D18	IDE IRQ0
17	GND	AM1	A21	DAP1	D19	DAP 2
18	AS	AM2	A20	IDECS01 #	D20	DAP 0
19	GND	AM3	A19	GND	D21	IDE CS03#
20	IACK	GND	A18	DRATED	D22	REDWC
21	IACKIN	SERCLK	A17	GND	D23	INDEX#
22	IACKOUT	SERDAT	A16	DRVSB #	GND	MOTEA#
23	AM4	GND	A15	GND	D24	DRUSA#
24	A07	IRQ7	A14	GND	D25	MOTEB#
25	A06	IRQ6	A13	GND	D26	STEP#
26	A05	IRQ5	A12	GND	D27	WD4TA#
27	A04	IRQ4	A11	GND	D28	TRK#
28	A03	IRQ3	A10	GND	D29	RDATA#
29	A02	IRQ2	A09	DSKCHG #	D30	SIDE1#
30	A01	IRQ1	A08	GND	D31	DIR
31	-12 V	+5 V STDBY	+12 V	VCC	GND	WGATE
32	+5 V	+5 V	+5 V	VCC	+5 V	WPT

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PCI Expansion Connector Pinout

The following PCI Expansion Female Connector diagram illustrates orientation and Table A-2 defines the connector pin assignments for connector J23.

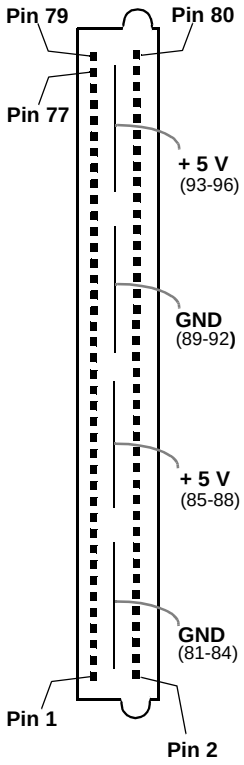

Table A-2 PCI Expansion Connector Pin Description

Left Side		Right Side		Left Side		Right Side	
Pin	**Name**	**Pin**	**Name**	**Pin**	**Name**	**Pin**	**Name**
1	+12 V	2	-12 V	49	C1BE0#	50	AD[8]
3	INTA#	4	INTB#	51	AD[6]	52	AD[7]
5	INTC#	6	INTD#	53	AD[4]	54	AD[5]
7	+12 V	8	CLK	55	AD[2]	56	AD[3]
9	RST#	10	REQ#	57	AD[0]	58	AD[1]
11	6NT#	12	AD[31]	59	NC	60	NC
13	AD[30]	14	AD[29]	61	BMODE1A#	62	BMODE1B#
15	AD[28]	16	AD[27]	63	IRQ4	64	IRQ3
17	AD[26]	18	AD[25]	65	IRQ7	66	IRQ5
19	AD[24]	20	C1BG3#	67	IRQ10	68	IRQ9
21	AD[22]	22	AD[23]	69	IRQ12	70	IRQ11
23	AD[20]	24	AD[21]	71	IRQ15	72	IRQ14
25	AD[18]	26	AD[19]	73	NC	74	NC
27	AD[16]	28	AD[17]	75	NC	76	NC
29	FRAME#	30	C1BG2#	77	NC	78	NC
31	TRDY#	32	IRDY#	79	NC	80	NC
33	STOP#	34	DEVSGL#	81	GND	82	GND
35	NC	36	LOCK#	83	GND	84	GND
37	NC	38	PERR#	85	+5 V	86	+5 V
39	PAR	40	SERR#	87	+5 V	88	+5 V
41	AD[15]	42	C1BG1#	89	GND	90	GND
43	AD[13]	44	AD[14]	91	GND	92	GND
45	AD[11]	46	AD[12]	93	+5 V	94	+5 V
47	AD[9]	48	AD[10]	95	+5 V	96	+5 V

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Appendix

B

System Driver Software

Contents

Introduction

The VMIVME-7589 provides high-performance video, and Local Area Network (LAN) access by means of on-board PCI-based adapters and associated software drivers. The PCI-based video adapter used on the VMIVME-7589 is the Cirrus Logic 5480. High-performance LAN operation including 10BaseT and 100BaseTx, is provided by the DEC 21143 Ethernet controller chip.

To optimize performance of each of these PCI-based subsystems, the VMIVME-7589 is provided with software drivers compatible with DOS, Windows for Workgroups™ Version 3.11, Windows® 95 OS, and Windows NT® operating systems. The following paragraphs provide instructions for loading and installing the adapter software.

Driver Software Installation

In order to properly use the Video and LAN adapters of the VMIVME-7589, the user must install the driver software provided as distribution diskettes with the unit. Detailed instructions for installation of the drivers during installation of Windows for Workgroups Version 3.11, Windows 95 OS, or Windows NT (Versions 3.5x and 4.0) operating systems are described in the following sections.

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Windows for Workgroups™ OS (Version 3.11)

1. Format and load the IDE hard drive with MS-DOS®.
2. Begin installation of Windows for Workgroups 3.11 OS, following the instruction provided by Microsoft for Express Setup. When you reach the 'WINDOWS FOR WORKGROUPS NETWORK SETUP' screen, it will show that 'NO NETWORK IS INSTALLED'.
3. The following steps will load the DEC Ethernet drivers, and configure the DEC 21143 adapter.

Note

If you do not require LAN operation, click the mouse on 'CONTINUE' and skip steps 4 through 12. Otherwise from the main 'NETWORK SETUP' screen, click the mouse on the 'NETWORKS' button.

4. Under 'NETWORKS', click the mouse on the circle to install 'MICROSOFT WINDOWS NETWORK'.
5. Then Click the mouse on 'OK'.
6. The 'NETWORK SETUP SCREEN' appears again with the option for 'SHARING'. Click on 'SHARING' and choose the options that fit your system requirements by placing an x in the boxes shown. Then click on 'OK'.
7. Again at the 'NETWORK SETUP SCREEN', click on 'CONTINUE'.
8. Under 'ADD NETWORK ADAPTER' click the mouse on 'UNLISTED or UPDATED NETWORK ADAPTER'. Then click the mouse on 'OK'.
9. Insert the VMIVME-7589 distribution disk marked 320-500013-008 into drive A: and type: `A:\32bit\WFW311\.` Then click the mouse on 'OK'.
10. Under 'UNLISTED' or 'UPDATED NETWORK ADAPTER', choose 'Digital Semiconductor 21143-based 10/100 mpbs Ethernet Controller (ND153)'. Then click the mouse on 'OK'.
11. Under 'MICROSOFT WINDOWS NETWORK NAMES', enter the network names you want for computer name, group name, etc. Then click the mouse on 'OK'.
12. Windows for Workgroups OS should now continue with regular installation. During the remaining installation steps, use the full path name, A:\32bit\WFW311\, whenever prompted for the DEC 21143 driver diskette.
13. After Windows for Workgroups OS installation is complete, you may choose to install the Cirrus Logic video drivers. If you do not require the Cirrus Logic video drivers for operation, please skip steps 14 through 21.
14. Insert the VMIVME-7589 distribution diskette marked 320-500013-001 into drive A:

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15. From the Program Manager Screen double-click the mouse on the 'MAIN' icon.
16. Next double-click the mouse on the 'MS-DOS' icon.
17. Type the following command: **A:\INSTALL <ENTER>**. This will create directories on the C: drive and copy the video drivers and utilities. The default selections may be chosen for simplicity.
18. After the files are installed, the installation utilities boots WinMode which will allow the selection of the system monitor type.
19. In the 'WINMODE' screen, adjust the monitor settings as required and then click on 'OK'.
20. Click the mouse on 'OK' to restart windows.
21. There will now be a 'VGA DISPLAY' icon in the 'PROGRAM MANAGER' window. In the 'VGA DISPLAY' window, there will be a 'WINMODE' icon that will allow the user to adjust the VGA display.
22. In order for the network to be setup properly, it is necessary to setup the proper connection type for your system.

Proceed with the following steps to set your network connection type.

Note

If you are not running a network, please skip steps 23 through 27.

23. From the 'PROGRAM MANAGER' screen, double-click on the 'NETWORK' icon.
24. Then double-click on 'NETWORK SETUP' icon.
25. Under 'NETWORK SETUP', double-click on 'Digital Semiconductor 21143-based 10/100 mpbs Ethernet Controller (ND153)'.
26. Under 'ADVANCED NETWORK-ADAPTER SETTINGS', choose 'CONNECTION TYPE' and choose the 'CONNECTION TYPE VALUE' of '*AUTO SENSE TYPE*'. Click on 'SET' and then 'OK'.
27. Under 'NETWORK SETUP', click on 'OK'. If the network connection type has changed, then click 'OK' at the next screen for the information message about 'SYSTEM.INI' and 'PROTOCOL.INI' and click on 'RESTART COMPUTER' for the new network settings to take effect.

The unit should now be configured for operation in the WINDOWS FOR WORKGROUPS 3.11 OS environment.

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Windows® 95 OS

1. Format the hard drive with MS-DOS.
2. Begin installation of Windows 95 OS, following the instructions provided by the Windows 95 OS manual.
3. When you reach the 'WINDOWS 95 SETUP WIZARD SCREEN', choose 'TYPICAL' under 'SETUP OPTIONS' and then click on 'NEXT'.
4. When you reach the 'ANALYZING YOUR COMPUTER' screen, place an x in the box for 'NETWORK ADAPTER', then click on 'NEXT'.
5. Under the 'WINDOWS COMPONENTS SCREEN', select 'INSTALL THE MOST COMMON COMPONENTS' and then click on 'NEXT'.
6. Continue with the installation until Windows 95 OS is completely installed and has rebooted.

If you do not require LAN operation, skip steps 7 through 24.

7. From the main Windows 95 OS screen, click on 'START'.
8. Then click on 'SETTINGS' and then 'CONTROL PANEL'.
9. Double-click on the 'SYSTEM' icon and select the 'DEVICE MANAGER' tab.
10. Double-click on 'OTHER DEVICES' and then double-click on 'PCI ETHERNET CONTROLLER'.
11. Select the 'DRIVER' tab and then select 'CHANGE DRIVER'.
12. In the 'SELECT HARDWARE TYPE' screen, choose 'NETWORK ADAPTERS' and click on 'OK'.
13. Insert the Diskette marked 320-500013-008 into drive A:
14. In the 'SELECT DEVICE' window, click on 'HAVE DISK' and type `A:\32bit\WIN95\INF` and then click on 'OK'.
15. Under 'SELECT NETWORK ADAPTERS' choose 'DIGITAL SEMICONDUCTOR 21143-BASED 10/100 MPBS ETHERNET CONTROLLER', then click on 'OK'.
16. Under 'PCI ETHERNET CONTROL PROPERTIES' select 'OK'. Then the system will prompt you for computer and workgroup names. Type in the names you wish to use in the spaces shown and then choose 'CLOSE'.
17. Windows 95 OS will then prompt for diskettes. Follow all instructions.
18. At the 'SYSTEM PROPERTIES' window, click on 'OK'.
19. The driver files are located at A:\32bit\WIN95\. If prompted for the Windows 95 OS system disk, indicate the location of the files. For example, if you are loadingfrom a CD-ROM located a D:, the desire response is D:\WIN95.

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20. From ‘CONTROL PANEL’, double-click on the ‘NETWORK’ icon.
21. Under ‘NETWORK’, click on ‘FILE AND PRINT SHARING’ and choose the appropriate items for your system, click on ‘OK’.
22. Under the ‘NETWORK’ window, double-click on ‘Digital Semiconductor 21143-based 10/100 mpbs Ethernet Controller (ND153)’.
23. At the ‘NETWORK’ window, click on ‘OK’. When prompted, insert the diskettes needed to complete the network installation.
24. When the system prompts you to restart your computer, click on ‘YES’ for the network settings to take effect.
25. From the main Windows 95 OS screen, click on ‘START’.
26. Next, click on ‘SETTINGS’ and the ‘CONTROL PANEL’.
27. Double-click on the ‘DISPLAY’ icon and select the ‘SETTINGS’ tab.
28. Click on ‘CHANGE DISLAY TYPE’, then click on ‘CHANGE’ in the ‘Adapter Type’ field.
29. Select ‘Cirrus Logic’ as the manufacturer, then click ‘HAVE DISK’.
30. Insert the diskette labeled 320-500013-004 into drive A:. Type ‘A:\’ as the files source (if not already displayed) and click on ‘OK’.
31. Under ‘SELECT DEVICE’, choose ‘Cirrus Logic 5480 PCI W/VPM (v.1.01b)’, then click on ‘OK’.
32. Insert the diskette labeled 320-500013-005 when prompted for the second disk, then click on ‘OK’.
33. When the CHOOSE DISPLAY TYPE’ screen returns, click on ‘CLOSE’.
34. Restart the computer if prompted to allow the new settings to take effect.

The unit should now be properly configured for operation in Windows 95 OS.

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Windows NT® OS (Version 3.51)

1. Format the hard drive with MS-DOS.
2. Install the Windows NT OS boot disk in drive A, and reboot the computer.
3. When prompted, insert Windows NT OS Setup Disk 2 into drive A:.
4. From the 'WELCOME TO SETUP' screen, press <ENTER> to set up Windows NT OS.
5. From the 'WINDOWS NT OS SETUP METHODS' screen, select the Express SETUP'.
6. Continue the installation procedure until the 'NETWORK ADAPTER CARD DETECTION' window is displayed. Click on 'CONTINUE' to manually select the network adapter card.
7. Choose 'CONTINUE' again when prompted.
8. In the 'ADD NETWORK ADAPTER' window, select the '<OTHER> REQUIRES DISK FROM MANUFACTURER' option, then click on 'CONTINUE'.
9. Insert disk 320-500013-008 into drive A:. Type A:\32bit\wnt351, then click 'OK'.
10. In the 'SELECT OEM OPTION' window, select Digital Semiconductor 21143-based 10/100 mpbs Ethernet Controller, then click n 'OK'.
11. In the 'DIGITAL SEMICONDUCTOR 21143-BASED 10/100 MPB ETHERNET CONTROLLER SETUP' window, select 'AUTOSENSE', then click on 'CONTINUE'.
12. A window will appear to allow the selection of network protocols. Deselect 'TCP/IP TRANSPORT' and select 'NetBEUI TRANSPORT'. Click on 'Continue'.
13. Enter the network information and account management information as required for the installation.
14. From the 'PROGRAM MANAGER' window, double-click on the 'MAIN' icon.
15. Then double-click on the 'CONTROL PANEL' icon.
16. Double-click on 'DISPLAY'.
17. Under 'DISPLAY SETTINGS' screen, click on 'CHANGE DISPLAY TYPE'.
18. Under 'DISPLAY TYPE' window, click on 'CHANGE'.
19. Under 'SELECT DEVICE' window, click on 'OTHER' button.
20. Insert disk 320-500013-003, then click on 'OK'.
21. Highlight 'CIRRUS LOGIC 256/64K/16M COLORS' and click on 'INSTALL'.
22. The message window 'INSTALLING DRIVERS' appears letting you know that the drivers were successfully installed. Click on 'OK'.
23. At the next screen, press 'OK' to restart.
24. Then press 'RESTART NOW'.

The unit should now be properly configured for Windows NT OS 3.51.

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Windows NT® OS (Version 4.0)

Windows NT 4.0 OS includes drivers for the on-board LAN and video adapters. The following steps are required to configure the LAN for operation:

1. Follow the normal Windows NT 4.0 OS installation until you reach the 'WINDOWS NT WORKSTATION SETUP' window which states that 'WINDOWS NT NEEDS TO KNOW HOW THIS COMPUTER SHOULD PARTICIPATE ON A NETWORK'.
2. Place a dot next to 'THIS COMPUTER WILL PARTICIPATE ON A NETWORK'.
3. Place a check mark next to 'WIRED TO THE NETWORK' and then click on 'NEXT'.
4. At the next screen, click on the 'SELECT FROM LIST' button.
5. Click on the 'HAVE DISK' button.
6. Insert disk 320-500013-008 into drive A:.
7. Type A:\32bit\wnt40\ND1540 and click on 'OK'.
8. In the "SELECT OEM OPTION', choose 'Digital Semiconductor 21143-based 10/100 mpbs Ethernet Controller (NDIS4)', then click 'OK'.
9. Select the above entry on the displayed list, click on 'NEXT'.
10. Select the NetBEUI Protocol (only), click on 'NEXT'.
11. Click 'CONTINUE' to allow an Autosense connection type.
12. Step through the remaining screens, providing the data pertinent to your network.
13. Continue through the setup procedure until the 'DETECTED DISPLAY' window appears, click on 'OK' to continue.
14. In the 'DISPLAY PROPERTIES' window, click on 'TEST'.

Please note that Windows NT OS 4.0 does not allow the selection of the Cirrus Logic 5480 drivers during initial setup.

If the display test is successful, click on 'OK' to continue. If the display test is not successful, you may have to adjust the display parameter to find a functional setting, for example a lower resolution or lower number of colors.

15. Continue with the procedure to the 'Windows NT Setup' window. Click on 'RESTART COMPUTER'.
16. When the computer reboots, double-click on 'MY COMPUTER' window.
17. Double-click on the 'CONTROL PANEL' icon in the 'MY COMPUTER' window.

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18. Double-click on the ‘DISPLAY’ icon in the ‘CONTROL PANEL’.
19. Select the ‘SETTINGS’ tab in the ‘DISPLAY PROPERTIES’ window, then click on the ‘DISPLAY TYPE’ button.
20. In the ‘DISPLAY TYPE’ window, click on ‘CHANGE’.
21. In the ‘CHANGE DISPLAY’ window, click on ‘HAVE DISK’.
22. Insert disk 320-500013-003 into drive A:, then click on ‘OK’.
23. “Cirrus Logic CL-GD54xx Graphics Adapter’ will be displayed in the ‘CHANGE DISPLAY’ window. Click on ‘OK’.
24. Proceed as directed, removing the driver disk from the floppy drive, and the computer will restart to activate the new settings. When the system reboots, the display settings may be configured for your display type.

The unit should now be configured for operation under Windows NT 4.0 OS.

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Appendix

C

AMI - Basic Input/Output System

Contents

Introduction

The VMIVME-7589 utilizies BIOS in the same manner as other PC / AT compatible computers. This appendix describes the menus and options associated with the VMIVME-7589.

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System BIOS Setup Utility

During boot-time, continuously press the F1 key until the AMIBIOS Hiflex Setup Utility screen is displayed. From this screen, the user can select any part of the AMI (system) BIOS that needs to be changed, such as floppy drive configuration or system memory.

Options available to the operator are designated with dark text in the following graphics. The parameters included are default values.

AMIBIOS HIFLEX SETUP UTILITY - VERSION 1.05

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Standard CMOS Setup

Advanced CMOS Setup

Advance Chipset Setup

Power Management Setup

PCI/Plug and Play Setup

Peripheral Setup

Auto - Detect Hard Disks

Change User Password

Change Supervisor Password

Change Language Setting

Auto Configuration with Optimal Settings

Auto Configuration with Fail Safe Settings

Save Settings and Exit

Exit Without Saving

Standard CMOS setup for changing time, date, hard disk type etc.

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Standard CMOS Setup

Selection of the first main menu item, the Standard CMOS Setup, allows the user to adjust the date and time in addition to defining the parameters and disk drives associated with the system.

Note that the values included for Date, Time, Floppy Drive, and Pro Master are example values. The default values are 'Auto.'

AMIBIOS SETUP - STANDARD CMOS SETUP

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Date (mm/dd/yyyy): **Wed Jan 01 1997**

Time (hh/mm/ss): **00:00:01**

Floppy Drive A: **1.44 MB 3 ½**

Floppy Drive B: **Not Installed**

	Type	Size	Cyln	Head	WPcom	Sec	LBA Mode	Blk Mode	PIO Mode	32bit Mode
Pri Master :	**Auto**						**On**	**On**	**Auto**	**Off**
Pri Slave :	**Not Installed**						**Off**	**Off**	**Off**	**Off**
Sec Master :	**Auto**						**On**	**On**	**0**	**Off**
Sec Slave :	**Not Installed**						**Off**	**Off**	**Off**	**Off**

Boot Sector Virus Protection **Disabled**

Month : Jan - Dec

Day : 01 - 31

Year : 1901 - 2099

ESC :Exit ↑↓ :Sel

PgUp/PgDn :Modify

F2/F3 :Color

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Date/Time Configuration

The Time field displays the time in the 24-hour clock format. (For P.M., add 12 to the hour. Enter 4:30 P.M. as 16:30:00.)

Floppy Disk Drive Configuration

Floppy Drive A: Supports a 720 Kbyte 3.5-inch drive, a 1.44 Mbyte 3.5-inch drive, or a system without a floppy drive. The default setting is 1.44 Mbyte 3.5-inch.

Floppy Drive B: The system uses only one floppy drive, so the default setting is Not Installed.

Use the arrow keys to select the floppy drive type.

Master and Slave Disk Drive Configuration

The VMIVME-7589 has the capability of utilizing up to two hard disk drives on the primary IDE bus. The conditions presented in the menu illustrate an example of a 1.3 Gbyte hard drive. The default setting is Auto.

The secondary IDE bus master is the resident 8 Mbyte flash disk. The secondary IDE bus slave device is not assignable.

Boot Sector Virus Protection

Enabling this feature prohibits writes to the boot sector (Head 0, Track0, Sector 1). This feature only works for IDE devices and for I/O calls made through INT 13H. The default setting is Disabled.

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Advanced CMOS Setup

From the Main Menu, selecting the Advanced CMOS Setup option displays options to establish system preferences to customize the system operations.

AMIBIOS SETUP - ADVANCED CMOS SETUP

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First Boot Device	**Floppy**	**Available Options:**
Pause on Config. Screen (sec)	**Disabled**	Floppy
System Cache	**L1/L2 On**	1st IDE HD
Num Lock	**On**	2nd IDE HD
Setup Prompt	**Enabled**	3rd IDE HD
Hard Disk Pre-Delay	**Disabled**	4th IDE HD
		ATAPI CDROM
		SCSI Device
		Network
		ESC :Exit ↑↓ :Sel
		PgUp/PgDn :Modify
		F2/F3 :Color

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First Boot Device

The BIOS Setup Program boots the system from the device selected in the First Boot Device option. The default setting enables the BIOS to boot the system from floppy disk drive A:, if unsuccessful, it will boot from disk drive C:.

The Boot options include: Floppy, 1st IDE HD, 2nd IDE HD, 3rd IDE HD, 4IDE HD, ATAPI SCSI Device, and Network. The default condition is Floppy.

Pause on Configuration Screen (seconds)

Sets a pause time for the configuration Screen display which occurs just before booting an operating system. Options include: Disabled, 1, 2, 3, 4, 5 (seconds). The default condition is Disabled.

System Cache

Enable / Disable the system cache. When set to Disabled, system performance will decrease significantly. Options are: L1/L2 On, L1/L2 Off, and L1 On. The default is L1/L2 On.

Num Lock

This option sets the initial state of the Num Lock Keyboard when the system boots. Options are: On and Off. The default is On.

Setup Prompt

Enables / Disables the screen prompt to enter the Setup utility. Options are: Enable and Disable. The default is Enable.

Hard Disk Pre-delay

Adds a delay before the first access of a hard disk by the BIOS. Some hard disk drives hang if accessed before they have initialized. This delay ensures the hard drive has initialized after power prior to being accessed. Options include: Disabled, 3, 6, 9, 12, 15, 21, and 30 (seconds). The default is Disabled.

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Advanced Chipset Setup

From the Main Menu, select the Advanced Chipset Setup option to enable the modification of the core logic of the system to processor interface. This setup menu modifies the Triton II chipset memory and PCI control.

AMIBIOS SETUP - ADVANCED CHIPSET SETUP

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PCI Latency Timer (PCI Clocks)	**64**	**Available Options:**
PCI VGA Palette Snoop	**Disabled**	Guarantees a PCI device access to the PCI bus within the specified number of PCI clocks.
		ESC :Exit ↑↓ :Sel
		PgUp/PgDn :Modify
		F2/F3 :Color

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PCI Latency Timer

Guarantees a PCI device access to the PCI bus within the specified number of PCI clocks. Options are: 8, 16, 32, 64, 96, or 128 (PCI clocks). The default is 64.

PCI VAG Palette Snoop

Enable the video palette snoop allows the ISA add-in card to share a common palette with the on-board graphics controller. Options are: Disable and Enable. The Default is Disable.

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Power Management Setup

From the **Main Menu**, selection of the **Power Management Setup** option enables the modification of the power management settings for the PCI interface items.

Power management is not supported in the current BIOS.

AMIBIOS SETUP - POWER MANAGEMENT SETUP

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Power Management Support	**Disabled**	**Available Options:** Advanced Power Management enables the power saving features of the computer. **ESC** :Exit ↑↓ :Sel **PgUp/PgDn** :Modify **F2/F3** :Color

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PCI/Plug and Play Setup

From the **Main Menu**, select the **PCI/Plug-and-Play Setup** option to modify the basic PCI, Plug and Play, and ISA / EISA parameters.

Configuration Mode

Selects the Plug and Play Configuration Mode. Options are: PnP OS, Use Setup, and Use ICU. The Default is PnP OS.

AMIBIOS SETUP - PCI/PLUG-AND-PLAY SETUP

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Configuration Mode	**PnP OS**	**Available Options:**
		PnP OS - For Plug-and-Play (PnP) Operating Systems (OS) such as Windows 95. Use Setup - For nonPnP Operating Systems. Use ICU - If ICU utility is used with MS-DOS/Windows version 3.xx.
		ESC :Exit ↑↓ :Sel **PgUp/PgDn** :Modify **F2/F3** :Color

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Peripheral Setup

From the main menu, select the Peripheral Setup option to modify the Floppy disk controller, the serial ports, or the parallel port operational parameters.

AMIBIOS SETUP - PERIPHERAL SETUP

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Primary PCI IDE Interface	**Enabled**	**Available Options:**
Secondary PCI IDE Interface	**Enabled**	Disabled
PCI IDE BusMaster	**Disabled**	Enabled
Floppy interface	**Enabled**	
USB Legacy Keyboard Support	**Enabled**	
Serial Port 1 Address	**Auto**	
Serial Port 2 Address	**N/A**	
Serial Port 2 Mode	**Normal**	
On-board Serial Port 2 Fast IR	**N/A**	
Serial Port 2 IR DMA Channel	**N/A**	
Parallel Port Address	**Auto**	
Parallel Port Mode	**Normal**	
Parallel Port ECP DMA Channel	**N/A**	
Serial Port 1 Status	COM1 3F8 IRQ4	
Serial Port 2 Status	COM2 2FB IRQ3	
Serial Port 2 Fast IR	Disabled	**ESC** :Exit ↑↓ :Sel
Parallel Port Status	LPT1 378 IRQ7	**PgUp/PgDn** :Modify
Parallel Port ECP	Disabled	**F2/F3** :Color

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Primary PCI IDE Interface

This option enables the Primary IDE controller channels from the PIIX4. Options are Enable and Disabled. Default is Enabled.

Secondary PCI IDE Interface

This option enables the Secondary IDE controller channels from the PIIX4. On the VMIVME-7589, the on-board flash is controlled via this interface. Options are Enabled and Disabled. Default is Enabled.

PCI IDE BusMaster

This option allows the utilization of the IDE devices capable BUSMaster IDE or BUSMaster IDE DMA. Options are Enabled and Disabled. Default is Disabled.

Floppy interface

This option designates the floppy interface. Options are Enabled and Disabled. Default is Enabled.

USB Legacy Keyboard Support

This option enables a USB Keyboard to emulate a PS/2 Keyboard. Options are Enabled and Disabled. Default is Enabled.

Serial Port 1 Address

This option defines the configuration of the serial port. Options include: Enabled, Disabled, COM1 3F8 IRQ4, COM2 2F8 IRQ3, COM3 3E8 IRQ4, COM4 3E8 IRQ3, COM1 3F8 IRQ3, COM2 2F8 IRQ4, COM3 3E8 IRQ3, and COM4 3E8 IRQ4. Default is Auto.

Serial Port 2 Address

This option allows the configuration on the serial port. Options include: Enabled and Disabled, COM1 3F8 IRQ4, COM2 2F8 IRQ3, COM3 3E8 IRQ4, COM4 3E8 IRQ3, COM1 3F8 IRQ3, COM2 2F8 IRQ4, COM3 3E8 IRQ3, and COM4 3E8 IRQ4. Default is Auto.

Serial Port 2 Mode

This option supports an infrared serial port mode if available. The supported selection is Normal.

Onboard Serial Port 2 Fast IR

N/A

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Serial Port 2 IR DMA Channel

N / A

Parallel Port Address

This option allows the configuration OS the unit's parallel port. Options include: Auto, Disable, LPT1 378 IRQ7, LPT2 278 IRQ7, LPT3 3BC IRQ7, LPT1, 378 IRQ5, LPT2 278 IRQ5, and LPT3 3DC IRQ5. The default is Auto.

Parallel Port Mode

This option configures the operating mode of the on-board parallel port. Normal mode is the AT-Spec input / output-only mode. ECP mode is the Extended Capabilities Port mode (IEEE 1284). EPP is Enhanced Parallel Port mode (Rev. 1.7). Options are Normal, ECP, and EPP. The default is Normal.

Parallel Port ECP DMA Channel

This option configures in conjunction with the parallel port mode selection. If the mode is selected to be ECP, this setting is configured to be Auto. The default is N / A.

Auto-Detect Hard Disk

Selection of this menu item automatically detects the attached IDE hard drive and then presents to the user the first main menu item, the **Standard CMOS Setup**. Refer to *Standard CMOS Setup* on page 103 for a detailed description of the menu.

Change User Password

The option is not enabled in the current BIOS.

Change Supervisor Password

The option is not enabled in the current BIOS.

Change Language Settings

The option is not enabled in the current BIOS.

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Auto Configuration with Optimal Settings

The **Optimal Settings** option loads the best-case BIOS values that optimize system performance. The system is delivered using the **Optimal Settings** BIOS values. Selecting this option causes the following message to display. Select **Y** to load the optimal values.

Auto Configuration with Fail-Safe Settings

The **Fail-Safe** BIOS Defaults option loads settings that are most likely to configure a workable computer when something is wrong. If you cannot boot the computer successfully, select the **Fail-Safe** BIOS options and try to diagnose the problem after the computer boots. These settings do not provide optimal performance. If CMOS RAM becomes corrupt, the **Fail-Safe** BIOS defaults load automatically. Selecting this option causes the following message to display. Select **Y** to load the failsafe values.

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Save Settings and Exit

Selection of this menu option enables the user to exit the Setup Utility after saving the all previous made BIOS setting. A selection of **N** will send the user back to the main menu.

Exit Without Saving

Selection of this menu option enables the user to exit the Setup Utility without saving the changes made to the BIOS settings. A selection of **N** will send the user back to the main menu. A selection of **Y** will cause the system to boot with the original BIOS settings.

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Appendix

D

Device Configuration: I/O and Interrupt Control

Contents

Introduction

This appendix provides the user with the information needed to develop custom applications for the VMIVME-7589. The CPU board on the VMIVME-7589 is unique in that the BIOS can not be removed; it must be used in the initial boot cycle. A custom application, like a revised operating system for example, can only begin to operate after the BIOS has finished initializing the CPU. The VMIVME-7589 will allow the user to either maintain the current BIOS configuration or alter this configuration to be more user specific, but this alteration can only be accomplished after the initial BIOS boot cycle has completed.

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BIOS Operations

When the VMIVME-7589 is powered on, control immediately jumps to the BIOS. The BIOS initiates a Power-on Self-Test (POST) program which instructs the microprocessor to initialize system memory as well as the rest of the system. The BIOS establishes the configuration of all on-board devices by initializing their respective I/O and Memory addresses and interrupt request lines. The BIOS then builds an interrupt vector table in main memory, which is used for interrupt handling. The default interrupt vector table and the default address map is described in Chapter 3 of this manual. Finally, the BIOS jumps to the hard drive or floppy drive to execute the operating system's boot program. This is the point at which a custom operating system could take over control of the board and proceed with a custom configuration and/or custom application. A user application could override the configuration set by the BIOS and reconfigure the system or it could accept what the BIOS initialized.

BIOS Control Overview

There are two areas on the VMIVME-7589 in which the user must be familiar in order to override the initial BIOS configuration. These include the device addresses and the device interrupts. This appendix reviews the details of these addresses and interrupts, and provides a reference list for the individual devices used on the board.

The VMIVME-7589 utilizes the high-performance Peripheral Component Interconnect (PCI) bus along with the Industrial Standard Architecture (ISA) bus. In general, the PCI bus is plug-and-play compatible. The components that are connected to the PCI bus are not always placed at a standard I/O or Memory address, nor are they connected to a standard interrupt request line as is the case with ISA bus devices. These PCI bus devices are re-established by the BIOS meaning that these devices will not always be located at the same address or connected to the same interrupt request line every time the CPU is booted. This appendix lists the defaults that are found by powering up a specific VMIVME-7589.

Functional Overview

The block diagram included in Figure D-1 on page 119 illustrates the VMIVME-7589 emphasizing the I/O features, including the optional PCI-to-VMEbus bridge.

The circled number in the upper left corner of a function block references the appropriate data book necessary for the programming of the function block.

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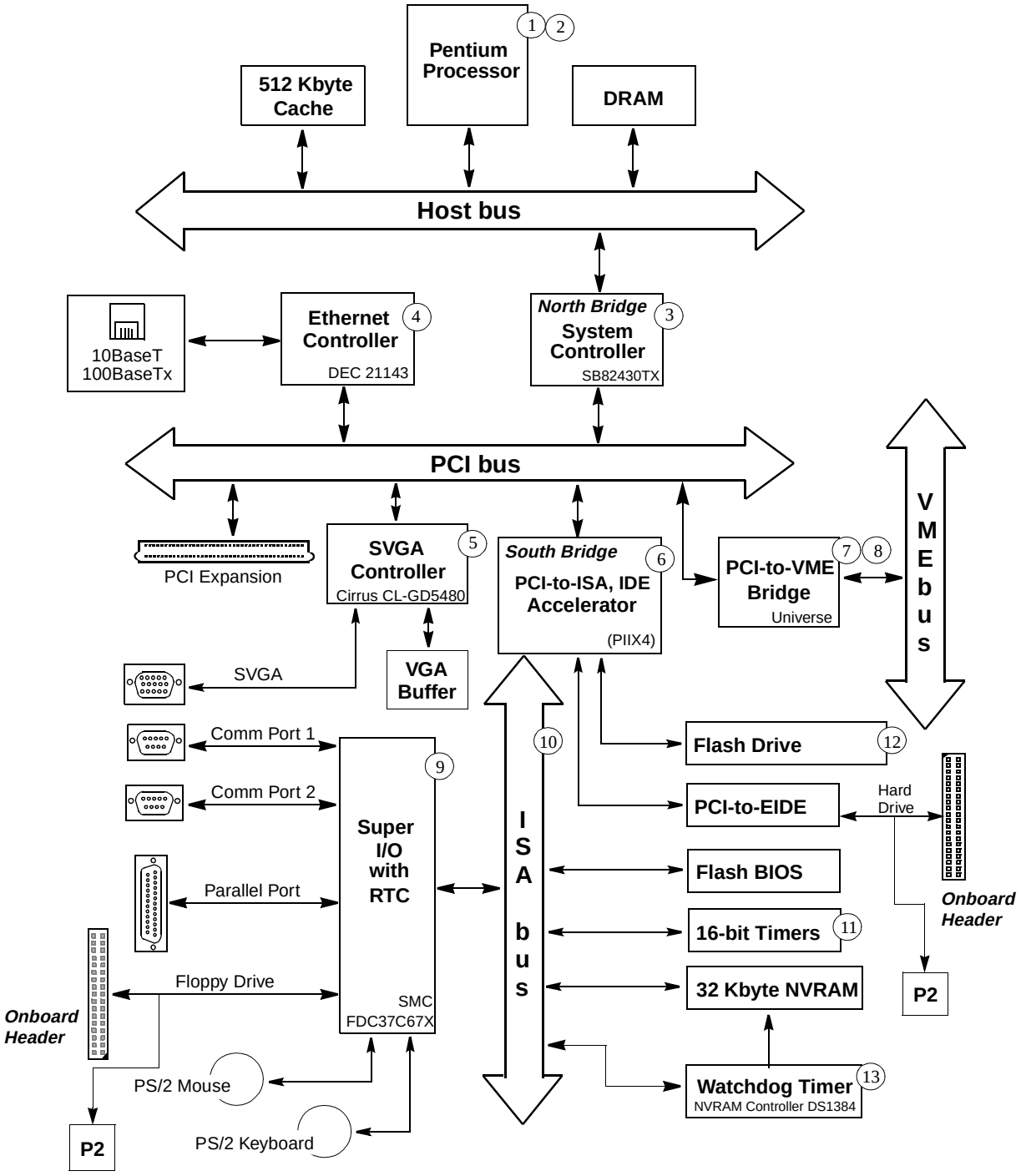

Figure D-1 VMIVME-7589 Block Diagram

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Data Book References

1. Pentium® Processor with MMX™ Technology

   January 1997, Order Number 243185-001
   Intel Corporation
   2200 Mission College Blvd.
   P.O. Box 58119
   Santa Clara, CA 95052-8119
   (408) 765-8080

2. Pentium® Processor at 150 MHz, 166 MHz, and 200 MHz

   February 1996, Order Number 242769-003
   Intel Corporation
   2200 Mission College Blvd.
   P.O. Box 58119
   Santa Clara, CA 95052-8119
   (408) 765-8080

3. Intel 82430FX PCIset System Controller (MTKE)

   Intel Corporation
   2200 Mission College Boulevard
   P.O. Box 58119
   Santa Clara, CA 95052-8119

4. Digital Semiconductor 21143 10/100 Mb/s Ethernet LAN Controller

   Digital Equipment Corporation
   Maynard, Mass.
   1-800-332-2717
   www.digital.com

5. Cirrus Logic - CL-GD5480

   Technical Reference Manual
   Cirrus Logic
   3100 West Warren Avenue
   Fremont, CA 94538
   (510) 623-8300

6. Intel 82430TX PCIset ISA Bridge

   82371AB PCI ISA IDE Xcellerator (PIIX4)
   2200 Mission College Boulevard
   P.O. Box 58119
   Santa Clara, CA 95052-8119

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7. VMIVME-7589 User Manual

   500-007589-000 Product Manual
   500-007589-001 VMIVME-7589, Tundra Universe™-Based VMEbus Interface Option Product Manual

8. PCI Local Bus Specification, Rev. 2.1

   PCI Special Interest Group
   P.O. Box 14070
   Portland, OR 97214
   (800) 433-5177 (U.S.)
   (503) 797-4207 (International)
   (503) 234-6762 (FAX)

9. SMC FDC37C67X Enhanced Super I/O Controller

   SMC Component Products Division
   300 Kennedy Drive
   Hauppauge, NY 11788
   (516) 435-6000
   (516) 231-6004 (FAX)

10. ISA & EISA, Theory and Operation

    Solari, Edward
    Annabooks
    15010 Avenue of Science, Suite 101
    San Diego, CA 92128 USA
    ISBN 0-929392 -15-9

11. 82C54 CHMOS Programmable Internal Timer

    Intel Corporation
    2200 Mission College Boulevard
    P.O. Box 58119
    Santa Clara, CA 95052-8119

12. Flash ChipSet Product Manual

    SanDisk Corporation
    140 Caspian Court
    Sunnyvale, CA 94089-9820

13. DS 1384 Watchdog Timekeeping Controller

    Dallas Semiconductor
    4461 South Beltwood Pwky.
    Dallas, TX 75244-3292

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Device Address Definition

The standard PC / AT architecture defines two distinctive types of address spaces for the devices and peripherals on the CPU board. These spaces have typically been named Memory address space and I / O address space. The boundaries for these areas are limited to the number of address bus lines that are physically located on the CPU board. The VMIVME-7589 has 32 address bus lines located on the board, thereby defining the limit of the address space as 4 Gbyte. The standard PC / AT architecture defines Memory address space from zero to 4 Gbyte and the separate I / O address space from zero to 64 Kbyte.

ISA Devices

The ISA devices on the VMIVME-7589 are configured by the BIOS at boot-up and fall under the realm of the standard PC / AT architecture. They are mapped in I / O address space within standard addresses and their interrupts are mapped to standard interrupt control registers. However, all of the ISA devices with the exception of the real-time clock, keyboard, and programmable timer are relocatable to almost anywhere within the standard 1 Kbyte of I / O address space. Table D-3 defines the spectrum of addresses available for reconfiguration of ISA devices.

As previously stated, in the standard PC / AT system, all I / O devices are mapped in I / O address space; however, one exception exists. The Dynamic Random Access Memory (DRAM), Battery-Backed SRAM, and Watchdog Timer are addressed in Memory address space. The BIOS places DRAM at address zero and extends to the physical limit of the on-board DRAM.

Table D-1 ISA Device Mapping Configuration

Device	Memory Space	I/O Address Space	PIC Interrupt Options	Byte Address Boundary	Default
Floppy	N / A	[0x100 - 0xFF8]	IRQ1 - IRQ15	8	$3F0
Parallel Port	N / A	[0x100 - 0xFFC] [0x100 - 0xFF8]	IRQ1 - IRQ15	4 8	$378
Serial Port 1	N / A	[0x100 - 0xFF8]	IRQ1 - IRQ15	8	$3F8
Serial Port 2	N / A	[0x100 - 0xFF8]	IRQ1 - IRQ15	8	$2F8
Real-Time Clock	Nonrelocatable				$070
Keyboard	Nonrelocatable				$060

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Table D-1 ISA Device Mapping Configuration (Continued)

Device	Memory Space	I/O Address Space	PIC Interrupt Options	Byte Address Boundary	Default
Auxiliary I/O	N/A	- Primary I/O [0x000 - 0xFFF] - Secondary I/O [0x000 - 0xFFF]	IRQ1, IRQ3-IRQ15	1 1	
Programmable Timer		Nonrelocatable 0X500	IRQ5	4	0X500
Watchdog Timer	Nonrelocatable 0XD8000	N/A	N/A	0XD	0XD8000
Battery-Backed SRAM	Nonrelocatable 0XD800E	N/A	N/A	(32K-0XD)	0XD800E

PCI Devices

PCI devices are fully configured under I/O and/or Memory address space. Table D-3 describes the PCI bus devices that are on-board the VMIVME-7589 along with each device's configuration spectrum.

The PCI bus includes three physical address spaces. As with ISA bus, PCI bus supports Memory and I/O address space, but PCI bus includes an additional Configuration address space. This address space is defined to support PCI bus hardware configuration (refer to the PCI bus Specification for complete details on the configuration address space). PCI bus targets are required to implement Base Address registers in configuration address space to access internal registers or functions. The BIOS uses the Base Address register to determine how much space a device requires in a given address space and then assigns where in that space the device will reside. This functionality enables PCI devices to be located in either Memory or I/O address space.

Table D-2 PCI Device Mapping Configuration

Device	Memory Space	I/O Address Space	PIC Interrupt Options
SVGA	Anywhere	N/A	N/A
Universe** PCI-to-VMEbus Bridge	Anywhere	N/A	PCI Defined
Ethernet	Anywhere	Anywhere	PCI Defined
Timer Interrupt Registers	N/A	Fixed	N/A

** Refer to the VMIVME-7589-001 User's Manual.

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Device Interrupt Definition

PC/AT Interrupt Definition

The interrupt hardware implementation on the VMIVME-7589 is standard for computers built around the PC / AT architecture. The PC / AT evolved from the IBM PC / XT architecture. In the IBM PC / XT systems, only eight Interrupt Request (IRQ) lines exist, numbered from IRQ0 to IRQ7. These interrupt lines were included originally on a 8259A Priority Interrupt Controller (PIC) chip.

The IBM PC / AT computer added eight more IRQx lines, numbered IRQ8 to IRQ15, by cascading a second slave 8259A PIC into the original master 8259A PIC. The interrupt line IRQ2 at the master PIC was committed as the cascade input from the slave PIC. This master / slave architecture, the standard PC / AT interrupt mapping, is illustrated in Figure D-2 on page 125 within the PCI-to-ISA Bridge PIIX4 82371AB section of the diagram.

To maintain backward compatibility with PC / XT systems, IBM chose to use the new IRQ9 input on the slave PIC to operate as the old IRQ2 interrupt line on the PC / XT Expansion Bus. Thus, in AT systems, the IRQ9 interrupt line connects to the old IRQ2 pin on the AT Expansion Bus (or ISA bus).

The BIOS defines the PC / AT interrupt line to be used by each device. The BIOS writes to each of the two cascaded 8259A PIC chips an 8-bit vector which maps each IRQx to its corresponding interrupt vector in memory.

ISA Device Interrupt Map

The VMIVME-7589 BIOS maps the IRQx lines to the appropriate device per the standard ISA architecture. Reference Figure D-2 on page 125. This initialization operation cannot be changed; however, a custom application could reroute the interrupt configuration after the BIOS has completed the initial configuration cycle.

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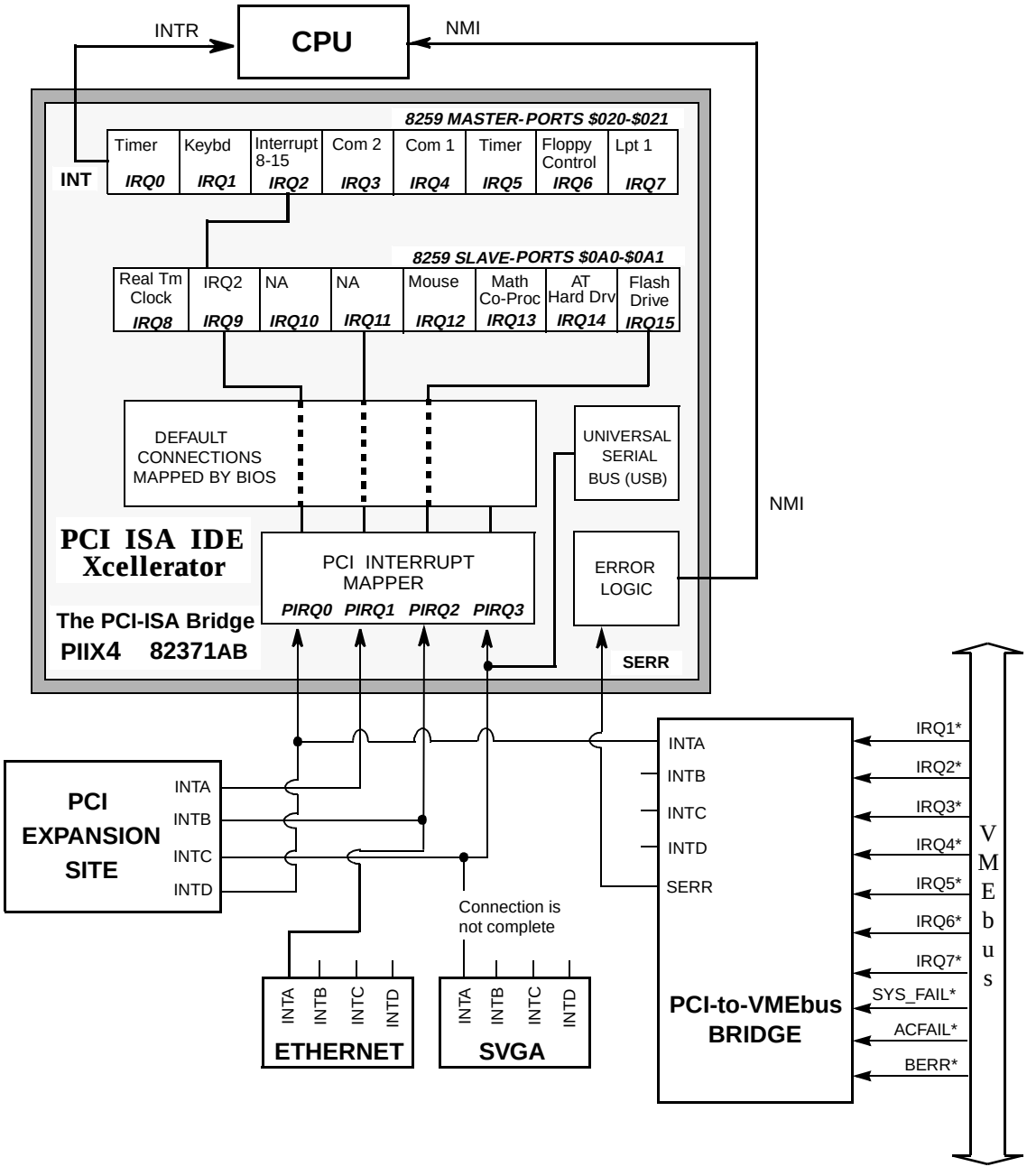

Figure D-2 BIOS Default Connections for the PC Interrupt Logic Controller

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PCI Device Interrupt Map

The PCI bus-based external devices include the PCI expansion site, the PCI-to-VMEbus bridge, and the VGA reserved connection. The default BIOS maps these external devices to the PCI Interrupt Request (PIRQx) lines of the PIIX4. This mapping is illustrated in Figure D-2 on page 125 and is defined in Table D-3.

The device PCI interrupt lines (INTA through INTD) that are present on each device *cannot* be modified.

Table D-3 Device PCI Interrupt Mapping by the BIOS

DEVICE	COMPONENT	VENDOR ID	DEVICE ID	CPU ADDRESS MAP ID SELECT	DEVICE PCI INTERRUPT	MOTHER-BOARD PCI INTERRUPT MAPPER	DATA BOOK REF. #	REVISION ID
PCI-to-VME Bridge Option: Tundra Universe™	Universe CA91C042	0x10E3	0x0	AD19	INTA	PIRQ0	7	N / A
PCI Bus Master I/O Controller	PLX PCI9060ES	0x114A	0x0001	AD20	N / A	N / A	7	N / A
PCI Expansion Site	N / A	Board Specific	Board Specific	N / A	INTA	PIRQ1	N / A	N / A
	N / A	Board Specific	Board Specific	N / A	INTB	PIRQ2	N / A	N / A
	N / A	Board Specific	Board Specific	N / A	INTC	PIRQ3	N / A	N / A
	N / A	Board Specific	Board Specific	N / A	INTD	PIRQ0	N / A	N / A
Timer INT Registers	PIIX4 82371AB Function	0x8086	0x7113	AD18	N / A	N / A	2	N / A
PCI-to-ISA Bridge	PIIX4 82371AB Function 00	0x8086	0x7000	AD18	N / A	N / A	2	N / A
SVGA Controller	Cirrus CL-GD5480	0x1013		AD25	INTA**	PIRQ3**	4	N / A
Ethernet Controller	DEC 21143	0x1011	0x0019	AD22	INTA	PIRQ2	6	N / A
PCI IDE Controller	PIIX4 82371AB Function 01	0x8086	0x7111	AD18	N / A	N / A	2	N / A
Universal Serial Bus (USB)***	PIIX4 82371AB Function 02	0x8086	0x7020	AD18	INTD	PIRQ3	2	N / A
PCI Host Bridge	Intel 430 TX	0x8086	0x7100	N / A	N / A	N / A	1	N / A

* To access these parts, use the revision number as the distinguishing factor.
** Not connected, for reference only
*** PIRQ4 interrupt is not enabled by the BIOS.

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The motherboard accepts these PCI device interrupts through the PCI interrupt mapper function. The BIOS default maps the PCI Interrupt Request (PIRQx) external device lines to one of the available slave PIC Interrupt Request lines, IRQ (9, 10, 11, or 15). The BIOS default mapping of the PIRQx to the slave PIC is defined in Table D-4.

Table D-4 Default PIRQx to IRQx BIOS Mapping

PCI INTx	PIC IRQx
PIRQ0	IRQ9
PIRQ1	IRQ11
PIRQ2	IRQ15

Using the interrupt steering registers of the 82371FB PIIX3, the user can override the BIOS defaults and map any of the PCI interrupts (PIRQ0-3) to0 any of the following PIC IRQx (ISA) interrupts: IRQ15, 14, 12-9, or 7-3.

If PCI interrupts are remapped by the user, care must be taken to ensure that all ISA and PCI functions that require an interrupt are included.

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Appendix

E

Sample C Software

Contents

Introduction

This appendix provides listings of a library of sample code that the programmer may utilize to build applications. These files are provided to the VMIVME-7589 user on disk 320-500013-010, Sample Application C Code for the VMIVME-7589, included in the distribution disk set.

Because of the wide variety of environments in which the VMIVME-7589 operates, the samples provided in this appendix are not necessarily intended to be verbatim boilerplates. Rather, they are intended to give the end user an example of the standard structure of the operating code.

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Directory PCVME

This directory contains listings of the source code used to generate an application that sets up the PC to VME interface in three segments using A16 addressing, A24 addressing, or A32 addressing.

** FILE: FLAT.C

```
**
*/

#include <stdio.h>
#include <dos.h>

#include "flat.h"

/*
** Keyboard controller defines
*/

#define RAMPORT    0x70
#define KB_PORT    0x64
#define PCNMIPORT  0xA0

#define INBA20     0x60
#define INBA20ON   0xDF
#define INBA20OFF  0xDD

/*
** macro to clear keyboard port
*/

#define kx() { while( inp( KB_PORT ) & 2 ); }

/*
** define GDT pointer structure
*/

static struct fword gdtptr;        /* fword ptr to gdt */

/*
** A20: Enable A20 line
**
** flag: enable  = 1
**       disable = 0
*/
```


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```
void a20( int flag )
{
  kx();
  outp( KB_PORT, 0xD1 );
  kx();
  outp( INBA20, flag ? INBA20ON : INBA20OFF );
  kx();
  outp( KB_PORT, 0xFF );
  kx();
}

/*
**  convert a linear address to a far pointer
*/

void far * linear_to_seg( FPTR lin )
{
   void far *p;
   FP_SEG(p) = (unsigned int)( lin >> 4 );
   FP_OFF(p) = (unsigned int)( lin & 0xF );
   return p;
}

/*
**  Adjust the GS register's limit to 4GB
**
**  Note: interrupts are enabled by this call.
*/

void extend_seg( void )
{
  /*
  **  compute linear address and limit of GDT
  */
  gdtptr.linear_add = seg_to_linear(( void far * ) GDT );
  gdtptr.limit = 15;
  /*
  **  disable regular interrupts
  */
  disable();
  /*
  **  disable NMI
  */
  outp( RAMPORT, inp( RAMPORT ) | 0x80 );
  /*
  **  call protected mode code
  */
  protinit( &gdtptr );
```


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```
 /*
 ** Turn interrupts back on
 */
 enable();
 /*
 ** Turn NMI back on
 */
 outp( RAMPORT, inp( RAMPORT ) & 0x7F );
}

void protinit( struct fword * address )
{
 asm {
  .386P
  push ds
  lds  bx,address
  lgdt FWORD ptr [bx]
  pop  ds
  mov  eax,cr0
  or   al,0x01
  mov  cr0,eax
  jmp  short nxt
 }
 nxt:
 asm {
  .386P
  mov  bx,8
  mov  gs,bx
  mov  es,bx
  and  al,0xfe
  mov  cr0,eax
 }
}

int fr_byte( FPTR adr )
{
 int d;
 asm {
  .386P
  xor  ax,ax      /* zero gs */
  mov  gs,ax
  mov  eax, adr
  mov  al,byte ptr gs:[eax]
  mov  d,ax
 }
 return d;
}
```


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```
int fr_word( FPTR adr )
{
 int d;
 asm {
  .386P
  xor  ax,ax      /* zero gs */
  mov  gs,ax
  mov  eax, adr
  mov  ax,word ptr gs:[eax]
  mov  d,ax
 }
 return d;
}

long fr_long( FPTR adr )
{
 long  d;
 asm {
  .386P
  xor  ax,ax      /* zero gs */
  mov  gs,ax
  mov  eax,adr
  mov  eax,dword ptr gs:[eax]
  mov  d,eax
 }
 return d;
}

void fw_byte( FPTR a, int d )
{
 asm {
  .386P
  xor  ax,ax      /* zero gs */
  mov  gs,ax
  mov  eax,a
  mov  bx,d
  mov  byte ptr gs:[eax],bl
 }
}

void fw_word( FPTR a, int d )
{
 asm {
  .386P
  xor  ax,ax      /* zero gs */
  mov  gs,ax
  mov  eax,a
  mov  bx,d
```


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```
    mov   word ptr gs:[eax],bx
  }
}

void fw_long( FPTR a, long d )
{
  asm {
    .386P
    xor   ax,ax      /* zero gs */
    mov   gs,ax
    mov   eax,a
    mov   ebx,d
    mov   dword ptr gs:[eax],ebx
  }
}

  /*
```


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** FILE: PCI.C

```
**
*/

#include <dos.h>
#include <stddef.h>
#include "pci.h"

#define HIGH_BYTE(ax) (ax >> 8)
#define LOW_BYTE(ax) (ax & 0xff)


int find_pci_device(unsigned short device_id,
        unsigned short vendor_id,
        unsigned short index,
        unsigned char *bus_number,
        unsigned char *device_and_function)
{
  int ret_status;
  unsigned short ax, bx, flags;

  _CX = device_id;
  _DX = vendor_id;
  _SI = index;
  _AH = PCI_FUNCTION_ID;
  _AL = FIND_PCI_DEVICE;

  geninterrupt(0x1a);

  ax = _AX;
  bx = _BX;
  flags = _FLAGS;

  if ((flags & CARRY_FLAG) == 0)
  {
   ret_status = HIGH_BYTE(ax);
   if (ret_status == SUCCESSFUL)
   {
     if (bus_number != NULL) *bus_number = HIGH_BYTE(bx);
     if (device_and_function != NULL) *device_and_function = LOW_BYTE(bx);
   }
  }
  else
  {
   ret_status = NOT_SUCCESSFUL;
  }
  return(ret_status);
```


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```
}


int read_configuration_area(unsigned char function,
                    unsigned char bus_number,
                    unsigned char device_and_function,
                    unsigned char register_number,
                    unsigned long *data)
{
  int ret_status;
  unsigned short ax, flags;
  unsigned long ecx;

  _BH = bus_number;
  _BL = device_and_function;
  _DI = register_number;
  _AH = PCI_FUNCTION_ID;
  _AL = function;

  geninterrupt(0x1a);

  ecx = _ECX;
  ax = _AX;
  flags = _FLAGS;

  if ((flags & CARRY_FLAG) == 0)
  {
   ret_status = HIGH_BYTE(ax);
   if (ret_status == SUCCESSFUL)
   {
    *data = ecx;
   }
  }
  else
  {
   ret_status = NOT_SUCCESSFUL;
  }
  return(ret_status);
}


int write_configuration_area(unsigned char function,
                unsigned char bus_number,
                unsigned char device_and_function,
                unsigned char register_number,
                unsigned long value)
{
  int ret_status;
```


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```
  unsigned short ax, flags;

  _BH = bus_number;
  _BL = device_and_function;
  _ECX = value;
  _DI = register_number;
  _AH = PCI_FUNCTION_ID;
  _AL = function;

  geninterrupt(0x1a);

  ax = _AX;
  flags = _FLAGS;

  if ((flags & CARRY_FLAG) == 0)
  {
   ret_status = HIGH_BYTE(ax);
  }
  else
  {
   ret_status = NOT_SUCCESSFUL;
  }
  return(ret_status);
}

/*
```


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** FILE: PCVME.C

```
**
*/

#include <stdlib.h>
#include <stdio.h>
#include <string.h>
#include <conio.h>
#include <ctype.h>
#include <dos.h>

#include "flat.h"
#include "pci.h"
#include "sysregs.h"
#include "pc.h"


#define  PCI_BASE16 0x10000000   /* PCI BASE for A16 */
#define  PCI_BASE24 0x10020000   /* PCI BASE for A24 */
#define  PCI_BASE32 0x20000000   /* PCI BASE for A32 */

/* function prototypes */
void far interrupt (* old_break)( void );
void far interrupt on_break( void );

/* global variables */
unsigned long vme_offset;
unsigned char bus, dev_func;
FPTR un_regs;
FPTR plx_regs;

void main( void )
{
 unsigned char pci_devices;
 int test_int;
 unsigned long temp_dword;

 old_break = getvect( 0x23 );
 setvect( 0x23, on_break );
 extend_seg();
 a20( 1 );


 pci_devices = 0;
 /* locate the UNIVERSE device on the PCI bus */
 test_int = find_pci_device(UNIVERSE_DID, UNIVERSE_VID, 0,
          &bus, &dev_func);
```


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```
 if(test_int == SUCCESSFUL)
 {
  pci_devices |= PCI_UNIVERSE;
  test_int = read_configuration_area( READ_CONFIG_DWORD, bus, dev_func,
                              0x10, &temp_dword );

  if(test_int == SUCCESSFUL)
  {
   un_regs = (FPTR) temp_dword;
  }
 }

 /* locate the PLX device on the PCI bus */
 test_int = find_pci_device(PLX_DID, PLX_VID, 0,
           &bus, &dev_func);
 if(test_int == SUCCESSFUL)
 {
  pci_devices |= PCI_PLX;
  test_int = read_configuration_area( READ_CONFIG_DWORD, bus, dev_func,
                              0x18, &temp_dword );

  if(test_int == SUCCESSFUL)
  {
   plx_regs = (FPTR) temp_dword;
  }
 }

 if( !(pci_devices & PCI_UNIVERSE) ) {
  printf("Unable to locate PCI device Tundra Universe\n");
 }

 if( !(pci_devices & PCI_PLX) ) {
  printf("Unable to locate PCI device PLX\n");
 }

 if( pci_devices != (PCI_UNIVERSE | PCI_PLX) ) exit( 1 );

 /* setup VME windows to VME base address 0000 Non-Privileged */
 fw_long( un_regs + 0x104, PCI_BASE16 ); /* pci base for A16 */
 fw_long( un_regs + 0x108, (PCI_BASE16 + 0x10000) ); /* 64K window */
 fw_long( un_regs + 0x10C, (0x00000000 - PCI_BASE16) ); /* vme translation */
 fw_long( un_regs + 0x100, (LSI_CTL_EN | LSI_CTL_VDW_32 | LSI_CTL_VAS_16)
);

 fw_long( un_regs + 0x118, PCI_BASE24 ); /* pci base for A24 */
 fw_long( un_regs + 0x11C, (PCI_BASE24 + 0x1000000) ); /* 16 Meg window */
 fw_long( un_regs + 0x120, (0x00000000 - PCI_BASE24) ); /* vme translation */
 fw_long( un_regs + 0x114, (LSI_CTL_EN | LSI_CTL_VDW_32 | LSI_CTL_VAS_24) );
```


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```
  fw_long( un_regs + 0x12C, PCI_BASE32 ); /* pci base for A32 */
  fw_long( un_regs + 0x130, (PCI_BASE32 + 0x1000000) ); /* 16 Meg window */
  fw_long( un_regs + 0x134, (0x00000000 - PCI_BASE32) ); /* vme translation */
  fw_long( un_regs + 0x128, (LSI_CTL_EN | LSI_CTL_VDW_32 | LSI_CTL_VAS_32)
);

  /* enable VME and Master Endian Conversion */
  fw_word( plx_regs, (VME_EN | MEC) );

  /* use the flat write / flat read functions to access VME */
  /* EX: ch_data = (unsigned char)(fr_byte( PCI_BASE16 + vme_offset )); */
  /* EX: fw_byte( PCI_BASE16 + vme_offset, ch_dat ); */

} /* end main */


void interrupt on_break( void )
{
  /* do nothing */
}


/*
```


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** FILE: FLAT.H

```
**
** Prototypes typedefs and macros for flat memory access
**
*/

typedef unsigned long FPTR;

/*
** Global descriptor table
*/

struct _GDT {
  unsigned int limit;
  unsigned int base;
  unsigned int access;
  unsigned int hi_limit;
};


static struct _GDT GDT[2]= {
  {0,0,0,0},                  /* Null selector slot */
  {0xFFFF,0,0x9200,0x8F}          /* 4 Gig data segment */
};

/*
** FWORD pointer to GDT
*/

struct fword {
  unsigned int limit;
  unsigned long linear_add;
};

/*
** convert segmented address to linear address
*/

#define seg_to_linear(fp) (((FPTR) FP_SEG(fp)<<4)+FP_OFF(fp))

/*
** flat memory function prototypes
*/

void a20( int );
void far * linear_to_seg( FPTR );
void extend_seg( void );
```


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```
void protinit( struct fword * );

int  fr_byte( FPTR );
void fw_byte( FPTR, int );

int  fr_word( FPTR );
void fw_word( FPTR, int );

long fr_long( FPTR );
void fw_long( FPTR, long );

/*
```


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** FILE: PC.H

```
**
*/

#define UNIVERSE_VID    0x10E3
#define UNIVERSE_DID    0x0000
#define PLX_VID         0x114A
#define PLX_DID         0x0001

#define PCI_UNIVERSE    0x01
#define PCI_PLX         0x02

/* lsi[X]_ctl - slave image control registers ( lsi0 - lsi7 ) */
#define    LSI_CTL_EN     0x80000000  /* R/W image enable                */
#define    LSI_CTL_PWEN   0x40000000  /* R/W posted write enable         */
#define    LSI_CTL_VDW_08 0x00000000  /* R/W VMEbus maximum data width
D08  */
#define    LSI_CTL_VDW_16 0x00400000  /* R/W VMEbus maximum data width
D16  */
#define    LSI_CTL_VDW_32 0x00800000  /* R/W VMEbus maximum data width
D32  */
#define    LSI_CTL_VDW_64 0x00C00000  /* R/W VMEbus maximum data width
D64  */
#define    LSI_CTL_VAS_16 0x00000000  /* R/W VMEbus address space A16      */
#define    LSI_CTL_VAS_24 0x00010000  /* R/W VMEbus address space A24      */
#define    LSI_CTL_VAS_32 0x00020000  /* R/W VMEbus address space A32      */
#define    LSI_CTL_VAS_R1 0x00030000  /* R/W VMEbus address space RSVD1    */
#define    LSI_CTL_VAS_R2 0x00040000  /* R/W VMEbus address space RSVD2    */
#define    LSI_CTL_VAS_CR 0x00050000  /* R/W VMEbus address space CR/CSR
*/
#define    LSI_CTL_VAS_U1 0x00060000  /* R/W VMEbus address space USER1    */
#define    LSI_CTL_VAS_U2 0x00070000  /* R/W VMEbus address space USER2    */
#define    LSI_CTL_PGM_D  0x00000000  /* R/W VMEbus data AM code           */
#define    LSI_CTL_PGM_P  0x00004000  /* R/W VMEbus program AM code        */
#define    LSI_CTL_SUPER  0x00001000  /* R/W VMEbus supervisory AM code    */
#define    LSI_CTL_VCT_S  0x00000000  /* R/W VMEbus single cycles only     */
#define    LSI_CTL_VCT_SB 0x00000100  /* R/W VMEbus single cycles and block */
#define    LSI_CTL_LAS_M  0x00000000  /* R/W PCIbus memory space           */
#define    LSI_CTL_LAS_IO 0x00000001  /* R/W PCIbus I/O space              */
#define    LSI_CTL_LAS_C  0x00000002  /* R/W PCIbus type 1 config space    */
#define    LSI_CTL_LAS_R  0x00000003  /* R/W PCIbus reserved               */


/*
```


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** FILE: PCI.H

```
**
*/

#define TRUE    1
#define FALSE0

#define CARRY_FLAG 0x01

/* PCI Functions */
#define PCI_FUNCTION_ID       0xB1
#define PCI_BIOS_PRESENT0x01
#define FIND_PCI_DEVICE0x02
#define FIND_PCI_CLASS_CODE0x03
#define READ_CONFIG_BYTE0x08
#define READ_CONFIG_WORD0x09
#define READ_CONFIG_DWORD     0x0A
#define WRITE_CONFIG_BYTE     0x0B
#define WRITE_CONFIG_WORD     0x0C
#define WRITE_CONFIG_DWORD    0x0D

/* PCI Return codes */

#define SUCCESSFUL0x00
#define NOT_SUCCESSFUL0x01

/* Prototypes */

int find_pci_device(unsigned short device_id,
            unsigned short vendor_id,
            unsigned short index,
            unsigned char *bus_number,
            unsigned char *device_and_function);

int read_configuration_area(unsigned char function,
                  unsigned char bus_number,
                  unsigned char device_and_function,
                  unsigned char register_number,
                  unsigned long *data);

int write_configuration_area(unsigned char function,
                   unsigned char bus_number,
                   unsigned char device_and_function,
                   unsigned char register_number,
                   unsigned long value);

/*
```


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** FILE: SYSREGS.H

```
**
*/

/* Command register */
#define   MEC     0x0001     /* Master endian conversion      */
#define   SEC     0x0002     /* Slave endian conversion       */
#define   ABLE    0x0004     /* Auxillary BERR logic enable   */
#define   BTO     0x0008     /* Auxillary BTO enable          */
#define   BTOV0   0x0010     /* Auxillary BTO value lsb       */
#define   BTOV1   0x0020     /* Auxillary BTO value msb       */
#define   BERRIM  0x0040     /* Auxillary BERR interrupt map  */
#define   MB_MSK0 0x0080     /* Mail-box 0 interrupt mask     */
#define   MB_MSK1 0x0100     /* Mail-box 1 interrupt mask     */
#define   MB_MSK2 0x0200     /* Mail-box 2 interrupt mask     */
#define   MB_MSK3 0x0400     /* Mail-box 3 interrupt mask     */
#define   VME_EN  0x0800     /* VMEbus interface enable       */

/* BERR status register */
#define   BERR_S  0x01       /* BERR status                   */

/* BERR mask register */
#define   BERR_M  0x01       /* BERR mask                     */

/* Mail Box 0 register */
#define   MB0_INT 0x01       /* MB0 interrupt bit             */
```


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Directory Timers

This directory contains sample code useful in the creation of applications involving the VMIVME-7589's three software controlled 16-bit timers. The code is written for the control of a single timer, but can be utilized in generating code for any timer configuration. The timers are described in Chapter 4 of the manual.

** FILE: PCI.C

```
**
*/

#include <dos.h>
#include <stddef.h>
#include "pci.h"

#define HIGH_BYTE(ax) (ax >> 8)
#define LOW_BYTE(ax) (ax & 0xff)


int find_pci_device(unsigned short device_id,
        unsigned short vendor_id,
        unsigned short index,
        unsigned char *bus_number,
        unsigned char *device_and_function)
{
  int ret_status;
  unsigned short ax, bx, flags;

  _CX = device_id;
  _DX = vendor_id;
  _SI = index;
  _AH = PCI_FUNCTION_ID;
  _AL = FIND_PCI_DEVICE;

  geninterrupt(0x1a);

  ax = _AX;
  bx = _BX;
  flags = _FLAGS;

  if ((flags & CARRY_FLAG) == 0)
  {
    ret_status = HIGH_BYTE(ax);
    if (ret_status == SUCCESSFUL)
    {
      if (bus_number != NULL) *bus_number = HIGH_BYTE(bx);
```


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```
    if (device_and_function != NULL) *device_and_function = LOW_BYTE(bx);
   }
  }
  else
  {
   ret_status = NOT_SUCCESSFUL;
  }
  return(ret_status);
}


int read_configuration_area(unsigned char function,
                            unsigned char bus_number,
                            unsigned char device_and_function,
                            unsigned char register_number,
                            unsigned long *data)
{
  int ret_status;
  unsigned short ax, flags;
  unsigned long ecx;

  _BH = bus_number;
  _BL = device_and_function;
  _DI = register_number;
  _AH = PCI_FUNCTION_ID;
  _AL = function;

  geninterrupt(0x1a);

  ecx = _ECX;
  ax = _AX;
  flags = _FLAGS;

  if ((flags & CARRY_FLAG) == 0)
  {
   ret_status = HIGH_BYTE(ax);
   if (ret_status == SUCCESSFUL)
   {
    *data = ecx;
   }
  }
  else
  {
   ret_status = NOT_SUCCESSFUL;
  }
  return(ret_status);
}
```


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```
int write_configuration_area(unsigned char function,
                unsigned char bus_number,
                unsigned char device_and_function,
                unsigned char register_number,
                unsigned long value)
{
  int ret_status;
  unsigned short ax, flags;

  _BH = bus_number;
  _BL = device_and_function;
  _ECX = value;
  _DI = register_number;
  _AH = PCI_FUNCTION_ID;
  _AL = function;

  geninterrupt(0x1a);

  ax = _AX;
  flags = _FLAGS;

  if ((flags & CARRY_FLAG) == 0)
  {
   ret_status = HIGH_BYTE(ax);
  }
  else
  {
   ret_status = NOT_SUCCESSFUL;
  }
  return(ret_status);
}

/*
```


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** FILE: TIMERS.C

```
**
*/

#include <stdlib.h>
#include <stdio.h>
#include <dos.h>
#include <ctype.h>
#include <conio.h>

#include "t7589t.h"

/* function prototypes */
void far interrupt irq_rcvd( void );
void init_timer_int( void );
void restore_orig_int( void );
void load_counter( int, unsigned int );
void read_counter( int, unsigned int *, unsigned char * );

/* global variables */
extern unsigned long t1_count;    /* timer 1 count */
extern unsigned long t2_count;    /* timer 2 count */
extern unsigned long t3_count;    /* timer 3 count */
extern unsigned char tmr_status;
extern unsigned int gpi_base;
extern unsigned int gpo_base;
extern unsigned int timer_base;
extern unsigned char pic1_org;
extern unsigned char gpo_org;

void far interrupt (* old_vect)(void);

/*********************************************************************/
/*  init_timer_int()                                                 */
/*                                                                   */
/*  purpose: Using the interrupt assigned, the original vector is    */
/*           saved and the vector to the new ISR is installed. The   */
/*           programmable-interrupt-controller (PIC) is enabled.     */
/*                                                                   */
/*********************************************************************/
/*  parameters: none                                                 */
/*********************************************************************/
/*  return value: none                                               */
/*********************************************************************/
void init_timer_int( void )
{
 disable();
```


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```
 old_vect = getvect( IRQ5 ); /* save vector for IRQ5 */
 setvect( IRQ5, irq_rcvd );

 /* enable interrupt 5 */
 outp(0x21, (pic1_org & 0xDF) ); /* 0 = enable 1 = disable */

 /* clear all three GPO inputs */
 outp( gpo_base, ( gpo_org & GPO_CLR ) );

 /* set all three GPO outputs to 1 to allow int status registers to function */
 outp( gpo_base, (gpo_org | GPO_T1 | GPO_T2 | GPO_T3 ) );

 enable();

} /* init_timer_int */

/*********************************************************************/
/*  restore_orig_int()                                               */
/*                                                                   */
/*  purpose: Using the interrupt assigned, the original vector is    */
/*        restored and the programmable-interrupt-controller         */
/*        is disabled.                                               */
/*                                                                   */
/*********************************************************************/
/*  parameters: none                                                 */
/*********************************************************************/
/*  return value: none                                               */
/*********************************************************************/
void restore_orig_int( void )
{
 disable();

 outp(0x21, pic1_org);

 setvect( IRQ5, old_vect );

 enable();

} /* restore_orig_int */

/*********************************************************************/
/*  load_counter()                                                   */
/*                                                                   */
/*  purpose: Loads the appropriate counter with the count passed     */
/*                                                                   */
/*                                                                   */
/*********************************************************************/
/*  parameters: int counter = 1, 2, 3 for COUNTER 1, 2, or 3         */
```


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```
/*            unsigned int count = count to be loaded          */
/*****************************************************************/
/*  return value: none                                           */
/*****************************************************************/
void load_counter( int counter, unsigned int count )
{
 int lsb, msb;

 lsb = count & 0xff;
 msb = count >> 8;

 switch( counter )
 {
  case 1: /* select counter 1, LSB then MSB, mode 2 */
   outp( timer_base + TIMER_CNTL, (CW_SC0 | CW_LSBMSB | CW_M2) );
   outp( timer_base + TIMER_CNTR1, (unsigned char) lsb );
   outp( timer_base + TIMER_CNTR1, (unsigned char) msb );
  break;

  case 2: /* select counter 2, LSB then MSB, mode 2 */
   outp( timer_base + TIMER_CNTL, (CW_SC1 | CW_LSBMSB | CW_M2) );
   outp( timer_base + TIMER_CNTR2, (unsigned char) lsb );
   outp( timer_base + TIMER_CNTR2, (unsigned char) msb );
  break;

  case 3: /* select counter 3, LSB then MSB, mode 2 */
   outp( timer_base + TIMER_CNTL, (CW_SC2 | CW_LSBMSB | CW_M2) );
   outp( timer_base + TIMER_CNTR3, (unsigned char) lsb );
   outp( timer_base + TIMER_CNTR3, (unsigned char) msb );
  break;
 }

} /* load_counter */

/*****************************************************************/
/*  read_counter()                                               */
/*                                                               */
/*  purpose: Reads the appropriate counter in the appropriate    */
/*           bank with the remainin count and status.            */
/*                                                               */
/*                                                               */
/*****************************************************************/
/*  parameters: int counter = 1, 2, 3 for COUNTER 1, 2, or 3     */
/*              unsigned int * count = remaining count           */
/*              unsigned char * status = counter status          */
/*****************************************************************/
/*  return value: none                                           */
/*****************************************************************/
```


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```
void read_counter( int counter,
                unsigned int * count, unsigned char * status )
{
 int lsb, msb;

 switch( counter )
 {
  case 1: /* select counter 1, LSB then MSB */
   outp( timer_base + TIMER_CNTL, ( CW_RBC | CW_RB_CNT | CW_RB_STAT |
CW_RB_C0 ) );
   *status = inp( timer_base + TIMER_CNTR1 ) & 0xFF;
   lsb = inp( timer_base + TIMER_CNTR1 ) & 0xFF;
   msb = inp( timer_base + TIMER_CNTR1 ) & 0xFF;
   msb = msb << 8;
   *count = ( lsb | msb );
  break;

  case 2: /* select counter 2, LSB then MSB */
   outp( timer_base + TIMER_CNTL, ( CW_RBC | CW_RB_CNT | CW_RB_STAT |
CW_RB_C1 ) );
   *status = inp( timer_base + TIMER_CNTR2 ) & 0xFF;
   lsb = inp( timer_base + TIMER_CNTR2 ) & 0xFF;
   msb = inp( timer_base + TIMER_CNTR2 ) & 0xFF;
   msb = msb << 8;
   *count = ( lsb | msb );
  break;

  case 3: /* select counter 3, LSB then MSB */
   outp( timer_base + TIMER_CNTL, ( CW_RBC | CW_RB_CNT | CW_RB_STAT |
CW_RB_C2 ) );
   *status = inp( timer_base + TIMER_CNTR3 ) & 0xFF;
   lsb = inp( timer_base + TIMER_CNTR3 ) & 0xFF;
   msb = inp( timer_base + TIMER_CNTR3 ) & 0xFF;
   msb = msb << 8;
   *count = ( lsb | msb );
  break;
 }

} /* read_counter */


/*****************************************************************/
/*  irq_rcvd()                                                   */
/*                                                               */
/*  purpose: Interrupt service routine used to service any of the */
/*        counters on the 7589.                                  */
/*                                                               */
/*                                                               */
```


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```
/*****************************************************************/
/*  parameters: none                                             */
/*****************************************************************/
/*  return value: none                                           */
/*****************************************************************/
void interrupt irq_rcvd(void)
{

 disable();

 asm {
  .386P
  push  eax
  push  ebx
 }

 tmr_status = inp( gpi_base ) & 0xFF;

 /* increment counts and clear status */
 if( tmr_status & GPI_T1 ) {
  t1_count++;
  outp( gpo_base, (gpo_org & (~GPO_T1)) );  /* clear timer 1 status bit */
 }
 if( tmr_status & GPI_T2 ) {
  t2_count++;
  outp( gpo_base, (gpo_org & (~GPO_T2)) );  /* clear timer 2 status bit */
 }
 if( tmr_status & GPI_T3 ) {
  t3_count++;
  outp( gpo_base, (gpo_org & (~GPO_T3)) );  /* clear timer 3 status bit */
 }

 outp( gpo_base, (gpo_org | GPO_T1 | GPO_T2 | GPO_T3) ); /* enable status */

 /* Non specific end of interrupt to PIC */
 outp(0x20, 0x20);  /* Master end of irq command */

 asm {
  .386P
  pop  ebx
  pop  eax
 }

 enable();

}

/*
```


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** FILE: T_TIMERS.C

```
*/

#include <stdlib.h>
#include <stdio.h>
#include <string.h>
#include <conio.h>
#include <ctype.h>
#include <dos.h>

#include "pci.h"
#include "t7589t.h"

/* TIMERS.C function prototypes */
void far interrupt irq_rcvd( void );
void init_timer_int( void );
void restore_orig_int( void );
void load_counter( int, unsigned int );
void read_counter( int, unsigned int *, unsigned char * );

/* global variables */
unsigned char bus, dev_func;

/* the following globals are used in other files as 'extern' variables */
unsigned char tmr_status;
unsigned long t1_count;     /* counts no. of times timer 1 ISR entered */
unsigned long t2_count;     /* counts no. of times timer 1 ISR entered */
unsigned long t3_count;     /* counts no. of times timer 1 ISR entered */
unsigned int pwr_mgm_base;
unsigned int gpi_base;
unsigned int gpo_base;
unsigned int timer_base;
unsigned char pic1_org;
unsigned char gpo_org;

void main( int argc, char * argv[] )
{
 unsigned long t1;
 int test_int;
 unsigned long temp_dword;

 timer_base = 0x500;

 /* locate the power management device on the PCI bus */
 test_int = find_pci_device(DID_PWR_MGM, VID_PWR_MGM, 0,
          &bus, &dev_func);
 if(test_int != SUCCESSFUL)
```


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```
{
  printf("\nUnable to locate power management device on PCI bus\n");
  exit( 1 );
}

/* get base address from config area */
test_int = read_configuration_area(READ_CONFIG_DWORD,
                        bus, dev_func, 0x40, &temp_dword);
if(test_int != SUCCESSFUL)
{
  printf("\nUnable to read POWER MGM. BASE ADDRESS @ 0x40 in config
space\n");
  exit( 1 );
}
pwr_mgm_base = temp_dword & 0x0000FFC0;
gpi_base = pwr_mgm_base + 0x31; /* PIX general purpose input bits 8-15 */
gpo_base = pwr_mgm_base + 0x37; /* PIX general purpose output bits 24-31 */

disable();

/* Read 8259 Programmable Interrupt controller */
pic1_org = inp(0x21) & 0xFF;

/* disable interrupt 5 */
outp(0x21, (pic1_org | 0x20) ); /* 0 = enable 1 = disable */

enable();

gpo_org = inp( gpo_base ) & 0xFF; /* save original general purpose out */


/* clear all three status bits in GPI */
outp( gpo_base, ( gpo_org & GPO_CLR ) );

/* set all three GPO outputs to 1 to allow int status registers to function */
outp( gpo_base, ( gpo_org | GPO_T1 | GPO_T2 | GPO_T3 ) );


/* setup timers interrupt service routine */
init_timer_int();

/*
** setup counter to generate an interrupt (counters 1)
*/

/* setup for interrupts to occur */
t1_count = 0;
t1 = 0;
```


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```
  tmr_status = 0;
  test_int = 100;

  /* load counter */
  load_counter( 1, 0xFFFF );

  do
  {
   if( t1_count ) {
     t1++;
     break;
   }
   test_int--;
   delay( 1 );

  } while( test_int );

  /* disable timers by reloading the control word */
  outp( timer_base + TIMER_CNTL, (CW_SC0 | CW_LSBMSB | CW_M2) );

  restore_orig_int();
  outp( gpo_base, gpo_org );
  exit( 1 );

} /* end main */

/*
```


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** FILE: PCI.H

```
**
*/

#define TRUE    1
#define FALSE0

#define CARRY_FLAG 0x01


/* PCI Functions */
#define PCI_FUNCTION_ID       0xB1
#define PCI_BIOS_PRESENT0x01
#define FIND_PCI_DEVICE0x02
#define FIND_PCI_CLASS_CODE0x03
#define READ_CONFIG_BYTE0x08
#define READ_CONFIG_WORD0x09
#define READ_CONFIG_DWORD      0x0A
#define WRITE_CONFIG_BYTE      0x0B
#define WRITE_CONFIG_WORD      0x0C
#define WRITE_CONFIG_DWORD     0x0D

/* PCI Return codes */

#define SUCCESSFUL0x00
#define NOT_SUCCESSFUL0x01


/* Prototypes */

int find_pci_device(unsigned short device_id,
              unsigned short vendor_id,
              unsigned short index,
              unsigned char *bus_number,
              unsigned char *device_and_function);

int read_configuration_area(unsigned char function,
                    unsigned char bus_number,
                    unsigned char device_and_function,
                    unsigned char register_number,
                    unsigned long *data);

int write_configuration_area(unsigned char function,
                     unsigned char bus_number,
                     unsigned char device_and_function,
                     unsigned char register_number,
                     unsigned long value);
```


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**FILE: PIC.H

```
/*                                                      */
/*    Bit definitions for the PC/AT programable interrupt controller (PIC) */
/*                                                      */
/*                                                      */

#define     PIC1        0x20    /* I/O port addr of PIC 1 */
#define     PIC1_MASK   0x21    /* I/O port addr of PIC 1 mask reg */
#define     PIC2        0xA0    /* I/O port addr of PIC 2 (AT only) */
#define     PIC2_MASK   0xA1    /* I/O port addr of PIC 2 mask reg */

#define     IRQ0_MASK   0x01    /* mask off int 0 - timer 0 sys tic */
#define     IRQ1_MASK   0x02    /* mask off int 1 - keyboard */
#define     IRQ2_MASK   0x04    /* mask off int 2 - rsvd XT; 8-15 AT */
#define     IRQ3_MASK   0x08    /* mask off int 3 - com port */
#define     IRQ4_MASK   0x10    /* mask off int 4 - com port */
#define     IRQ5_MASK   0x20    /* mask off int 5 - HD XT; LPT AT */
#define     IRQ6_MASK   0x40    /* mask off int 6 - Floppy Disk */
#define     IRQ7_MASK   0x80    /* mask off int 7 - LPT */

#define     IRQ8_MASK   0x01    /* mask off int 8 - RTC */
#define     IRQ9_MASK   0x02    /* mask off int 9 - Re-directed IRQ2 */
#define     IRQ10_MASK  0x04    /* mask off int 10 - Unassigned */
#define     IRQ11_MASK  0x08    /* mask off int 11 - Unassigned */
#define     IRQ12_MASK  0x10    /* mask off int 12 - Unassigned */
#define     IRQ13_MASK  0x20    /* mask off int 13 - Co-processor */
#define     IRQ14_MASK  0x40    /* mask off int 14 - HD AT */
#define     IRQ15_MASK  0x80    /* mask off int 15 - Unassigned */

#define     PIC_EOI     0x20    /* PIC End Of Interrupt */

/*
```


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** FILE: T7589T.H

```
**
*/

#define    DID_PWR_MGM    0x7113
#define    VID_PWR_MGM    0x8086

#define    IRQ5        0x0D

#define    GPI_T1       0x80   /* PIX General Purpose Input 15 (tmr 1)  */
#define    GPI_T2       0x40   /* PIX General Purpose Input 14 (tmr 2)  */
#define    GPI_T3       0x20   /* PIX General Purpose Input 13 (tmr 3)  */
#define    GPO_T1       0x40    /* PIX General Purpose Output 30 (tmr 1) */
#define    GPO_T2       0x10    /* PIX General Purpose Output 28 (tmr 2) */
#define    GPO_T3       0x08    /* PIX General Purpose Output 27 (tmr 3) */

#define    GPO_CLR      0xA7    /* PIX General Purpose Output CLR TMRS   */

#define    TIMER_CNTR1    0x00    /* Timer counter 1 offset          */
#define    TIMER_CNTR2    0x01    /* Timer counter 2 offset          */
#define    TIMER_CNTR3    0x02    /* Timer counter 3 offset          */
#define    TIMER_CNTL     0x03    /* Timer control offset           */

/*************************************************************************/
/* 8254 Control word                                                     */
/*************************************************************************/
#define    CW_SC0       0x00    /* W Selcect counter 0             */
#define    CW_SC1       0x40    /* W Selcect counter 1             */
#define    CW_SC2       0x80    /* W Selcect counter 2             */
#define    CW_RBC       0xC0    /* W Read back command              */
#define    CW_CLC       0x00    /* W Cntr latch command (cnt/stat)      */
#define    CW_SLC       0x00    /* W Status latch command          */
#define    CW_LSB       0x10    /* W LSB only                  */
#define    CW_MSB       0x20    /* W MSB only                   */
#define    CW_LSBMSB      0x30    /* W LSB first then MSB            */
#define    CW_M0        0x00    /* W Mode 0                    */
#define    CW_M1        0x02    /* W Mode 1                    */
#define    CW_M2        0x04    /* W Mode 2                    */
#define    CW_M3        0x06    /* W Mode 3                    */
#define    CW_M4        0x08    /* W Mode 4                    */
#define    CW_M5        0x0A    /* W Mode 5                     */
#define    CW_BCD       0x01    /* W Binary Coded Decimal          */
#define    CW_RB_CNT      0x00    /* W Read back count             */
#define    CW_RB_STAT     0x00    /* W Read back status            */
#define    CW_RB_C0       0x02    /* W Read back counter 0         */
#define    CW_RB_C1       0x04    /* W Read back counter 1         */
#define    CW_RB_C2       0x08    /* W Read back counter 2         */
```


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Directory WATCHDOG

This directory contains sample code useful in the creation of applications involving the VMIVME-7589's watchdog timer function as described in Chapter 4.

** FILE:WDTO.C

```
**
**     Watchdog timeout
*/

#include   <stdlib.h>
#include   <stdio.h>
#include   <dos.h>
#include   <time.h>
#include   <conio.h>
#include   <ctype.h>
#include   "watchdog.h"

unsigned char far * wd_ptr;
char usr[80];
unsigned char dog;

void main( void ) {

 wd_ptr = (unsigned char far *) MK_FP( 0xD800, 0 );

 /* set WatchDog Alarm Mask 1 - deactivated and update with 0 time */
*(wd_ptr + WD_CMD) = ( WD_TE | WD_WAM );
*(wd_ptr + WD_MSEC) = 0; /* load with 0 to disable */
*(wd_ptr + WD_SEC) = 0;  /* load with 0 to disable */
*(wd_ptr + WD_CMD) = ( WD_TE | WD_WAM ); /* allow update with 0 time */
*(wd_ptr + WD_CMD) = WD_WAM; /* set watchdog alarm mask to 1 */

 printf("\nJumper J30 installed? [Y/N]: ");
 scanf("%s%*c", usr );
 fflush( stdin );
 if( toupper( usr[0] ) != 'Y' ) exit( 1 );

 printf("\n");

*(wd_ptr + WD_MSEC) = 0x99; /* 00.99 seconds */
*(wd_ptr + WD_SEC) = 0x99;  /* 99.00 seconds */
*(wd_ptr + WD_CMD) = ( WD_TE | WD_PU ); /* set for 3 ms pulse */

 printf("Reset time out in 100 seconds (1 min 40 sec)\n\n");
```


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```
  /* read one of the alarm regs to cause reload and prevent time out */
  /* dog = *(wd_ptr + WD_MSEC); */

} /* end main */


/*
```


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** FILE: WATCHDOG.H

```
**
** DS1384 REGISTER OFFSETS
*/
                              /* 7 6 5 4 3 2 1 0 */
#define       CLK_MSEC       0x00    /* 00-99                    */
#define       CLK_SEC        0x01    /* 00-59 0                  */
#define       CLK_MIN        0x02    /* 00-59 0                  */
#define       CLK_MINAL      0x03    /* 00-59 M                  */
#define       CLK_HRS        0x04    /* 01-12+A/P OR 00-23       */
#define       CLK_HRSAL      0x05    /* 01-12+A/P OR 00-23       */
#define       CLK_DAY        0x06    /* 01-07 0 0 0 0 0          */
#define       CLK_DAYAL      0x07    /* 01-07 M 0 0 0 0          */
#define       CLK_DATE       0x08    /* 01-31 0 0                */
#define       CLK_MONTH      0x09    /* 01-12     0              */
#define       CLK_YRS        0x0A    /* 00-99                    */
#define       WD_CMD         0x0B    /* command register         */
#define       WD_MSEC        0x0C    /* milli second watchdog time   */
#define       WD_SEC         0x0D    /* seconds watchdog time        */

/*
** DS1384 COMMAND REGSITER BIT DEFINITIONS
*/

#define       WD_TE          0x80    /* transfer enable 1 - allow updates */
#define       WD_IPSW        0x40    /* interrupt switch 0 - WD out INTA  */
#define       WD_IBHL        0x20    /* int. B output 0 - current sink    */
#define       WD_PU          0x10    /* pulse/level 1 - 3 ms pulse        */
#define       WD_WAM         0x08    /* watchdog alarm mask 0 - active    */
#define       WD_TDM         0x04    /* time-of-day alarm mask 0 - active */
#define       WD_WAF         0x02    /* watchdog alram flag               */
#define       WD_TDF         0x01    /* time-of-day flag                  */
```


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