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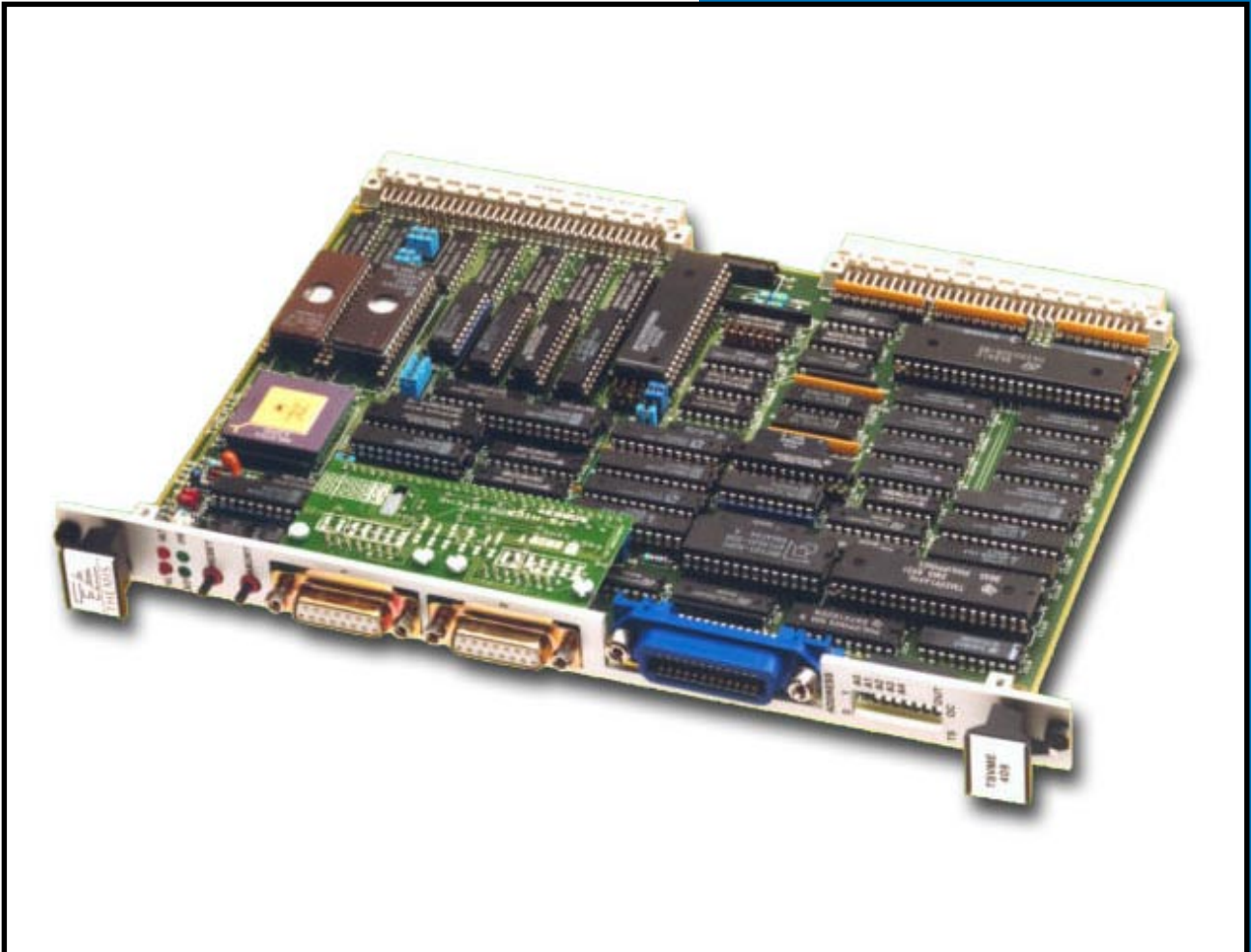
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TSVME 409

*CPU/IPC
GPIB Controller*



Main specifications

- IPC (Intelligent Peripheral Controller) architecture based on 12.5 MHz 68010 CPU
- IEEE 488 Listener / Talker / Controller interface based on TMS 9914A GPIB controller
- 1 MB shared memory with parity
- 2 RS232 serial ports on front panel
- one 68230 PI/T providing a timer and two 8-bit buffered parallel I/O (accessible on P2)
- Complete VME A24D16 master/slave interface

INDUSTRIAL I/O BOARD

Whenever it is desired to combine the master CPU and the GPIB controller on a single VME bus slot, or to offload the master CPU from GPIB protocol handling, or simply to ensure high performance on the GPIB bus, the **TSVME409** appears as an efficient solution.

The TSVME409 is a double Eurocard intelligent IEEE-488 controller, designed around a 68010 CPU at 12.5 MHz and an enhanced GPIB interface. The processor handles the protocol and data buffers in up to 1 MB of shared DRAM with parity control. The firmware is stored on the 128 KB of EPROM. The board has a full master/slave VMEbus interface, with mailbox interrupts and interrupter. GPIB address is selectable through a switch group accessible from the front panel.

The TSVME 409's high data throughput is achieved through the use of a proprietary data flow sequencer. A 512-byte FIFO is connected to the TMS9914A chip in DMA mode. This architecture allows sustained data transfers at up to 500 Kbyte/s on the IEEE-488 bus.

Additional features include two RS232 serial lines and a 68230 PI/T, providing a timer and two 8-bit buffered parallel I/O (accessible from P2).

Four LEDs on front panel indicate the FAIL-line state, the HALT state, a VMEbus access (BUSY) and a GPIB access.

Two push-buttons are available on front panel : RESET and ABORT.

The TSVME409 board comes with 2 EPROMs containing the VBUG monitor and the IEEE-488 primitives.

VBUG features a board-level self-test and extremely efficient debugging tools, including line-by-line assembler/disassembler, transparent mode, host downloading, symbol support and memory windowing.

The IEEE-488 primitives allow the user to write instrument control programs without dealing explicitly with the GPIB bus protocol. Dynamic interrupt handling , including sleep/wake-up mechanism, is fully supported. All primitives are accessed through a single entry point in the EPROM, thus facilitating the use of high level languages like C.

ORDERING INFORMATION :

TSVME 409	IEEE 488 interface, Intelligent Peripheral Controller
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☛ **CUSTOMIZED BOARDS** : VME Boards are usually delivered with a standard, general-purpose configuration. Application-related configuration can be made either by the customer, or before shipping, in our factory. Given the jumper, solder beads and wrapping configuration, we deliver boards ready to be plugged into the destination VME system.

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