CPV5000 CompactPCI® Single Board Computer Installation and Reference Guide

CPV5000A/IH3

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Preface

The *CPV5000 Single Board Computer Installation and Reference Guide* describes the installation, components, and configurations of the CPV5000. The document should be used by anyone who wants general as well as technical information about the CPV5000 Single Board Computer.

All Motorola PWBs (printed wiring boards) are manufactured by UL-recognized manufacturers, with a flammability rating of 94V-0.

Printed in the United States of America
November 1998

Safety Summary
Safety Depends On You

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the equipment. Motorola, Inc. assumes no liability for the customer's failure to comply with these requirements.

The safety precautions listed below represent warnings of certain dangers of which Motorola is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. The equipment is supplied with a three-conductor ac power cable. The power cable must be plugged into an approved three-contact electrical outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

Do Not Operate in an Explosive Atmosphere.

Do not operate the equipment in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment constitutes a definite safety hazard.

Keep Away From Live Circuits.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified maintenance personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone.

Do not attempt internal service or adjustment unless another person capable of rendering first aid and resuscitation is present.

Use Caution When Exposing or Handling the CRT.

Breakage of the Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, avoid rough handling or jarring of the equipment. Handling of the CRT should be done only by qualified maintenance personnel using approved safety mask and gloves.

Do Not Substitute Parts or Modify Equipment.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

WARNING

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

All Motorola PWBs (printed wiring boards) are manufactured by UL-recognized manufacturers, with a flammability rating of 94V-0.

WARNING

This equipment generates, uses, and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference (EMI) if not installed and used in a cabinet with adequate EMI protection.

If any modifications are made to product, the modifier assumes responsibility for radio frequency interference issues. Changes or modifications not expressly approved by Motorola Computer Group could void the user's authority to operate the equipment.

CE European Notice: Board products with the CE marking comply with the EMC Directive (89/336/EEC). Compliance with this directive implies conformity to the following European Norms:

EN55022 (CISPR 22) Radio Frequency Interference, Class B

EN50082-1 (IEC801-2, IEC801-3, IEC801-4) Electromagnetic Immunity

The product also fulfills EN60950 (product safety) which is essentially the requirement for the Low Voltage Directive (73/23/EEC).

This board product was tested in a representative system to show compliance with the above mentioned requirements. A proper installation in a CE-marked system will maintain the required EMC/safety performance.

For minimum RF emissions, it is essential that you implement the following conditions:

- Install shielded cables on all external I/O ports
- Connect conductive chassis rails to earth ground to provide a path for connecting shields to earth ground
- Tighten all front panel screws

Lithium battery caution

The board contains a lithium battery to power the clock and calendar circuitry.

CAUTION:
Danger of explosion if battery is incorrectly replaced.

Replace only with the same or equivalent type recommended by the equipment manufacturer. Dispose of used batteries according to the manufacturer's instructions.

ATTENTION
Il y a danger d'explosion s'il y a remplacement incorrect de la batterie.

Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabricant.

VORSICHT!
Explosionsgefahr bei unsachgemäβem Austausch der Batterie.

Ersatz nur durch denselben oder einen vom Hersteller empfohlenen gleichwertigen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.

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CPV5000 Single Board Computer Overview 1

About this Book: Changes between IH2 and IH3

This book replaces CPV5000A/IH2. The main differences are to reflect that:

- the board now supports AMD processors as well as standard P55C Intel processors (see CPU Voltage Settings, page 3-5, for information on setting the appropriate voltage jumper for your processor), and
- the board now supports 233 MHz and 266 MHz processors (see CPU speed settings, page 3-4).

Note: It was not noted in previous versions of this book that having the 5V power supply lag the 3.3V power supply as the board is powered up can cause the CPV5000 to inaccurately report the CPU clock speed. In order to prevent this, it is necessary that the 5V power supply ramp up at the same time (or before) the 3.3V supply does.

Introduction

The CPV5000 is a CompactPCI PCI Industrial Computer Manufacturers Group (PICMG) compatible Single Board Computer (SBC). The CPV5000 is available with a 64-bit Pentium® P55C processor or an AMD K-6® processor. The CPV5000's 6U, 8HP Compact PCI standard form factor is designed for installation into PICMG CompactPCI compliant CompactPCI backplanes.

The CPV5000 supports either Fast Page Mode (FPM) or up to 256 MB Extended Data Out (EDO) Single Inline Memory Module (SIMM), 512 KB L2 cache is included.

The on-board PCI devices consist of a PCI Ultra SCSI controller, PCI 10/100 Ethernet controller, and a PCI SVGA controller. The CPV5000 has an optional, on-board EIDE drive and a floppy drive. All I/O features are available through front panel connectors or through the IEEE1101.11 compliant 80mm rear transition module.

Additional features

The CPV5000 also supports these features:

- Parallel port interface (available through rear I/O and front panel on a Micro-D connector)
- Two high speed 16650 serial ports (available through rear I/O and front panel on a stacked Micro-D connector)
- Two USB ports (available through rear I/O and dual connectors on front panel)
- PS/2 keyboard and mouse connector
- Video signals available through rear I/O and the front panel
- Ultra SCSI support via AIC7880
- SCSI signals available through rear I/O and front panel connector
- Ethernet, 10/100 Intel® 82558 Ether Express Pro compatible
- Green PC modes standby and suspend

  Video power down modes standby and suspend

  IDE power down modes standby and suspend
- A standard time of year clock with battery backup integrated into the SMC Ultra I/O port

Input/Output interfaces

Refer to Table 1-1 for brief descriptions of the input/output interfaces on the CPV5000.

Note When the identical function is available through the CPV5000's front panel and the rear transition module, you can use either the front or the rear, not both.

Table 1-1. Input/Output interfaces

Function	CPV5000		CPV5000 Transition Module	
	Front Panel	On-board	On-board	Rear Panel
Speaker	N/A		Header	
Reset	Push button		Header	
Disk active LED	Green		Header	
IDE interface		44-(2x22) pin header	Two 40-pin headers	
Floppy disk interface		26-pin	34-pin header	
Bi-directional, EPP/ECP parallel port	25-pin micro-D			25-pin D
Serial port 1 (16550)	9-pin micro-D			9-pin D
Serial port 2 (16550)	9-pin micro-D			9-pin D
PS/2 keyboard	6-pin mini-DIN			6-pin mini-DIN
PS/2 mouse				6-pin mini-DIN
SVGA	15-pin D			
Ethernet	RJ-45			
SCSI	68-pin D		68-pin D	68-pin D
USB	Two 4-pin connectors			

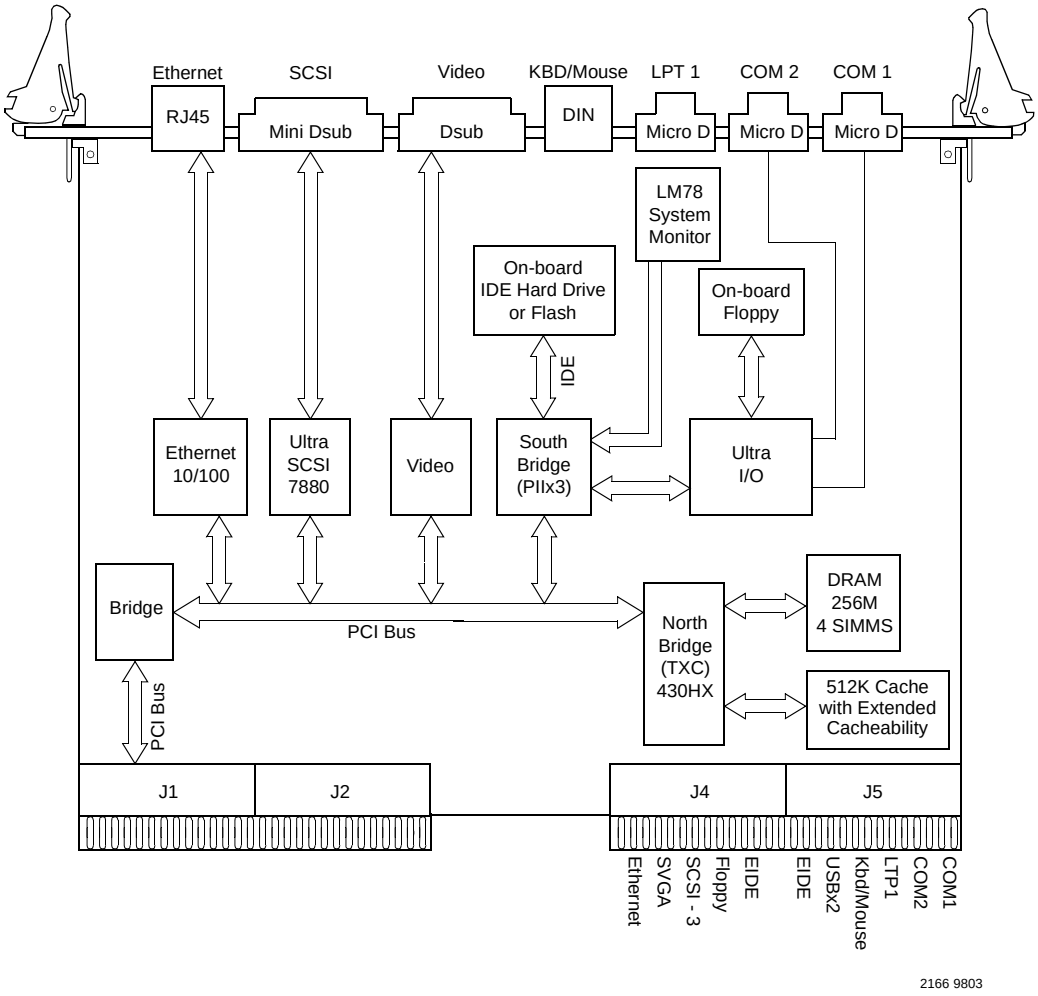

Figure 1-1. Block diagram

Special functions

The CPV5000 uses three functions that are designed for use in certain applications. These are:

- Watchdog Timer

  The watchdog timer is a count down timer. When the counter reaches zero, it can set a flag in a register, optionally assert IOCHK (NMI), and optionally perform an SBC reset.

- Temperature Monitoring (LM78)

  Temperature monitoring monitors the CPV5000 for an over temperature condition to a resolution of +/- 0.5 ° C. On an over temperature condition, a flag can be set in a register or an interrupt can be generated.

- System Monitoring (LM78)

  The LM78 is a highly integrated data acquisition system for hardware monitoring of a microprocessor-based system. On the CPV5000, the LM78 monitors backplane and CPU voltage, CPU temperature (user definable threshold), fan rotation (CPU, chassis), and intrusion with status interrogated through local NMI or SMI.

Additional information resources

For additional information, go to these Web sites:

Motorola Computer Group:

http://www.mcg.mot.com

National Semiconductor (for LM78 Microprocessor system hardware monitor specifications):

http://www.national.com

American Megatrends:

http://www.ami.com

Getting Started 2

This chapter provides basic installation information.

Note This document treats the CPV5000 as a component of a system, and assumes installation into a PICMG CompactPCI compliant CompactPCI backplane.

Antistatic precautions

Caution Take care when handling the CPV5000. The CPV5000 and its active components are sensitive to electrostatic discharge (ESD), and can easily be damaged. Motorola recommends that you use an antistatic wrist strap when handling the CPV5000 and associated components. In addition, follow these rules:

- Do not allow any circuit board or component to touch non-conductors.
- Make sure that your clothing does not make contact with any circuit board or component.
- Keep any loose circuit boards inside or on top of their conductive plastic wrappers.
- Before you touch a loose circuit board or component, ensure that any static electricity is discharged.

2

Before installing the CPV5000

After removing the CPV5000 from its packaging:

- Check for obvious physical damage.
- Verify that the coin cell battery is in its holder and inserted correctly.
- Verify that the CPU fan is connected.
- Install main memory SIMMs. Refer to Chapter 3 and Chapter 4 for information about the SIMM headers and the installation of main memory SIMMs.
- A minimum of two, identical, main memory SIMMs are required. The SIMMs may be installed in either bank.
- Set the CPU speed using J10, J14, J15, J29 (refer to CPU speed settings, page 3-4).
- Set the CPU type (AMD/Intel) using J30 (refer to CPU Voltage Settings, page 3-5).

Warning

Make sure that you disconnect the chassis from the main power supply before you continue.

Installation instructions

Use these steps to install the CPV5000 into your computer chassis.

1. Follow the instructions in your chassis user manual to remove any outer cover.
2. Locate the CPV5000 position slot (normally slot one, the far right slot when viewed from the front).
3. Remove any filler panel (or existing CPU board) that might fill that slot.
4. Install the top and bottom edge of the CPV5000 in the guides of the chassis.
5. Ensure that the levers of the two injector/ejectors are in the inward position.
6. Slide the CPV5000 into the chassis until resistance is felt.
7. Simultaneously move the injector/ejector levers in an outward direction.
8. Verify that the CPV5000 is properly seated and secure it to the chassis using the two screws located adjacent to the injector/ejector levers**.**
9. Connect the appropriate cables to the CPV5000.
10. Repeat steps 3 through 8 for installing the transition module.

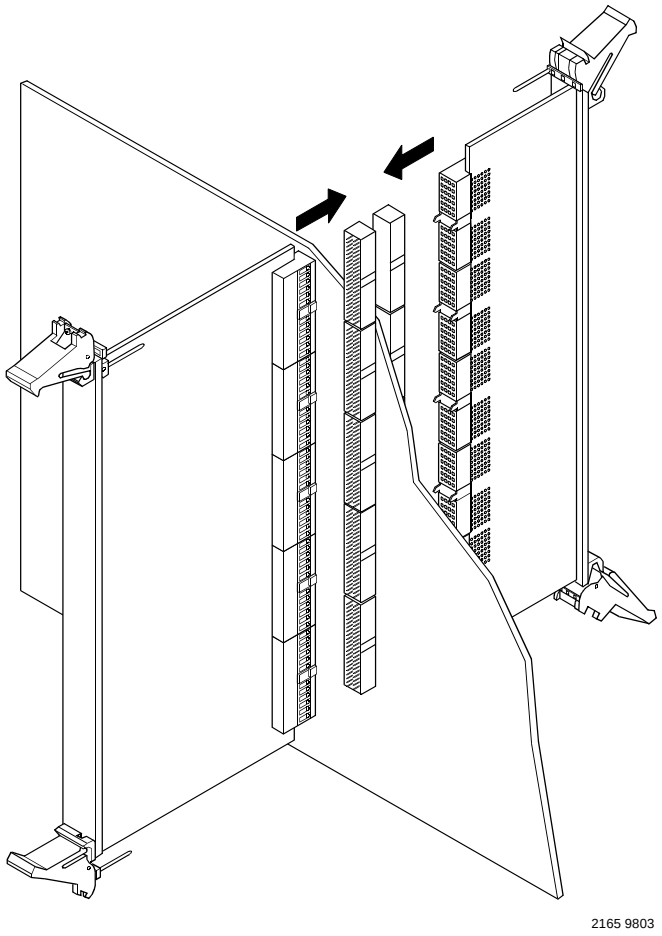

Figure 2-1. Installing the CPV5000

Powering up the CPV5000

When you are ready to power up the CPV5000:

- If the power supply in your system is not auto-sensing, verify that the chassis power supply voltage setting matches the voltage present in the country of use.
- On powering up, the CPV5000 displays the AMIBIOS revision and then runs a memory test.

If the <DEL> key is pressed during the memory test, the CPV5000 will enter the Basic Input/Output System (BIOS) setup after completing the memory test. If the BIOS setting for quick boot is enabled, the memory test may have completed before the VGA has initialized fully. Refer to Chapters 6 and 7 for more information about start up tests and BIOS setup.

The initial boot sequence is complete when the BIOS is displayed.

Coin Battery

The Real time clock and CMOS backup battery is socketed. The battery has a series resistor and diode to conform to industry safety requirements. The battery is rated at 280mA/Hr and has an expected shelf life of 10 years.

2

Front panel

The CPV5000's front panel has connectors for keyboard/mouse, SCSI, video, parallel printer, COM1/2, and ethernet. Indicator lights on the front panel display power, hard disk activity, watchdog alarm, and speaker status.

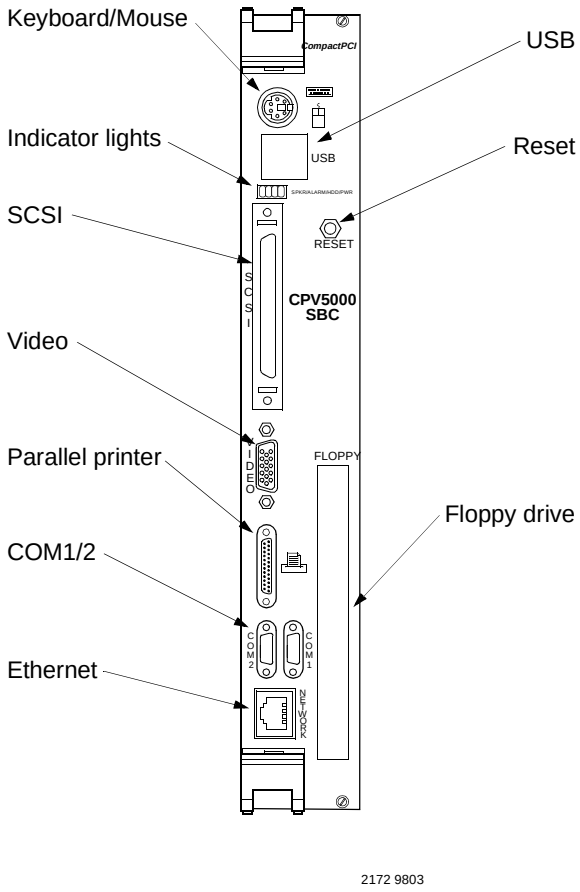

Figure 2-2. Front panel connectors and LEDs

Connectors and Components on the CPV5000

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Components

The CPV5000 single board computer carries components on both sides. Figure 3-1 shows the location of the connectors and headers.

Table 3-1. Major chip functions

Reference	Description	Manufacturer	Part Number
U20	Ethernet	Intel	S82557
U24	PCI-PCI Bridge	Digital	21150-AA
U40	Ultra I/O	SMC	FDC37C932
U28	Video	Cirrus Logic	GD5446-HC-A
U38	SCSI Adaptor	Adaptec	AIC-7880P
U29	PCI-ISA Bridge	Intel	SB82371SB
U43	PCI Host Bridge	Intel	FW82439HX

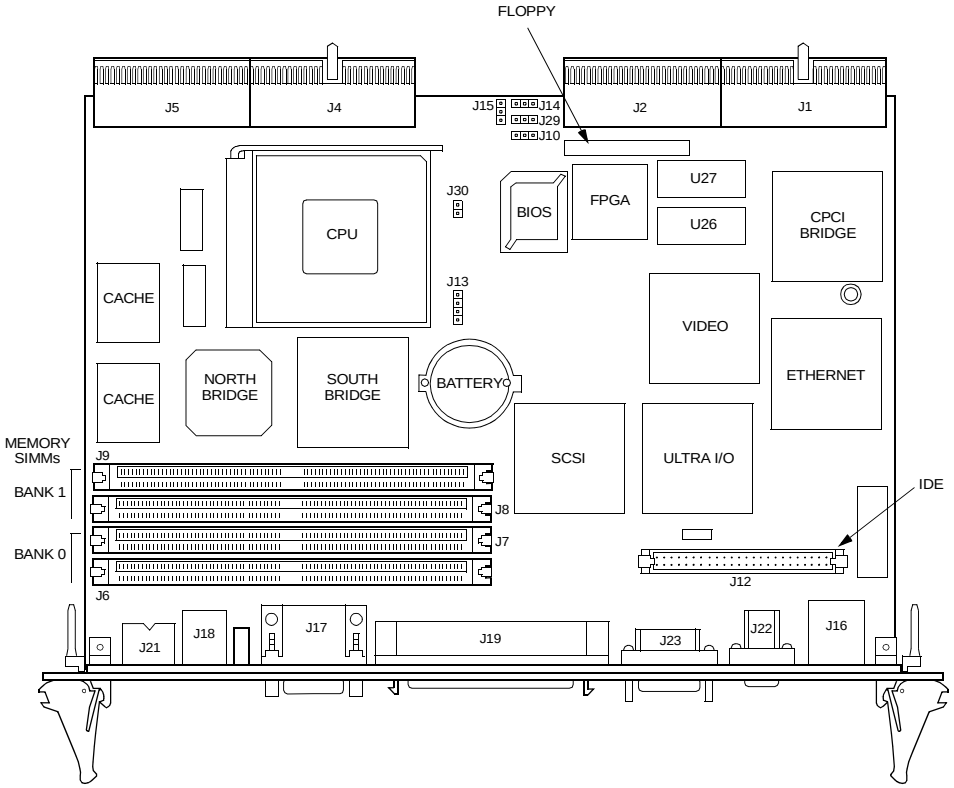


Figure 3-1. Location of main components on the CPV5000

Connecting to and configuring headers

The CPV5000 provides several headers for attaching peripheral devices. Before you install the CPV5000, you may want to connect your peripheral cables to the headers. Headers are circuit board-mounted components, as opposed to connectors which are located on the CPV5000's front panel and transition module.

Note When the identical function is available through the CPV5000's front panel and the rear transition module, you can use either the front or the rear, not both.

Please note the following cautions when connecting peripherals to the CPV5000.

Warning Always remove power from the system before connecting peripherals to the CPV5000. To reduce the risk of personal injury, disconnect the power cord from the power source. Only qualified, experienced electronics personnel should access the interior of a chassis.

Caution The components of the CPV5000 are sensitive to static discharge. While out of the unit, the CPV5000 should be placed on a static-dissipative surface or into a static-shielding bag.

CPU speed settings

Table 3-2 describes the possible jumper settings for different speed CPUs. Install a shorting block across two pins on each of the four speed configuration jumpers to configure any given speed.

Table 3-2. CPU speed settings

CPU Speed	J10	J15	J14	J29
166 Mhz	2-3	1-2	1-2	2-3
200 Mhz	2-3	2-3	1-2	2-3
233 Mhz	2-3	2-3	2-3	2-3
266 Mhz	2-3	1-2	2-3	1-2
300 Mhz	2-3	1-2	1-2	1-2

CPU Voltage Settings

J30 has been added to the CPV5000 with the introduction of the AMD processor, because Intel and AMD processors run on different core voltages. If you are using an Intel processor, then you should jumper J30. If you are using an AMD processor, then leave the jumper off.

If your board does not have a J30 jumper, then it is not equipped to use the AMD processors.

Figure 3-2. J30: CPU Voltage Settings

Ethernet configuration

The Ethernet configuration jumper is a three by four jumper block. A four position shorting block is installed to select the Ethernet routing. To maintain signal integrity, the Ethernet signals can be routed to the front connector or the rear connector, but not both. Table 3-3 indicates which side the shorting block should be installed to select the front or rear connector.

Table 3-3. Ethernet configuration jumpers

Jumper J28	Ethernet Routing
Row 1-2	Rear connector
Row 2-3	Front connector

USB configuration

The USB configuration jumper is a two by four jumper block. A four position shorting block is installed to select the USB routing. To maintain signal integrity, the USB signals can be routed to the rear connector. If rear connector routing is selected, no USB devices can be installed on the front connector. Table 3-4 indicates which side the shorting block should be installed to select the front or rear connector.

Table 3-4. USB configuration jumpers

Jumper J27	USB Routing
Installed	Rear connector
Removed	Front connector

Front panel connectors

Table 3-5 specifies the connectors that are available from the front panel.

Table 3-5. Front panel connectors

Location	Type	Description
J23	25-pin micro-D	Parallel connector
J22	2x9-pin micro-D	Serial port 1, serial port 2
J16	RJ45 connector	Ethernet connector
J19	68-pin high density	SCSI connector
J17	15-pin high density D-SUB	Video connector
J18	2x4-pin USB	USB port 1, USB port 2
J21	6-pin PS/2 female connector	Keyboard/mouse

Rear I/O connectors

Table 3-6 specifies the connectors that are available to support devices at the rear of the chassis.

Table 3-6. Rear I/O connectors

Location	Type	Description
J5, J8	2x40-pin shrouded header	2xEIDE connector
J9	34-pin shrouded header	Floppy connector
J16	25-pin D-SUB	Parallel connector
J16, J10	2x9-pin D-SUB	Serial port 1, serial port 2
J13	RJ45 connector	Ethernet connector
J17	68-pin high density connector	SCSI connector
J16	15-pin high density D-SUB	Video connector
J2	10-pin unshrouded connector	Miscellaneous LM78 inputs
J12	2x4-pin USB	USB port 1, USB port 2
J14	6-pin PS/2 female connector	Keyboard/mouse (PS/2 connector)
J15	6-pin PS/2 female connector	Mouse (PS/2 connector)
J7	4-pin latching connector	External power (+12V)
J3, J4	4-pin latching connector	Fan power and Tach inputs

On-board connectors

Table 3-7 specifies the connectors that are available to support devices on the CPV5000.

Table 3-7. On-board connectors

Location	Type	Description
J12	44 (2x22) pin shrouded header	EIDE connector
J20	26-pin flex cable header	Floppy connector

Connectors J4 and J5

The following table describes the common product pin-out for the CompactPCI user I/O connector as seen from the rear of the backplane. This signal arrangement is proposed for bringing out the I/O signals common to 6U CompactPCI processor boards based on the ”Win-tel” architecture.

Table 3-8. J4 connector pin assignments

Pin #	Row F	Row E	Row D	Row C	Row B	Row A	
25	GND	VCC	NC	NC	NC	NC	GND
24	GND	BTI*	GND	DASP*b	CS3FX*b	CS1FX*b	GND
23	GND	DA2b	DA0b	GND	DA1b	IOCS16*b	GND
22	GND	INTRQb	DMAK*b	NC	IORDYb	GND	GND
21	GND	DIOR*b	GND	DIOW*b	GND	DMARQb	GND
20	GND	PDIAG*b	GND	DD15b	DD0b	DD14b	GND
19	GND	DD1b	DD13b	DD2b	DD12b	DD3b	GND
18	GND	DD11b	DD4b	DD10b	DD5b	DD9b	GND
17	GND	DD6b	DD8b	DD7b	GND	DRESET*b	GND
16	GND	GND	ERX-	ERX+	ETX-	ETX+	GND
15	GND	EACT*	ELINK*	VCC	VCC	GND	GND
KEY							
11	GND	GND	GND	NC	GND	BLUE	GND
10	GND	GREEN	RED	VSYNC	HSYNC	DDCCLK	GND
9	GND	NC	DDCDAT	NC	GND	GND	GND
8	GND	SCD12*	SCD13*	SCD14*	SCD15*	SCDPH*	GND
7	GND	SCD0*	SCD1*	SCD2*	SCD3*	SCD4*	GND
6	GND	SCD5*	SCD6*	SCD7*	SCDPL*	GND	GND
5	GND	GND/NDET*	VCC(1)	VCC(1)	GND/WDET*	GND/SLED*	GND
4	GND	ATN*	GND	BSY*	ACK*	SRST*	GND
3	GND	MSG*	SEL*	C/D*	REQ*	I/O*	GND
2	GND	SCD8*	SCD9*	SCD10*	SCD11*	PBYPASS*	GND
1	GND	FAN3	FAN2	OPEN	SSDA	SSCL	GND

* - signal is active low

note(1): These two lines are current limited to approximately 0.75A via a positive temperature coefficient (PTC) resistor and are intended for use as SCSI terminator power.

J4 Signal Descriptions

General

VCC - 5v power

GND - to digital signal ground plane

NC - no connect

RESERVED - do not connect to

Misc. Signals, TTL levels

BTI* - LM78 pin 38 BTI# digital input (see National Semiconductor LM78 datasheet: http://www.national.com)

PBYPASS* - LM78 pin 16 PBYPASS# output

FAN[3:2] - LM78 fan tach inputs 3..2

OPEN* - latched input (use N.O. switch), reset by LM78 register, LM78 pin 15

SSDA - LM78 I2C serial data I/O

SSCL - LM78 I2C serial clock input

Ethernet, RS422 levels

ERX+/- - differential receive line pair (CPV5000 requires transformer to connect to network)

ETX+/- - differential transmit line pair (CPV5000 requires transformer to connect to network)

EACT* - Ethernet activity LED signal, TTL active low

ELINK* - Ethernet link LED signal, TTL active low

EIDEb (ATA-2), TTL levels

IOCS16*b - indicates a 16 bit register has been decoded

DMARQb - drive DMA request

DMAK*b - drive DMA acknowledge

DIOR*b - drive I/O read

DIOW*b - drive I/O write

DASP*b - drive active/slave present

IORDYb - indicates drive is ready for I/O cycle(s)

DD[15:0]b - drive data lines, bits 15-0

DRESET*b - drive reset signal

CS1FX*b - chip select drive 0, also command register block select

CS3FX*b - chip select drive 1, also command register block select

DA[2:0]b - drive register and data port address lines

INTRQb - drive interrupt request

PDIAG*b - passed diagnostics output from drive 1 and monitored by drive 0

SCSI, X3T10 SPI/single ended levels

ATN* - Attention

BSY* - Busy

C/D* - Command or Data

I/O* - Input or Output data direction

MSG* - Message phase

ACK* - Acknowledge

SCD[15:0]* - SCSI data lines

SCDPH* - SCSI parity high byte, provides parity for SCD[15:8]

SCDPL* - SCSI parity low byte, provides parity for SCD[7:0]

SEL* - Select

REQ* - Request

SRST* - SCSI bus reset

GND/NDET* - narrow detect, may be pulled low to indicate that bits[7:0] are connected (GND on CPV5000)

GND/WDET* - wide detect, may be pulled low to indicate that bits[15:8] are connected (GND on CPV5000)

GND/SLED* - SCSI active LED signal, TTL active low (GND on CPV5000)

VGA Video, VGA levels

BLUE - blue signal

HSYNC - horizontal sync

GREEN - green signal

RED - red signal

VSYNC - vertical sync

DDCDAT - VESA Display Data Channel data (I2C)

DDCCLK - VESA Display Data Channel clock (I2C)

Table 3-9. J5 connector pin assignments

Pin #	Row F	Row E	Row D	Row C	Row B	Row A	Row Z
22	GND	SPKR*OC	VCC	DIAG*OC	GND	PBRESET*	GND
21	GND	AUXCLK	AUXDAT	VCC (1)	KBDCLK	KBDDAT	GND
20	GND	SMBCLK	GND	SMBALERT*	SMDATA	VCC(1)	GND
19	GND	UDATA0-	UDATA0+	VCC(2)	GND	STB*	GND
18	GND	VCC(2)	GND	UDATA1-	UDATA1+	AFD*	GND
17	GND	PD0	ERR*	PD1	INIT*	PD2	GND
16	GND	SLIN*	PD3	PD4	PD5	PD6	GND
15	GND	PD7	ACK*	BUSY	PE	SLCT	GND
14	GND	DTRa	GND	RIa	CTSa	RTSa	GND
13	GND	TXDa	DSRa	RXDa	VCC	DCDa	GND
12	GND	DTRb	VCC	RIb	CTSb	RTSb	GND
11	GND	TXDb	DSRb	RXDb	GND	DCDb	GND
10	GND	DSKCHG*	HDSEL*	RDATA*	WPROT*	TR0*	GND
9	GND	WGATE*	WDATA*	STEP*	DIR*	MTR1*	GND
8	GND	DS0*	DS1*	MTR0*	INDEX*	DRVDENS1	GND
7	GND	DRVDENS0	DASP*	DA1	CS3FX*	CS1FX*	GND
6	GND	DA2	DA0	PDIAG*	GND	IOCS16*	GND
5	GND	DIOR*	DMACK*	DIOW*	IORDY	DMARQ	GND
4	GND	INTRQ	DD15	GND	DD0	DD14	GND
3	GND	DD1	DD13	DD2	DD12	DD3	GND
2	GND	DD11	DD4	DD10	DD5	DD9	GND
1	GND	DD6	DD8	DD7	DRESET*	RESET*	GND

* - signal is active low

Note(1): These two lines are current limited to approximately 0.75A via a positive temperature coefficient (PTC) resistor and are intended for use as keyboard and/or mouse power.

Note(2): These two lines are current limited to approximately 0.75A via a PTC resistor and are intended for use as USB device power.

J5 Signal Descriptions

General

VCC	5v power supply
GND	digital signal ground plane
NC	no connect
RESERVED	do not connect to

Miscellaneous Signals

SPKR*OC	PC/AT speaker output, open collector (may have pull-up on host card)
DIAG*OC	diagnostic/alarm output, open collector (may have pull-up on host card)
PBRESET*	push button system reset input (pulled up, filtered, and debounced on host card)
RESET*	system reset output, TTL totem-pole [on CPV5000, asserted only when 5V power is out of tolerance and upon manual reset (push-button) assertion]

Keyboard/Auxiliary Device, TTL levels

AUXCLK	clock for PS/2 auxiliary device (mouse)
AUXDAT	serial data line for PS/2 auxiliary device (mouse)
KBDCLK	clock for PC/AT or PS/2 keyboard
KBDDAT	serial data line for PC/AT or PS/2 keyboard

Universal Serial Bus (USB) (0 & 1), USB levels

UDATAn+	(+) signal of differential data pair for USB channel
UDATAn-	(-) signal of differential data pair for USB channel

Parallel LPT Port, TTL levels (some signals are redefined when used in EPP/ECP modes)

ACK*	pulsed by peripheral to acknowledge data sent
BUSY	indicates that the printer cannot accept more data
ERR*	peripheral detected an error
PD[7:0]	parallel data lines, bits 7-0
PE	paper end, indicates the printer is out of paper
AFD*	auto feed, causes printer to line feed
INIT*	initializes the printer
SLIN*	select in, selects the printer
STB*	data strobe, indicates data is valid
SLCT	select, peripheral indicates it is selected

Serial COM Ports (a & b), RS232 levels

CTS	clear to send
DCD	data carrier detected
DSR	data set ready
DTR	data terminal ready
RI	ring indicator
RTS	request to send
RXD	serial receive data
TXD	serial transmit data

Floppy Disk Drive, TTL levels

DSKCHG*	indicates the drive door has been opened
DIR*	controls direction of the head during step operations
DRVDENS[1:0]	drive density select
DS[1:0]*	drive address select

HDSEL*	selects top or bottom side head
INDEX*	indicates the beginning of a track
MTR[1:0]*	motor enables
RDATA*	read data
STEP*	step head in or out
TR0*	indicates that head is positioned above track 00
WDATA*	write data to drive
WGATE*	enables head write circuitry of drive
WPROT*	indicates a disk is write-protected

EIDEa (ATA-2), TTL levels

IOCS16*	indicates a 16 bit register has been decoded
DMARQ	drive DMA request
DMAK*	drive DMA acknowledge
DIOR*	drive I/O read
DIOW*	drive I/O write
DASP*	drive active/slave present
IORDY	indicates drive is ready for I/O cycle(s)
DD[15:0]	drive data lines, bits 15-0
DRESET*	reset signal to drive
CS1FX*	chip select drive 0, also command register block select
CS3FX*	chip select drive 1, also command register block select
DA[2:0]	drive register and data port address lines
INTRQ	drive interrupt request
PDIAG*	passed diagnostics output from drive 1 and monitored by drive 0

Parallel port connector

The parallel port is normally used for connecting a cable to a printer. This port is available as a 25-pin micro-D connector on the front panel of the CPV5000 front panel or as a 26-pin header and 25-pin standard D connector on the rear panel of the CPV5000 transition module. Signaling is IEEE 1284 compliant.

Table 3-10. Parallel connector pin assignments

Pin Number	Signal Mnemonic	Signal Description
1	STROBE-	Data at parallel port is valid
2	D0	Data bus (bit 0)
3	D1	Data bus (bit 1)
4	D2	Data bus (bit 2)
5	D3	Data bus (bit 3)
6	D4	Data bus (bit 4)
7	D5	Data bus (bit 5)
8	D6	Data bus (bit 6)
9	D7	Data bus (bit 7)
10	ACK-	Acknowledge data retrieval
11	BUSY	Printer cannot accept any more data
12	PE	Paper error
13	SELECT	Set high when selected
14	AFD-	Auto feed
15	ERR-	Error
16	INIT-	Initializes printer
17	SLIN-	Selects the printer
18	GND	Ground
19	GND	Ground
20	GND	Ground
21	GND	Ground
22	GND	Ground
23	GND	Ground
24	GND	Ground
25	GND	Ground

EIDE hard drive connectors

Up to four Enhanced Integrated Drive Electronics (EIDE) hard disk drives can be attached to the CPV5000.

Note The red stripe on the 40-pin EIDE ribbon cable should be near pins 1 and 2 on the 40-pin connector. The CPV5000 and EIDE hard drive(s) will not work correctly if the cable is plugged in backwards. EIDE cables should be no more than 18 inches (46 cm) long.

Table 3-11. EIDE connector pin assignments

Pin Number	Signal Mnemonic	Signal Description	Pin Number	Signal Mnemonic	Signal Description
1	RESET-	Reset signal to drive	23	IOW-	Drive I/O write
2	GND	Ground	24	GND	Ground
3	DD7	Data Bus Bit 7	25	IOR-	Drive I/O read
4	DD8	Data Bus Bit 8	26	GND	Ground
5	DD6	Data Bus Bit 6	27	IORDY	IDE I/O channel ready
6	DD9	Data Bus Bit 9	28	NC	Not connected
7	DD5	Data Bus Bit 5	29	DMACK-	Drive DMA acknowledge
8	DD10	Data Bus Bit 10	30	GND	Ground
9	DD4	Data Bus Bit 4	31	IRQ	
10	DD11	Data Bus Bit 11	32	IOCS16-	16 bit register has been decoded
11	DD3	Data Bus Bit 3	33	DA1	Address bus bit 1
12	DD12	Data Bus Bit 12	34	PDIAG-	Output from drive 1 & monitored by drive 0
13	DD2	Data Bus Bit 2	35	DA0	Address bus bit 0
14	DD13	Data Bus Bit 13	36	DA2	Address bus bit 2
15	DD1	Data Bus Bit 1	37	CS1-	Chip select drive 0, also command register block select

Table 3-11. EIDE connector pin assignments (Continued)

Pin Number	Signal Mnemonic	Signal Description	Pin Number	Signal Mnemonic	Signal Description
16	DD14	Data Bus Bit 14	38	CS3-	Chip select drive 1, also command register block select
17	DD0	Data Bus Bit 0	39	DASP-	Drive active/slave present
18	DD15	Data Bus Bit 15	40	GND	Ground
19	GND	Ground	41	+5V	
20	NC	Not connected	42	+5V	
21	DMARQ	Drive DMA request	43	GND	Ground
22	GND	Ground	44	NC	Not connected

Floppy connector

One diskette drive can be attached to the CPV5000 via the 26-pin header (J20) for on-board mounting. Alternatively, two diskette drives can be remotely attached to the CPV5000 via the 34-pin header on the transition module. Note that the floppy disk drive controller cable should be no more than three feet (91 cm) long.

The floppy disk drives may be any combination of 360 KB and 1.2 MB 5.25 inch drives or 720 KB, 1.44 MB, and 2.88 MB 3.5 inch drives. Both drives should be jumper-configured as drive one.

Table 3-12. Floppy connector pin assignments

Pin Number	Signal Mnemonic	Signal Description
1	+5V	Drive power
2	INDEX-	Beginning of a track
3	+5V	Drive power
4	DSO-	Drive select 0
5	+5V	Drive power
6	DSKCHG-	Notifies disk controller the drive door has opened
7	NC	Not connected
8	NC	Not connected
9	NC	Not connected
10	MTR0-	Motor enable outputs
11	NC	Not connected
12	DIR	Controls direction of FDD head during seek operations
13	NC	Not connected
14	STEP-	Supplies step pulses to move head during seek operations
15	GND	Ground
16	WDATA-	Writes serial data to disk drive
17	GND	Ground
18	WGATE-	Enables head of disk drive to write to disk
19	GND	Ground

Table 3-12. Floppy connector pin assignments (Continued)

Pin Number	Signal Mnemonic	Signal Description
20	TR0-	Indicates head of FDD is at track 0
21	GND	Ground
22	WPROT-	Indicates a disk is write-protected
23	GND	Ground
24	RDATA-	Raw red data from disk drive
25	GND	Ground
26	HDSEL-	Determines the side of floppy disk being accessed

PS/2 keyboard/mouse connector

The PS/2 connector is a 6-pin connector mounted on the end bracket of the CPV5000. The PS/2 Y adapter cable supplied attaches to this connector. The CPV5000 transition module has two connectors for the keyboard and mouse.

Note Power present on the J15 connector is only for use by a keyboard/pointing device.

Table 3-13. Keyboard/mouse connector pin assignments

Pin Number	Signal Mnemonic	Signal Description
1	KBDDAT	Data line for keyboard
2	MDAT	Data line for mouse
3	GND	Ground
4	KBDVCC	Keyboard power (current limited to .75 Amp
5	KBDCLK	Clock for keyboard
6	MCLK	Clock for mouse
7	GND	Common ground

Serial ports COM1 and COM2 connectors

Serial ports allow you to connect serial devices (a serial mouse, serial printers) to the CPV5000 via appropriate serial cables.

COM1 and COM2 are 9-pin micro-D connectors located on the CPV5000 front panel and regular D connectors on the transition module.

Table 3-14. COM1 and COM2 pin assignments

Pin Number	Signal Mnemonic	Signal Description
1	DCD-	Data Carrier Detect
2	RX	Receive Data
3	TX	Transmit Data
4	DTR-	Data Terminal Ready
5	GND	Signal Ground
6	DSR-	Data Set Ready
7	RTS-	Request to Send
8	CTS-	Clear to Send
9	RI-	Ring Indicator

Fan power connector

Table 3-15. Fan power pin assignments

Pin Number	Signal
1	+5V
2	Tach
3	Ground
4	+12V

USB ports 1 and 2

USB ports 1 and 2 are available through the CPV5000's front panel or the transition module's rear panel.

Table 3-16. USB ports pin assignments

Pin Number	Signal Mnemonic	Signal Description
1	+5V	Current limited USB power
2	DATA-	USB serial communications differential pair
3	DATA+	
4	Ground	USB port common

Ethernet connector

An Ethernet RJ45 connector is available through the CPV5000's front panel or the transition module's rear panel.

Table 3-17. Ethernet connector pin assignments

Pin Number	Signal Mnemonic	Signal Description
1	TX+	Transmit data
2	TX-	Transmit data return
3	RX+	Receive data
4,	NC	Not connected
5	NC	Not connected
6	RX-	Receive data
7	NC	Not connected
8	NC	Not connected

SCSI connector

A SCSI connector is available through the CPV5000's front panel or the transition module's rear panel. For information on SCSI termination, see Ultra SCSI controller, page 4-11.

Table 3-18. 68-pin SCSI-3 connector pin assignments

Pin Number	Signal Mnemonic	Signal Name	Pin Number	Signal Mnemonic	Signal Description
1	GND	Ground	35	D12-	SCSI data bus (bit 12)
2	GND	Ground	36	D13-	SCSI data bus (bit 13)
3	GND	Ground	37	D14-	SCSI data bus (bit 14)
4	GND	Ground	38	D15-	SCSI data bus (bit 15)
5	GND	Ground	39	DPH-	SCSI data parity
6	GND	Ground	40	D0	SCSI data bus (bit 0)
7	GND	Ground	41	D1	SCSI data bus (bit 1)
8	GND	Ground	42	D2	SCSI data bus (bit 2)
9	GND	Ground	43	D3	SCSI data bus (bit 3)
10	GND	Ground	44	D4	SCSI data bus (bit 4)
11	GND	Ground	45	D5	SCSI data bus (bit 5)
12	GND	Ground	46	D6	SCSI data bus (bit 6)
13	GND	Ground	47	D7	SCSI data bus (bit 7)
14	GND	Ground	48	DPL-	SCSI data parity
15	GND	Ground	49	GND	Ground
16	GND	Ground	50	GND	Ground
17	TERMPWR	Terminator power	51	TERMPWR	Terminator power
18	TERMPWR	Terminator power	52	TERMPWR	Terminator power
19	NC	Not connected	53	NC	Not connected
20	GND	Ground	54	GND	Ground
21	GND	Ground	55	ATN-	Attention
22	GND	Ground	56	GND	Ground
23	GND	Ground	57	BUSY-	Busy
24	GND	Ground	58	ACK-	Acknowledge
25	GND	Ground	59	RESET-	SCSI reset
26	GND	Ground	60	MSG-	Message
27	GND	Ground	61	SEL-	Select

Table 3-18. 68-pin SCSI-3 connector pin assignments (Continued)

Pin Number	Signal Mnemonic	Signal Name	Pin Number	Signal Mnemonic	Signal Description
28	GND	Ground	62	CD-	Command/data
29	GND	Ground	63	REQ-	Request
30	GND	Ground	64	IO-	Input/output
31	GND	Ground	65	D8	SCSI data bus (bit 8)
32	GND	Ground	66	D9	SCSI data bus (bit 9)
33	GND	Ground	67	D10	SCSI data bus (bit 10)
34	GND	Ground	68	D11	SCSI data bus (bit 11)

Video connector

Table 3-19. Video connector pin assignments

Pin Number	Signal Mnemonic	Signal Description
1	RED	Red signal
2	GREEN	Green signal
3	BLUE	Blue signal
4	NC	Not connected
5	DACVSS	Video return
6	DACVSS	Video return
7	DACVSS	Video return
8	DACVSS	Video return
9	NC	Not connected
10	DACVSS	Video return
11	NC	Not connected
12	DDCDAT	Display data channel data signal for DDC2 support
13	HSYNC	Horizontal synchronization
14	VSYNC	Vertical synchronization
15	DDCCLK	Display data channel clock signal for DDC2 support

Reset switch

Table 3-20. Reset switch pin assignments

Pin Number	Signal Mnemonic
1	Ground
2	FR RSET-

Functional Description 4

The CPV5000 is designed to operate with a Pentium or a K-6 microprocessor. It supports both read and write burst mode bus cycles and includes an on-chip 16 KB cache that is split into 8 KB code and data caches employing a write-back policy.

Peripheral component interconnect (PCI) local bus

The PCI local bus is a high-performance, 32-bit bus with multiplexed address and data lines. It is intended for use as an interconnect mechanism between highly-integrated peripheral controller components, peripheral add-in boards, and processor/memory systems.

The CPV5000 supports a 32-bit PCI interface on the physical CompactPCI connector. On-board devices connect directly to the primary bus. Off-board access is supported through the DEC 21150 PCI-PCI bridge. The PCI interface has a read or write bandwidth of at least 120Mbytes per second.

PCI device mapping and routing

Table 4-1 lists all PCI components with ID codes.

Table 4-1. PCI components

Device Name	Manufacturer	Part #	Device ID	Vendor ID	BIOS Extension
Host Bridge TXC	Intel	82439HX	0x1250	0x8086	N/A
ISA Bridge PIIX3	Intel	82371	0x7000	0x8086	N/A
Ethernet	Intel	82557	0x1229	0x8086	No
SVGA Video	Cirrus Logic	CL-GD5446	0x00B8	0x1013	Yes
SCSI*	Adaptec	AIC 7880	0x8078	0x9004	Yes
Bridge 1	Digital	21150	0x0022	0x1011	N/A

*Disable in BIOS setup

PCI routing table

Table 4-2 shows PCI interrupt routing.

Table 4-2. PCI interrupt routing

Description	Bus #	IDSel	Device #	Req/Gnt	INTA	INTB	INTC	INTD
Host Bridge	0	-	0x00	N/A	---			
PIIX3	0	AD18	0x07	PHOLD	---			
Ethernet	0	AD31	0x14	0	PIRQB			
Video	0	AD30	0x13	-	PIRQC			
Bridge 1	0	AD29	0x12	1	---			
SCSI	0	AD28	0x11	2	PIRQD			
Slot 1	1	AD31	0x0F	1-0	PIRQD	PIRQA	PIRQB	PIRQC
Slot 2	1	AD30	0x0E	1-1	PIRQC	PIRQD	PIRQA	PIRQB
Slot 3	1	AD29	0x0D	1-2	PIRQB	PIRQC	PIRQD	PIRQA
Slot 4	1	AD28	0x0C	1-3	PIRQA	PIRQB	PIRQC	PIRQD
Slot 5	1	AD27	0x0B	1-4	PIRQD	PIRQA	PIRQB	PIRQC
Slot 6	1	AD26	0x0A	1-5	PIRQC	PIRQD	PIRQA	PIRQB
Slot 7	1	AD25	0x09	1-6	PIRQB	PIRQC	PIRQD	PIRQA

Applications

The PCI local bus provides an industry standard, high-performance local bus architecture. The processor/cache/memory subsystem is connected to PCI through a PCI bridge. This bridge provides a low latency path through which the processor directly accesses PCI devices mapped anywhere in the memory or I/O address spaces. It also provides a high-bandwidth path allowing PCI masters direct access to main memory.

Watchdog timer

The watchdog timer supports four modes of operation:

- Disabled

- Set a flag in a register in ISA I/O memory map
- Item 2 + Assert a selectable ISA interrupt
- Item 2 + Assert NMI followed by a system reset.

The watchdog timer is programmable via registers in the ISA I/O memory map. The watchdog timer is protected from being accidentally enabled. The timer supports a range of count down time-outs from 18 milliseconds to 291 seconds.

I/O address map

PCI system memory and I/O are configured or enumerated dynamically each time the system boots or by an operating system (Plug and Play), but there are legacy I/O locations that remain constant.

Table 4-3 shows I/O addressing. Functions listed with (opt) are not normally occupied by on-board resources. BIOS Setup or special utilities may be used to enable or relocate these features from their default values.

Table 4-3. I/O addresses

Address	Function
0000-000F	DMA controller 1
0020-0021	Interrupt controller 1
0040-0043	Counter timer
0060-0064	Keyboard, NMI, speaker
0070-0071	Real time clock/NMI mask
0050-0057[1]	LM78 System monitor (opt)
0058-005F[1]	WatchDog timer, ENUM (opt)
0080-009F	DMA page register, POST checkpoint
00A0-00BF	Interrupt controller 2
00C0-00DF	DMA controller 2
00F0	Reset coprocessor
0170-0177[2]	Secondary IDE channel (opt)
01F0-01F7[2]	Primary IDE channel
0278-027F[3]	Parallel port 2 (opt)
02E8-02EF[3]	Serial port 4 (opt)
02F8-02FF[2]	Serial port 2 (default)
0376-0377[2]	Secondary IDE port (opt)
0378-037F[2]	Parallel port 1 (default)
03BC-03C3[3]	Parallel port 3 (opt)
03E8-03EF[3]	Serial port 3 (opt)
03F0-03F5	Floppy channel
03F6-03F7	Primary IDE and floppy
03F8-03FF[2]	Serial port 1 (default)
040A-043F	DMA scatter/gather
0480-048F	DMA high pages
04D0-04D1	Edge/level interrupts
04D6	DMA2 extended mode

Table 4-3. I/O addresses (Continued)

Address	Function
0678-067A[3]	Parallel port 2 (opt)
0778-077A[3]	Parallel port 1 (opt)
07BC-07BE[3]	Parallel port 3 (opt)
0CF8-0Cff	PCI configuration

1. The WatchDog timer and LM78 are normally disabled but may be relocated and enabled *via* PCI configuration.
2. These ports are available if the listed function is not enabled in the BIOS.
3. This is an alternate range that may be selected in the BIOS setup.

Memory address mapping

PCI system memory and I/O are configured or enumerated dynamically each time the system boots or by an operating system (Plug and Play), but there are legacy memory locations that remain constant.

Refer to Table 4-4 for memory address information.

Table 4-4. Memory address

Address Range	Function
000000H-09FFFFH	640 KB conventional RAM
0A0000H-0BFFFFH	VGA DRAM (typically on the PCI backplane)
0C0000H-0C7FFFH	VGA ROM (typically on the PCI backplane)
0C8000H-0DFFFH	Expansion ROM
0E0000H-0EFFFFH	System BIOS extensions
0F0000H-0FFFFFH	AMI system BIOS

Video controller

The on board video is enabled or disabled dependent on whether or not a CPCI bus video adapter module is installed. This enables the user to upgrade video simply by installing a new module.

- No external video installed: on board video enabled
- External video installed: on board video disabled

The CPV5000 has a Cirrus Logic 64-bit VisualMedia Accelerator chip. Table 4-5 and Table 4-6 list the chip's video modes.

Table 4-5. Standard video modes

Mode#	VESA Mode #	# of Colors	Char. xRow	Char. Cell	Pixels	Display Mode	Pixel Freq. MHz	Horiz. Freq kHz	Vert. Freq. Hz
00/01	-	16/256	40x25	9x16	360x400	Text	14	31.5	70
02/03	-	16/256	80x25	9x16	720x400	Text	28	31.5	70
04/05	-	4/256	40x25	8x8	320x200	Graphics	12.5	31.5	70
6	-	2/256	80x25	8x8	640x200	Graphics	25	31.5	70
7	-	mono	80x25	9x16	720x400	Text	28	31.5	70
0D	-	16/256	40x25	8x8	320x200	Graphics	12.5	31.5	70
0E	-	16/256	80x25	8x8	640x200	Graphics	25	31.5	70
0F	-	mono	80x25	8x14	640x350	Graphics	25	31.5	70
10	-	16/256	80x25	8x14	640x350	Graphics	25	31.5	70
11	-	2/256	80x30	8x16	640x480	Graphics	25	31.5	60
11+	-	2/256	80x30	8x16	640x480	Graphics	31.5	37.9	72
11+	-	2/256	80x30	8x16	640x480	Graphics	31.5	37.9	75
12	-	16/256	80x30	8x16	640x480	Graphics	25	31.5	60
12+	-	16/256	80x30	8x16	640x480	Graphics	31.5	37.9	72
12+	-	16/256	80x30	8x16	640x480	Graphics	31.5	37.5	75
13	-	256/256	40x25	8x8	320x200	Graphics	12.5	31.5	70

Table 4-6. Extended video modes

Mode#	VESA Mode #	# of Colors	Char. xRow	Char. Cell	Screen Format	Display Mode	Dot Clock MHz	Horiz. Freq kHz	Vert. Freq. Hz
14	-	16/256K	132x25	8x16	1056x400	Text	41.5	31.5	70
54	10A	16/256K	132x43	8x8	1056x350	Text	41.5	31.5	70
55[7]	109	16/256K	132x25	8x14	1056x350	Text	41.5	31.5	70
58, 6A	102	16/256K	100x37	8x16	800x600	Graphics	36	35.2	56
58, 6A	102	16/256K	100x37	8x16	800x600	Graphics	40	37.8	60
58, 6A	102	16/256K	100x37	8x16	800x600	Graphics	50	48.1	72
58, 6A	102	16/256K	100x37	8x16	800x600	Graphics	49.5	46.9	75
5C	103	256/256K	100x37	8x16	800x600	Graphics	36	35.2	56
5C	103	256/256K	100x37	8x16	800x600	Graphics	40	37.9	60
5C	103	256/256K	100x37	8x16	800x600	Graphics	50	48.1	72
5C	103	256/256K	100x37	8x16	800x600	Graphics	49.5	46.9	75
5Di	104	16/256K	128x48	8x16	1024x768	Graphics	44.9	35.5	43[4]
5D	104	16/256K	128x48	8x16	1024x768	Graphics	65	48.3	60
5D	104	16/256K	128x48	8x16	1024x768	Graphics	75	56	70
5D	104	16/256K	128x48	8x16	1024x768	Graphics	77	58	72
5D	104	16/256K	128x48	8x16	1024x768	Graphics	78.7	60	75
5E	100	256/256K	80x25	8x16	640x400	Graphics	25	31.5	70
5F	101	256/256K	80x30	8x16	640x480	Graphics	25	31.5	60
5F	101	256/256K	80x30	8x16	640x480	Graphics	31.5	37.9	72
5F	101	256/256K	80x30	8x16	640x480	Graphics	31.5	37.5	75
60i	105	256/256K	128x48	8x16	1024x768	Graphics	44.9	35.5	43[4]
60	105	256/256K	128x48	8x16	1024x768	Graphics	65	48.3	60
60	105	256/256K	128x48	8x16	1024x768	Graphics	75	56	70
60	105	256/256K	128x48	8x16	1024x768	Graphics	77	58	72
60	105	256/256K	128x48	8x16	1024x768	Graphics	78.7	60	75
64	111	64K	-	-	640x480	Graphics	25	31.5	60
64	111	64K	-	-	640x480	Graphics	31.5	37.9	72
65[3]	114	64K	-	-	800x600	Graphics	31.5	37.5	75
65[3]	114	64K	-	-	800x600	Graphics	40	37.8	60
65[3]	114	64K	-	-	800x600	Graphics	50	48.1	72
65[3]	114	64K	-	-	800x600	Graphics	49.5	46.9	75
66	110	32K[3]	-	-	640x480	Graphics	25	31.5	60
66	110	32K[3]	-	-	640x480	Graphics	31.5	37.9	72

Table 4-6. Extended video modes (Continued)

Mode#	VESA Mode #	# of Colors	Char. xRow	Char. Cell	Screen Format	Display Mode	Dot Clock MHz	Horiz. Freq kHz	Vert. Freq. Hz
66	110	32K[3]	-	-	640x480	Graphics	31.5	37.5	75
67	113	32K[3]	-	-	800x600	Graphics	36	35.2	56
67	113	32K[3]	-	-	800x600	Graphics	40	37.8	60
67	113	32K[3]	-	-	800x600	Graphics	50	48.1	72
67	113	32K[3]	-	-	800x600	Graphics	49.5	46.9	75
68i	116	32K[3]	-	-	1024x768	Graphics	44.9	35.5	43[4]
68	116	32K[3]	-	-	1024x768	Graphics	65	48.3	60
68	116	32K[3]	-	-	1024x768	Graphics	75	56	70
68	116	32K[3]	-	-	1024x768	Graphics	78.7	60	75
69i	-	32K[3]	-	-	1280x1024	Graphics	75	48	43[4,8]
6Ci	106	16/256K	160x64	8x16	1280x1024	Graphics	75	48	43[4,8]
6Di	107	256/256K	160x64	8x16	1280x1024	Graphics	75	48	43[4,8]
6D	107	256/256K	160x64	8x16	1280x1024	Graphics	108	65	60[8]
6D	107	256/256K	160x64	8x16	1280x1024	Graphics	126	76	71.2
6D	107	256/256K	160x64	8x16	1280x1024	Graphics	135	80	75
71	112	16M	-	-	640x480	Graphics	25	31.5	60
72	-	16M+A[5]	-	-	800x600	Graphics	36	35.2	56
72	-	16M+A[5]	-	-	800x600	Graphics	40	37.8	60
74i	117	64K	-	-	1024x768	Graphics	44.9	35.5	43[4]
74	117	64K	-	-	1024x768	Graphics	65	48.3	60
74	117	64K	-	-	1024x768	Graphics	75	56	70
74	117	64K	-	-	1024x768	Graphics	78.7	60	75
76	-	16M+A[5]	-	-	640x480	Graphics	25	31.5	60
76	-	16M+A[5]	-	-	640x480	Graphics	31.5	37.9	72
76	-	16M+A[5]	-	-	640x480	Graphics	31.5	37.5	75

[1] Some modes are not supported by all the CL-GD543X controllers.

[2] Some modes are not supported by all monitors. The best quality refresh rate for the monitor type selected will automatically be used.

[3] 32K direct color/256 color mixed mode

[4] A character “i” stands for interlaced mode, 43.5 Hz or 87 Hz interlaced.

[5] 16M colors, but with a 32 bit-per-pixel format, 16M+A indicates the same.

[6] Implementations using CL-GD5434 restrict 1024x768 at 72 Hz refresh. In those implementations, 70 Hz refresh will be substituted. For a higher refresh rate select 75 Hz.

[7] Mode 55 will use a 16 dot high font, with the bottom two lines truncated, in the absence of the 8x14 font TSR (TSRFONT). The characters “g,” “j,” “p,” “q,” “y,” and “Ø” are truncated using a middle and bottom line algorithm to avoid truncation of descenders. For compatibility with some DOS applications which use the 8x14 font, the TSRFONT utility should be used.

[8] VESA has recently proposed a new specification for 43 Hz interlaced, and 60 Hz timing for 1280x1024 resolution modes. Cirrus Logic currently uses timings for these modes that differ from those proposed by VESA.

Ultra SCSI controller

The Adaptec 7880 chip is used for on-board support for Ultra SCSI. The user can enable or disable this feature through the BIOS Setup screen. Connection to the SCSI device is available on the front panel and the rear I/O transition module via a 68-pin, high-density connector.

The Ultra SCSI circuitry provides for automatic termination when a device is plugged into the rear or front. Devices can be connected to the rear, the front, or both at the same time. Ground pins on the SCSI connector are reassigned to act as cable or device detects. Two ground pins are used to distinguish between 16-bit or 8-bit devices. The active terminator used is a Dallas Semiconductor DS2105Z. This part has a power down pin (PD-) that disconnects the termination from the bus when driven low. This pin has an internal pull up resistor.

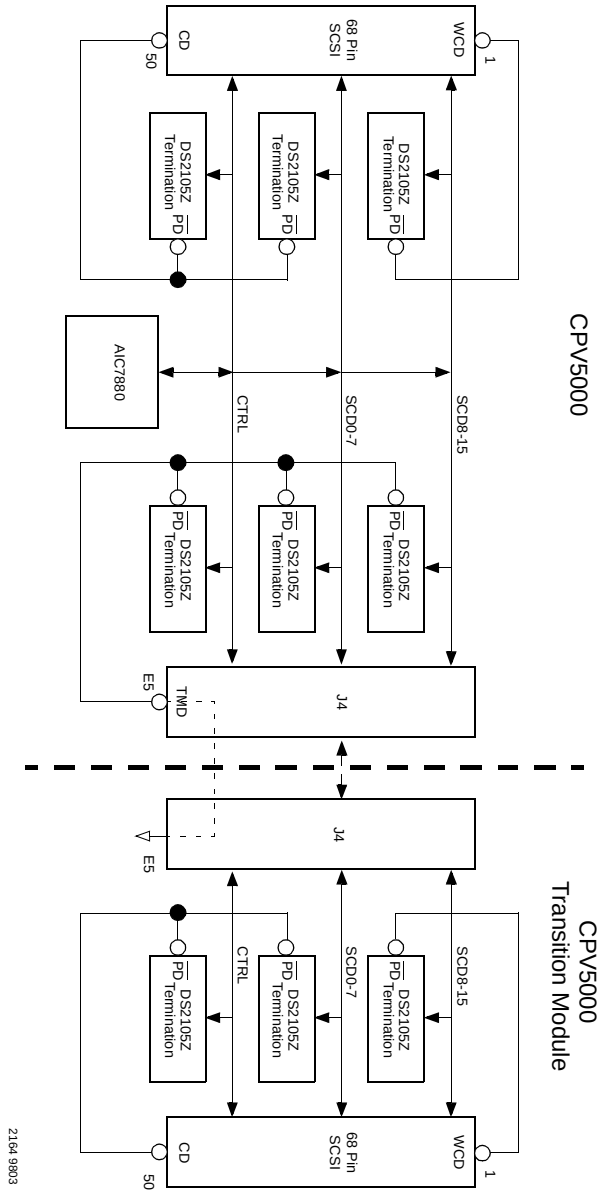


Figure 4-1. SCSI termination

Figure 4-1 shows the termination scheme. When a CPV5000 board is installed into a system with no rear I/O, the terminators next to J4 are active. This provides termination at the end of the SCSI bus right at J4. If a non-wide device is plugged into the CPV5000's 68-pin connector, pin 50 will become grounded. This will cause the terminators for the CTRL and SCD0-7 signals to be turned off. The last device on the cable provides termination for these signals.

If a wide device is plugged into the CPV5000's 68-pin connector, pin 1 will be grounded, and all three terminators will be turned off. In this case, a wide device must be connected at the end of the cable.

If a rear I/O transition module is plugged in, pin E5 will be grounded. This will disable the CPV5000's terminators next to J4 since the end of the SCSI bus will be at the 68-pin connector on the rear I/O board. If a non-wide device is plugged into the rear I/O's 68-pin connector, pin 50 will become grounded. This will cause the terminators for the CTRL and SCD0-7 signals to be turned off. The last device on the cable provides termination for these signals.

If a wide device is plugged into the rear I/O's 68-pin connector, pin 1 will be grounded, and all three terminators will be turned off. In this case, a wide device must be connected at the end of the cable. If a 68-pin to 50-pin SCSI adapter is used it must have straight through connections with no pins hooked together.

EIDE interface

The EIDE interface supports primary and secondary both interfaced via the rear I/O transition module. The primary EIDE channel is available for the connection of on-board devices through an on-board height density connector. The IDE interface supports ATAPI modes 0 to 4.

Each IDE interface supports two IDE devices (master and slave). The IDE interface supports disk drives up to 8.2Gbytes and CD-ROM drives.

Note If the on-board IDE hard drive is used, it will be connected to the primary IDE port. If this is the case, only one drive can be connected to the primary rear I/O EIDE port, and the drive must be jumpered different (master or slave) than the on-board drive.

Table 4-7 shows all possible on-board drive options.

Table 4-7. On-board drive options

Drive option 1	Drive option 2
Floppy	Not installed
IDE hard drive	Not installed
IDE flash drive	Not installed
Floppy	IDE hard drive
Floppy	IDE flash drive
IDE flash drive	IDE hard drive

Floppy interface

The floppy interface supports up to two floppy drives. The supported floppy drives include:

- 5.25 inch - 360Kb, 1.2MB
- 3.5 inch - 720KB, 1.44MB

The floppy interface connector consists of a 34(2x17) pin shrouded header available on the rear I/O transition module, or a flex cable connector for on-board drive mounting.

Note The rear I/O connected floppy and the on-board floppy connection are mutually exclusive. You cannot use both at the same time.

Parallel port

The parallel port supports ECP, EPP modes of operation.

The parallel interface connector is a 25-pin D-connector header available on the rear I/O transition module, or a 25-pin micro-D connector on the front panel.

Serial ports

The CPV5000 supports two serial ports. The ports support 16550 operation. The serial interface connector is a 9-pin D style connector available on the rear I/O transition module, or 9-pin micro-D connectors available on the front panel. The serial ports are ESD protected to 15KV.

USB

The CPV5000 supports two USB ports with transfer capability from 1.2Mbits/second to 12Mbits/second.

Both ports are supported by two USB connectors on the front panel and the rear I/O transition module. USB signals can be routed to the front or rear I/O connectors using a four-position jumper block. USB can be enabled or disabled in the BIOS setup.

- Jumper installed - rear connection
- Jumper removed - front connection

Keyboard/mouse interface

The keyboard and mouse is supported by a single PS/2 connector on the front panel and separate PS/2 style connectors on the rear I/O transition module. The front I/O keyboard/mouse connector utilizes a standard splitter cable to connect to a mouse and keyboard.

Ethernet

The Intel 82558 chip is used for on-board support for 10/100MB Ethernet. The user can enable or disable this feature through the BIOS Setup screen. Ethernet connection is available on the front panel or rear I/O transition module via a RJ45 connector. Front or rear connections are selectable using a four position jumper block. Both link and activity LED's are incorporated into the connector in order to indicate network status.

DMA channels

Table 4-8. DMA channels

Channel	Function
DMA 0	ISA memory refresh
DMA 1	Reserved
DMA 2	Floppy disk controller
DMA 3	Reserved
DMA 4	Cascade for DMA 1
DMA 5	Reserved
DMA6	Reserved
DMA 7	Reserved

Interrupts

Table 4-9. Interrupts

Channel	Function
NMI	Reports parity / System errors
SMI	System management
0	System timer
1	Keyboard
2	Cascade for IRQ 8-15
3	COM 2/serial port 2
4	COM 1/serial port 1
5	Parallel port 2
6	Floppy controller
7	Parallel port 1
8	Real time clock
9	Software redirect to IRQ2
10	Reserved
11	Reserved / special features
12	Reserved / PS/2 mouse
13	Coprocessor
14	Hard disk controller
15	Reserved

FPGA Access, Watchdog and ENUM registers

The LM78 and the FPGA's watchdog timer is addressed through the Programmable Chip Select in the South Bridge. The PCS is set to a default address of 0050h by the BIOS. This can be changed at any time by an application program if this becomes a conflict. In most cases, the application program will read the PCS register to determine the base address.

To read the PCR register, do a configuration read from the PIIX3 South Bridge Device 07h, Function 00h, register 78h and 79h.

The watchdog timer and ENUM registers are accessed via three I/O offsets: 0Bh, 0Dh, and 0Fh. The LM78 is accessed through port offsets 00h to 07h. The following sections describe the function of these registers.

Port offset 0Bh: board status and watchdog strobe

An ISA write to I/O offset 0Bh will reset the watchdog timer to the value of the watchdog delay programmed into the watchdog register.

Table 4-10. I/O offset 0Bh (write)

Bit	7	6	5	4	3	2	1	0
Function	Do not care							

Table 4-11. I/O offset 0Bh (read)

Bit	7	6	5	4	3	2	1	0
Function	Hardware version number				Reserved	Watchdog flag	Reserved	Reserved

Bit 2, the watchdog flag bit, is set by the watchdog Timer when the timer reaches zero. This can only be reset by clearing the watchdog timer via the watchdog register.

I/O port offset 0Dh: FPGA register index port

A Field Programmable Gate Array (FPGA) on the CPV5000 contains the watchdog timer and miscellaneous registers. The value written to the index port selects which FPGA register is accessible from port offset 00Fh. Index-0 is selected at reset and is selected after any output to the FPGA data port offset 0Fh. This last feature helps to protect registers that control important board operations.

Table 4-12. FPGA register index port

Bit	7	6	5	4	3	2	1	0
Function	Not used					FPGA register index		

Table 4-13. FPGA register index

Index bits 2-0	Index Function
0000	Reserved
0001	Reserved
0010	Reserved
0011	Watchdog index
0100	Reserved
0101	Reserved
0110	Reserved
0111	Reserved
1000	Reserved
1001	Reserved
1010	Reserved
1011	ENUM status/control
1110	ENUM storage

I/O port offset 0Fh: FPGA register data port

All communication of data from the CPV5000 is implemented through the FPGA register data port. The function of each bit is dependent on the data in the I/O port offset 0Dh: FPGA register index port.

Table 4-14. FPGA register data port

Bit	7	6	5	4	3	2	1	0
Function	Data from or to the selected FPGA register							

Watchdog register: FPGA index - 03h

The watchdog timer is designed to be used in critical control applications. The function of the watchdog is to stop a program or part of the hardware from going into a runaway or locked out mode.

Watchdog index mode

When the timer is enabled, the watchdog strobe register must be written to at regular intervals to stop the watchdog from triggering. The exact data that is written is irrelevant. It is the write operation to the register that resets the watchdog timer.

The watchdog has four modes when triggered:

1. Disabled
2. Set the WD bit in the watchdog strobe register (073h)
3. Item 2 + Assert IOCHK
4. Item 3 + Reset the CPV5000.

The watchdog is enabled by writing 03h to ISA I/O offset 00Dh (Index), then writing data to the control register at ISA I/O offset 00Fh.

Each time data is written to or read from ISA I/O offset 00Fh, this must be preceded by a write of 03h to ISA I/O offset 0Dh. This is to prevent accidental use of the watchdog timer. The index register is always reset to 00h after a read or write to I/O offset 00Fh.

The strobe register is at I/O offset 00Bh. A write to ISA I/O offset 00Bh will reset the watchdog timer to the delay value in the watchdog register. The status of the WD (watchdog) bit is read at ISA I/O offset 00Bh.

Table 4-15. Watchdog register

Bit	7	6	5	4	3	2	1	0
Function	Clear watchdog	Reserved		Watchdog mode		Watchdog delay mode		

Bit 7 - clear watchdog bit

This bit at logic 1 will clear the watchdog timer function. This bit has to be written with a 0 to start the watchdog timer. When the watchdog flag in the I/O Port offset 0Bh (Read) is set, the flag can only be reset by a write of a 1 to this register.

Bits 4-3 watchdog mode

These two bits control the mode of the watchdog timer.

Table 4-16. Watchdog mode

Data	Mode
00	Disable the watchdog timer
01	Set the watchdog flag when timer counts to zeroes
10	Set the watchdog flag and assert IOCHRDY when the timer counts to zeroes
11	Set the watchdog flag and assert IOCHRDY and RESET the CPV5000 when the timer counts to zeroes

Bits 2-0 watchdog timer delay

Bits 2 to 0 control the delay of the watchdog timer until the function bits 4 to 3 are activated.

Table 4-17. Watchdog timer delay

Data	Watchdog count down delay
000	17.8 milliseconds
001	71.1 milliseconds
010	284 milliseconds
011	1.14 seconds
100	4.55 seconds
101	18.22 seconds
110	72.8 seconds
111	291 seconds

ENUM status and control register: FPGA index - 11h

The ENUM status and control register is used to get the status of the ENUM- line for hot swap enabled systems. This register is used to check the level of the ENUM- line to check the source of the interrupt.

ENUM status and control

The level of the ENUM- line can be read at bit 0 of this register. Bits 1, 2, and 3 are read/write and can be used to store control bits. The control bits are not defined for any particular purpose at this time.

Table 4-18. Register data port when I/O port 75h: FPGA register index port - 01h

Bit	7	6	5	4	3	2	1	0
Function	Reserved				Control bits			ENUM-

ENUM storage register: FPGA index - 12h

The ENUM storage register is used to store a byte of information for hot swap enabled systems.

A byte of information can be stored and read back at this location.

Table 4-19. ENUM Storage

Bit	7	6	5	4	3	2	1	0
Function	Read/write byte storage							

Installing Options 5

System memory configurations

The CPV5000 provides four 72-pin SIMM sites for memory expansion, organized as two memory banks. Each bank consists of two sockets providing a 64-bit wide data path and eight parity bits. Memory timing requires 60 ns or 70 ns fast page mode devices.

The CPV5000 supports up to 256 MB of on-board FPM memory or up to 256 MB of on-board EDO memory in various configurations. EDO memory is often used for improved performance with or without secondary cache. EDO memory is available in a x32 SIMM and is non-parity. EDO and FPM cannot be combined in the same bank. The BIOS automatically detects the memory size and type.

With FPM memory, parity generation/checking is provided for each byte. Additionally, the chip set provides single bit Error Checking and Correction (ECC) and double bit detection.

Five SIMM sizes: 1 MB, 2 MB, 4 MB, 8 MB, 16 MB, and 32 MB are supported. Sockets 6 and 7 comprise bank 0, sockets 8 and 9 comprise bank 1. A bank must be completely filled to be operable.

Table 5-1 lists memory configurations supported. The table lists memory configurations using x36 FPM DRAM SIMMs. The CPV5000 also supports x32 EDO DRAM SIMMs similarly.

Table 5-1. Memory configurations

Total System Memory	SIMM J6, J7 (Bank 0) SIMM Type (Amount)	SIMM J8, J9 (Bank 1) SIMM Type (Amount)
8 MB	1M X 36 (4 MB)	EMPTY
16 MB	1M X 36 (4 MB)	1M X 36 (4 MB)
24 MB	1M X 36 (4 MB)	2M X 36 (8 MB)
40 MB	1M X 36 (4 MB)	4M X 36 (16 MB)
72 MB	1M X 36 (4 MB)	8M X 36 (32 MB)
136 MB	1M X 36 (4 MB)	16M X 36 (64 MB)
16 MB	2M X 36 (8 MB)	EMPTY
24 MB	2M X 36 (8 MB)	1M X 36 (4 MB)
32 MB	2M X 36 (8 MB)	2M X 36 (8 MB)
48 MB	2M X 36 (8 MB)	4M X 36 (16 MB)
80 MB	2M X 36 (8 MB)	8M X 36 (32 MB)
144 MB	2M X 36 (8 MB)	16M X 36 (64 MB)
32 MB	4M X 36 (16 MB)	EMPTY
40 MB	4M X 36 (16 MB)	1M X 36 (4 MB)
48 MB	4M X 36 (16 MB)	2M X 36 (8 MB)
64 MB	4M X 36 (16 MB)	4M X 36 (16 MB)
96 MB	4M X 36 (16 MB)	8M X 36 (32 MB)
160 MB	4M X 36 (16 MB)	16M X 36 (64 MB)
64 MB	8M X 36 (32 MB)	EMPTY
72 MB	8M X 36 (32 MB)	1M X 36 (4 MB)
80 MB	8M X 36 (32 MB)	2M X 36 (8 MB)
96 MB	8M X 36 (32 MB)	4M X 36 (16 MB)
128 MB	8M X 36 (32 MB)	8M X 36 (32 MB)
192 MB	8M X 36 (32 MB)	16M X 36 (64 MB)
128 MB	16M X 36 (64 MB)	EMPTY
136 MB	16M X 36 (64 MB)	1M X 36 (4 MB)
144 MB	16M X 36 (64 MB)	2M X 36 (8 MB)
160 MB	16M X 36 (64 MB)	4M X 36 (16 MB)
192 MB	16M X 36 (64 MB)	8M X 36 (32 MB)
256 MB	16M X 36 (64 MB)	16M X 36 (64 MB)

Installing DRAM SIMMs

To install SIMMs, locate the memory banks on the single board computer.

Before installing SIMMs, remove power from the system and disconnect all power cords. After power has been removed, remove the CPV5000 from the chassis.

Caution

Only qualified, experienced electronics personnel should access the interior of a chassis. The components of the CPV5000 are sensitive to static discharge. While out of the chassis, components should be placed on a static-dissipative surface or into a static-shielding bag.

Installation instructions

No tools are required for this procedure.

1. Remove power from the chassis and disconnect all power cords. Remove the CPV5000 from the chassis.
2. Locate the SIMM slots on the CPV5000.
   Hold the SIMM so the notched edge is aligned with the notch on the SIMM socket.
3. Insert the SIMM at a 45 degree angle.
4. Gently push the SIMM into an upright position until it locks into place.
5. Install the CPV5000 in the chassis and connect the power cords. Apply power to the chassis.

Upgrading the CPU

The processor module is user-upgradeable. The computer has a ZIF (Zero Insertion Force) socket that accepts a PGA (Pin Grid Array) style package.

The CPV5000 is designed to support either an Intel MMX Pentium® or an AMD K-6® processor.

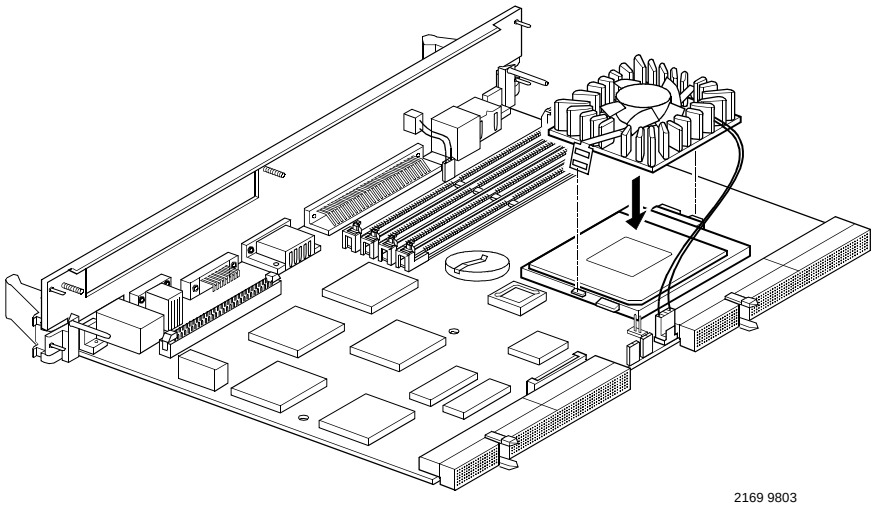
Installation instructions

No tools are required for this procedure.

1. Remove power from the chassis and disconnect all power cords. Remove the CPV5000 from the chassis.
2. Locate the CPU socket.
3. Place the CPV5000 on a flat surface and remove the fan and heat sink by disconnecting the cable, and then releasing the retaining clip.
4. Release the (ZIF) lever by first pushing the lever away from the socket and then lifting up. Lift the processor from the socket. Insert the replacement CPU making sure pin 1 on the CPU lines up with pin 1 on the socket.
5. After checking that the CPU is fully seated in the socket, push the lever down until it locks in place.
6. Set the proper core CPU voltage using J30.

   If you are using an Intel processor, then you should jumper J30. If you are using an AMD processor, then leave the jumper off.

   If your board does not have a J30 jumper, then it is not equipped to use the AMD processors.
7. Attach the fan to the CPU using the spring clip that attaches to the socket.



8. Connect the fan power cable.
9. Check the CPU speed jumper settings.

Table 5-2. CPU speed settings

CPU Speed	J10	J15	J14	J29
166 Mhz	2-3	1-2	1-2	2-3
200 Mhz	2-3	2-3	1-2	2-3
233 Mhz	2-3	2-3	2-3	2-3
266 Mhz	2-3	1-2	2-3	1-2
300 Mhz	2-3	1-2	1-2	1-2

10. Install the CPV5000 in the chassis and connect the power cords.

Removing and replacing the battery

Caution Replace the battery with the same type or with an equivalent type that is recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

1. Remove power from the chassis and disconnect all power cords. Remove the CPV5000 from the chassis.
2. Locate the battery on the CPV5000. See Figure on page 3-2.
3. Remove the existing battery by lifting up on the battery's edges and sliding it out of the holder. Do not try to lift up on the spring clip. The clip is there to hold the battery in place–it does not function as a release clip.
4. Insert the new battery into the holder.

Note Ensure that you insert the battery with the plus sign (+) facing upwards.

5. Install the CPV5000 in the chassis and connect the power cords.
6. When the CPV5000 powers on, the optimal BIOS setting will have to be loaded.

For information on how to load the BIOS settings, see Chapter 7, *Starting WinBIOS Setup*.

Installing the on-board disk drives

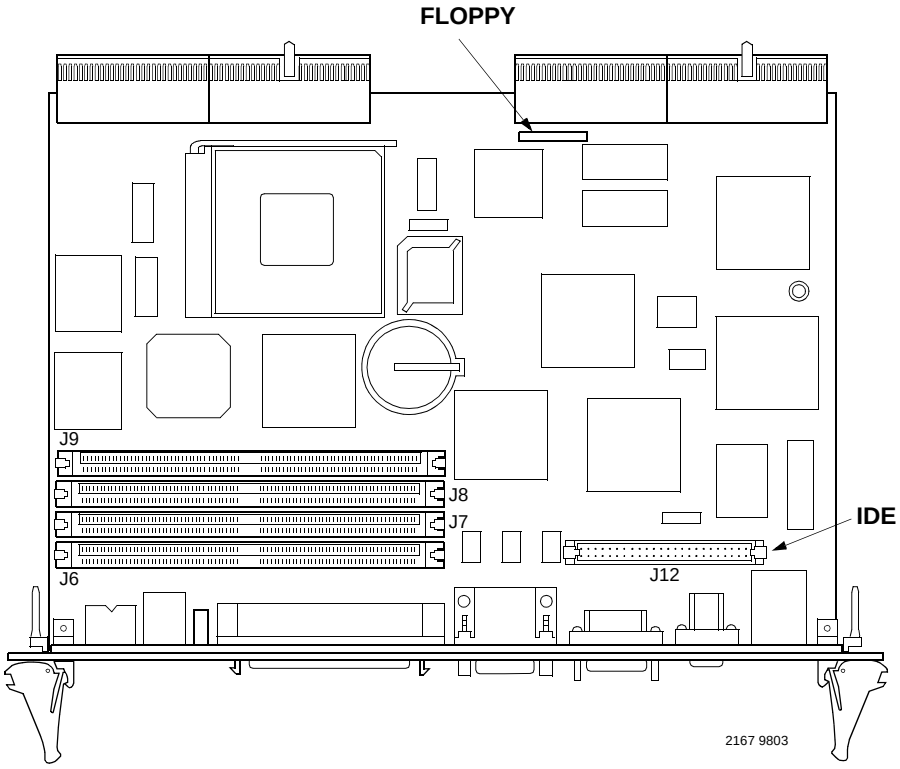
The CPV5000 has an optional, on-board EIDE drive and a floppy drive.

Installation instructions

Use the following procedure to install the on-board disk and floppy drives.

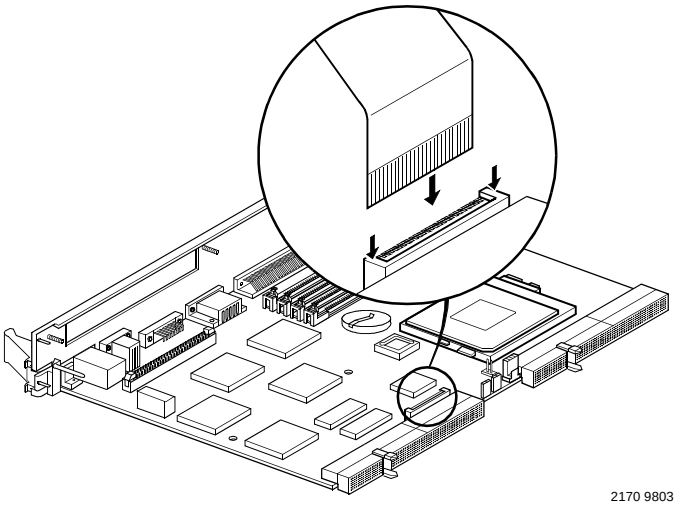
A number one Phillips screwdriver is needed for this procedure.

1. Remove power from the chassis and disconnect all power cords. Remove the CPV5000 from the chassis.
2. Locate the drive headers on the CPV5000.



Note The flex cable going from the floppy drive to the CPV5000 has contacts on one side only. The shiny contacts go toward the front panel at both ends, and the blue side goes toward the backplane connectors.

3. If installing a floppy drive, attach one end of the cable to its connector on the CPV5000. To attach the cable, push up on each end of the plastic connector. The connector releases so that the cable can be inserted in the connector. Insert the cable into the connector and push down on each end. Attach the other end of the cable in step 7.



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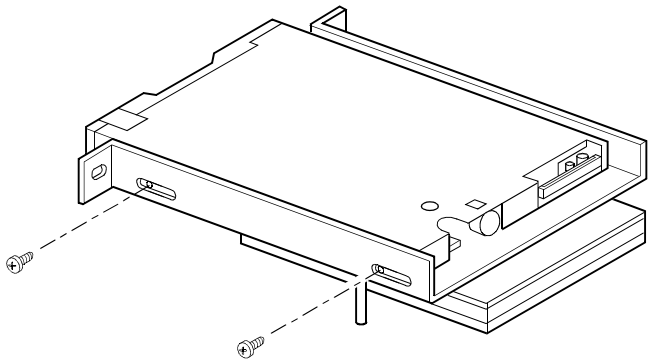
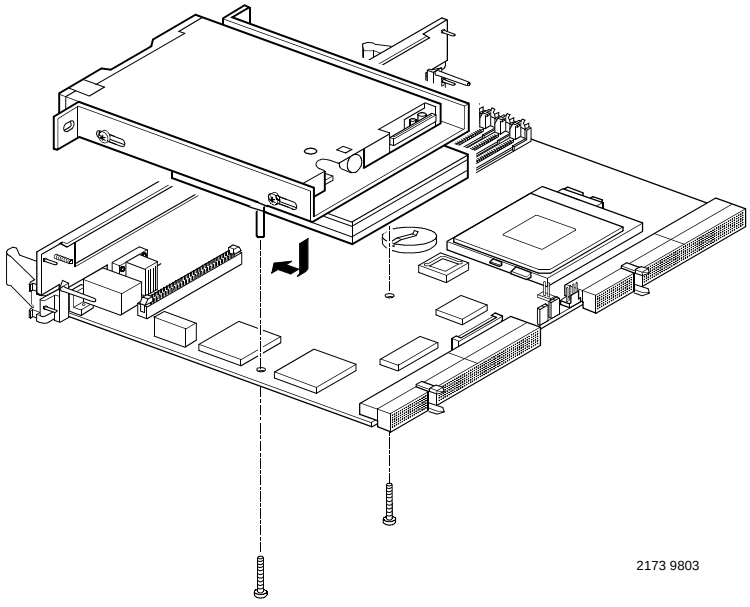
4. Install the floppy drive in the drive carrier. Attach the floppy drive to the carrier with two screws on each side.

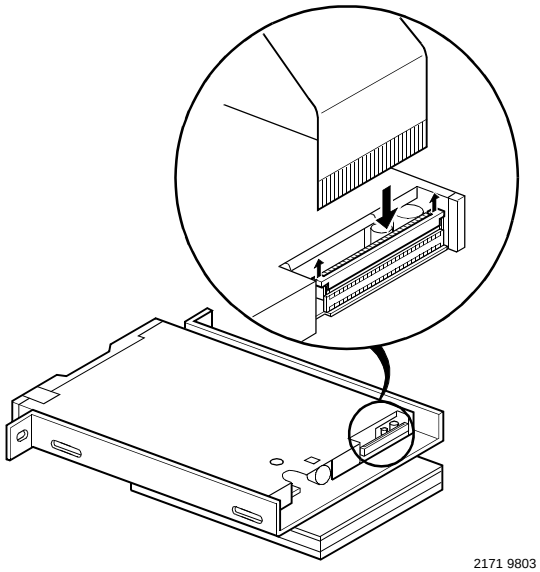


5. If you are installing a hard drive, attach the cable to the drive and the IDE connector on the CPV5000.

6. Attach the drive carrier to the CPV5000 using two screws.



7. Attach the remaining end of the floppy cable. Push up on the tabs on the connector and insert the floppy cable. Push down on the tabs to secure the cable.



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8. Install the CPV5000 in the chassis and connect the power cords.

Power On Self-Tests 6

This chapter contains information to help you troubleshoot the system. It describes error reporting methods and suggests appropriate solutions to various problems. **A**merican **M**egatrends **I**nc. **B**asic **I**nput/**O**utput **S**ystem **(AMIBIOS)** provides all IBM® standard **P**ower-**O**n **S**elf **T**est **(POST)** routines as well as enhanced AMIBIOS POST routines. AMIBIOS POST supports CPU internal diagnostics.

POST phases

When the system is powered on, AMIBIOS executes two types of POST routines. The two types of POST routines are:

- System test and initialization – tests and initializes AMIBIOS for normal operations
- System configuration verification – compares the defined configuration with the hardware actually installed.

BIOS error reporting

BIOS errors are reported by a series of beep sounds or when an error message is displayed to the screen. Refer to Table 6-1 for BIOS error reporting information. This section contains information on the following:

- Beep codes
  Refer to Table 6-2 for beep code information.
- AMIBIOS displayed error messages
  Refer to Table 6-3 for AMIBIOS displayed error message information.

Table 6-1. BIOS error reporting

If ...	Then ...
The error occurs before the display device is initialized.	A series of beeps sound. Beep codes indicate that a fatal error has occurred. AMIBIOS beep codes are described in Table 6-2.
The error occurs after the display device is initialized.	The error message is displayed. AMIBIOS error messages are explained in Table 6-3. A prompt to press <F1> can also appear with displayed error messages.

Beep codes

Fatal errors, which halt the boot process, are communicated through a series of audible beeps. If AMIBIOS POST can initialize the system video display, it displays the error message on the screen. Displayed error messages, in most cases, allow the system to continue to boot. AMIBIOS displayed error messages are described in Table 6-3.

Table 6-2. Beep codes

Beeps	Error message	Description
1	Refresh Failure	The memory refresh circuitry is faulty.
2	Parity Error	Parity error in the base memory (the first 64 KB block memory)
3	Base 64 KB Memory Failure	Memory failure in first 64 KB
4	Timer Not Operational	A memory failure in the first 64 KB of memory, or Timer 1 is not functioning
5	Processor Error	The CPU generated an error.
6	8042 - Gate A20 Failure	Cannot switch to protected mode
7	Processor Exception Interrupt Error	The CPU on the CPU board generated an exception interrupt.
8	Display Memory Read/Write Error	The system video adapter is either missing or its memory is faulty. This is not a fatal error.
9	ROM Checksum Error	The ROM checksum value does not match the value encoded in AMIBIOS.
10	CMOS Shutdown Register Read/Write Error	The shutdown register for CMOS RAM has failed.
11	Cache Memory Bad – Do Not Enable Cache	The cache memory test failed. Cache memory is disabled. Do not press <Ctrl> <Alt> <Shift> <+> to enable cache memory.

AMIBIOS displayed error messages

The following section describes the operation of the CPV5000 when the BIOS detects an error during power up of the CPV5000. The explanation assumes that a copy of AMI diagnostics is available to assist with debug of the problem.

If an error occurs after the system display initializes, error messages are displayed as follows:

```
ERROR Message Line 1
```

If this message appears, press <F1> to continue.

The following message may also appear:

```
RUN SETUP UTILITY.
```

Press <F1> to run WINBIOS Setup if this message appears. Refer to Table 6-3 for AMIBIOS displayed error message information.

Table 6-3. AMIBIOS error messages

Message	Explanation
8042 Gate-A20 error	Gate A20 on the keyboard controller (8042) is not working. Replace the 8042.
Address line short!	Error in the address decoding circuitry
C: drive error	No response from drive C:. Run the AMIDiag hard disk utility. Check the C: hard disk type in Standard Setup.
C: drive failure	No response from hard disk drive C:. Replace the drive.
Cache memory bad, Do not enable cache	Cache memory is defective. Run AMIDiag.
CH-2 timer error	An AT system has two timers. There is an error in timer 2.
CMOS battery state low	CMOS RAM is powered by a battery. The battery power is low. Replace the battery.
CMOS checksum failure	CMOS RAM checksum is different than the previous value. Run WINBIOS Setup.
CMOS system options not set	The values stored in CMOS RAM are destroyed. Run WINBIOS Setup.

Table 6-3. AMIBIOS error messages (Continued)

Message	Explanation
CMOS display type mismatch	The video type in CMOS RAM does not match the type detected. Run WINBIOS Setup.
CMOS memory size mismatch	The amount of memory found by AMIBIOS is different than the amount in CMOS RAM. Run WINBIOS Setup.
CMOS time and date not set	Run Standard Setup to set the date and time.
D: drive error	No response from drive D:. Run the AMIDiag Hard Disk Utility. Check the hard disk type in Standard Setup.
D: drive failure	No response from hard disk drive D:. Replace the drive.
Diskette boot failure	The boot diskette in drive A: cannot be used to boot the system. Use another boot diskette and follow the screen instructions.
Display switch not set properly	Some systems require a video switch be set to either color or monochrome. Turn the system off, set the switch properly, then power on.
DMA error	Error in the DMA controller
DMA 1 error	Error in the first DMA channel
DMA 2 error	Error in the second DMA channel
FDD controller failure	AMIBIOS cannot communicate with the floppy disk drive controller. Check all appropriate connections after the system is powered down.
HDD controller Failure	AMIBIOS cannot communicate with the hard disk drive controller. Check all appropriate connections after the system is powered down.
INTR1 error	Interrupt channel 1 failed POST
INTR2 error	Interrupt channel 2 failed POST
Invalid boot diskette	AMIBIOS can read the diskette in floppy drive A, but it cannot boot the system with it. Use another boot diskette and follow the screen instructions.
Keyboard is locked. You must unlock it.	The keyboard lock on the system is engaged. The system must be unlocked to continue to boot.
Keyboard error	The keyboard has a timing problem. Make sure a keyboard controller AMIBIOS is installed. Set keyboard in Advanced Setup to “not installed” to skip the keyboard POST routines.
KB/Interface error	There is an error in the keyboard connector.

Table 6-3. AMIBIOS error messages (Continued)

Message	Explanation
No ROM Basic	Cannot find a proper bootable sector on either drive A: or C:. AMIBIOS cannot find ROM Basic.
Off board parity error	Parity error in memory installed on an adapter board in an expansion slot. The format is: OFF BOARD PARITY ERROR ADDR = (XXXX) XXXX is the hex address where the error occurred. Run AMIDiag to find and correct memory problems.
On board parity error	Parity error in CPV5000 DRAM memory. The format is: ON BOARD PARITY ERROR ADDR = (XXXX) XXXX is the hex address where the error occurred. Run AMIDiag to find and correct memory problems.
Parity error ????	Parity error in system memory at an unknown address. Run AMIDiag to find and correct memory problems.

POST memory test

Normally, the only visible POST routine is the memory test. When the system is powered on the following screen appears:

```
AMIBIOS (C) 1995 American Megatrends Inc.

xxxxx KB OK

Hit <DEL> if you want to run SETUP



(C) American Megatrends Inc.

XX-XXXX-XXXXXX-XXXXXXXX-XXXXXX-XXXX-X
```


An AMIBIOS identification string is displayed at the left bottom corner of the screen, below the copyright message. After POST completes the following message appears:

```
Hit <DEL> if you want to run SETUP

Press <Del> to access WINBIOS Setup.
```

ISA NMI handler messages

Refer to Table 6-4 for ISA NMI Handler messages.

Table 6-4. ISA NMI handler messages

ISA NMI Message	Explanation
Memory parity error at xxxxx	Memory failed. If the memory location can be determined, it is displayed as xxxxx. If not, the message is memory parity error ????.
I/O board parity error at xxxxx	An expansion board failed. If the address can be determined, it is displayed as xxxxx. If not, the message is I/O board parity error ????.
DMA bus time-out	A device has driven the bus signal for more than 7.8 microseconds.

BIOS revision

The monitor displays this message before displaying the AMI configuration screen. The actual BIOS revision should be quoted in all communication with Motorola.

AMIBIOS configuration screen

When the POST routines complete successfully, AMIBIOS displays a screen similar to the following:


```
AMIBIOS System Configuration (C) Copyright 1985-95 American Megatrends Inc.
Main Processor          : Pentium         Base Memory Size   : 640 KB
Numeric Coprocessor     : Present         Ext. Memory Size   : 7808 KB
Floppy Drive A:         : 1.2 MB _        Display Type       : EGA/VGA
Floppy Drive B:         : 1.44 MB _       Serial Port(s)     : 3F8
ROM-BIOS Date:          : 07/15/95        Parallel Port(s)   : 378
```

POST checkpoint codes

When AMIBIOS performs the POST routine, it writes diagnostic codes, that is checkpoint codes, to I/O port 0080h. If the computer cannot complete the boot process, diagnostic equipment can be attached to the computer to read I/O port 0080h. The following AMIBIOS POST checkpoint codes are valid for all AMIBIOS products with a core BIOS date of 7/15/95 (Enhanced). These options allow detailed analysis of a board that fails to operate correctly.

Uncompressed initialization codes

The uncompressed initialization checkpoint codes available are listed in order of execution in Table 6-5.

Table 6-5. Uncompressed initialized codes

Checkpoint code	Description
D0h	The NMI is disabled. Power on delay is starting. Next, the initialization code checksum will be verified.
D1h	Initializing the DMA controller, performing the keyboard controller BAT test, starting memory refresh, and entering 4 GB flat mode next.
D3h	Starting memory sizing next.
D4h	Returning to real mode. Executing any OEM patches and setting the stack next.
D5h	Passing control to the uncompressed code in shadow RAM at E000:0000h.The initialization code is copied to segment 0 and control will be transferred to segment 0.
D6h	Control is in segment 0. Next, checking if <Ctrl> <Home> was pressed and verifying the system BIOS checksum. If either <Ctrl> <Home> was pressed or the system BIOS checksum is bad, next will go to checkpoint code E0h. Otherwise, going to checkpoint code D7h.
D7h	Passing control to the interface module next.
D8h	The main system BIOS runtime code will be decompressed next.
D9h	Passing control to the main system BIOS in shadow RAM next.

Runtime checkpoint codes

The runtime checkpoint codes are listed in order of execution in Table 6-6. These codes are uncompressed in F0000h shadow RAM.

Table 6-6. Runtime checkpoint codes

Checkpoint code	Description
03h	The NMI is disabled. Next, checking for a soft reset or a power on condition.
05h	The BIOS stack has been built. Next, disabling cache memory.
06h	Uncompressing the POST code next.
07h	Next, initializing the CPU and the CPU data area.
08h	The CMOS checksum calculation is performed next.
0Bh	Next, performing any required initialization before the keyboard BAT command is issued.
0Ch	The keyboard controller input buffer is free. Next, issuing the BAT command to the keyboard controller.
0Eh	The keyboard controller BAT command result is verified. Next, performing any necessary initialization after the keyboard controller BAT command test.
0Fh	The initialization after the keyboard controller BAT command test is carried out. The keyboard command byte is written next.
10h	The keyboard controller command byte is written. Next, issuing the pin 23 and 24 blocking and unblocking commands.
11h	Next, checking if the <End> or <Ins> keys were pressed during power on. Initializing CMOS RAM if the initialize CMOS RAM in every boot AMIBIOS POST option was set in AMIBCP or the <End> key was pressed.
12h	Next, disabling DMA controllers 1 and 2 and interrupt controllers 1 and 2.
13h	The video display is disabled. Port B has initialized. Next, initializing the chipset.
14h	The 8254 timer test will begin next.
19h	The 8254 timer test is over. Starting the memory refresh test next.
1Ah	The memory refresh line is toggling. Checking the 15 second on/off time next.
23h	Reading the 8042 input port and disabling the MEGAKEY Green PC feature next. Making the BIOS code segment writable and performing any necessary configuration before initializing the interrupt vectors.

Table 6-6. Runtime checkpoint codes (Continued)

Checkpoint code	Description
24h	The configuration required before interrupt vector initialization has completed. Interrupt vector initialization is about to begin.
25h	Interrupt vector initialization is complete. Clearing the password if the POST DIAG switch is on.
27h	Any initialization before setting video mode is performed next.
28h	Initialization before setting the video mode is complete. Configuring the monochrome mode and color mode settings next.
2Ah	Bus initialization system, static, output devices are done next, if present.
2Bh	Passing control to the video ROM to perform any required configuration before the video ROM test.
2Ch	All necessary processing before passing control to the video ROM is done. Looking for the video ROM next and passing control to it.
2Dh	The video ROM has returned control to BIOS POST. Performing any required processing after the video ROM had control.
2Eh	Completed post-video ROM test processing. If the EGA/VGA controller is not found, performing the display memory read/write test next.
2Fh	The EGA/VGA controller was not found. The display memory read/write test is about to begin.
30h	The display memory read/write test passed. Look for retrace checking next.
31h	The display memory read/write test or retrace checking failed. Performing the alternate display memory read/write test next.
32h	The alternate display memory read/write test passed. Looking for alternate display retrace checking next.
34h	Video display checking is over. Setting the display mode next.
37h	The display mode is set. Displaying the power on message next.
38h	Initializing the bus input, IPL, and general devices next, if present. See Table 6-7 for additional information.
39h	Displaying bus initialization error messages. See Table 6-7 for additional information.
3Ah	The new cursor position is read and saved. Displaying the Hit <DEL> message next.
40h	Preparing the descriptor tables next.

Table 6-6. Runtime checkpoint codes (Continued)

Checkpoint code	Description
42h	The descriptor tables are prepared. Entering protected mode for the memory test next.
43h	Entered protected mode. Enabling interrupts for diagnostics mode next.
44h	Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next.
45h	Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next.
46h	The memory wraparound test has completed. The memory size calculation has completed. Writing patterns to test memory next.
47h	The memory pattern was written to extended memory. Writing patterns to the base 640 KB memory next.
48h	Patterns written in base memory. Determining the amount of memory below 1 MB next.
49h	The amount of memory below 1 MB was found and verified. Determining the amount of memory above 1 MB memory next.
4Bh	The amount of memory above 1 MB was found and verified. Checking for a soft reset and clearing the memory below 1 MB for the soft reset next. If this is a power on situation, going to checkpoint 4Eh next.
4Ch	The memory below 1 MB was cleared *via* a soft reset. Clearing the memory above 1 MB next.
4Dh	The memory above 1 MB was cleared *via* a soft reset. Saving the memory size next. Going to checkpoint 52h next.
4Eh	The memory test started, but not as the result of a soft reset. Displaying the first 64 KB memory size next.
4Fh	The memory size display has started. The display is updated during the memory test. Performing the sequential and random memory test next.
50h	The memory below 1 MB was tested and initialized. Adjusting the displayed memory size for relocation and shadowing next.
51h	The memory size display was adjusted for relocation and shadowing. Testing the memory above 1 MB next.
52h	The memory above 1 MB was tested and initialized. Saving the memory size information next.

Table 6-6. Runtime checkpoint codes (Continued)

Checkpoint code	Description
53h	The memory size information and the CPU registers are saved. Entering real mode next.
54h	Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next.
57h	The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next.
58h	The memory size was adjusted for relocation and shadowing. Clearing the Hit <DEL> message next.
59h	The Hit <DEL> message is cleared. The <WAIT...> message is displayed. Starting the DMA and interrupt controller test next.
60h	The DMA page register test passed. Performing the DMA Controller 1 base register test next.
62h	The DMA controller 1 base register test passed. Performing the DMA controller 2 base register test next.
65h	The DMA controller 2 base register test passed. Programming DMA controllers 1 and 2 next.
66h	Completed programming DMA controllers 1 and 2. Initializing the 8259 interrupt controller next.
7Fh	Extended NMI source enabling is in progress.
80h	The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next.
81h	A keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command next.
82h	The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
83h	The command byte was written and global data initialization has completed. Checking for a locked key next.
84h	Locked key checking is over. Checking for a memory size mismatch with CMOS RAM data next.
85h	The memory size check is complete. Displaying a soft error and checking for a password or bypassing WINBIOS Setup next.

Table 6-6. Runtime checkpoint codes (Continued)

Checkpoint code	Description
86h	The password was checked. Performing any required programming before WINBIOS Setup next.
87h	The programming before WINBIOS Setup has completed. Uncompressing the WINBIOS Setup code and executing the AMIBIOS Setup or WINBIOS Setup utility next.
88h	Returned from WINBIOS Setup and cleared the screen. Performing any necessary programming after WINBIOS Setup next.
89h	The programming after WINBIOS Setup has completed. Displaying the power on screen message next.
8Bh	The first screen message was displayed. The <WAIT...> message is displayed. Performing the PS/2 mouse check and extended BIOS data area allocation check next.
8Ch	Programming the WINBIOS Setup options next.
8Dh	The WINBIOS Setup options are programmed. Resetting the hard disk controller next.
8Fh	The hard disk controller was reset. Configuring the floppy drive controller next.
91h	The floppy drive controller was configured. Configuring the hard disk drive controller next.
95h	Initializing the bus option ROMs from C800 next. See Table 6-7 for additional information.
96h	Initializing before passing control to the adaptor ROM at C800.
97h	Initialization before the C800 adaptor ROM gains control has completed. The adaptor ROM check is next.
98h	The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.
99h	Any initialization required after the option ROM test completed. Configuring the timer data area and printer base address next.
9Ah	Set the timer and printer base addresses. Setting the RS-232 base address next.
9Bh	Returned after setting the RS-232 base address. Performing any required initialization before the coprocessor test next.
9Ch	Required initialization before the coprocessor test is over. Initializing the coprocessor next.

Table 6-6. Runtime checkpoint codes (Continued)

Checkpoint code	Description
9Dh	Coprocessor initialized. Performing any required initialization after the coprocessor test next.
9Eh	Initialization after the coprocessor test completes. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next.
A2h	Displaying any soft errors next.
A3h	The soft error display has completed. Setting the keyboard typematic rate next.
A4h	The keyboard typematic rate is set. Programming the memory wait states next.
A5h	Memory wait state programming is over. Clearing the screen and enabling parity and the NMI next.
A7h	NMI and parity enabled. Performing any initialization required before passing control to the adaptor ROM at E000 next.
A8h	Initialization before passing control to the adaptor ROM at E000h completed. Passing control to the adaptor ROM at E000h next.
A9h	Returned from adaptor ROM at E000h control. Performing any initialization required after the E000 option ROM had control next.
AAh	Initialization after E000 option ROM control has completed. Displaying the system configuration next.
ABh	Building the multiprocessor table, if necessary.
ACh	Uncompressing the DMI data and initializing DMI POST next.
B0h	The system configuration is displayed.
B1h	Copying any code to specific areas.
00h	Code copying to specific areas is complete. Passing control to INT 19h boot loader next.

Bus checkpoint codes

The system BIOS passes control to different buses at various checkpoints, see Table 6-7 for a description of the bus checkpoint codes.

Table 6-7. Bus checkpoint codes

Checkpoint code	Description
2Ah	Initializing the different bus system, static, and output devices, if present.
38h	Initialized bus input, IPL, and general devices, if present.
39h	Displaying bus initialization error messages, if any.
95h	Initializing bus adaptor ROMs from C8000h through D8000h.

Additional bus checkpoints

While control is in the bus routines, additional checkpoints are output to I/O port address 0080h as data to identify the routines being executed. There are two byte checkpoints and these are:

- The low byte - The low byte of the checkpoint is the system BIOS checkpoint where control is passed to the different bus routines.
- The high byte - The high byte of checkpoint indicates that the routine is being executed in different buses.

Refer to Table 6-8 for additional bus checkpoint information.

Table 6-8. Additional bus checkpoints

Bits	Description	
Bits 7 to 4	0000	Function 0. Disable all devices on the bus.
	0001	Function 1. Initialize static devices on the bus.
	0010	Function 2. Initialize output devices on the bus.
	0011	Function 3. Initialize input devices on the bus.
	0100	Function 4. Initialize IPL devices on the bus.
	0101	Function 5. Initiate general devices on the bus.
	0110	Function 6. Initialize error reporting on the bus.
	0111	Function 7. Initialize add-on ROMs for all buses.
Bits 3 to 0		Specify the bus
	0	Generic DIM Device Initialization Manager
	1	Onboard System devices
	2	ISA devices
	3	EISA devices
	4	ISA PnP devices
	5	PCI devices

WinBIOS Setup 7

This chapter contains information on WinBIOS Setup. WinBIOS Setup configures system information that is stored in CMOS RAM.

Starting WinBIOS Setup

When the Power-On Self Test (POST) executes, the following message appears on the screen:

```
Hit <DEL> if you want to run SETUP
```

You must then press <DEL> to run WinBIOS Setup.

If the BIOS setting for quick boot is enabled, the <DEL> key may have to be pressed before the VGA has initialized.

WinBIOS Setup features

This section describes the WinBIOS Setup features.

Icon-based user interface

WinBIOS Setup functions are all available in an easily-accessible graphical user interface.

Automatic option selection

AMIBIOS can be configured to reflect dependencies between AMIBIOS features and WinBIOS Setup options.

For example, the external cache option in Advanced Setup can be programmed either to display if the computer has secondary cache memory or to be absent if there is no secondary cache memory.

Help screens

WinBIOS Setup provides Help screens for Advanced Setup, Chipset Setup, Power Management Setup, and Peripheral Setup.

Help on mouse and keyboard is also available. Choose Help by pressing <Alt> <H>.

Automatic WinBIOS Setup option selection

If selecting a certain setting for one WinBIOS Setup option determines the settings for one or more other WinBIOS Setup options, AMIBIOS automatically assigns the dependent settings and does not permit the end user to modify these settings unless the setting for the parent option is changed.

For example, the Serial Port options in Peripheral Setup can be set to 2F8h, 3F8h, 2E8h, or 3E8h. If 2F8h is chosen by the end user for Serial Port 1, AMIBIOS disables 2F8h for Serial Port 2. Invalid options are grayed and cannot be selected.

Point and click interface

WinBIOS Setup uses the familiar point and click navigation technique. The end user can point with the mouse anywhere on the screen, click the left mouse button, and WinBIOS Setup control is transferred to the new location. The previous window is closed. All parameters that were changed will automatically be saved, pending the selection on the exit screen.

Mouse support

The following devices are supported:

- PS/2-type mouse
- bus mouse that uses IRQs 3, 4, or 5
  IRQ2 is not supported
- Microsoft-compatible mouse that uses the M, V, W Series M, and M+ protocols

- Logitech C-series-compatible mouse that uses the MM protocol

Memory test tick sound

AMIBIOS permits the end user to press <Esc> or <Del> during the memory test to disable the ticking sound and bypass the memory test. The memory click test will only be heard when the Quick boot is disabled.

Using a mouse with WinBIOS Setup

WinBIOS Setup can be accessed via keyboard, mouse, or pen. The mouse click functions are as follows:

- Single click to change or select both global and current fields
- Double-click to perform an operation in the selected field

Using the keyboard with WinBIOS Setup

WinBIOS Setup has a built-in keyboard driver that uses simple keystroke combinations. Refer to Table 7-1 for keystroke combination information.

Table 7-1. Keystroke combinations

Keystroke	Function
<Tab>	Move to the next window or field
→, ←, ↑, ↓	Move to the next field to the right, left, above, or below
<Enter>	Select in the current field
+	Increments a value
-	Decrements a value
<Esc>	Closes the current operation and return to previous level
<PgUp>	Returns to the previous page
<PgDn>	Advances to the next page
<Home>	Returns to the beginning of the text
<End>	Advances to the end of the text
<Alt> <H>	Access a help window
<Alt> <Spacebar>	Exit WinBIOS Setup
Alphabetic keys	A to Z are used in the Virtual Keyboard, and are not case-sensitive.
Numeric keys	0 to 9 are used in the Virtual Keyboard and Numeric Keypad.

WinBIOS Setup main menu

The WinBIOS Setup main menu is organized into four windows. Each window corresponds to a section in this chapter. Each section contains several icons. Clicking on each icon activates a specific function. The WinBIOS Setup icons and functions are described in this chapter. Refer to Table 7-2 for WinBIOS Setup main menu information.

Table 7-2. WinBIOS Setup main menu

Windows	Function
Setup	Setup is described starting on page 7-6. This section has Six icons that permits you to set system configuration options such as date, time, hard disk type, floppy type, and many others.
Utilities	Utilities is described beginning on page 7-26. Utilities has two icons that perform system functions.
Security	Security is described beginning on page 7-27. Security has three icons that control AMIBIOS security features.
Default	Default is described beginning on page 7-30. This section has three icons that permits you to select a group of settings for all WinBIOS Setup options.

WinBIOS Setup types

WinBIOS Setup can have up to six separate screens. Different types of system configuration parameters are set on each screen. Refer to Table 7-3 for WinBIOS Setup information.

Table 7-3. WinBIOS Setup

Type	Description	Turn to
Standard Setup	Set the time and date. Configure disk drives.	7-6
Advanced Setup	Configure basic system performance parameters	7-12
Chipset Setup	Configure features specific to the chipset used in the computer	7-16
Power Management Setup	Configure power conservation features	7-19
PCI/PnP Setup	Configure PCI and Plug-and-Play features	7-22
Peripheral Setup	Configure I/O support	7-24

Standard Setup

Standard Setup options are displayed by choosing the Standard icon from the WinBIOS Setup menu. All Standard Setup options are described in this section.

Date/time

Select the Date/Time option to change the date or time. The current date and time are displayed. Enter new values through the displayed window.

Floppy drive A and B

Choose the floppy drive A or B icon to specify the floppy drive type. The settings are 360 KB 5.25 inch, 1.2 MB 5.25 inch, 720 KB 3.5 inch, 1.44 MB 3.5 inch, or 2.88 MB 3.5 inch.

Pri Master
Pri Slave
Sec Master
Sec Slave

Choose these icons to configure the hard disk drive named in the option. When you click on an icon, the following parameters are listed:

- Type
- LBA/Large Mode
- Block Mode
- 32-Bit Mode
- PIO Mode

All parameters, except type**,** relate to IDE drives**.**

Configuring an MFM drive

If configuring an MFM hard disk drive, you must know the drive parameters (number of heads, number of cylinders, number of sectors, the starting write precompensation cylinder, and drive capacity). Choose **Type** and choose the appropriate hard disk drive type (1 - 46). See Table 7-6 for a list of the old MFM hard drive types. If the drive parameters of your MFM drive do not match any drive type listed in Table 7-6, select *User* in the **Type** field and enter the drive parameters that appear on the screen.

User-defined drive

If you are configuring a SCSI drive or an MFM, RLL, ARLL, or ESDI drive with drive parameters that do not match drive types 1-46, you can select the User in the Type field. You must then enter the drive parameters on the screen that appear. Refer to Table 7-4 for drive parameter information. The drive parameters include the following:

- Cylinder -- Number of cylinders
- Hd -- Number of heads
- WP -- Starting write precompensation cylinder
- Sec -- Number of sectors
- Size -- Drive capacity

Table 7-4. Drive parameter descriptions

Parameter	Description
Type	Number for a drive with certain identification parameters
Cylinders	Number of cylinders in the disk drive
Heads	Number of heads
Write Precompensation	The size of a sector gets progressively smaller as the track diameter diminishes. Yet each sector must still hold 512 bytes. Write precompensation circuitry on the hard disk compensates for the physical difference in sector size by boosting the write current for sectors on inner tracks. This parameter is the track number where write precompensation begins.
Landing Zone	This number is the cylinder location where the heads will normally park when the system is shut down.
Sectors	This is the number of sectors per track. MFM drives have 17 sectors per track. RLL drives have 26 sectors per track. ESDI drives have 34 sectors per track. SCSI and IDE drives have more sectors per track.
Capacity	The formatted capacity of the drive is (Number of heads) x (Number of cylinders) x (Number of sectors per track) x (512 bytes per sector).

Configuring IDE drives

If the hard disk drive to be configured is an IDE drive, select the appropriate drive icon (Pri Master, Pri Slave, Sec Master, or Sec Slave). Select the IDE Detect icon to automatically detect all drive parameters.

AMIBIOS automatically detects the IDE drive parameters (including ATAPI CD-ROM drives) and displays them. Click on the OK button to accept these parameters, or you can set the parameters manually if you are absolutely certain that you know the correct IDE drive parameters.

Click on LBA/Large Mode and choose On to enable support for IDE drives with capacities greater than 528 MB.

The LBA mode set depends on the operating system in use. Refer to Table 7-5 for LBA mode information.

Table 7-5. LBA mode

Operating System	Necessary Action
SCO® UNIX ® 3.2.4	LBA mode must be disabled in WINBIOS Setup.
Novell NetWare®	LBA mode must be disabled in WINBIOS Setup.
DOS	LBA mode must be enabled in WINBIOS Setup if the IDE hard disk capacity is greater than 528 MB.
Windows 95®	LBA mode must be enabled in WINBIOS Setup if the IDE hard disk capacity is greater than 528 MB.
Windows® 3.11	LBA mode must be enabled in WINBIOS Setup if the IDE hard disk capacity is greater than 528 MB.
Windows NT®	LBA mode must be enabled in WINBIOS Setup if the IDE hard disk capacity is greater than 528 MB.

Click on Block Mode and choose On to support IDE drives that use block mode.

Click on 32-Bit Mode and click On to support IDE drives that permit 32-bit accesses.

Click on PIO Mode to select the IDE Programmed I/O mode. PIO programming also works with ATAPI CD-ROM drives. The settings are Auto, 0, 1, 2, 3, 4, or 5. Click on Auto to allow AMIBIOS to automatically find the PIO mode that the IDE drive being configured uses. If you select 0-5, you must make absolutely certain that you are selecting the PIO mode supported by the IDE drive being configured.

Configuring a CD-ROM drive

Select the appropriate drive icon (Pri Master, Pri Slave, Sec Master, or Sec Slave). Choose the Type parameter and select CDROM. You can boot the computer from a CD-ROM drive. You can also choose Auto and let AMIBIOS automatically set the correct drive parameters.

Hard disk drive type

Refer to Table 7-6 for hard disk drive type information.

Table 7-6. Hard drive type information

Type	Cylinders	Heads	Write	Landing Zone	Sector	Capacity
1	306	4	128	305	17	10 MB
2	615	4	300	615	17	20 MB
3	615	6	300	615	17	31 MB
4	940	8	512	940	17	62 MB
5	940	6	512	940	17	47 MB
6	615	4	65535	615	17	20 MB
7	462	8	256	511	17	31 MB
8	733	5	65535	733	17	30 MB
9	900	15	65535	901	17	112 MB
10	820	3	65535	820	17	20 MB
11	855	5	65535	855	17	35 MB
12	855	7	65535	855	17	50 MB
13	306	8	128	319	17	20 MB
14	733	7	65535	733	17	43 MB

Table 7-6. Hard drive type information (Continued)

Type	Cylinders	Heads	Write	Landing Zone	Sector	Capacity
16	612	4	0	663	17	20 MB
17	977	5	300	977	17	41 MB
18	977	7	65535	977	17	57 MB
19	1024	7	512	1023	17	60 MB
20	733	5	300	732	17	30 MB
21	733	7	300	732	17	43 MB
22	733	5	300	733	17	30 MB
23	306	4	0	336	17	10 MB
24	925	7	0	925	17	54 MB
25	925	9	65535	925	17	69 MB
26	754	7	754	754	17	44 MB
27	754	11	65535	754	17	69 MB
28	699	7	256	699	17	41 MB
29	823	10	65535	823	17	68 MB
30	918	7	918	918	17	53 MB
31	1024	11	65535	1024	17	94 MB
32	1024	15	65535	1024	17	128 MB
33	1024	5	1024	1024	17	43 MB
34	612	2	128	612	17	10 MB
35	1024	9	65535	1024	17	77 MB
36	1024	8	512	1024	17	68 MB
37	615	8	128	615	17	41 MB
38	987	3	987	987	17	25 MB
39	987	7	987	987	17	57 MB
40	820	6	820	820	17	41 MB
41	977	5	977	977	17	41 MB
42	981	5	981	981	17	41 MB

Table 7-6. Hard drive type information (Continued)

Type	Cylinders	Heads	Write	Landing Zone	Sector	Capacity
43	830	7	512	830	17	48 MB
44	830	10	65535	830	17	69 MB
45	917	15	65535	918	17	114 MB
46	1224	15	65535	1223	17	152 MB

Advanced Setup

Advanced Setup options are displayed by choosing the advanced icon from the WINBIOS Setup main menu. All Advanced Setup options are described in this section.

Quick boot

Set this option to enabled to instruct AMIBIOS to boot quickly when the computer is powered on. This option replaces the Above 1 MB Memory Test Advanced Setup option. Refer to Table 7-7 for a description of the Advanced Setup settings.

Table 7-7. Advanced Setup settings

Setting	Description
Disabled	AMIBIOS tests all system memory. AMIBIOS waits up to 40 seconds for a READY signal from the IDE hard disk drive. AMIBIOS waits for 0.5 seconds after sending a RESET signal to the IDE drive to allow the IDE drive time to get ready again. AMIBIOS checks for a <Del> key press and runs WINBIOS Setup if the key has been pressed.
Enabled	AMIBIOS does not test system memory above 1 MB. AMIBIOS does not wait up to 40 seconds for a READY signal from the IDE hard disk drive. If a READY signal is not received immediately from the IDE drive, AMIBIOS does not configure that drive. AMIBIOS does not wait for 0.5 seconds after sending a RESET signal to the IDE drive to allow the IDE drive time to get ready again. You cannot run WINBIOS Setup at system boot, because there is no delay for the Hit <Del> to run Setup message.

BootUp sequence

This option sets the sequence of boot drives that the AMIBIOS attempts to boot from after AMIBIOS POST completes.

The first boot device can be any of the following: IDE floppy, floptical, CD ROM, SCSI, or network.

The second boot device can be any of the following: Disabled, IDE loptical, or CD ROM.

The third boot device can be any of the following: Disabled, IDE optical, or CD ROM.

BootUp NumLock

Set this option to Off to turn the Num Lock key off when the computer is booted. This enables you to use the arrow keys on both the numeric keypad and the keyboard. The settings are On or Off.

Floppy drive swap

Set this option to Enabled to permit drives A: and B: to be swapped. The settings are Enabled or Disabled.

Floppy drive seek

Set this option to Enabled to specify that floppy drive A: will perform a seek operation at system boot.

Mouse support

When this option is set to Enabled, AMIBIOS supports a PS/2-type mouse. The settings are Enabled or Disabled.

Primary display

This option specifies the type of display monitor and adapter in the computer. The settings are Mono, CGA40, CGA80, EGA/VGA, or Absent.

Password check

This option enables password checking every time the computer is powered on or every time WINBIOS Setup is executed. If Always is chosen, a user password prompt appears every time the computer is turned on. If Setup is chosen, the password prompt appears if WINBIOS is executed.

Internal cache

This option specifies the caching algorithm used for L1 internal cache memory. Refer to Table 7-8 for a description of the internal cache settings.

Table 7-8. Internal cache

Setting	Description
Disabled	Neither L1 internal cache memory on the CPU or L2 secondary cache memory is enabled.
WriteBack (default)	Enable and Use the write-back caching algorithm for the on chip L1 cache.

External cache

This option specifies the caching algorithm used for L2 secondary external cache memory. Refer to Table 7-9 for a description of external cache settings.

Table 7-9. External cache

Setting	Description
Disabled	L2 secondary cache memory is disabled.
WriteBack (default)	Use the write-back caching algorithm for the external L2.
WriteThru	Use the write-through caching algorithm for the external L2.

System BIOS shadow cacheable

When this option is set to Enabled, the contents of the F0000h system memory segment can be read from or written to L2 secondary cache memory. The contents of the F0000h memory segment are always copied from the BIOS ROM to system RAM for faster execution.

The settings are Enabled or Disabled. Enabling this option can significantly affect the performance of some option modules and devices, as follows:

C000, 16K Shadow
C400, 16K Shadow
C800, 16K Shadow
CC00, 16K Shadow
D000, 16K Shadow
D400, 16K Shadow
D800, 16K Shadow
DC00, 16K Shadow

These options control the location of the contents of the 16KB of ROM beginning at the specified memory location. If no adaptor ROM uses the named ROM area, this area is made available to the local bus. For more information, refer to Table 7-10 which shows an example for C000, 16K shadow.

Table 7-10. System BIOS shadow cacheable

Setting	Description
Shadow	The contents of C0000h - C3FFFh are written to the same address in system memory (RAM) for faster execution.
Cache	The contents of the named ROM area are written to the same address in system memory (RAM) for faster execution, if an adaptor ROM will be using the named ROM area. Also, the contents of the RAM area can be read from and written to cache memory.
Disabled	The ROM is not copied to RAM. The contents of the ROM cannot be read from or written to cache memory.

Chipset setup

This section describes the setup of the memory timings for the CPV5000. These setting can significantly affect the performance and reliability of the CPV5000. Motorola recommends that you use the default optimal settings.

Memory hole

Use this option to specify an area in memory that cannot be addressed on the ISA bus. The settings are Disabled, 512 to 640 KB, or 15 to 16 MB. Accesses to memory holes are automatically forwarded to PCI.

IRQ12/M mouse function

Set this option to Enabled to specify that IRQ12 will be used for the mouse. The settings are Disabled or Enabled.

DRAM speed

Specify the RAS access speed of the SIMMs installed in the CPV5000 as system memory. The settings are 60 ns or 70 ns. The default is 70 ns. Manual setting is not supported.

Note If you have installed SIMMS with different speeds in the CPV5000, select the speed of the slowest SIMM. You must always use SIMMS that have the same speed within a memory bank.

Refresh rate

This option is only available in manual DRAM setup. The DRAM refresh rate is adjusted to the frequency selected by this field. The options are for 50 MHz, 60 MHz, or 66 MHz.

Turbo lead readoff

This option is only available in manual DRAM setup. This option can be enabled to bypass the first input register in the DRAM data pipeline. This results is a reduction of one clock cycle from the read leadoff timing.

Read burst timing

This option is only available in manual DRAM setup. This option controls the read burst timings. The options are x444, x333 and x222. The slowest option is x444. The option x222 is only available for EDO DRAM.

Write burst timing

This option is only available in manual DRAM setup. This option controls the write burst timings. The options are x444, x333, and x222. The slowest option is x444.

Fast RAS to CAS delay clock cycle setting

This option is only available in manual DRAM setup. This option controls the delay between RAS and CAS. When disabled, the delay is three clock cycles. When enabled, the delay is two clock cycles.

Leadoff timing

This option is only available in manual DRAM setup. There are four parameters that are set by this option: Read Leadoff timing, Write leadoff timing, RAS #pre-charge, and Refresh RAS assertion. There are four options; 7/6/3/4, 6/5/3/4, 7/6/4/5, and 6/5/4/5.

Speculative readoff

This option is only available in manual DRAM setup. The option, when enabled, can improve leadoff performance by one clock cycle. The option, when enabled, allows the DRAM controller to start a read request before the memory request has been decoded by the TXC. If the cycle does not actually target DRAM, the DRAM cycle is terminated.

Turnaround insertion

This option is only available in manual DRAM setup. When this option is enabled, an extra clock cycle is inserted between back to back DRAM cycles. When disabled, the TXC controls back to back DRAM cycles.

NA Disable (NAD) for external cache

When this option is enabled, the next address pin of the TXC is asserted to enable CPU pipelining. This option should be enabled. If this option is disabled, the CPU will not enable memory read/write pipeline modes, this will slow CPV5000 memory performance significantly.

Extended cachebility

This option should be enabled if the total system DRAM is greater than 64 MB. The 512K cache module is capable of supporting memory configurations up to 256 MB.

ECC test enable

This option enables the ECC test mode. This ECC mode can detect and correct a single bit error, detect double bit errors, and detect all errors confined to a single nibble. When this mode is enabled, all DRAM leadoff latencies are increased by one cycle.

DRAM data integrity mode

The DRAM data integrity mode has three options:

- Disable

  When this option is enabled, no checks are performed for parity or ECC.

- Parity

  This option enables byte level parity checking. Parity checking only functions correctly when 36-bit DRAM SIMMs are used. A parity error asserts SERR#.

- ECC Level 1

  This option asserts SERR# when an uncorrectable error is detected. This results in a system halt. Only single bit errors are correctable. The corrected data is transferred to the requester (CPU or PCI). The corrected data is not written to DRAM.

Bad parity on uncorrectable err

This option is not available unless the DRAM data integrity mode is set to ECC.

SERR# output type

This controls the output driver of the SERR# pin. This should be set to Open Drain when used in a PCI system.

SERR# duration mode

This should be set to Pulse (NMI) for correct CPV5000 operation.

Power Management Setup

Power Management Setup options are displayed by choosing the power management icon from the WINBIOS Setup main menu. All Power Management Setup options are described in this section.

Power management

Set this option to Enabled to enable the power management and Advanced Power Management (APM) features. The settings are Enabled or Disabled.

Instant on support

Set this option to Enabled to allow the computer to go to full power on mode when leaving a power-conserving state. This option is only available if supported by external computer hardware. AMIBIOS uses the RTC Alarm function to wake the computer at a specified time. The settings are Enabled or Disabled.

Green PC monitor power state

This option specifies the power management state that the Green PC-compliant video monitor enters after the specified period of display inactivity has expired. The settings are: Disabled, Off, Standby, or Suspend.

Video power down mode

This option specifies the power management state that the video subsystem enters after the specified period of display inactivity has expired. The settings are: Disabled, Standby, or Suspend.

Hard disk power down mode

This option specifies the power management state that the hard disk drive enters after the specified period of display inactivity has expired. The settings are Disabled, Standby, or Suspend.

Hard disk timeout

This option specifies the length of a period of hard disk inactivity. When this period expires, the hard disk drive enters the power-conserving mode specified in the Hard Disk Power Down Mode option. The settings are Disabled, 1 Minute, and all one minute intervals up to and including 15 Minutes.

Full on to standby timeout

This option specifies the length of the period of system inactivity when the computer is in Full-On mode before the computer is placed in Standby mode. In Standby mode, some power use is curtailed. The settings are Disabled, 1 Minute, 2 Minutes, and all one minute intervals up to and including 15 Minutes.

Standby to suspend timeout

This option specifies the length of the period of system inactivity when the computer is already in Standby mode before the computer is placed in Suspend mode. In Suspend mode, nearly all power use is curtailed. The settings are Disabled, 1 Minute, 2 Minutes, and all one minute intervals up to and including 15 Minutes.

Slow clock ratio

This option specifies the speed at which the system clock runs in power saving modes. The settings are expressed as a ratio between the normal clock speed and the power down clock speed. The settings are 1:1, 1:2 (half as fast as normal), 1:4 (the normal power down clock speed), 1:8, 1:16, 1:32, 1:64, or 1:128.

Display activity

This option specifies if AMIBIOS is to monitor activity on the display monitor for power conservation purposes. When this option is set to Monitor and there is no display activity for the length of time specified by the value in the Full-On to Standby Timeout (Minute) option, the computer enters a power saving state. The settings are Monitor or Ignore.

Enabling event monitoring

These options enable event monitoring. When the computer is in a power saving mode, activity on the named interrupt request line is monitored by AMIBIOS. When any activity occurs, the computer enters Full On mode.

Each of the following IRQ options can be set to Monitor or Ignore.

IRQ 3
IRQ 4
IRQ 5
IRQ 7
IRQ 9
IRQ 10
IRQ 11
IRQ 12
IRQ 13
IRQ 14
IRQ 15

PCI/PnP setup

PCI/PnP setup options are displayed by choosing the PCI/PnP Setup icon from the WINBIOS Setup main menu. All PCI/PnP setup options are described in this section.

Plug and play aware OS

Set this option to Yes if the operating system installed in the computer is Plug and Play-aware. AMIBIOS only detects and enables PnP ISA adapter boards that are required for system boot. Set this option to No if the operating system does not use PnP. You must set this option correctly or PnP-aware adapter boards installed in your computer will not be configured properly. The settings are No or Yes.

PCI latency timer (in PCI clocks)

This option sets latency of all PCI devices on the PCI bus. The settings are in units equal to PCI clocks. The settings are 32, 64, 96, 128, 160, 192, 224, or 248.

PCI VGA palette snoop

This option must be set to Enabled if any ISA adapter board installed in the computer requires VGA palette snooping. The settings are Disabled or Enabled.

PCI IDE bus master

Set this option to Enabled to specify that the IDE controller on the PCI local bus has bus mastering capability. The settings are Disabled or Enabled.

Offboard PCI IDE board

This option specifies if an offboard PCI IDE controller adapter board is used in the computer. You must also specify the PCI expansion slot where the offboard PCI IDE controller board is installed. If an offboard PCI IDE controller is used, the onboard IDE controller on the CPV5000 is automatically disabled. The settings are: Disabled, Auto, Slot1, Slot2, Slot3, or Slot4.

If Auto is selected, AMIBIOS automatically determines the correct setting for this option.

In the AMIBIOS for the EBM3x-PA CPV5000, this option forces IRQ 14 and 15 to a PCI slot on the PCI local bus. This is necessary to support non-compliant PCI IDE adapter boards.

DMA channels

This option can be used to reserve a DMA channel for use by legacy ISA adapter boards. The settings are: Disabled, DMA Ch1, DMA Ch 3, DMA Ch 5, DMA Ch 6, or DMA Ch 7.

ISA/PCI IRQ allocation

The following options specify the bus that the named interrupt request lines (IRQs) are used on. These options allow you to specify IRQs for use by legacy ISA adapter boards.

These options determine if AMIBIOS should remove an IRQ from the pool of available IRQs passed to BIOS configurable devices. The available IRQ pool is determined by reading the ESCD NVRAM. If more IRQs must be removed from the pool, the end user can use these PCI/PnP Setup options to remove the IRQ by assigning the option to the ISA/EISA setting. Onboard I/O is configurable by AMIBIOS. The IRQs used by onboard I/O are configured as PCI/PnP. The settings are PCI/PnP or ISA/EISA.

Up to four IRQs can be allocated to the PCI BUS. The IRQs are allocated according to PCI slot position and the capabilities of the PCI option board.

Assuming all IRQs are available to the PCI bus the order of allocation is as follows: 11, 10, 9, 15, 5, 3, 7, 4, 12, 14.

IRQ3
IRQ4
IRQ5
IRQ7
IRQ9
IRQ10
IRQ11

IRQ12
IRQ14
IRQ15

Reserved memory size

This option specifies the size of the memory area reserved for legacy ISA adapter boards.

The settings are: Disabled, 16K, 32K, or 64K.

Reserved memory address

This option specifies the beginning address (in hex) of the reserved memory area. The specified ROM memory area is reserved for use by legacy ISA adapter boards.

The settings are C0000, C4000, C8000, CC000, D0000, D4000, D8000, or DC000.

This address must be set if the reserved memory size is enabled.

Peripheral setup

Peripheral setup options are displayed by choosing the peripheral setup icon from the WINBIOS Setup main menu. All peripheral setup options are described in this section.

Onboard FDC

This option enables the floppy drive controller on the CPV5000. The settings are Auto, Enabled, or Disabled.

Onboard serial port 1/COM 1

This option enables serial port 1 on the CPV5000 and specifies the base I/O port address for serial port 1. The settings are: Auto, 3F8h, 2F8h, 3E8h, 2E8, or Disabled.

Onboard serial port 2/COM 2

This option enables serial port 2 on the CPV5000 and specifies the base I/O port address for serial port 2. The settings are: Auto, 3F8h, 2F8h, 3E8h, 2E8, or Disabled.

Onboard parallel port

This option enables the parallel port on the CPV5000 and specifies the parallel port base I/O port address. The settings are: Auto, 378h, 278h, 3BCh, or Disabled.

Parallel port mode

This option specifies the parallel port mode. ECP and EPP are both bidirectional data transfer schemes that adhere to the IEEE P1284 specifications. Refer to Table 7-11 for parallel port mode setting information.

Table 7-11. Parallel port mode

Setting	Description
Normal	The normal parallel port mode is used. This is the default setting.
Bi-Dir	Use this setting to support bidirectional transfers on the parallel port.
EPP	The parallel port can be used with devices that adhere to the Enhanced Parallel Port (EPP) specification. EPP uses the existing parallel port signals to provide asymmetric bidirectional data transfer driven by the host device.
ECP	The parallel port can be used with devices that adhere to the Extended Capabilities Port (ECP) specification. ECP uses the DMA protocol to achieve transfer rates of approximately 2.5 MB. ECP provides symmetric bidirectional communications.

Parallel port DMA

This option is only available if the setting for the Parallel Port Mode option is ECP. The settings are Disabled, DMA CH (channel) 0, DMA CH 1, or DMA CH 3.

Onboard IDE

This option specifies the onboard IDE controller channels that will be used. The settings are Primary, Secondary, Both, or Disabled.

Utility menu

There are two icons in the utility menu. These icons are:

- Detect IDE
- Language

Detect IDE

This is an option to detect the characteristics of the IDE disks connected to the primary and secondary IDE connectors. The auto-detection will only operate if the IDE ports are enabled in the peripheral menu under the option of onboard IDE.

When the IDE disks are detected they are set as USER defined.

Language

English is the only language supported by the BIOS screens.

Security

Three icons appear in the WINBIOS security Setup screen. These icons are:

- Supervisor
- User
- Anti-Virus

Supervisor and user icons

The Supervisor and the User icons configure password support. If you use the Supervisor and User passwords, the Supervisor password must be set first.

Two levels of passwords

The system can be configured so that all users must enter a password every time the system boots, or when WINBIOS Setup is executed, using either the supervisor password or user password. Both passwords have the same level of access to make changes to the system settings.

If the supervisor password is used to enter the BIOS screens the user password can be changed or deleted without knowing the current user password.

If you do not want to use a password, press <Enter> when the password prompt appears.

Setting a password

The password check option is enabled in **Advanced Setup** by choosing either Always (the password prompt appears every time the system is powered on) or Setup (the password prompt appears only when WINBIOS is run). The password is stored in CMOS RAM. You can enter a password by performing any of the following actions:

- Typing the password on the keyboard
- Selecting each letter using the mouse

When you select Supervisor or User, AMIBIOS prompts for a password. You must set the Supervisor password before you can set the User password. Enter a one to six character password. The password does not appear on the screen when typed. If you forget the password, you must drain CMOS RAM and reconfigure the system.

Changing a password

Select the appropriate password icon (Supervisor or User) from the Security section of the WINBIOS Setup main menu. Type the password and press <Enter>. The screen does not display the characters entered. After the new password is entered, retype the new password as prompted and press <Enter>.

If the password confirmation is incorrect, an error message appears. If the new password is entered without error, press <Esc> to return to the WINBIOS Main Menu. The password is stored in CMOS RAM after WINBIOS completes. The next time the system boots, you are prompted for the password if the password function is present and is enabled.

Remember the password

When the password is changed, keep a record of the new password. If you forget the password, the only method of recovery is to power the CPV5000 down and remove the battery for one minute. Reinsert the battery before applying power to the CPV5000. All CMOS settings are lost when the battery is removed.

Anti-Virus

When this icon is selected from the Security section of the WINBIOS Setup main menu, AMIBIOS issues a warning when any program or virus issues a Disk Format command or attempts to write to the boot sector of the hard disk drive. The settings are Enabled or Disabled. If enabled, the following message appears when a write is attempted to the boot sector.

Note You may have to type **N** several times to prevent the boot sector write.

A typical operating system installation will write to the boot sector of the hard disk drive. It is recommended that this option not be enabled during operating system installation.

```
Boot Sector Write!!!

Possible VIRUS. Continue (Y/N)?
```

The following message appears after any attempt to format any cylinder, head, or sector of any hard disk drive via the BIOS INT 13 Hard Disk Drive Service.

```
Format!!!

Possible VIRUS: Continue (Y/N)?
```

It is beyond the scope of this manual to advise on the correct answer to the response to the questions.

Default

The icons in this section permit you to select a group of settings for all WINBIOS Setup options. You can use these icons to quickly set system configuration parameters. You can use these icons to choose a group of settings that have a better chance of working when the system is having configuration-related problems.

Original

Choose the Original icon to return to the system configuration values present in WINBIOS Setup when you first began this WINBIOS Setup session.

Optimal

You can load the optimal default settings for the WINBIOS by selecting the Optimal icon. The Optimal default settings are best-case values that should optimize system performance. If CMOS RAM is corrupted, the Optimal settings should be loaded.

Fail-Safe

You can load the Fail-Safe WINBIOS Setup option settings by selecting the Fail-Safe icon from the Default section of the WINBIOS Setup main menu.

The Fail-Safe settings provide far from optimal system performance, but are the most stable settings. Use this option as a diagnostic aid if the system is behaving erratically.

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