
# CompactRIO PROFIBUS DP

## DP Slave - Getting Started

**V1.4/03.03.2010**

## Revision History

| Version | Date | Description | Resp. |
|---|---|---|---|
| | | | |
| V1.4 | 03.03.2010 | Minor Fixes | SF |
| V1.3 | 17.02.2010 | National Instruments specific changes | SF, JK |
| V1.2 | 16.06.2009 | Minor fixes | BS, MF |
| V1.1 | 28.04.2009 | Minor fixes | SF, BS |
| V1.0 | 28.02.2008 | Initial Version | |

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# 1 Introduction

This document describes the set into operation procedure of the CompactRIO PROFIBUS DP module (cRIO PB) as DP-Slave.

## 1.1 Prerequisites:

- A COMSOFT cRIO PB module and COMSOFT cRIO PB driver software on CD
- National Instruments CompactRIO system with real time controller and chassis
- The National Instruments LabVIEW Real time and FPGA Development System from Version 8.5 installed on a Windows PC
- A PROFIBUS DP Master System connected to the cRIO PB Slave module.

*Note: The CompactRIO PROFIBUS DP modules require 2.5 W of power, so you must use it in Slot 1 while leaving Slot 2 empty.*

*Note: The CompactRIO PROFIBUS DP modules is supported only in CompactRIO reconfigurable chassis, such as an NI cRIO-911x, and NI Single-Board RIO devices.*

# 2 Installation

- Install the cRIO PB module in the CompactRIO chassis in slot 1
- Switch on the CompactRIO system
- Start the Setup from the COMSOFT driver CD delivered with the package
- Check with the NI MAX (Measurement & Automation explorer) the proper installation of the cRIO system:

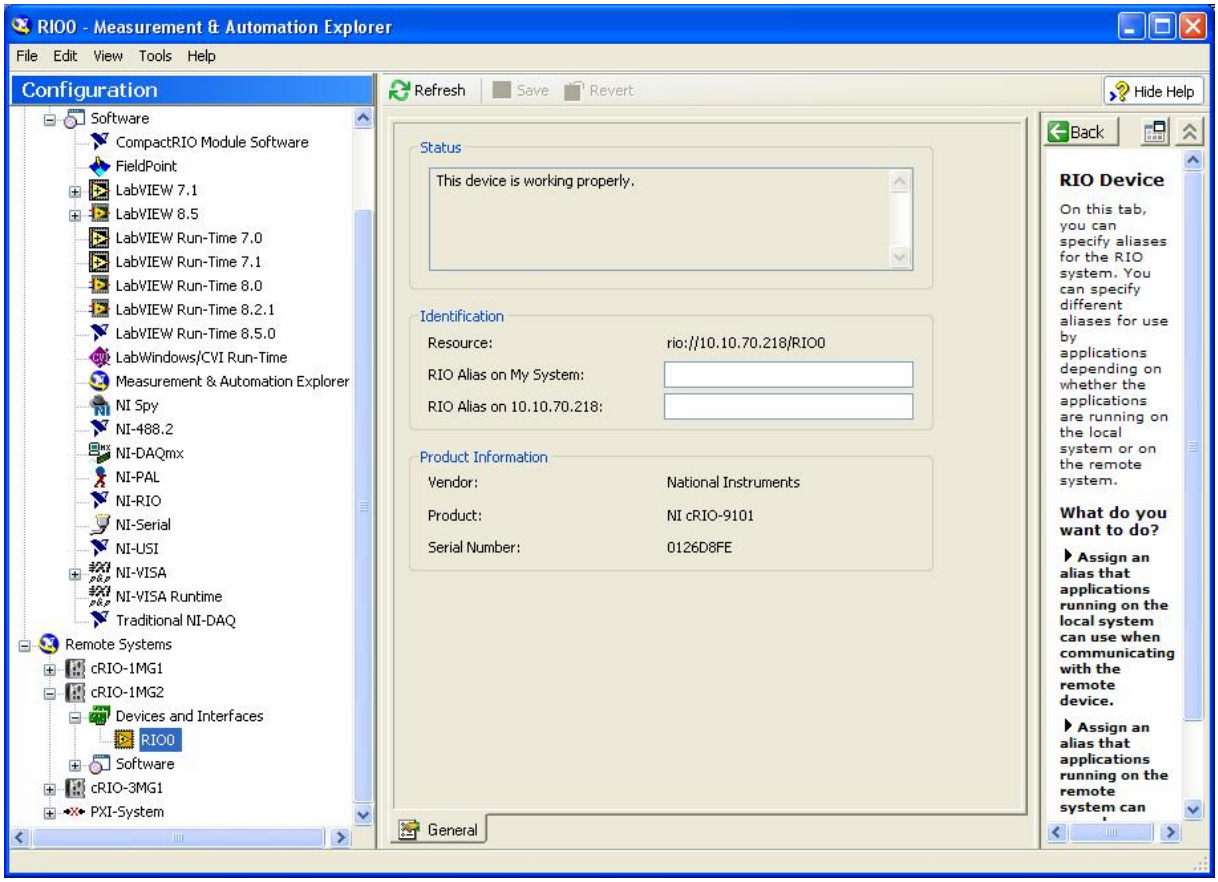



Figure 1: Measurement and Automation Explorer

*Note: The CompactRIO PROFIBUS DP modules require 2.5 W of power, so you must use it in Slot 1 while leaving Slot 2 empty.*
*Note: The cRIO PB module will not be displayed here.*

# 3 Configuring the DP Master with the cRIO PB Slave module

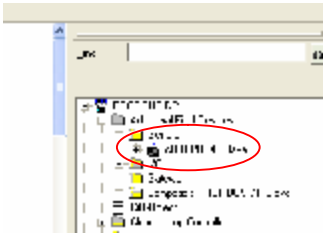
To get the cRIO PB Slave module into operation it has to be configured in the used DP Master system. The cRIO PB Slave module ships with a GSD file that can be imported in the DP Master configuration tool. The cRIO PB GSD file **COMS0B57.GSD** is located in the cRIO PB installation directory *[Program Files]\Comsoft GmbH\cRIO PB\GSD*.

Perform the following steps (example with Siemens S7 HW_KONFIG):

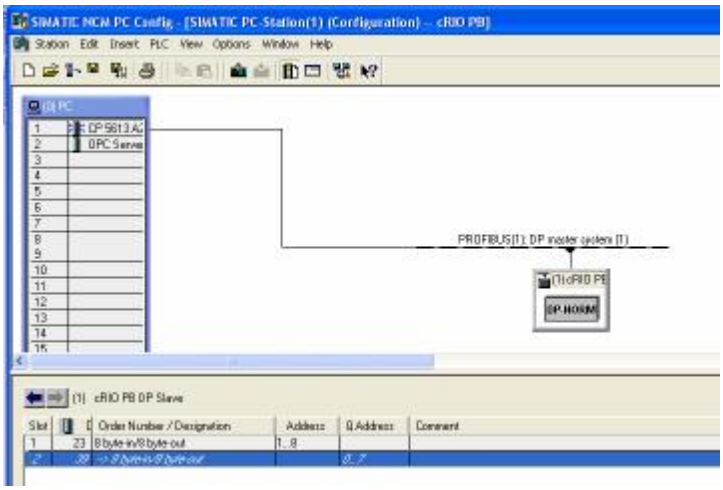
1. Import the **COMS0B57.GSD** file in the DP Master configuration tool

Figure 2: GSD Import with Siemens S7 HW Konfig

After importing the GSD file, the cRIO PB module can be located in the device catalogue:



2. Add the cRIO PB DP Slave to the DP Master system and select a slot module from the device catalogue. cRIO PB offers slot modules from 4 Byte input/4 Byte output up to 240 Byte input / 240 Byte output.



3. Store the DP Master configuration

# 4 cRIO PB Setting into Operation

Within scope of delivery basic driver VIs to communicate with the cRIO PB module on FPGA level are included. Additionally there are detailed sample VIs available using the basic driver VIs and demonstrating the following DP Slave functions:

- Configuring AutoSlaveMode
- Read and Write IO data from/to the cRIO PB Slave

Due to FPGA capacity reasons, the cRIO PB driver VIs use **FPGA memory** to exchange buffers in both directions with the cRIO PB module via the SPI bus.

The FPGA works as SPI Master, the cRIO PB module works as SPI Slave.

## 4.1 AutoSlaveMode

From firmware version 3.4.15 the cRIO PB module supports the so called AutoSlaveMode, which means, that the cRIO PB automatically activates DP Slave mode after power on and adopts the DP Master I/O configuration without any manual initialization. To activate the AutoSlaveMode the VI **CS_cRIO_PBS_FPGA_InitDP-Slave_AutoSlave.vi** within scope of delivery has to be used.

With the AutoSlaveMode not active, the cRIO PB module is compatible to previous driver versions. It is not recommended to use this operation mode for future applications.

To start the example project click onto the cRIO PB Slave icon in the COMSOFT start menu section:

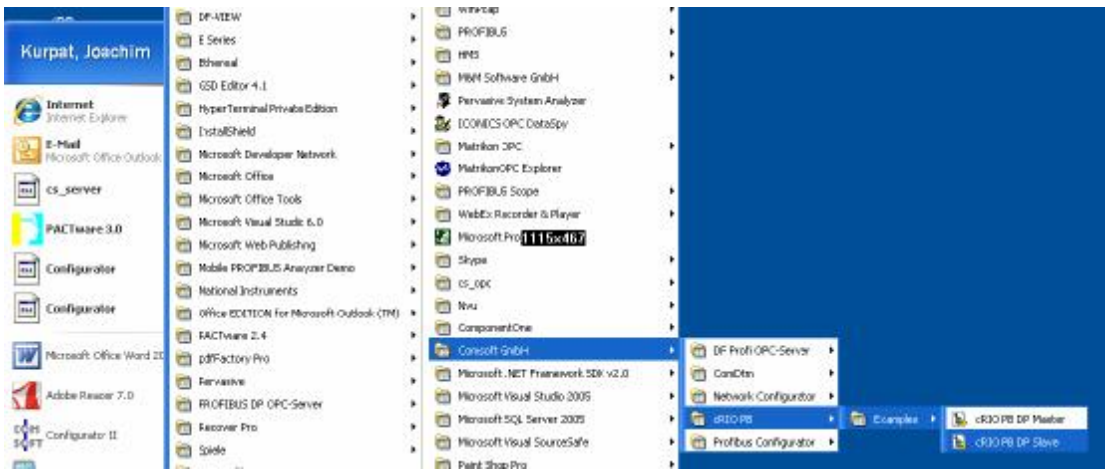



Figure 3: Open cRIO PB DP Slave example

- The FPGA example project opens:

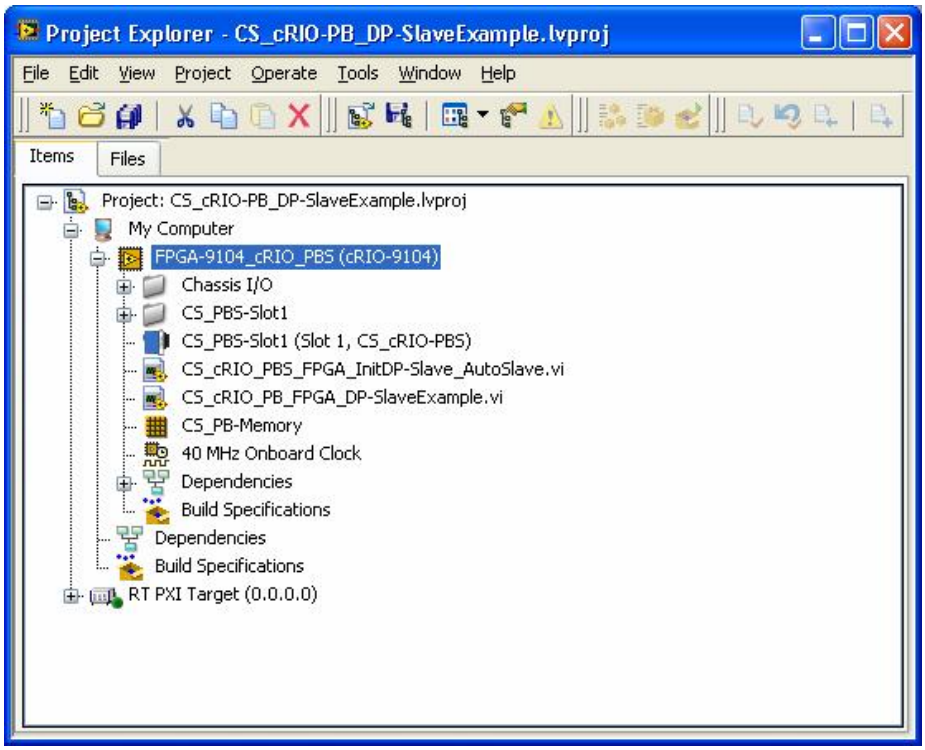



Figure 4: cRIO PBS Example project

- Open the VI CS_cRIO_PBS_FPGA_InitDP-Slave_AutoSlave.vi
- Run the VI

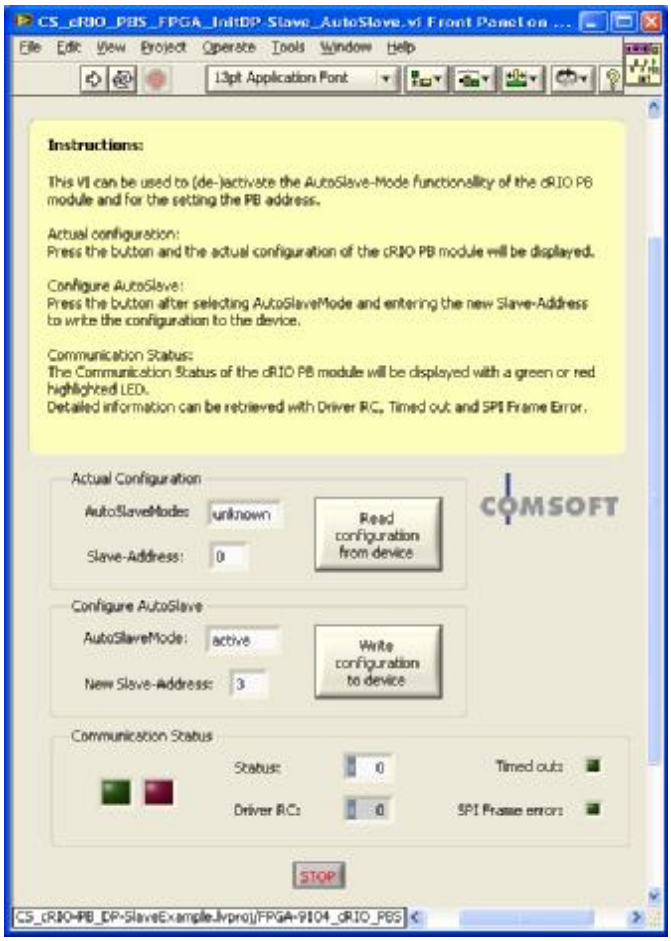



Figure 5: Open VI CS_cRIO_PBS_FPGA_InitDP-Slave_AutoSlave.vi

This VI can be used to (de-)activate the AutoSlaveMode functionality of the cRIO PB module and for the setting the PB address.

**Actual Configuration**

Reads the actual configuration (AutoSlaveMode active/inactive and the configured PROFIBUS address) from the cRIO PB module for information purposes

**Configure AutoSlave**

Writes the selected configuration (AutoSlaveMode active/inactive and the selected PROFIBUS address) to the cRIO PB module.
*Note: The configured PROFIBUS address is only valid with AutoSlaveMode activated*

**Communication Status**

The Communication Status informs about the successful configuration of the cRIO PB module and is displayed by a green (success) or red (failure) LED.

Detailed information about the communication status can be retrieved from Driver RC, Timed out and SPI Frame Error.

## 4.2 DP Slave example

The cRIO PB installation setup installs a LabVIEW FPGA example project from which all necessary components can be retrieved and copied to the own FPGA project.

*Note: To run the example, install the cRIO PB module in **Slot 1** of the cRIO chassis.*

- To start the example project click onto the cRIO PB DP Slave icon in the COMSOFT start menu section:

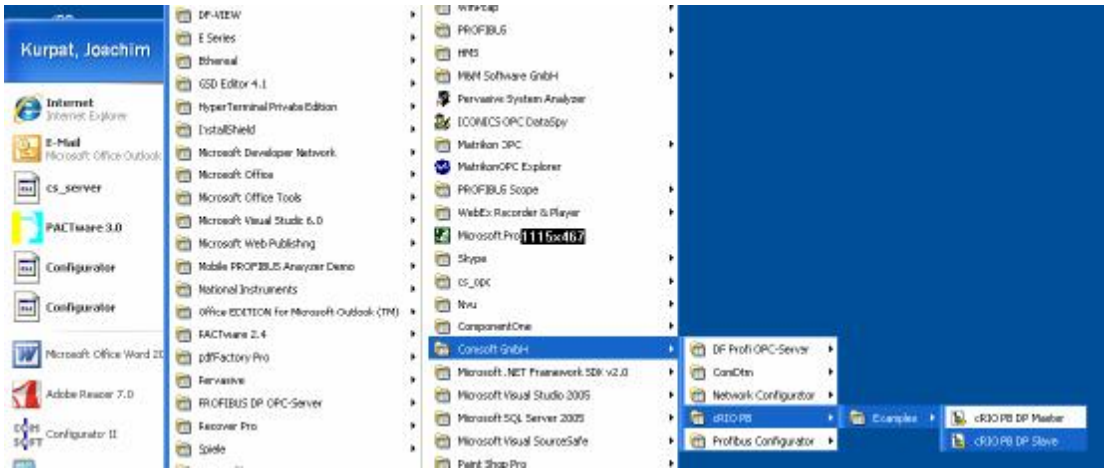



Figure 6: Open cRIO PB DP Slave example

- The FPGA example project opens:

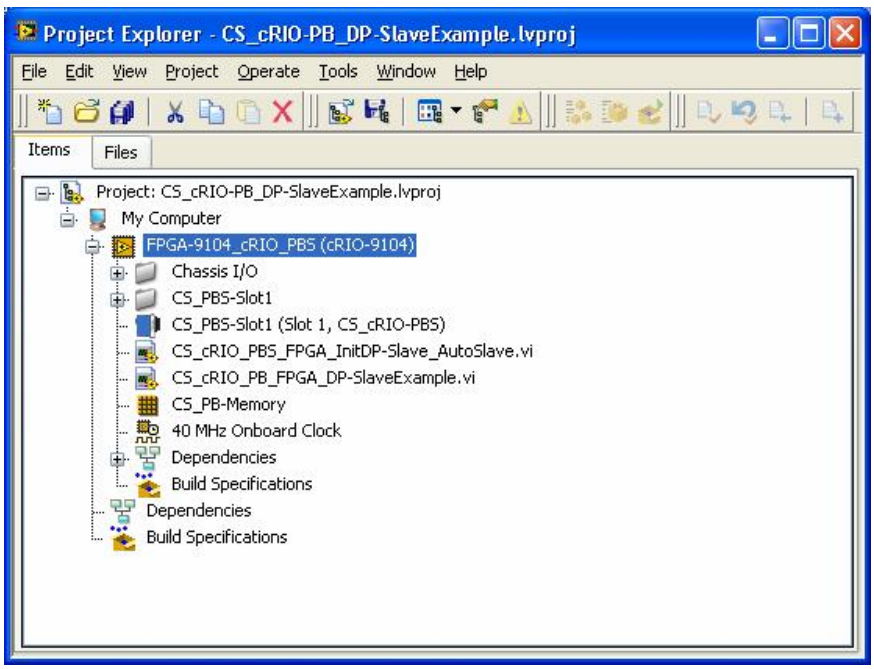



Figure 7: cRIO PBS Example project

- Create a new LabVIEW project on base of the used cRIO system:

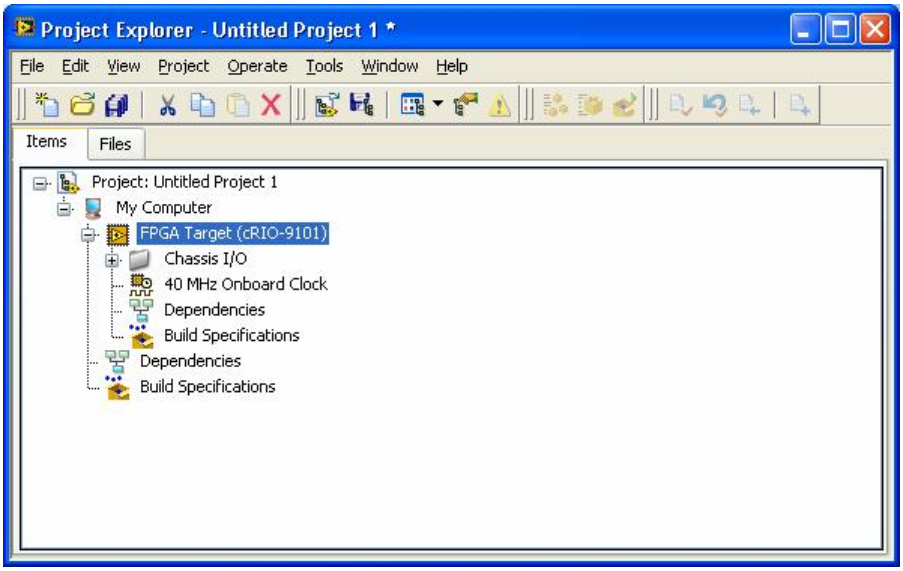



Figure 8: New LabVIEW cRIO FPGA project

- Copy the following components from the example project to the own project:
  - CS_PBS-Slot1
  - CS_PBS-Slot1 (Slot 1, CS_cRIO-PBS)
  - CS_PB-Memory
  - CS_cRIO_PB_FPGA_DP-SlaveExample.vi

The project now looks similar to:

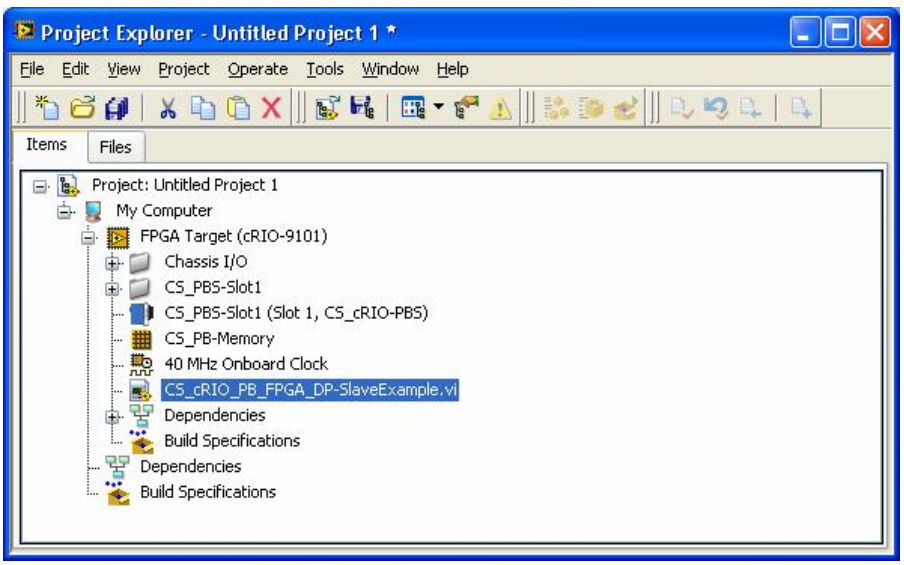



Figure 9: cRIO PB FPGA project

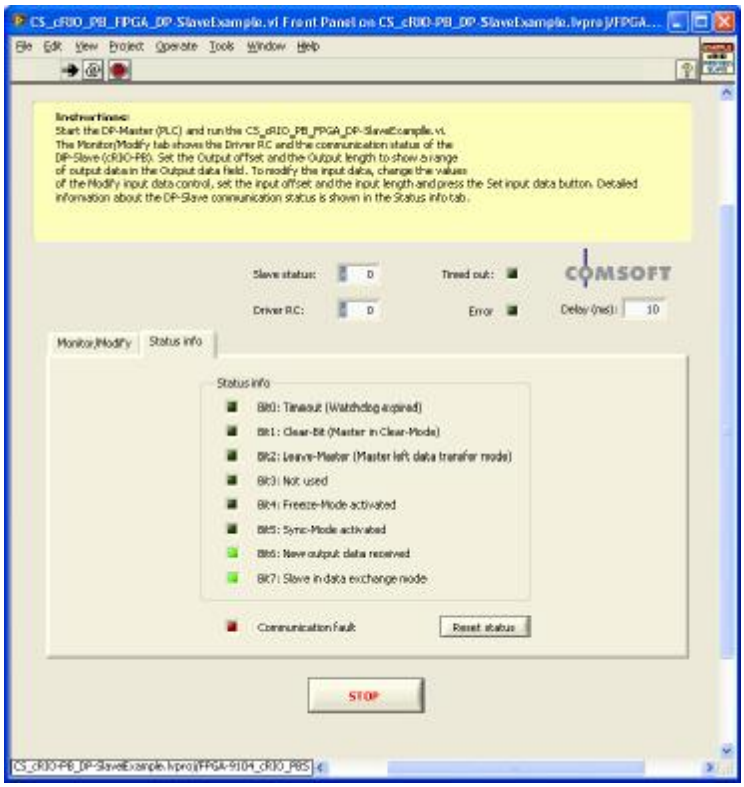
- Open the CS_cRIO_PB_FPGA_DP-SlaveExample.vi
- Run the example
- Switch to the Status info tab
- 


Figure 10: cRIO PB DP Slave example – status dialog

**Status info**

Displays the communication status of the slave.

*Bit7: Slave in data exchange mode* must be switched on.

*Bit6: New output data received* may be switched on, if the DP Master updates the cRIO PB DP slave output data with new values.

If *Bit7* is not switched on, the cRIO PB DP Slave does not exchange data with the DP Master.

See detailed information in chapter 5.2.2.3.

- If the cRIO PB Slave is in data exchange mode switch to the Monitor/Modify tab

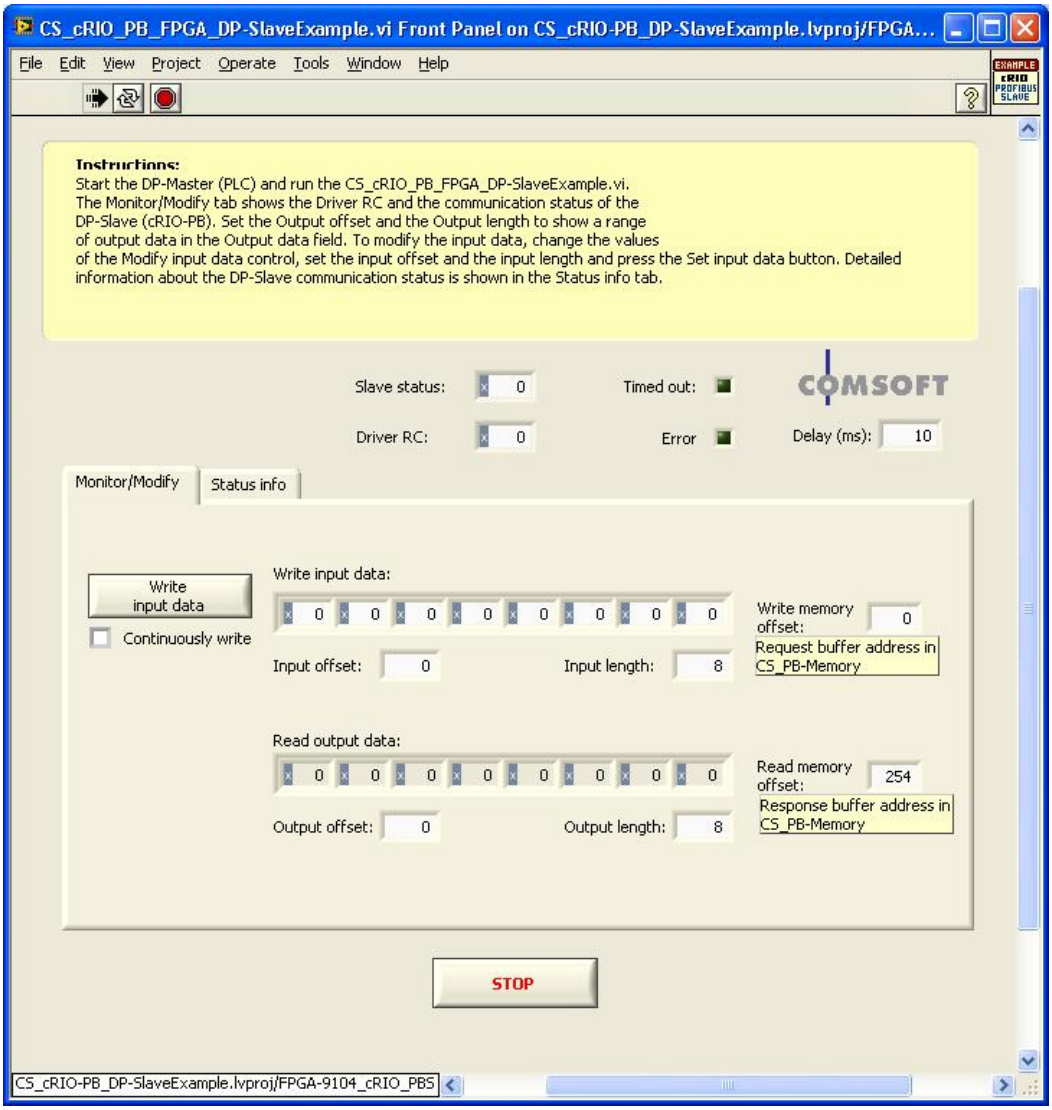



Figure 11: cRIO PB DP Slave example – Input/Output dialog

**Driver RC**

Displays the communication status of the cRIO PB module. (see chapter 5.2.2.2 for detailed information.

*Note: If Driver RC is not 0, cRIO PB DP Slave related Input- and Output data are not valid.*

**Timed Out**

SPI communication time out

**Error**

SPI Frame error

**Write input data**

The *Write input data* section assigns the slaves input data, which are transmitted **to** the DP Master. The array control storing the input data is limited to 8 Bytes due to FPGA capacity. By the parameters **Input Offset** and **Input Length** any input data in the slaves input data stream can be modified. The input data are modified by clicking on to the button *Write input data*. The offset can be used for optimization. The data block can be partially addressed and not the whole length has to be transmitted with every update.

*Note: Don't assign a length greater than the real input data length of the cRIO PB DP Slave. The length complies with the used slot module (in the example here **8byte-in**/8byte-out) in the DP Master configuration tool (see chapter 0 ff.). The length is not checked due to FPGA capacity.*

**Read Output data**

The Output data are received **from** the DP Master and displayed. The array indicator to display the slave output data is limited to 8 Bytes due to FPGA capacity. By the parameters **Output Offset** and **Output Length** any output data in the slave output data stream can be displayed. The offset can be used for optimization. The data block can be partially addressed and not the whole length has to be transmitted with every update.

*Note: Don't assign a length greater than the real output data length of the cRIO PB DP Slave. The length complies with the used slot module (in the example here 8byte-in/**8byte-out**) in the DP Master configuration tool (see chapter 0 ff.).The length is not checked due to FPGA capacity.*

**Write memory offset**

The *Write memory offset* is the address of the request header and output data in the CS_PB-Memory.

**Read memory offset**

The *Read memory offset* is the address of the response header and input data in the CS_PB-Memory.

# 5 cRIO PB SPI Interface description

The data exchange between the FPGA module and cRIO PB module is based on Master/Slave SPI communication. The FPGA acts as a SPI Master, the cRIO PB acts as a DP Slave.

The FPGA module exchanges buffers with the cRIO module in both directions whereas the FPGA module sends a **Request Buffer** and the cRIO PB module answers with a **Response Buffer**.

With a single driver call Input data are transmitted to the cRIO PB Slave module and Output data and status information are received from the cRIO PB Slave module.

The central driver VI *CS_cRIO_PBS[1]FPGA_SPI_ReadWrite.vi* 

transmits the request buffer to the cRIO PB Slave module and returns the response buffer received from the cRIO PB Slave module.

The *CS_cRIO_PBS[1]FPGA_SPI_ReadWrite.vi* uses a byte oriented (U8) FPGA memory block named **CS_PB-Memory**. This block is mandatory and must be allocated within the LabVIEW FPGA project:

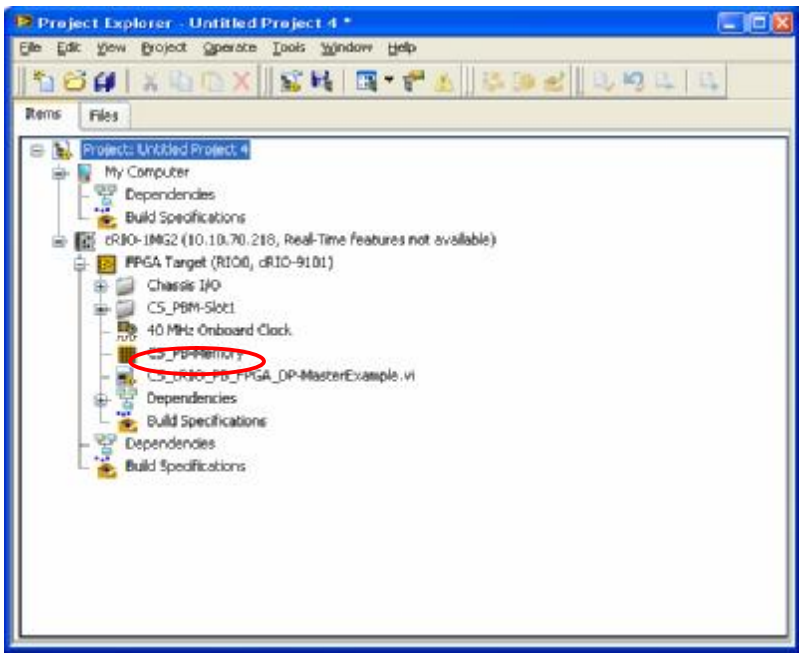



Figure 12: CS-PB-Memory in cRIO FPGA project

The minimum size of the **CS_PB-Memory** is **254 bytes (U8)** storing the header and the max. Input- and Output data for the cRIO PB Slave module with overlapping request- and response buffers. If separate request- and response buffers are used, the minimum size is **508 bytes (U8)**. See chapter 5.1 for details.

# 5.1 Driver VI description

The cRIO PB driver VI  handles the bidirectional SPI based communication between the FPGA module and cRIO PB module. The driver VI uses a FPGA memory buffer named **CS_PB-Memory**. This name is mandatory and cannot be changed.

To use the driver VI, 3 steps are necessary:

1. Prepare the Request buffer with header and data field in the **CS_PB-Memory**
2. Call the driver VI
3. Check the error and time out parameters

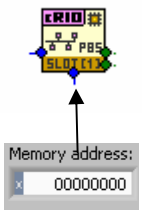
   Decode the header and the data field in the Response buffer in **CS_PB-Memory**

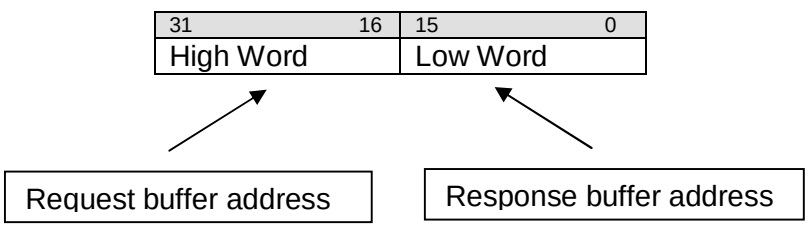
## 5.1.1 Parameters

### 5.1.1.1 Memory address

The CS_PB-Memory buffer stores the **Request buffer** as well as the **Response buffer**. To optimize the necessary amount of memory the 2 buffers can be used as overlapping or separate buffers.

To control the buffer allocation the input parameter **Memory address** is used. **Memory address** is a 32 Bit value, where the high word assigns the offset for the **Request buffer** and the low word the offset for the **Response buffe**r in CS_PB-Memory**.**



Examples:

| Memory address | Description |
|---|---|
| 0x00000000 | Overlapping Request- and Response buffer, both buffers start at address 0 in CS_PB-Memory.<br>The Request buffer is overwritten by the incoming Response buffer.<br>Necessary buffer size of CS_PB-Memory is 254 Bytes [U8] |
| 0x000000FE | Separate Request- and Response buffer.<br>Request buffer starts at address 0.<br>Response buffer starts at address 254 (00FE).<br>The Request buffer is not overwritten by the incoming Response buffer.<br>Necessary buffer size of CS_PB-Memory is 508 Bytes [U8]. |

*Note: The minimum size of CS_PB-Memory is **254** Bytes.*

### 5.1.1.2 Timeout

Timeout value in ms. Specifies how long to wait for the response from the cRIO PB module.

### 5.1.1.3 Timed Out

If the cRIO PB module does not respond and the timeout expires the driver VI returns *Timed Out* = TRUE otherwise *Timed Out* = FALSE. If *Timed Out* = TRUE the data in the Response buffer is not valid.

### 5.1.1.4 Error

If wrong or corrupt data are received from the cRIO PB module the driver VI returns *Error* = TRUE otherwise *Error* = FALSE. If *Error* = TRUE the data in the Response buffer are not valid.

# 5.2 Buffer structure

## 5.2.1 Request buffer

The request buffer, transmitted to the cRIO PB module consists of a constant 14 byte header and a variable data field.

*Note: All 2 Byte values (U16) are in little Endean format, that means they must be written in high byte/low byte order to the buffer.*

| Header | Data field |
|---|---|

### 5.2.1.1 Header structure

| Index | Format | Size | Description | Details |
|---|---|---|---|---|
| 0 | U8 | 1 Byte | Command | cRIO PB specific Command |
| 1 | U8 | 1 Byte | cRIO PB Slave address | 0-125 |
| 2-3 | U16 | 2 Byte | Output offset | 0-239 |
| 4-5 | U16 | 2 Byte | Output length | 0-240 |
| 6-7 | U16 | 2 Byte | Input offset | 0-239 |
| 8-9 | U16 | 2 Byte | Input length | 0-240 |
| 10 | U8 | 1 Byte | Reserved | 0 |
| 11 | U8 | 1 Byte | Reserved | 0 |
| 12 | U8 | 1 Byte | Clear slave status | See chapter 5.2.1.3 |
| 13 | U8 | 1 Byte | Reserved | 0 |

### 5.2.1.2 Command description

| Value | Description | Parameters |
|---|---|---|
| 0x82 | **READ_WRITE_SLAVE** – Transmits input data to cRIO PB DP Slave and receives output data from cRIO PB DP Slave | **Output length:** Size of cRIO PB DP Slave output data received from DP Master<br>*The value may not exceed the **real output data length** of the cRIO PB DP Slave*<br>**Output Offset:** Offset in cRIO PB DP Slaves output data stream<br>*The value may not exceed the **real output data length -1** of the cRIO PB DP Slave*<br>**Input Length**: Size of cRIO PB DP Slave Input data transmitted to the DP Master<br>*The value may not exceed the **real input data length** of the cRIO PB DP Slave.*<br>**Input Offset:** Offset in DP Slave input data stream<br>*The value may not exceed the **real input data length -1** of the cRIO PB DP Slave* |

### 5.2.1.3 Reset Status

Reset Status allows resetting the cRIO PB Slave Status bits described in chapter 5.2.2.3. Every bit set to 1 will reset the corresponding status bit in the cRIO PB Slave.

e.g.: The cRIO PB Slave sets bit 6 in the slave status to indicate that the DP Master updated the output data with new values. Bit 6 will not be reset by the cRIO PB Slave automatically. Only if the application sets bit 6 in the Clear Slave Status within the next READ_WRITE_SLAVE command, cRIO PB Slave will reset the slave status bit 6.

#### 5.2.1.4 Data field

The data field is byte oriented (U8) and stores the input data transmitted to the cRIO PB Slave

| |
|---|
| Byte 1 |
| Byte 2 |
| Byte 3 |
| .. |
| Byte n |

### 5.2.2 Response buffer

The response buffer received from the cRIO PB Slave module consists of a constant 14 byte header and a variable data field.

| Header | Data field |
|---|---|

*Note: All 2 Byte values (U16) are in little Endean format, that means in high byte/low byte.*

#### 5.2.2.1 Header structure

| Index | Format | Size | Description | Details |
|---|---|---|---|---|
| 0 | U8 | 1 Byte | Command | Same value as in request buffer |
| 1 | U8 | 1 Byte | cRIO PB DP Slave address | Same value as in request buffer |
| 2-3 | U16 | 2 Byte | Output offset | Same value as in request buffer |
| 4-5 | U16 | 2 Byte | Output length | Same value as in request buffer |
| 6-7 | U16 | 2 Byte | Input offset | Same value as in request buffer |
| 8-9 | U16 | 2 Byte | Input length | Same value as in request buffer |
| 10 | U8 | 1 Byte | Reserved | 0 |
| 11 | U8 | 1 Byte | Reserved | 0 |
| 12 | U8 | 1 Byte | Slave status | See chapter 5.2.2.3 below |
| 13 | U8 | 1 Byte | Driver RC | See chapter 5.2.2.2 below |

#### 5.2.2.2 Driver RC

The Driver RC assigns the communication status of the cRIO PB module.

*Note: If Driver RC is not 0, DP Slave related Input and Output data are not valid.*

| Value | Description | Reason | Help |
|---|---|---|---|
| 0x00 | No errors | cRIO PB module works without any problems | - |
| 0x01 | Error at undefined location | unknown | The error is not handled. Verify functionality with the standard examples and Contact Comsoft Support |
| 0x02 | Unknown command value | The 'command' value in the request header / contains an unknown value | Verify the request header and the correct transfer to the driver VI. The commands are listed in chapter 5.2.1.2. |
| 0x13 | cRIO PB module does not support DP Master mode | The cRIO PB Slave module is configured for operation only as DP Slave and not as DP Master/DP Slave | Contact Support |
| 0x14 | cRIO PB module hardware error | The B.I.S.T of the cRIO PB module reported a hardware error. The module is not operable. | Contact Support |
| 0x15 | cRIO PB module in AutoSlaveMode | cRIO PB module in AutoSlaveMode (no start as DP Master or former DP Slave mode possible) | Deactivate AutoSlaveMode (see chapter 4.1) |
| 0x17 | cRIO PB module not active | cRIO PB not initialized as DP Master or AutoSlaveMode not active | Activate AutoSlaveMode (see chapter 4.1) |

### 5.2.2.3 Slave status

The Slave status indicates the communication status of the cRIO PB Slave. The status value consists of 8 separate bits. The status is active if the bit is set to 1.

Bit 0, Bit 1 and Bit 2 indicate the reason why the cRIO PB Slave does not exchange data with DP Master.

Bit 7 must be set for normal operation otherwise Input- and Output data are not valid.

| Value | Description | Reason | Help |
|---|---|---|---|
| Bit 0 | Timeout | Timeout expired because of missing or too slowly scanning DP Master | Check DP Master<br>Switch off DP Slave related timeout in DP Master configuration<br>Increase calculated timeout value in the DP Master Parameter set |
| Bit 1 | Clear-Bit | DP Master does not reach operation mode but stays in clear mode | Check DP Master |
| Bit 2 | Leave-Master | DP Master stopped scanning the DP Slaves | Check DP Master |
| Bit 3 | Reserved | | |
| Bit 4 | Freeze Mode activated | DP Master activated the Freeze mode | cRIO PB Slave does not update the Output data until the DP Master deactivates the Freeze mode |
| Bit 5 | Synch Mode activated | DP Master activated the Synch mode | cRIO PB Slave does not update the Input data until the DP Master deactivates the Synch mode |
| Bit 6 | New output data received | DP Master updated output data with new values | - |
| Bit 7 | Slave in data exchange mode | DP Master exchanges data with DP Slave | If Bit 7 is **not** set, Input- and Output data are not valid |

#### 5.2.2.4 Data field

The data field is byte oriented (U8) and stores the output data received from the DP Master. The count of output data received is indicated by the header member *output_length*.

| |
|---|
| Byte 1 |
| Byte 2 |
| Byte 5 |
| .. |
| Byte n |

# 5.3 Buffer examples

## 5.3.1 READ_WRITE_SLAVE- Input and Output data

Transmits input data to DP Master and receives output data from DP Master.

cRIO PB Slave with address 16 and 4 Bytes output data and 8 Bytes input data. All input data are written and all output data are read.

| Request Buffer | | | Response Buffer | | |
|---|---|---|---|---|---|
| Index | Value | Description | Index | Value | Description |
| 0 | 0x82 | Command | 0 | 0x82 | Command |
| 1 | 0x10 | Address | 1 | 0x10 | Address |
| 2 | 0x00 | Output Offset HB | 2 | 0x00 | Output Offset HB |
| 3 | 0x00 | Output Offset LB | 3 | 0x00 | Output Offset LB |
| 4 | 0x00 | Output Length HB | 4 | 0x00 | Output Length HB |
| 5 | 0x04 | Output Length LB | 5 | 0x04 | Output Length LB |
| 6 | 0x00 | Input Offset HB | 6 | 0x00 | Input Offset HB |
| 7 | 0x00 | Input Offset LB | 7 | 0x00 | Input Offset LB |
| 8 | 0x00 | Input Length HB | 8 | 0x00 | Input Length HB |
| 9 | 0x08 | Input Length LB | 9 | 0x08 | Input Length LB |
| 10 | 0x00 | Reserved | 10 | 0x00 | Reserved |
| 11 | 0x00 | Reserved | 11 | 0x00 | Reserved |
| 12 | 0x00 | Clear Slave Status | 12 | 0x00 | Slave Status |
| 13 | 0x00 | Reserved | 13 | 0x00 | Driver RC |
| Request Buffer Data Field | | | Response Buffer Data Field | | |
| 14 | XX | Input Byte 1 | 14 | YY | Output Byte 1 |
| 15 | XX | Input Byte 2 | 15 | YY | Output Byte 2 |
| 16 | XX | Input Byte 3 | 16 | YY | Output Byte 3 |
| 17 | XX | Input Byte 4 | 17 | YY | Output Byte 4 |
| 18 | XX | Input Byte 5 | | | |
| 19 | XX | Input Byte 6 | | | |
| 20 | XX | Input Byte 7 | | | |
| 21 | XX | Input Byte 8 | | | |

### 5.3.2 READ_WRITE_SLAVE – Output data

Receives output data from DP Master.

cRIO PB Slave with address 16 and 4 Bytes output data. No input data are written and all output data are read.

| Request Buffer | | | Response Buffer | | |
|---|---|---|---|---|---|
| Index | Value | Description | Index | Value | Description |
| 0 | 0x82 | Command | 0 | 0x82 | Command |
| 1 | 0x10 | Address | 1 | 0x10 | Address |
| 2 | 0x00 | Output Offset HB | 2 | 0x00 | Output Offset HB |
| 3 | 0x00 | Output Offset LB | 3 | 0x00 | Output Offset LB |
| 4 | 0x00 | Output Length HB | 4 | 0x00 | Output Length HB |
| 5 | 0x04 | Output Length LB | 5 | 0x04 | Output Length LB |
| 6 | 0x00 | Input Offset HB | 6 | 0x00 | Input Offset HB |
| 7 | 0x00 | Input Offset LB | 7 | 0x00 | Input Offset LB |
| 8 | 0x00 | Input Length HB | 8 | 0x00 | Input Length HB |
| 9 | 0x00 | Input Length LB | 9 | 0x00 | Input Length LB |
| 10 | 0x00 | Reserved | 10 | 0x00 | Reserved |
| 11 | 0x00 | Reserved | 11 | 0x00 | Reserved |
| 12 | 0x00 | Reserved | 12 | 0x00 | Slave Status |
| 13 | 0x00 | Reserved | 13 | 0x00 | Driver RC |
| Request Buffer Data Field | | | Response Buffer Data Field | | |
| | | | 14 | YY | Output Byte 1 |
| | | | 15 | YY | Output Byte 2 |
| | | | 16 | YY | Output Byte 3 |
| | | | 17 | YY | Output Byte 4 |