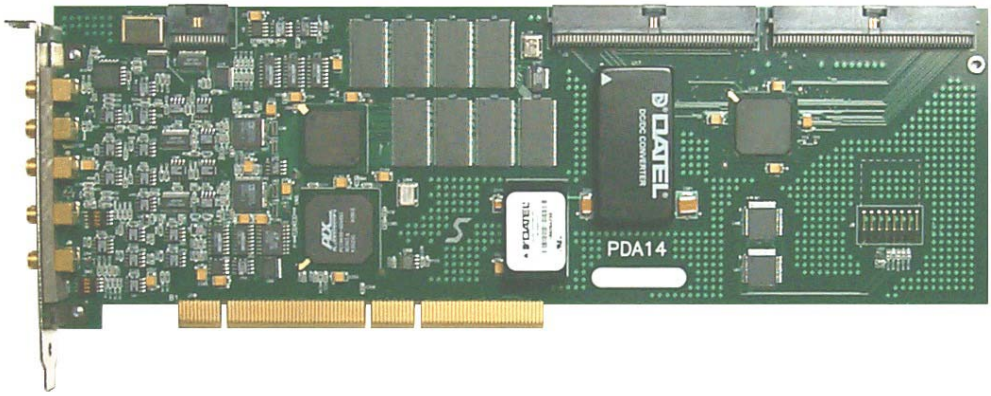
Product Information Sheet

PDA14

2 Channel, 14-Bit Waveform Digitizer



FEATURES

- 2 Channels at up to 100 MHz Sample Rate
- 14 Bits of Resolution
- Bandwidth from DC-50 MHz
- 512 Megabytes of On-Board Memory
- 500 MB/s Transfer via Signatec Auxiliary Bus (SAB)
- 266 MB/s Transfer (Peak) Over PCI Bus
- 64/32 Bit PCI Plug and Play Compatible Board

APPLICATIONS

- Radar
- Mass Spectroscopy
- Mass Spectrometry – Time of Flight
- Communications
- Ultrasound
  Medical Diagnostics / Non Destructive Testing
- Laser Doppler Velocimetry
- High Speed Waveform Capture

OVERVIEW

The PDA14 is a dual channel waveform capture board which provides a tremendous combination of high speed and high resolution along with an extremely large memory capacity. The entire 512 MB memory may be used as a giant FIFO for acquiring data directly to either the SAB or PCI bus. Tests have shown that a very large FIFO memory is required to prevent data loss when performing continuous data streaming over the PCI bus.

The PDA14 is a 64-bit PCI compatible board equipped with standard 'Plug and Play' features common in PCI systems. It is capable of Bus Master DMA data transfers at up to a peak of 266 megabytes/second and a sustained rate of 250 megabytes/second. It can also operate in 32-bit PCI slots in which case the transfer rate will be limited to about 125 megabytes per second.

The PDA14 incorporates the advanced Signatec Auxiliary Bus (SAB) that allows for data transfers of up to 500 megabytes/second. This allows for the high-speed transfer of data to fast processor boards, such as Signatec's PMP8A, or other peripherals. The SAB also incorporates device control features for operating the PDA14 independent of the host bus.

The PDA14 is equipped with an interconnect port to allow multiple boards to be interconnected in a Master/Slave configuration. Up to three Slave boards may be operated with one Master. Master/Slave connections are via a ribbon cable that connects at the top of the board. In this configuration the clock and trigger signals from the Master drive the Slave boards so that data sampling on all boards occurs simultaneously.

The PDA14 has six software selectable signal amplitude ranges from a maximum of 3.0 volts down to 200 millivolts full scale.

External clock and trigger signals are provided via SMA connectors on the back bracket. Also provided is a user selectable digital output signal for synchronization purposes. Effectively, twenty-two internal clock frequencies may be selected, from 100 MHz down to 97.7 kHz in factors of 2 or from 62.5 MHz down 61.0 kHz in factors of 2. The PDA14 supports single shot, segmented, and pretrigger triggering modes.

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HARDWARE DESCRIPTION

The figure on the next page shows a simplified mechanization for the PDA14. The input signals may be set for either DC or AC coupling. The signal conditioning provides six voltage ranges from 200 millivolts to 3.0 volts peak-to-peak full scale. A low pass filter sets the channel bandwidth to 50 MHz. For test purposes, the ADC input may be fed a sine wave test signal (not shown) for measuring the AC performance at 25 MHz.

The data input to RAM FIFO 1 can be considered to be two separate 16-bit data streams. The latches and multiplexers at the output of the ADCs allows for capturing data from both channels or from channel 1 only or channel 2 only.

The Pretrigger Samples Shift Registers are programmable in length up to 4k samples. They can be used to capture pretrigger samples in either the Single Shot or Segmented trigger modes. Before a trigger is received, data is written into the shift registers but goes no further. After receiving a trigger, data samples start to be written into RAM FIFO 1. See the section "Trigger Modes and Options" for trigger mode details.

The ADCs always operate at either 100 MHz or 62.5 MHz when the internal clock is used or else at the external clock frequency. Operation at reduced rates is accomplished by dropping out the appropriate data bytes from the data stream. Thus the effective sample rate is divided from 2 to 1024 in factors of 2.

Data is written into the SDRAM via FIFO1 and read from RAM via FIFO2. The RAM operates at a clock rate of 133 MHz so it has a bandwidth capability of slightly greater than 500 MB/s. When data is being acquired at a rate of 250 MB/s or less (62.5 MHz on 2 channels or 100 MHz on single channel), it is possible to operate the board in Buffered Acquisition mode. In this mode the RAM is operated as a very large FIFO for acquiring data directly to the PCI bus or SAB.

The PDA14 has 12 operating modes as follows:

- Standby
- Acquisition to RAM
- Acquisition to PCI Bus
- Buffered Acquisition to PCI bus (RAM as FIFO)
- Acquisition to SAB
- Buffered Acquisition to SAB (RAM as FIFO)
- Data Transfer, RAM to PCI bus
- Data Transfer, RAM to SAB
- Write RAM (from PCI bus)
- Write RAM (from SAB)
- Read Time Stamps (from PCI bus)
- Read Time Stamps (from SAB)

The RAM write mode is typically used to test the on-board memory by writing data via the PCI bus and reading back via a RAM-to-PCI transfer.

External Inputs/Outputs

Besides the signal input, the PDA14 also provides SMA connections for a clock input, a trigger input, and a digital output signal. The clock input can be selected as the ADC sample clock. The external trigger can be used to synchronize the start of data acquisition with an external event. Trigger parameters such as trigger level, slope, etc. are user programmable. The digital output is a user selectable signal. The list of selections is TBD.

Trigger Modes and Options

In data acquisition mode three triggering modes are available: single shot, segmented, or pretrigger. In the single shot mode, following the detection of a trigger signal, all of the active memory is filled. In the segmented mode a separate trigger signal is required to successively fill each memory segment until all of the active memory is filled. In the pretrigger mode the board is armed and continuously fills the entire active memory until a stop trigger is detected, after which a programmed number of post trigger samples are taken before acquisition is terminated. The pretrigger mode may be used to see signal information both before and after the trigger signal.

Samples Settings

There are several board settings that affect the quantity and method of acquiring samples.

Active Memory Size – In the "post-trigger modes" this is the number of samples that will be taken after which the memory will be considered "full" and the acquisition is terminated. When a full condition is detected, a flag is set which may be read by the PC or software selected to cause a PC interrupt or send an interrupt over the SAB. The amount of memory that is activated for data acquisition may be set from 8 bytes to the full 512 megabytes in steps of 8 bytes.

Segment Size – In Segmented Mode this is the number of samples that will be taken each time a valid trigger signal is detected.

Pretrigger Samples – In Single Shot or Segmented Modes, this is the number of samples that will be recorded into RAM that occurred before the trigger.

Delayed Trigger – This sets a delay between the actual applied trigger and the effective trigger for the board. The delay range is from 0 to 64k digitizer clock cycles. In Pretrigger Samples mode the delayed trigger setting establishes the number of post-trigger samples that will be recorded.

Time Stamps

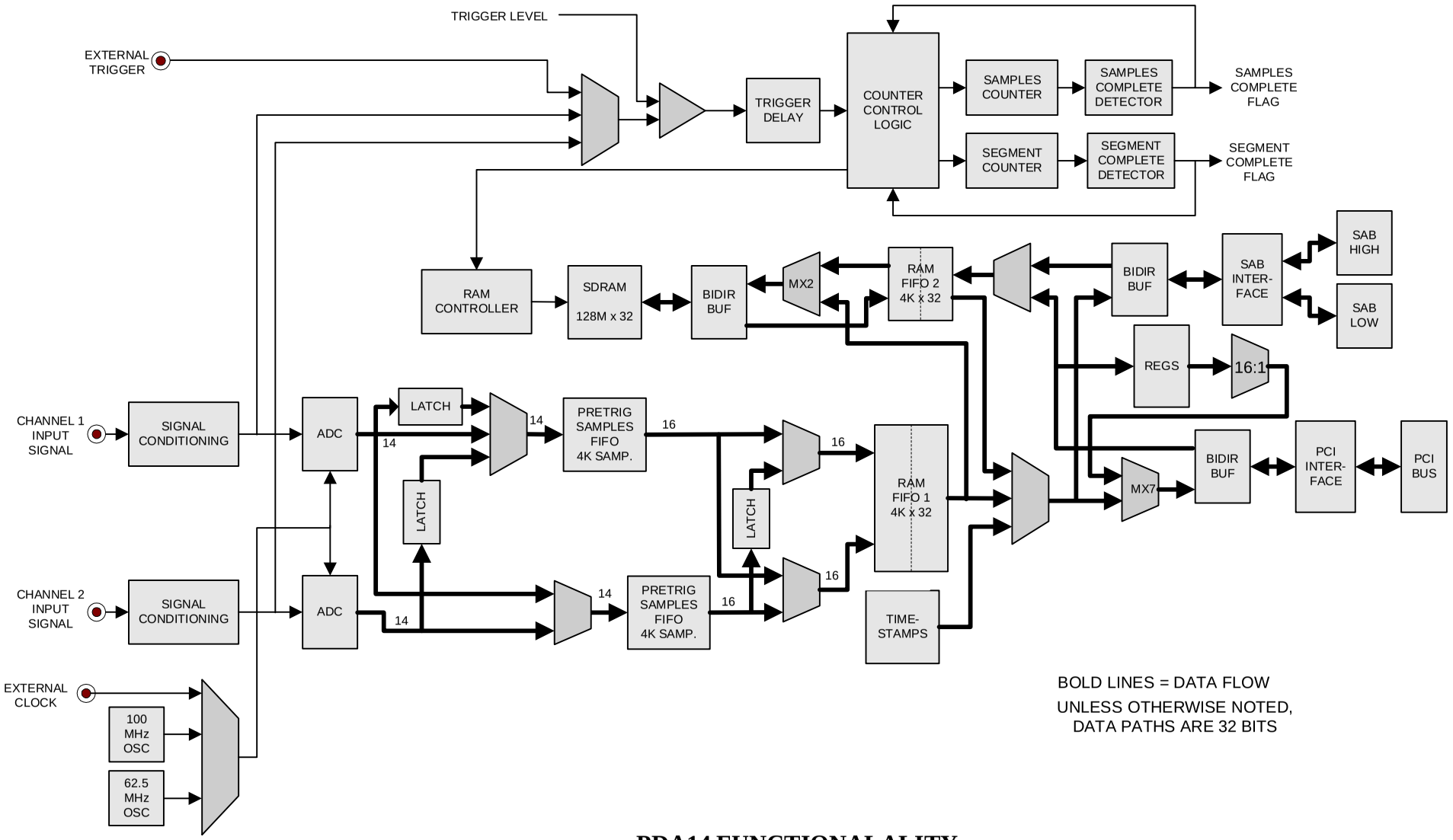
In Segmented Mode "time stamps" allow for storing the time relationship between the memory segments. Time Stamps are 32 bit timer values with a clock resolution of 7.5 nanoseconds. Up to 2048 time stamps are accumulated in memory separate from the data. Time stamps are read after the acquisition is completed.

SAB Operation

The PDA14 can perform SAB data transfers at 64 bits, or at 32 bits over either the high (SABH) or low (SABL) bus ports. This provides flexibility when multiple boards are incorporated into a system. At 64 bits the maximum transfer rate is 500 MB/s.

PCI Operation

The PDA14 is capable of sustaining a long-term data-transfer rate, over the PCI bus, of 250 megabytes per second when installed in a 64 bit PCI slot. It can also be installed in traditional 32-bit slots in which case the maximum rate is about 125 megabytes per second.



PDA14 FUNCTIONALALITY

SOFTWARE, SYSTEM, AND PERFORMANCE DETAILS

Software

The PDA14 is supplied with the following software:

- Windows NT/2000/XP and Linux Drivers
- C Function Library with source code
- PDA14 Class (C++) that wraps the Library functions and handles the tedious initializations and basic operations.
- Software manual that describes how to use the available library of functions to create larger applications or systems.
- A board diagnostics self test program.
- Multiple Coding examples
  - ✓ Acquire with DMA transfer to PC
  - ✓ Digital oscilloscope interface software
  - ✓ Using multiple PDA14 boards (with Master/Slave support)
  - ✓ SAB data transfer examples

Maestro support for the PDA14

- Menu driven board settings for multiple PDA14 boards
- Using the PDA14 as a high-speed recording system
- Using the PDA14 as a high-speed recording system with the PMP8A (or any other SAB Active Slave capable device)
- Data Analysis tools for poking/peeking onboard memory

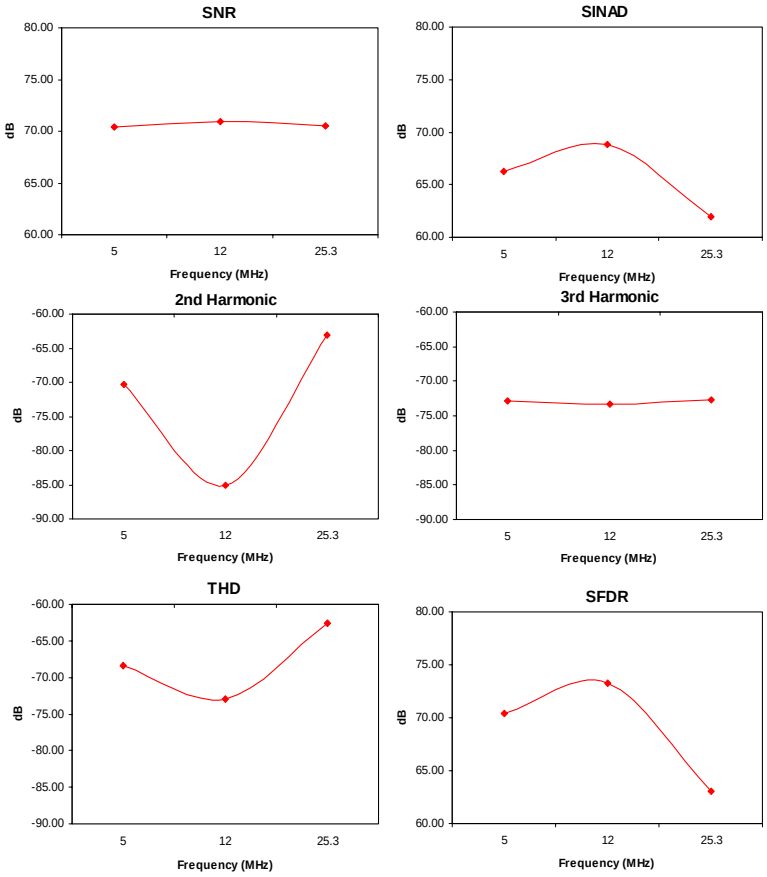
System Capabilities

The system solution offered by Signatec is based on supplying a comprehensive range of products incorporating the Signatec Auxiliary Bus. This 64-bit bus provides transfer rates up to 500 MB/s. SAB boards act as modular building blocks for constructing high performance systems that mechanize a wide variety of applications. Shown in the figure below are elements of such a system. Many systems can be constructed using standard desktop PC's. For demanding applications Signatec can supply a total turnkey system utilizing one of our industrial computer systems.

Devices connected to the SAB may communicate via SAB interrupt and control lines. This allows the boards to accomplish multiple acquisition, transfer, and processing cycles under control of the signal processor device, without PC intervention. Bypassing the host bus and operating system can significantly improve system performance.

Typical Performance

(dB versus Frequency in MHz)



DEFINITION OF TERMS

SINAD: Signal to Noise and Distortion: The ratio of the fundamental sinusoidal signal power to the total noise and distortion component power. In other words this is the ratio of the fundamental signal power to the measured power from the remainder of the detectable spectrum from dc to 50 MHz.

SNR: Signal to Noise Ratio: The ratio of the fundamental sinusoidal signal power to the noise power. For this data sheet noise is considered to be the power from all spectral components except for the fundamental signal, the first harmonic, and the second harmonic.

THD: Total Harmonic Distortion: The ratio of the total power of the second and third harmonics to the fundamental sinusoidal power.

Second Harmonic Distortion: The ratio of the power at twice the fundamental frequency to the power of the fundamental sinusoid.

Third Harmonic Distortion: The ratio of the power at three times the fundamental frequency to the power of the fundamental sinusoid.

SFDR: Spurious Free Dynamic Range: The ratio of the fundamental sinusoidal power to the power of the next highest spurious signal. Normally the highest spurious signal is the second or third harmonic.

TEST METHOD

A filtered sine wave signal is applied to the channel 1 and channel 2 inputs. Test frequencies used are 5.0, 12.0, and 25.3 MHz. The digitizer clock setting is 100 MHz. The voltage range is 600mV. Signal amplitude is set for 95% of full scale. Performance measurements are made using a 4096 point FFT with a Blackman-Harris window. Signatec uses the first 10 bins to represent the DC term, 64 bins centered around the peak for the fundamental signal power, 9 bins centered at twice the fundamental for the second harmonic and 9 bins centered at three times the fundamental for the third harmonic. All other bins are considered to be noise. (NOTE: large number of bins for the fundamental is necessary so that energy in the side lobes of the window function is not misinterpreted as noise or spurs.)

PDA14 SPECIFICATIONS AND ORDERING INFORMATION

External Signal Connections (SMA)

Analog Input, Channel 1
Analog Input, Channel 2
Clock Input
Trigger Input
Digital Output

Analog Inputs

Full Scale Volt. Ranges: 200mV, 333mV, 600mV, 1.00V, 1.66V, 3.00V

Impedance	: 50 ohms
Bandwidth	: 50 MHz
Equivalent Noise	: 0.5 lsb RMS (typical)
Coupling	: AC or DC[1]

External Trigger

Impedance	: 1k ohms
Trigger Level	: ±1.75 Volts
Adjustment Method	: via 12 bit DAC
Bandwidth	: 50 MHz
Coupling	: DC

External Clock

Signal Type	: sine wave or square wave
Coupling	: AC
Impedance : 50 ohms	
Frequency	: 30 MHz to 100 MHz
Amplitude	: 100 mV p-p to 2.0 V p-p

Digital Output

Type	: TTL Logic Level
Max. Frequency	: 100 MHz
Suggested Load	: 1k ohms
Amplitude	: TTL

DC Offset Voltage

Resolution:	: 12 bit DAC
Range	: ± 1.1 x FS ADC input

Digitizer

Voltage Range	: 2.0V p-p full scale
Resolution	: 14 bits
Linearity, Integral	: ±0.5 lsb max.
Linearity, Differential	: ±0.75 lsb max.
Aperture Jitter	: < 0.5 pS typical

Internal Clock

Available Rates	: 100 MHz down to 97.6 kHz in factors of 2 62.5 MHz down to 61.0 kHz in factors of 2
Accuracy	: ± 0.01%

Trigger Modes

Post Trigger	: single start trigger fills active memory
Pre-trigger	: single trigger stops acquisition
Segmented	: start trigger for each memory segment

Trigger Options

Pre-trigger Samples	: samples prior to trigger are stored; Single Channel: 8k max.; Dual Channel: 4k max per channel
Delayed Trigger	: delay from trigger to data storage; Up to 64k digitizer clock cycles

Memory

Active Size	: Up to 256 MegaSamples
Segment Size	: Up to 128 Megasamples
Start Address Setting	: Anywhere in memory
Segment re-arm time[2]	: 150 nanoseconds
Addressing	: DMA transfer from starting address
Memory Address (PC)	: Plug and Play selected

I/O Addressing

PCI Controller Address : 64 bytes, Plug and Play selected
Control/Status Registers: 32 bytes, Plug and Play selected

Signatec Auxiliary Bus

Data Transfer Modes	: Block or Packet
Data Transfer Rates	: 500 MB/s max @ 64 bits
Data Direction	: output only

Power Requirements

+12V	: 400mV Amps max.
+5V	: 1.5 Amps max.
+3.3V	: 2.3 Amps max.

Absolute Maximum Ratings

Analog Inputs	: ±5 volts
Trigger Input	: ±5 volts
Clock Input	: 5 volts peak to peak
Ambient Temperature	: 0 to 50 C

PDA14 Board

Part Number: PDA14

SAB Cables

Refer to the "SAB Cable Assembly Ordering Guide" to select and order the appropriate cable assemblies.

Master-Slave Cables

The PDA14 may be software configured to operate as a Master or a Slave in a multiple board system. In order to operate in a Master/Slave configuration a 20-pin ribbon cable is required to connect the boards. This cable is ordered using the basic part number PDA14MS-X where X is the total number of boards connected together. Master/Slave boards must occupy adjacent slots. The maximum number of boards to be connected is one master and three slaves.

Documentation & Accessories

The PDA14 is supplied with a comprehensive operator's manual, which thoroughly describes the operation of both the hardware and the software. Also supplied are two four-foot coaxial cables with BNC to SMA connectors. Extra cables may be purchased from Signatec. Supplied software disks contain a function library for Microsoft Visual C/C++, example programs, and all source code to libraries and examples.

Customer Support

The Signatec Web Site: www.signatec.com is the primary access point for software updates, documentation updates, or technical support. For the best technical support it is very important to follow the instructions on the technical support page.

Product Warranty

All Signatec products carry a full 3-year warranty. During the warranty period, Signatec will repair or replace any defective product at no cost to the customer. This warranty does not cover customer misuse or abuse of the products or physical damage not reported within 15 days of the time of shipment by Signatec.

Notes:

1. Selected via dip switch.
2. In segmented mode, time from the end of a segment until a trigger will be accepted to begin another segment acquisition.

Signatec reserves the right to make changes in this specification at any time without notice. The information furnished herein is believed to be accurate, however no responsibility is assumed for its use.

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Signatec, Inc. • 359 San Miguel Drive, Suite 300 • Newport Beach, CA 92660 USA • Phone (949) 729-1084 • Fax (949) 729-9114 • http://www.signatec.com