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# ADS-21AC
# Low-Power, 12-Bit, 1.3 MHz Sampling A/D Converter

**FEATURES**

- **12-Bit resolution**
- **1.3 MHz throughput rate**
- **S/H included**
- **Single 46-pin DIP**

## GENERAL DESCRIPTION

DATEL's ADS-21AC Sampling Converter combines a 12-bit A/D hybrid and a S/H hybrid (the ADC-505 and SHM-45) in one space-saving package. The ADS-21AC functional block diagram shows the A/D conversion technique used to achieve the 1.3 MHz throughput rate in a conservative low-power design. Designed and manufactured at DATEL's modern, certified hybrid assembly facility using state-of-the-art integrated circuits, the ADS-21AC provides the highest quality and performance for signal processing applications.

The ADS-21AC's 1.3 MHz throughput rate can typically be increased to about 1.5 MHz before any performance degradation. This superior performance gives design engineers a high-resolution, high-speed A/D capable of easily meeting the 1.3 MHz throughput rate for many signal processing applications.

The ADS-21AC features six pin-programmable input ranges: 0 to +10V, 0 to −5V, 0 to −10V, 0 to −20V, ±5V and ±10V dc. The input impedance is specified at 1.0 K ohm. Other specifications include no missing codes over temperature, a maximum gain tempco of ±40 ppm/°C and a maximum differential linearity tempco of ±2.5ppm/°C. Power required by both models is +/−15V dc and +/-5V dc at 2.7W maximum.

All digital inputs and three-state outputs are TTL-compatible. Output coding can be selected as straight binary/offset binary or complementary binary/complementary offset binary by using the $\overline{\text{COMP BIN}}$ pin. An overflow pin indicates when inputs are below or above the normal full-scale range.

Manufactured using thick-film and thin-film hybrid technology, this converter's remarkable performance is based on a digital subranging architecture. DATEL further enhances this technology by using a proprietary custom chip and unique laser trimming schemes. The ADS-21AC uses hermetically sealed hybrids packaged in a 46-pin DIP capable of operation over the 0°C to +70°C temperature range.

These devices are ideally suited for spectrum, waveform, vibration, and transient analysis applications in military and industrial instrumentation systems. For information on versions with high reliability screening or extended temperature operation, contact the factory.

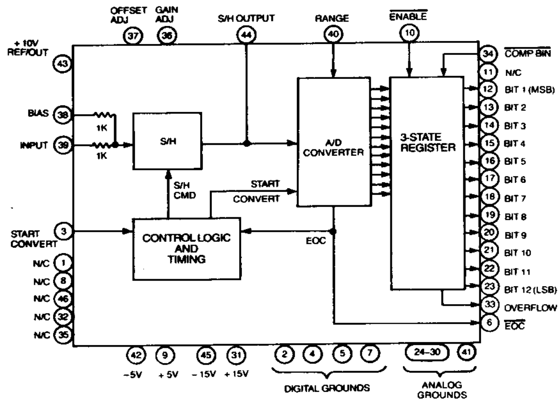


**Figure 1. ADS-21AC Functional Diagram**

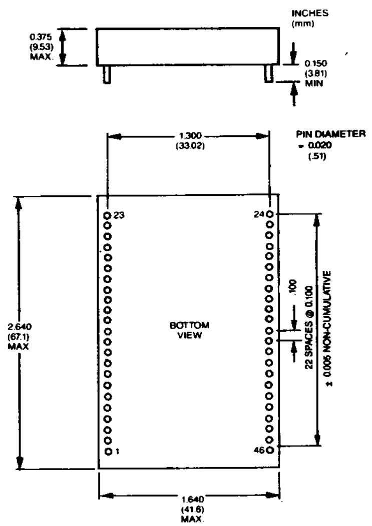


**Figure 2. Mechanical Dimensions**



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## ABSOLUTE MAXIMUM RATINGS

| PARAMETERS | MINIMUM | MAXIMUM | UNITS |
|---|---|---|---|
| +15V Supply (Pin 31) | −0.3 | + 18 | Volts dc |
| −15V Supply (Pin 45) | +0.3 | −18 | Volts dc |
| +5V Supply (Pin 9) | −0.5 | +7 | Volts dc |
| −5V Supply (Pin 42) | +0.5 | −7 | Volts dc |
| Digital Inputs (Pins 3, 10, 34) | −0.3 | +5.5 | Volts dc |
| Analog Input (Pin 39) | −15 | +15 | Volts dc |
| Lead temp. (10 Sec.) | | 300 | °C |

## FUNCTIONAL SPECIFICATIONS

Apply over the operating temperature range and over the operating power supply range unless otherwise specified. For test aspects, contact the factory.

| DESCRIPTION | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|
| **INPUTS** | | | | |
| **Input Voltage Ranges** | — | 0 to +10 | — | Volts dc |
| | — | 0 to −5V | — | Volts dc |
| | — | 0 to −10V | — | Volts dc |
| | — | 0 to −20V | — | Volts dc |
| | — | ±10, ±5 | — | Volts dc |
| **Input Impedance** | | | | |
| **0 to −10V, 0 to +10V, 0 to −20V, ±10V** | — | 1K | — | ohm |
| **0 to −5V, ±5V** | — | 500 | — | ohms |
| **Logic Levels: Logic 1** | 2.0 | — | — | Volts dc |
| **Logic 0** | — | — | 0.8 | Volts dc |
| **Logic Loading: Logic 1** | — | — | 2.5 | µA |
| **Logic 0** | — | — | −100 | µA |
| **OUTPUTS** | | | | |
| **Output Coding Options:** | straight binary/offset binary, complementary binary, complementary offset binary | | | |
| **Logic Levels: Logic 1** | 2.4 | — | — | Volts dc |
| **Logic 0** | — | — | 0.4 | Volts dc |
| **Logic Loading: Logic 1** | — | — | −160 | µA |
| **Logic 0** | — | — | 6.4 | mA |
| **Internal Reference (Pin 43)** | | | | |
| **Voltage, +25°C** | 9.98 | — | 10.02 | Volts dc |
| **Drift** | — | ±5 | ±30 | ppm/°C |
| **External Current (for Pin 39).** | — | — | 1.5 | mA |
| **SAMPLE MODE DYNAMICS** | | | | |
| **Frequency Response:** | | | | |
| **Small Signal (−3dB)** | — | 16 | — | MHz |
| **Slew Rate** | — | 300 | — | V/µS |
| **SAMPLE-TO-HOLD SWITCHING** | | | | |
| **Aperture Delay Time** | — | 6 | — | nS |
| **Aperture Uncertainty (Jitter)** | — | ±50 | — | pS |
| **Settling Time:** | | | | |
| **10V to ± .01% FS (± 1mV)** | — | 60 | 100 | nS |
| **10V to ±.1% FS (± 10mV)** | — | 40 | — | nS |
| **DYNAMIC PERFORMANCE** | | | | |
| **Feedthrough Rejection** | — | −74 | — | dB |
| **Signal to Noise Ratio (SNR)** | −72 | −80 below FS | — | dB |
| **Inband Harmonics (See Fig. 6)** | | | | |
| **dc to 100KHz** | −72 | −80 below FS | — | dB |
| **100KHz to 500KHz** | −72 | −75 below FS | — | dB |
| **HOLD-TO-SAMPLE DYNAMICS** | | | | |
| **Acquisition Time:** | | | | |
| **10V step to ±1.0mV (.01% FS)** | — | 160 | 200 | nS |
| **10V step to ±10mV (.1% FS)** | — | 100 | 170 | nS |

| DESCRIPTION | MIN. | TYP. | MAX. | UNITS |
|---|---|---|---|---|
| **PERFORMANCE FOR ±10V RANGE** | | | | |
| **Integral Nonlinearity** | | | | |
| **+25°C** | — | — | ±0.0125 | %FSR±½LSB |
| **0°C to +70°C** | — | — | ±0.0125 | %FSR±½LSB |
| **Integral Nonlin. Tempco** | — | — | ±3 | ppm/°C |
| **Differential Nonlinearity:** | | | | |
| **+25°C** | — | — | ±0.0125 | %FSR±½LSB |
| **0°C to +70°C** | — | — | ±0.0125 | %FSR±½LSB |
| **Differential Nonlin Tempco** | — | — | ±2 | ppm/°C |
| **Full-Scale Absol. Accuracy:** | | | | |
| **+25°C** | — | ±5 | ±12 | LSB |
| **0°C to +70°C** | — | ±6 | ±15 | LSB |
| **Unipolar Zero Error, +25°C** | — | ±2 | ±5 | LSB |
| **Unipolar Zero Tempco** | — | ±13 | ±25 | ppm/°C |
| **Bipolar Zero Error** | — | — | ±5 | LSB |
| **Bipolar Zero Tempco** | — | ±13 | ±25 | ppm/°C |
| **Bipolar Offset Error, +25°C** | — | ±2 | ±8 | LSB |
| **Bipolar Offset Tempco** | — | ±17 | ±40 | ppm/°C |
| **Gain Error, +25°C** | — | ±3 | ±8 | LSB |
| **Gain Tempco** | — | ±18 | ±40 | ppm/°C |
| **Conversion Times:** | | | | |
| **+25°C** | — | 750 | 770 | nSec |
| **0°C to +70°C** | — | — | 825 | nSec |
| **Throughput Rate:** | | | | |
| **+25°C** | 1.3 | — | — | MHz |
| **0°C to +70°C** | 1.1 | — | — | MHz |
| **No Missing Codes (12 Bits):** | Over the Operating Temp. Range | | | |
| **POWER SUPPLY REQUIREMENTS** | | | | |
| **Power Supply Range:** | | | | |
| **+15V dc Supply** | +14.25 | +15 | +15.75 | Volts dc |
| **−15V dc Supply** | −14.25 | −15 | −15.75 | Volts dc |
| **+5V dc Supply** | +4.75 | +5 | +5.25 | Volts dc |
| **−5V dc Supply** | −4.75 | −5 | −5.25 | Volts dc |
| **Power Supply Current:** | | | | |
| **+15V Supply** | — | +45 | +60 | mA |
| **−15V Supply** | — | −35 | −50 | mA |
| **+5V Supply** | — | +65 | +100 | mA |
| **−5V Supply** | — | −150 | −210 | mA |
| **Power Dissipation** | — | 2.3 | 2.7 | Watts |
| **Power Supply Rejection** | — | 0.01 | 0.05 | %FSRV/%V |
| **PHYSICAL-ENVIRONMENTAL** | | | | |
| **Operating Temp. Range*** | 0 | — | +70 | °C |
| **Storage Temperature Range** | −65 | — | +125 | °C |
| **Package Type** | 46-pin DIP | | | |
| **Pins** | 0.020 brass | | | |
| **Weight** | 2 oz (50g) approx. | | | |

*For extended temperature range versions, contact the factory.

## TECHNICAL NOTES

1. Use external potentiometers to remove system errors or the small initial errors to zero. Use a 20K trimming potentiometer for gain adjustment with the wiper tied to pin 36 (ground pin 36 for operation without adjustments). Use a 20K trimming potentiometer with the wiper tied to pin 37 for zero/ offset adjustment (leave pin 37 open for operation without adjustment).
2. Rated performance requires using good high frequency circuit board layout techniques. The analog and digital grounds are connected internally. Avoid ground-related problems by connecting the digital and analog grounds to one point, the ground plane beneath the converter (versus at the power supply terminals when the power supplies are located some distance from the ground plane). Due to the inductance and resistance of the power supply return paths, return the analog and digital ground separately to the power supplies. This prevents contamination of the analog ground by noisy digital ground currents.


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3. Bypass all the analog and digital supplies and the +10V reference (pin 43) to ground with a 4.7μF, 25V tantalum electrolytic capacitor in parallel with a 0.1μF ceramic capacitor. Bypass the +10V reference (pin 43) to analog ground (pin 30). The −5V dc supply is treated as an analog supply and analog ground (pins 24-30) should be treated as its return path for decoupling purposes.
4. The COMP BIN input (pin 34) allows selection of binary/offset binary or complementary binary/complementary offset binary. Refer to Table 2 for the desired coding selection. The COMP BIN pin has an internal pull-up resistor and is TTL-compatible for those users desiring logic control of this function.
5. An overflow signal, pin 33, indicates when analog input signals are below or above the desired full-scale range. The overflow pin also has a three-state output and is enabled by pin 10 (Enable for bits 1 through 12 and overflow.)
6. The internal Sample/Hold control signal goes low following the rising edge of a start convert pulse and high 30 nanoseconds minimum before EOC goes low. This S/H low signal indicates that the converter can accept a new analog input.

**Table 1. Input/Output Connections**

| PIN | FUNCTION | PIN | FUNCTION |
|---|---|---|---|
| 1 | N/C | 24 | ANA GND |
| 2 | DIG GND | 25 | ANA GND |
| 3 | START CONVERT | 26 | ANA GND |
| 4 | DIG GND | 27 | ANA GND |
| 5 | DIG GND | 28 | ANA GND |
| 6 | EOC | 29 | ANA GND |
| 7 | DIG GND | 30 | ANA GND |
| 8 | N/C | 31 | +15V |
| 9 | +5V | 32 | N/C |
| 10 | ENABLE | 33 | OVERFLOW |
| 11 | N/C | 34 | COMP BIN |
| 12 | BIT 1 (MSB) | 35 | N/C |
| 13 | BIT 2 | 36 | GAIN ADJUST |
| 14 | BIT 3 | 37 | OFFSET ADJUST |
| 15 | BIT 4 | 38 | BIAS |
| 16 | BIT 5 | 39 | INPUT |
| 17 | BIT 6 | 40 | RANGE |
| 18 | BIT 7 | 41 | ANA GND |
| 19 | BIT 8 | 42 | −5V |
| 20 | BIT 9 | 43 | +10V REF OUT |
| 21 | BIT 10 | 44 | S/H OUT |
| 22 | BIT 11 | 45 | −15V |
| 23 | BIT 12 (LSB) | 46 | N/C |

**Table 2. Input Connections**

| INPUT VOLTAGE RANGE | CONNECT INPUT PIN 38 TO: | CONNECT PIN 40 (RANGE) TO: | BINARY/ OFFSET BINARY CONNECT PIN 34 TO: | COMP. BINARY/ COMP. OFFSET BINARY CONNECT PIN 34 TO: |
|---|---|---|---|---|
| 0 to −5V | 39 | 44 | — | 2,4,5,7 |
| 0 to −10V | — | 44 | — | 2,4,5,7 |
| 0 to −20V | 44 | 44 | — | 2,4,5,7 |
| 0 to +10V | EXT. −10V Ref.* | 44 | 2,4,5,7 | — |
| ±5V | 39 | 43 | 2,4,5,7 | — |
| ±10V | — | 43 | 2,4,5,7 | — |

*May be Referenced to +10V Ref. (Pin 43)

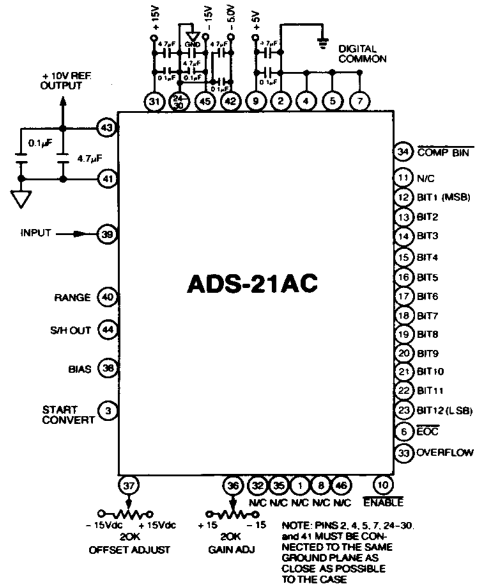


**Figure 3. Connection Diagram**

## CALIBRATION PROCEDURE

Removal of system errors or the small initial errors is accomplished as follows:

1. Connect the converter per Figure 3 and Table 2 for the appropriate full-scale range (FSR). Apply a pulse of 100 nanoseconds minimum to the START CONVERT input (pin 3) at a rate of 500 KHz. This rate chosen to reduce flicker if LED's are used on the outputs for calibration purposes.
2. Zero Adjustment.

   Apply a precision voltage reference source between the analog input (pin 39) and ground (pin 24). Adjust the output of the reference source per Table 4a and 4b for the unipolar zero adjustment (+½ LSB) or the bipolar zero adjustment (zero +½ LSB) for the appropriate FSR. Adjust the zero/offset trimming potentiometer so that the output code flickers equally between 0000 0000 0000 and 0000 0000 0001 or between 1111 1111 1111 and 1111 1111 1110 depending on the output coding selected per Tables 2 and 6.

   For bipolar operation, adjust the potentiometer until the displayed code flickers equally between 1000 0000 0000 and 1000 0000 0001 with COMP BIN tied high or between 0111 1111 1111 and 0111 1111 1110 with COMP BIN tied low. Refer to Table 5.
3. Full-Scale Adjustment.

   Set the output of the voltage reference used in step 2 to the value shown in Table 4a or 4b for the unipolar or bipolar gain adjustment (+FS − 1½ LSB) for the appropriate FSR. Adjust the gain trimming potentiometer so that the output code flickers equally between 1111 1111 1110 and 1111 1111 1111 or between 0000 0000 0001 and 0000 0000 0000 depending on the output coding selected per Tables 2 and 4.
4. To confirm proper operation of the device, vary the precision reference voltage source to obtain the output coding listed in Tables 5 and 6.



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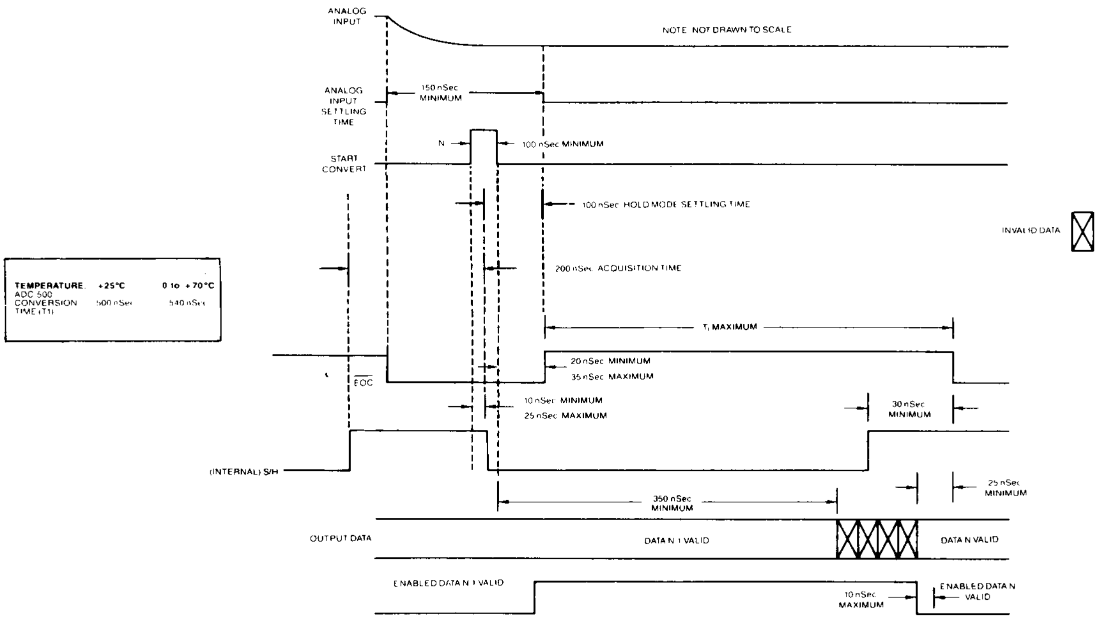


**Figure 4. Timing Diagram**

## TIMING

Figure 4 shows the relationship between the various input signals. The timing cited in Table 3 applies over the operating temperature range and over the operating power supply range. These times are guaranteed by design.

**Table 3. Signal Timing Summary**

| LINE | DURATION IN NANOSECONDS |
|---|---|
| Start Convert | 100 nSec maximum |
| Analog Input Settling Time | 150 nSec minimum |
| Start Convert Low to $\overline{EOC}$ High Propagation Delay | 35 nSec maximum |
| Start Convert Low to Previous Output Data Invalid | 350 nSec minimum |
| Data Valid Before $\overline{EOC}$ Goes Low | 25 nSec minimum |
| Enable to Output Data Valid Propagation Delay | 10 nSec maximum |

## THEORY OF OPERATION

The sample-and-hold is used to capture fast signals for the ADC to then digitize. The ADS-21AC consists of a fast sample-and-hold device (SHM-45) coupled to a high-performance analog-to-digital converter (ADC-500). Figure 5 is a detailed block diagram showing DATEL's SHM-45 along with the ADC-500's internal registers and logic. The ADC-500 used in the ADS-21AC employs a subranging architecture with digital error correction. Also known as a two-step method of conversion, this technique uses a single 7-bit flash converter twice in the conversion process to yield a final resolution of 12 bits. Refer to the Timing Diagram shown in Figure 4 for further clarification.

The SHM-45 used in the ADS-21AC acquires the input signal on the internal hold capacitor (200 nanoseconds maximum acquisition time to 0.01%). The SHM-45 is then put into the hold mode prior to the analog-to-digital conversion. In the hold mode, the SHM-45 requires a maximum of 100 nanoseconds to have its output buffer settle to 0.01% accuracy. The ADC-500 requires a maximum of 150 nanoseconds since the previous conversion for the Input signal to settle before initiating a conversion. The input of the ADC-500 starts settling to its final value while the SHM-45 is in the acquisition mode. The missing 50 nanoseconds of the required maximum analog input settling time is made up by the time the sample/hold is in the acquisition mode. Thus by the end of the SHM-45's hold mode settling time, the ADC-500's input is fully settled.

The SHM-45 is in the sample mode when the internal ADC-500's S/$\overline{H}$ control is high. During this period of time, the A/D is not performing a conversion.

The S/$\overline{H}$ control pin goes low after the rising edge of the start convert pulse, a minimum of 10 nanoseconds and a maximum of 25 nanoseconds later. To assure the SHM has 200 nSec maximum acquisition time, the start convert pulse should be given a minimum of 190 nanoseconds after the desired start of the acquisition time. The width of the start convert pulse should be 100 nsec minimum to assure the hold mode settling time of 100 nanoseconds is observed. The 100 nanoseconds takes into



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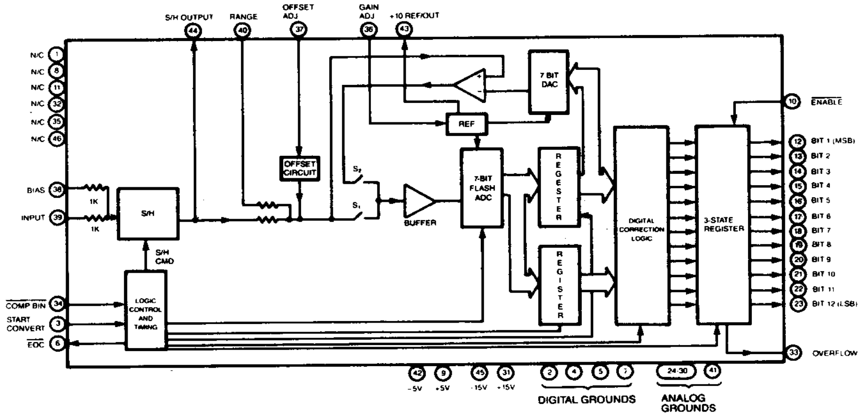


**Figure 5. Detailed Block Diagram**

account the min-max propagation delays of the start convert high to S/$\overline{H}$ control low propagation delays and the start convert low to $\overline{EOC}$ high propagation delays.

The analog input, having been configured for the appropriate range, is buffered and then digitized by the 7 bit flash analog-to-digital converter to determine the seven most significant bits. The seven bits of data are then stored in a register and provided to the input of a 7-bit digital-to-analog converter. This DAC has 13 bits of linearity.

The first pass finished, internal switching occurs effectively subtracting the output of the DAC from the analog input. The result is a voltage difference between the first 7-bit digitization and the analog input. This voltage difference is amplified and converted by the 7-bit analog-to-digital converter. The result of this second conversion is then latched to determine the least 7 significant bits. The outputs from the two registers are then added by the digital correction logic to produce a 12-bit word. $\overline{EOC}$ goes low, indicating the conversion is complete, and the output is present at the three-state output buffers.

Once the second step of the flash analog-to-digital converter is finished, the analog input can change even though the conversion cycle has not been completed ($\overline{EOC}$ going low). The internal Sample/$\overline{Hold}$ control signal line goes low a minimum of 30 nanoseconds before $\overline{EOC}$ goes low, indicating that the SHM-45 can be put back into the sample mode. This feature improves the overall throughput of the ADC-SHM system.

Data from the previous conversion would be valid up to 350 nanoseconds after the falling edge of the start convert pulse. Data from the new conversion is valid a minimum of 25 nanoseconds before $\overline{EOC}$ goes low and valid up to 350 nanoconds after the falling edge of the next start convert pulse. There is 10 nanosecond maximum delay after the three-state output buffers are enabled before the data is valid.

The overall throughput of the ADS-21AC using the ADC-500 and the SHM-45 internally consists of 200 nanoseconds for the sample time, 100 nanoseconds for the hold and input settling time, 15 nanoseconds for observance of min-max propagation delays and 470 nanoseconds for the conversion process (S/$\overline{H}$ control pin saves 30 nanoseconds). However, total guaranteed throughput of the ADS-21AC is a maximum of 770 nanoseconds for the system for a guaranteed throughput rate of 1.3 MHz. Retriggering of the start convert pulse before $\overline{EOC}$ goes low will not initiate a new A/D conversion.

The performance characteristics shown in Table 7 and Figure 6 apply over the operating temperature range and over the operating power supply range unless otherwise specified. These characteristics are guaranteed by design.

**Table 4a. Zero And Gain Adjust For Unipolar Use**

| UNIPOLAR FSR | ZERO ADJUST +½ LSB | GAIN ADJUST +FS – 1½ LSB |
|---|---|---|
| 0 to –5V | –0.61mV | – 4.9982V |
| 0 to –10V | –1.22mV | – 9.9963V |
| 0 to –20V | –2.44mV | –19.9927V |
| 0 to +10V | +1.22mV | + 9.9963V |

**Table 4b. Zero And Gain Adjust For Bipolar Use**

| BIPOLAR FSR | ZERO ADJUST ZERO +½ LSB | GAIN ADJUST +FS – 1½ LSB |
|---|---|---|
| ±10V dc | +2.44 mV | +9.9927V dc |
| ±5V dc | +1.22 mV | +4.9963V dc |

**Table 5. Output Coding for Bipolar Operation**

| BIPOLAR SCALE | INPUT RANGES VOLTS dc | | OUTPUT COMING OFFSET BINARY | COMP. OFFSET BINARY |
|---|---|---|---|---|
| | ±5V | ±10V | MSB LSB | MSB LSB |
| + FS – 1 LSB | +4.9976V | +9.9951V | 1111 1111 1111 | 0000 0000 0000 |
| + ¾ FS | +3.7500V | +7.5000V | 1110 0000 0000 | 0001 1111 1111 |
| + ½ FS | +2.5000V | +5.0000V | 1100 0000 0000 | 0011 1111 1111 |
| 0 | 0.0000V | 0.0000V | 1000 0000 0000 | 0111 1111 1111 |
| – ½ FS | –2.5000V | –5.0000V | 0100 0000 0000 | 1011 1111 1111 |
| – ¾ FS | –3.7500V | –7.5000V | 0010 0000 0000 | 1101 1111 1111 |
| – FS +1 LSB | –4.9976V | –9.9951V | 0000 0000 0001 | 1111 1111 1110 |
| – FS | –5.0000V | –10.0000V | 0000 0000 0000 | 1111 1111 1111 |



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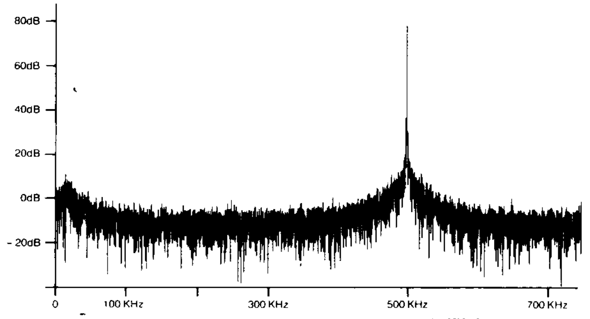
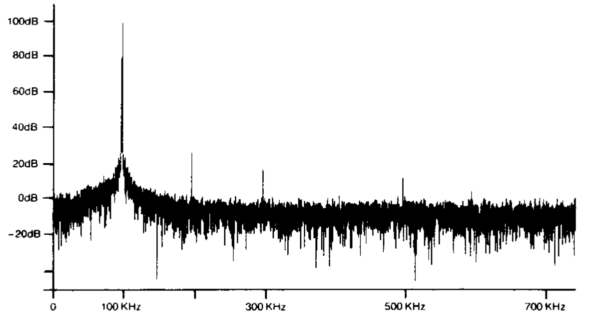
**Table 6. Output Coding For Unipolar Operation**

| UNIPOLAR SCALE | INPUT RANGES VOLTS dc | | | | OUTPUT CODING | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | STRAIGHT BINARY | | | COMP. BINARY | | |
| | 0 to −5V | 0 to −10V | 0 to +10V | 0 to −20V | MSB | | LSB | MSB | | LSB |
| +FS −1 LSB | −4.998V | −9.9976V | +9.9976V | −19.9951V | 1111 | 1111 | 1111 | 0000 | 0000 | 0000 |
| 7/8 FS | −4.375V | −8.750V | +8.750V | −17.500V | 1110 | 0000 | 0000 | 0001 | 1111 | 1111 |
| 3/4 FS | −3.750V | −7.500V | +7.500V | −15.00V | 1100 | 0000 | 0000 | 0011 | 1111 | 1111 |
| 1/2 FS | −2.500V | −5.00V | +5.00V | −10.00V | 1000 | 0000 | 0000 | 0111 | 1111 | 1111 |
| 1/4 FS | −1.250V | −2.500V | +2.500V | −5.000V | 0100 | 0000 | 0000 | 1011 | 1111 | 1111 |
| 1/8 FS | −0.625V | −1.250V | +1.250V | −2.500V | 0010 | 0000 | 0000 | 1101 | 1111 | 1111 |
| 1 LSB | −0.0012V | −0.0024V | +0.0024V | −0.0049V | 0000 | 0000 | 0001 | 1111 | 1111 | 1110 |
| 0 | 0.0000V | 0.0000V | 0.000V | 0.0000V | 0000 | 0000 | 0000 | 1111 | 1111 | 1111 |




ADS-21AC FFT Report for Total Harmonic Distortion — 500 KHz Input




ADS-21AC FFT Report for Total Harmonic Distortion — 100 KHz Input

**Figure 6. Harmonic Distortion Performance**

**Table 7. Performance Characteristics At Different Temperatures**

| CHARACTERISTICS | VALUE |
|---|---|
| Conversion Rate (Changing Inputs):<br>+25°C<br>0°C to +70°C | <br>1.3 MHz minimum<br>1.1 MHz minimum |
| Harmonic Distortion (Below E5)<br>+25°C<br>0°C to +70°C | <br>−72dB minimum<br>−72dB minimum |

**ORDERING INFORMATION**

| MODEL NO. | TEMP RANGE | THROUGHPUT RATE |
|---|---|---|
| ADS-21AC* | 0 to +70°C | 1.3MHz |

*Contact factory for high reliability or extended temperature range versions.



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