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MD-CPU330

MX-CPU330

MR-CPU330

MC68030 CPU

25 MHz

1 to 8 MB DRAM

- ▼ MC68030 at 25 MHz
- ▼ Optional MC68882 at 25 MHz
- ▼ 1, 2, 4, or 8 MB Dual-Accessed DRAM with Express Memory Architecture
- ▼ Sockets for up to 1 MB ROM/EPROM
- ▼ Battery-Backed Clock/Calendar
- ▼ 32 KB of Battery-Backed SRAM
- ▼ Dbus-68 Expansion Bus
- ▼ Two Serial Ports Using SCN68562 DUSCC
- ▼ Two 16-Bit Programmable Timers
- ▼ Interrupt Handler for all Seven VMEbus IRQs
- ▼ Four Mailboxes in Short I/O Space
- ▼ Watchdog Timer with Software Enable
- ▼ Time-Slice Generator with Selectable Periods
- ▼ System Controller Jumper Enabled
- ▼ Fair, ROR Requester with BCAP
- ▼ Hardware-Synchronized Local Reset for Multiprocessing Applications
- ▼ Front Panel Software-Readable Hex Switch
- ▼ Multicolor Front Panel Status Light
- ▼ Programmable Control and Status Registers
- ▼ Industrial, Extended Temperature, and Rugged Versions Available
- ▼ MR-CPU330 Designed to Meet MIL-STD-810E Vibration and Shock Methods 514.4 & 516.4

Multifunction CPU for Real-Time Applications

Designed for stand-alone or distributed real-time applications, the CPU330 is a fast, flexible, and economical real-time processor. The high-speed MC68030 processor operates at 25 MHz. Supporting up to 8 MB of DRAM and a block transfer rate greater than 22 MB/s, the CPU330 easily accommodates applications requiring high-speed data transfers. Utilizing MATRIX Corporation's Express Memory Architecture, the board's memory refresh overhead is cut by 51% over standard memory architecture designs. The dual-accessed DRAM has software-selectable VMEbus addressing. The queued refresh scheme and the support of cache burst fill requests (4-2-2-2) are standard.

Fully Featured

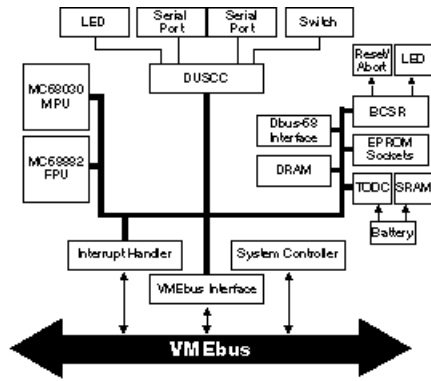
Two serial ports controlled by the SCN68562 communications controller allow access to peripherals over standard EIA-232/422 protocols. Control and status registers are programmable by software. The SRAM (32K x 8) is battery-backed as is the time-of-day clock/calendar (TODC). The interrupt handler responds to all seven VMEbus IRQs, ACFAIL, SYSFAIL, and local interrupts with software-controlled masks and real-time status sense. The time-slice generator has four selectable periods: off, 1, 10, and 20 ms.

Flexibility

The CPU330's daughter board interface uses the public domain Dbus-68 standard to simplify the design of application-specific daughter boards. The Dbus-68 features full 32-bit address and data paths and supports off-the-shelf daughter boards such as SCSI, serial, parallel, and Ethernet. The CPU330's flexibility is further enhanced by its software-programmable board configurations and status registers for address maps, interrupt control, and other on-board control.

Software Support

Real-time operating systems are supported by MATRIX and third-party resources. Contact MATRIX for assistance with software selection.



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