FORCE COMPUTERS
A SOLECTRON COMPANY

SPARC/CPU-50

Installation Guide

P / N 213379 Revision AD
November 2001

Copyright

A SOLECTRON COMPANY

World Wide Web: www.forcecomputers.com
24-hour access to on-line manuals, driver updates, and application notes is provided via SMART, our SolutionsPLUS customer support program that provides current technical and services information.

Headquarters

The Americas

Force Computers Inc.
5799 Fontanoso Way
San Jose, CA 95138-1015
U.S.A.

Tel.: +1 (408) 369-6000
Fax: +1 (408) 371-3382
Email: support@fci.com

Europe

Force Computers GmbH
Prof.-Messerschmitt-Str. 1
D-85579 Neubiberg/München
Germany

Tel.: +49 (89) 608 14-0
Fax: +49 (89) 609 77 93
Email: support@force.de

Asia

Force Computers Japan KK
Shiba Daimon MF Building 4F
2-1-16 Shiba Daimon
Minato-ku, Tokyo 105-0012 Japan

Tel.: +81 (03) 3437 3948
Fax: +81 (03) 3437 3968
Email: smiyagawa@fci.com

213379 420 000 AD

Table of Contents

List of Tables and Figures

Using This Manual

This section does not provide information on the product, but on standard features of the manual itself:

- Its structure
- Special layout conventions
- Related documents

Audience of the Manual and Overview of the Manual

This *Installation Guide* is intended for hard- and software developers as well as support and service engineers installing the SPARC/CPU-50. It is packaged and shipped together with the product.

Note: **Please take a moment to examine the Table of Contents to see how this documentation is structured. This will be of value to you when looking for information in the future.**

This *Installation Guide* includes the installation instructions for powering up the board, in detail:

- The default configuration of the board, for example, the default switch setting
- Initialization prerequisites and procedures
- Connector pinouts

The installation instructions are also published in the product's *Technical Reference Manual* – a separate manual delivered as separate price list item. The *Technical Reference Manual* includes:

- An overview of the product, its specification and ordering information
- A detailed hardware description
- The data sheets of SPARC/CPU-50 components that are relevant for configuring and integrating the board into systems
- A detailed software description

Publication History of the Manual

Table a History of manual publication

SAP No.	Ed./Rev.	Date	Description
208916	1.0	Mar. 1998	First print
208916	2.0	Mar. 1998	Extended technical data for environmental conditions, clarified mechanical construction, and corrected Ethernet #2 OpenBoot alias
208916	3.0	June 1998	Editorial changes
208916	4.0	Jan.1999	Added descriptions for installing Solaris Removed descriptions for installing Solaris 2.5.1 core system support SPARC/MEM-50-x-5 information added Memory module installation notice added Ethernet interface information corrected Battery maintenance safety note changed
208916	5.0	Mar.1999	Solaris installation updated Maximum power consumption for SPARC/CPU-50G corrected Maximum power consumption for SPARC/CPU-50/mmm-333-4-2 added
208916	6.0	Nov. 1999	Editorial changes Solaris installation updated
208916	6.1	July 2000	Replacement of ‘Universe II‘ with ‘Universe IIb‘
213379	AA	Sept. 2000	Added VMEbus information on section “VMEbus Interface” on page 10
213379	AB	August 2001	Added “Sicherheitshinweise” on page xv
213379	AC	September 2001	Corrected “Sicherheitshinweise” on page xv
213379	AD	November 2001	Editorial changes

Table b **Fonts, notations and conventions**

Notation	Description
	All numbers are decimal numbers except when used with the following notations:
`0000.0000`$_{16}$	Typical notation for hexadecimal numbers (digits are 0 through F), e.g. used for addresses and offsets. Note the dot marking the 4th (to its right) and 5th (to its left) digit.
`0000`$_{8}$	Same for octal numbers (digits are 0 through 7)
`0000`$_{2}$	Same for binary numbers (digits are 0 and 1)
`Program`	Typical character format used for names, values, and the like. It is used to indicate when to type literally the same word. Also used for on-screen output.
Variable	Typical character format for words that represent a part of a command, a programming statement, or the like, and that will be replaced by an applicable value when actually applied.

Table c **Product naming conventions**

Name	Description
SPARC/CPU-50	Refers to all available product configurations
Base-50(G)	Refers to all base board configurations as described below
Base-50G	Refers to base board with 2-slot front panel (incl. UPA64S slot)
Base-50	Refers to base board with 1-slot front panel (no UPA64S slot)
I/O-50(G)T	Refers to all I/O-board configurations as described below
I/O-50GT	Refers to I/O board supporting UPA64S slot
I/O-50T	Refers to I/O board without UPA64S-slot support

Icons for Ease of Use: Safety Notes and Tips & Tricks

There are 3 levels of safety notes used in this manual which are described below in short by displaying a typical layout example.

Be sure, to always read and follow the safety notes of a section first – before acting as documented in the other parts of the section.

Danger

Dangerous situation: injuries to people and severe damage to objects possible.

Caution

Possibly dangerous situation: no injuries to people but damage to objects possible.

Note: **No danger encountered. Only application hints and time-saving tips & tricks or information on typical errors when using the information mentioned below this safety hint.**

Safety Notes

This section provides safety precautions to follow when installing, operating, and maintaining the SPARC/CPU-50. For your protection, follow all warnings and instructions found in the following text.

General

This *Installation Guide* provides the necessary information to install and handle the SPARC/CPU-50. As the product is complex and its usage manifold, we do not guarantee that the given information is complete. In case you need additional information, ask your Force Computers representative.

The SPARC/CPU-50 has been designed to meet the standard industrial safety requirements. It must not be used except in its specific area of office telecommunication industry and industrial control.

Only personnel trained by Force Computers or qualified persons in electronics or electrical engineering are authorized to install, uninstall or maintain the SPARC/CPU-50. The information given in this manual is meant to complete the knowledge of a specialist and must not be taken as replacement for qualified personnel.

Make sure that contacts and cables of the board cannot be touched while the board is operating.

Installation

Electrostatic discharge and incorrect board installation and uninstallation can damage circuits or shorten their life. Therefore:

- **Before installing or uninstalling the board in a VMEbus rack:**
  - **Check all installed boards for steps that you have to take before turning off the power**
  - **Take those steps**
  - **At last turn off the power**
  - **see table 2 “Environmental Requirements of the SPARC/CPU-50” on page 5**
  - **see table 1 “SPARC/CPU-50 Maximum Power Consumption” on page 4**
- **Before touching integrated circuits, ensure that you are working in an electrostatic-free environment.**

- **When plugging the board in or removing it, do not press on the front panel but use the handles.**
- **Before installing or uninstalling the board, read section 1 “Installation” on page 1.**
- **Before installing or uninstalling an additional device or module, read the respective documentation.**
- **Ensure that the board is connected to the VMEbus via both connectors, the P1 and the P2, and that power is available on all of them.**

Power Up

If an unformated floppy disk resides in a floppy drive connected to the SPARC/CPU-50 during powering up, the SPARC/CPU-50 does not boot and the OpenBoot does not appear. Therefore: Never boot the SPARC/CPU-50 with an unformated floppy disk residing in a floppy drive connected to the SPARC/CPU-50.

Operation

While operating the board ensure that the environmental and power requirements as given in table 2 “Environmental Requirements of the SPARC/CPU-50” on page 5 and table 1 “SPARC/CPU-50 Maximum Power Consumption” on page 4 are met.

When operating the board in areas of strong electromagnetic radiation ensure that the board is bolted on the VMEbus rack and shielded by closed housing.

EMC

If boards are integrated into open systems, always cover empty slots.

The front panel of the SPARC/CPU-50(G)T provides 1 cutout for a UPA64S card module. Accordingly the I/O-50(G) front panel provides two cutouts for PMC modules. If the board is shipped without the module installed, the front-panel cutout is covered by a blind panel to ensure proper EMC shielding. To ensure proper EMC shielding, always operate the SPARC/CPU-50(G)T with the blind panel or with a UPA64S card and the I/O-50(G) with blind panels or with PMC modules installed.

Expansion

Check the total power consumption of all components installed (see the technical specification of the respective components). For the total power consumption of the SPARC/CPU-50, see table 1 “SPARC/CPU-50 Maximum Power Consumption” on page 4.

Ensure that any individual output current of any source stays within its acceptable limits (see the technical specification of the respective source).

Only replace components or system parts with those recommended by Force Computers. In case you use components other than those recommended by Force Computers, you are fully responsible for the impact on EMI and the eventually changed functionality of the product.

Power Module

The VMEbus power module must be installed if no I/O-50(G)T is installed (see section 2.2.2 “Uninstalling the VMEbus Power Module” on page 18). To protect its components, the SPARC/CPU-50 only powers up, if both the 5 V and the 12 V supply voltages are stable and within their tolerance limits. This is in compliance with the VMEbus specification. However, there are not fully VMEbus compliant systems with power supplies which do not turn on their 12 V supply if the 5 V supply is not loaded. To prevent such systems from running into a power-up deadlock, use a VMEbus board in the system design which loads the 5 V.

Memory Module

Do not install SPARC/MEM-50x and SPARC/MEM-50x-5 memory modules on the same board, otherwise system malfunction may occur.

IOBP

The SPARC/IOBP-50/x is especially designed for the Base-50(G) and for the I/O-50(G)T. Do not use any other I/O panels on the Base-50(G). In addition note the following:

- **Either use the front-panel or the I/O panel Ethernet interface, not both. Check the configuration of your I/O panel.**
- **SW5-2 on the Base-50(G) must be configured to disable the corresponding backplane SCSI termination. This is necessary because the I/O panel provides automatic termination.**

System Controller

If more than one system controller is active in the VMEbus system, the board or other VMEbus participants can be damaged. This is of major importance because this board uses ETL-buffers (enhanced tranceiver logic) which are able to source 60 mA and sink 90 mA on the VMEbus side. Therefore, ensure that only one CPU board is configured to be system controller in the VMEbus system.

Flash Programming

Before programming the boot flash EPROM on-board, save the area containing the OpenBoot image for reprogramming purposes. For example, damage to the image in the boot flash EPROM can occur, if power fails during on-board reprogramming.

Protect your Environment

Always dispose used batteries and/or old boards according to your country's legislation.

Battery Change

The Lithium battery of the RTC/NVRAM provides a data retention of at least 7 years summing up all periods of actual battery use. Therefore Force Computers assumes that there usually is no need to exchange the Lithium battery except for example in the case of long-term spare part handling.

Please observe the following:

- **Exchange the battery before 7 years of actual battery use have elapsed.**
- **Exchanging the battery always results in data loss of the devices which use the battery as power backup. Therefore, back up affected data before exchanging the battery.**
- **Always use the same type of Lithium battery as is already installed.**
- **Use appropriate tools to remove the battery**
- **When installing the new battery ensure that the marked dot on top of the battery covers the dot marked on the chip.**

RJ-45 Connector

If an RJ-45 connector is available on the board, take into account that the RJ-45 connector type is used for telephone connectors and for twisted pair Ethernet (TPE) connectors. Note that mismatching these 2 connectors may destroy your telephone as well as your SPARC/CPU-50. Therefore:

- **Make sure that TPE connectors near your working area are clearly marked as network connectors.**
- **Make sure that TPE bushing of the system is connected only to safety extra low voltage (SELV) circuits.**
- **Verify that the length of the electric cable connected to a TPE bushing does not exceed 1 kilometer outside the building.**
- **If in doubt, ask your system administrator.**

Sicherheitshinweise

Dieser Abschnitt enthält Sicherheitshinweise, die bei Einbau, Betrieb und Wartung des SPARC/CPU-50 zu beachten sind.

Allgemein

Wir sind darauf bedacht, alle notwendigen Informationen zum Einbau und zum Umgang mit dem SPARC/CPU-50 in diesem Handbuch bereit zu stellen. Da es sich jedoch bei dem SPARC/CPU-50 um ein komplexes Produkt mit vielfältigen Einsatzmöglichkeiten handelt, können wir die Vollständigkeit der im Handbuch enthaltenen Informationen nicht garantieren. Falls Ihnen Informationen fehlen sollten, wenden Sie sich bitte an Ihren Vertreter von Force Computers.

Das SPARC/CPU-50 erfüllt die für die Industrie geforderten Sicherheitsvorschriften und darf ausschliesslich für Anwendungen in der Telekommunikationsindustrie und im Zusammenhang mit Industriesteuerungen verwendet werden.

Einbau, Wartung und Betrieb dürfen nur von durch Force Computers ausgebildetem oder im Bereich Elektronik oder Elektrotechnik qualifiziertem Personal durchgeführt werden. Die in diesem Handbuch enthaltenen Informationen dienen ausschliesslich dazu, das Wissen von Fachpersonal zu ergänzen, können dieses jedoch nicht ersetzen.

EMV

Wenn Boards in ein offenes System eingebaut werden, decken Sie freie Steckplätze ab.

Die Frontplatte des SPARC/CPU-50(G)T hat eine Aussparung für ein UPA64S Karten-Modul. Entsprechend bietet die I/O-50(G) Frontplatte zwei Aussparungen für zwei PMC Module. Wenn das Board ohne installiertes Modul geliefert wird, ist die Aussparung in der Frontplatte durch eine Blende abgedeckt, um EMV-Schutz zu gewährleisten.

Um EMV-Schutz zu gewährleisten, betreiben Sie das SPARC/CPU-50(G)T mit der Blende oder der UPA64S-Karte und das I/O-50(G) mit den zwei Blenden oder den installierten PMC-Modulen.

Installation

Elektrostatische Entladung und unsachgemäße Installation und Ausbau des Boards kann Schaltkreise beschädigen oder ihre Lebensdauer verkürzen. Deswegen sind folgende Punkte vor der Installation zu überprüfen:

- **Beachten Sie das folgende vor Einbau oder Ausbau des Boards in einem VME Rack**:
  - **Überprüfen Sie alle installierten Boards auf Schritte, die Sie vor dem Abschalten unternehmen müssen.**
  - **Unternehmen Sie diese Schritte.**
  - **Schalten Sie dann den Strom ab.**
  - **Überprüfen Sie die “Environmental Requirements der SPARC/CPU-50” auf Seite 5**
  - **Überprüfen Sie Tabelle 4 “SPARC/CPU-50 Maximum Power Consumption” auf Seite 4**
- **Bevor Sie integrierte Schaltkreise berühren, vergewissern Sie sich, dass Sie in einem ESD-geschützten Bereich arbeiten.**
- **Drücken Sie beim Einbau oder Ausbau des Boards nicht auf die Frontplatte, sondern benutzen Sie die Griffe.**
- **Lesen Sie vor Einbau oder Ausbau des Boards den Abschnitt “Installation” auf Seite 1.**
- **Lesen Sie vor dem Einbau oder Ausbau von zusätzlichen Geräten oder Modulen das jeweilige Benutzerhandbuch.**
- **Vergewissern Sie sich, dass das Board über die Stecker P1 und P2 an den VMEbus angeschlossen ist und Strom an allen Power Pins anliegt.**

Hochfahren

Wenn während des Hochfahrens eine unformatierte Diskette in einem Diskettenlaufwerk ist, das mit dem SPARC/CPU-50 verbunden ist, bootet das SPARC/CPU-50 nicht, und OpenBoot erscheint nicht. Fahren Sie deshalb niemals das SPARC/CPU-50 hoch, wenn eine unformatierte Diskette in einem mit dem SPARC/CPU-50 verbundenen Diskettenlaufwerk ist.

Betrieb

Achten Sie darauf, dass die Umgebungs- und die Leistungsanforderungen während des Betriebs eingehalten werden.
Wenn Sie das Board in Gebieten mit elektromagnetischer Strahlung betreiben, stellen Sie sicher, dass das Board mit dem CompactPCI System verschraubt ist und das System durch ein Gehäuse abgeschirmt wird.

Stellen Sie sicher, dass Anschlüsse und Kabel des Boards während des Betriebs nicht berührt werden können.

Austausch/ Erweiterung

Verwenden Sie bei Austausch oder Erweiterung nur von Force Computers empfohlene Komponenten und Systemteile. Andernfalls sind Sie für mögliche Auswirkungen auf EMV und geänderte Funktionalität des Produktes voll verantwortlich.

Überprüfen Sie die gesamte aufgenomme Leistung aller eingebauten Komponenten (siehe die technischen Daten der entsprechenden Komponente). Stellen Sie sicher, dass die Ausgangsströme jedes Verbrauchers innerhalb der zulässigen Grenzwerte liegen (siehe die technischen Daten des entsprechenden Verbrauchers).

Power Modul

Das VMEbus Power Modul muss installiert werden, wenn das I/O-50(G)T nicht installiert wurde (siehe Abschnitt 3.2.2 “Uninstalling the VMEbus Power Module” auf Seite 18). Zum Schutz seiner Komponenten fährt das SPARC/CPU-50 nur hoch, wenn sowohl die 5V und 12V Spannungsversorgung stabil ist und innerhalb der Toleranzen liegt. Dies geschieht in Übereinstimmung mit der VMEbus Spezification. Es gibt jedoch auch System, die nicht völlig VMEbus-kompatibel sind. Deren Spannungsversorgung startet die 12V Spannung nicht, wenn die 5V Spannung nicht existiert. Um bei solchen Systemen einen Stillstand zu vermeiden, verwenden Sie in dem System ein VMEbus Board, das die 5V lädt.

IOBP

Das SPARC/IOBP-50/x wurde speziell für das Base-50(G) und das I/O-50(G)T entwickelt. Verwenden Sie keine anderen I/O Panels mit dem Base-50(G). Außerdem beachten Sie bitte das folgende:

- **Verwenden Sie entweder die Ethernet-Schnittstelle an der Frontplatte oder am I/O Panel und nicht beide. Überprüfen Sie die Konfiguration Ihres I/O Panels.**
- **SW5-2 auf dem Base-50(G) muß so konfiguriert sein, dass die entsprechend SCSI-Backplane Terminierung ausgeschaltet ist. Dies muß aufgrund der automatischen SCSI-Terminierung durch das I/O Panels geschehen.**

Speicher-modul

Installieren Sie keine SPARC/MEM-50x und SPARC/MEM-50x-5 Speichermodule auf demselben Board, um Systemfehler zu vermeiden.

System Controller

Bei mehr als einem aktiven System Controller im VMEbus System können das Board oder andere VMEbus-Karten beschädigt werden. Das ist aufgrund der vom Board verwendeten ETL-Buffer (Enhanced Transceiver Logic) sehr wichtig, die 60mA erzeugen und auf der VMEbus-Seite 90mA herabsenken. Vergewissern Sie sich deshalb, dass nur ein CPU Board im VMEbus System als System Controller eingestellt ist.

Flash Programmierung

Bevor Sie das Boot Flash EPROM on-board programmieren, speichern Sie den Bereich, der das OpenBoot Image enthält, für den Fall von Umprogrammierungen. Es kann zum Beispiel das Image im Boot Flash EPROM beschädigt werden, falls es bei der On-Board Umprogrammierung zu einem Stromausfall kommt.

RJ-45 Stecker

Das CPU Board ist mit RJ-45 Steckern ausgestattet. Dieser Stecker wird sowohl für Telefonanschlüsse als auch für Netzwerkkabel (Twisted Pair Ethernet - TPE) verwendet. Die Verwechslung dieser Anschlüsse kann sowohl das Telefon als auch das Board zerstören. Beachten Sie deshalb die folgenden Punkte:

- **Vergewissern Sie sich, dass Anschlüsse an Ihrem Arbeitsplatz deutlich als Netzwerkanschlüsse gekennzeichnet sind.**
- **Schließen Sie TPE-Stecker/Netzwerkstecker Ihres Systems nur an Sicherheitskleinspannungskreise (SELV) an.**
- **Vergewissern Sie sich, dass die an einem TPE-Anschluss angeschlossene Leitung eine Gesamtlänge von 100 Metern nicht überschreitet.**

Falls Sie Fragen haben, wenden Sie sich an Ihren Systemadministrator.

Umwelt-schutz

Entsorgen Sie alte Boards gemäß der in Ihrem Land gültigen Gesetzgebung, wenn möglich umweltfreundlich.

Batterie

Die Lithium-Batterie der RTC/NVRAM hat einen Datenretention von mindestens sieben Jahren reiner Betriebsdauer. Darum geht Force Computers davon aus, dass die Batterie normalerweise nicht ausgewechselt weren muss, außer zum Beipiel bei der Langzeitlagerung von Ersatzteilen. Die folgenden Sicherheitshinweise müssen beim Austausch einer Batterie beachtet werden:

- **Wechseln Sie die Batterie aus, bevor die sieben Jahre reiner Betriebsdauer abgelaufen sind.**
- **Das Austauschen von Batterien führt immer zu einem Datenverlust bei den Bauteilen, die diese Batterie als Strom-Backup verwenden. Sichern Sie daher die betroffenen Daten vor dem Austausch der Batterie.**
- **Es darf nur der Batterietyp verwendet werden, der auch bereits eingesetzt ist.**
- **Verwenden Sie die entsprechenden Werkzeuge zum Batterieentfernen.**
- **Achten Sie beim Einbau der neuen Batterie das der Punkt auf der Batterie den Punkt auf dem Chip bedeckt.**

1 Installation

The following section provides you with information about which variants of the SPARC/CPU-50 are available and how to install them .

1.1 Variants

This section describes the SPARC/CPU-50 variants you may purchase from Force Computers. It is intended to get an overview over all possible configurations with named components which will help to find the information necessary for your configuration in this manual.

Installation

1. Read the overview on the CPU board variants in the remaining parts of this section to get familiar with the naming conventions used in this manual.
2. Read section 1.2 “Installation Prerequisites and Requirements” on page 3 and section 1.2 “Installation Prerequisites and Requirements” on page 3.
3. Depending on the variant under consideration, proceed with reading the respective information in section 2 “Base-50(G) Installation” on page 13 and section 3 “I/O-50(G)T Installation” on page 47.

CPU Board Variants

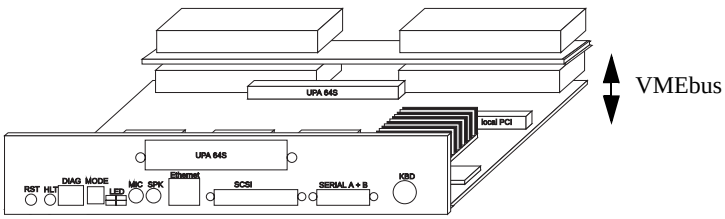
There are 3 variants of the SPARC/CPU-50 all built from the major components shown in figure 4 “Mechanical Construction of Fully-Equipped CPU Board (Schematic)” on page 3:

…CPU-50G

- The SPARC/CPU-50G consists of
  - The 2-slot high base board Base-50G which provides the option to install a UPA64S card
  - The VMEbus power module installed in the 2nd slot of the Base-50G.

Figure 1 **SPARC/CPU-50G (Schematic View)**

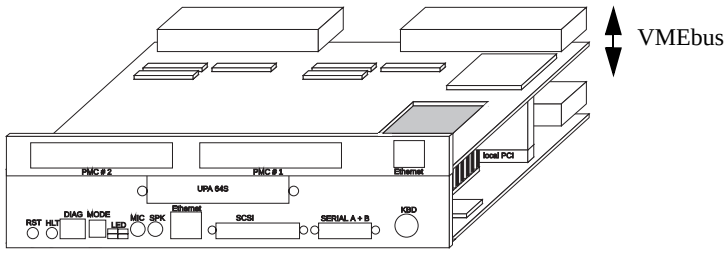
Base-50G with VMEbus power module



…CPU-50GT

- The SPARC/CPU-50GT consists of
  - The 2-slot high base board Base-50G, which provides the option to install a UPA64S card,
  - The 1-slot high I/O board I/O-50GT.

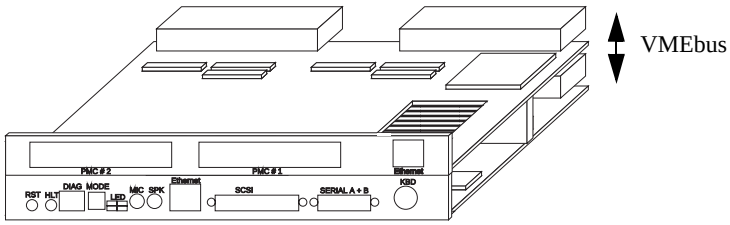
Figure 2 SPARC/CPU-50GT (Schematic View)



…CPU-50T

- The SPARC/CPU-50T consists of
  - The 1-slot high base board Base-50
  - The 1-slot high I/O board I/O-50T.

Figure 3 SPARC/CPU-50T (Schematic View)



Major Components

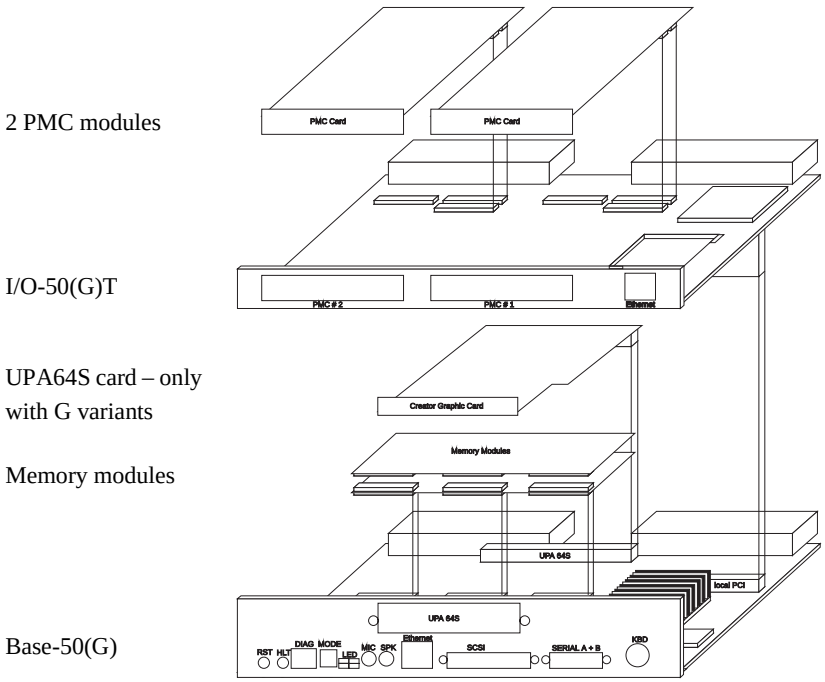
The following figure is intended to provide an overview of all major components of a SPARC/CPU-50.

Note: **Note that in the following figure the terms Base-50(G) and I/O-50(G)T are generalizations of the available base board and I/O board variants.**

In general:

- Base-50 and Base-50G are collectively called Base-50(G)
- I/O-50T and I/O-50GT are collectively called I/O-50(G)T.

Figure 4 Mechanical Construction of Fully-Equipped CPU Board (Schematic)



1.2 Installation Prerequisites and Requirements

Note: **Before powering up check this section for installation prerequisites and requirements, section "Safety Notes" on page xiii for relevant safety notes and check the consistency of the current switch setting (see section 2.4 "Switch Settings" on page 21).**

1.2.1 Requirements

The installation requires only

- Power supply
- Minimum airflow meeting the thermal requirements
- 2 slots of a VMEbus backplane with P1 and P2 connectors

Power Supply

The power supply needs to provide the following voltages:

- +5V, +12V, and –12V

Concerning the SPARC/CPU-50, the power supply must meet the specifications given in the following table.

Table 1 SPARC/CPU-50 Maximum Power Consumption

CPU Board	+5V	+12V	-12V	Major Components of CPU Board Configuration
SPARC/…				
...CPU.50/mmm-333-4-2	7.1A	500mA	200mA	- (1-slot board)
…CPU-50G	7.5A	500mA	200mA	including VMEbus power module and 1 MEM-50L/64, but excluding any I/O board
…CPU-50(G)T	9A	500mA	200mA	including the I/O-50(G)T and 1 MEM-50L/64, but excluding any UPA64S card and excluding any PMC module
…CPU-50GT	12A	500mA	200mA	including I/O-50GT and UPA64S Creator 3D graphics card and 1 MEM-50L/64, but excluding any PMC module

Caution

The VMEbus power module must be installed if no I/O-50(G)T is installed (see section 2.2.2 “Uninstalling the VMEbus Power Module” on page 18).
To protect its components, the SPARC/CPU-50 only powers up, if both the 5V and the 12V supply voltages are stable and within their tolerance limits. This is in compliance with the VMEbus specification. However, there are not fully VMEbus compliant systems with power supplies which do not turn on their 12V supply if the 5V supply is not loaded. To prevent such systems from running into a power-up deadlock, use a VMEbus board in the system design which loads the 5V.

Thermal Requirements

The operating temperature is 0×C to +55×C (humidity 5% to 95% non-condensing at +40×C), when operating the SPARC/CPU-50 in systems providing a minimum forced airflow of 300 LFM (linear feet per minute). The typical operating temperature of the system is 0 °C to +40 °C.

Table 2 Environmental Requirements of the SPARC/CPU-50

	Operating	Non-operating
Temperature	0°C to +55°C	–40°C to +85°C
Forced air flow	300 LFM (linear feet per minute)	–
Temp. change	+/– 0.5°C/min	+/– 1°C/min
Rel. humidity	5% to 95% noncondensing at +40°C	5% to 95% noncondensing at +40°C
Altitude	–300 m to +3,000 m	–300 m to +13,000 m

Backplane Configuration

The CPU board includes an IACK daisy-chain driver. If the CPU board is plugged in slot 1 and configured accordingly by SW800-1 and SW800-2 (see table 9 “Default Switch Settings” on page 21), the board acts as IACK daisy-chain driver. Plugged in any other slot the board closes the IACKIN-IACKOUT path. Therefore:
If not on an active backplane,

- Remove the jumper on the backplane connecting BG3IN* and BG3OUT* for the SPARC/CPU-50 slots which actually are connected to the backplane.
- Assemble the jumpers for BG3IN* and BG3OUT* on
  - Lower and higher slots on the backplane where no board is plugged
  - On the middle slot of a SPARC/CPU-50GT which has no backplane connection due to the installation space for a UPA64S card.

Slot-1 Function

If more than one system controller is active in the VMEbus system, the board or other VMEbus participants can be damaged. This is of major importance because this board uses ETL-buffers (enhanced tranceiver logic) which are able to source 60 mA and sink 90 mA on the VMEbus side.

Note: **Always ensure that only one CPU board is configured to be system controller in the VMEbus system.**

Audio Interfaces

Simultaneous use of the audio interfaces available on the front panel and on the backplane can damage on-board hardware or connected devices. For example: never use the headphone/line audio output at the backplane, if a headphone is plugged into the front-panel jack.

Note: **Always use at most one of the interfaces if an audio interface is available on both the front panel and the backplane.**

Table 3 Audio Interfaces Requirements

Interface	Description
Stereo Micro In (op-amp pre-amp with 18 dB gain)	• Signal level: single-ended condensator microphones with signal level – Up to 12mV with 20 dB gain inside Codec enabled – Up to 120mV with 20 dB gain inside Codec disabled • Availability: on front panel and as factory option on backplane instead of Aux#2 In
Stereo Head-phone/ Line Out	• Signal level: maximum $2V_{RMS}$ line-level signal output (also designed to directly drive headphones) • Availability: on front panel and on backplane
Stereo Line In	• Signal level: typical 47 kΩ audio input impedance; maximum full scale input of $2V_{RM}$ • Availability: on backplane
Stereo Aux#1 In	• Signal level: ~10 kΩ input impedance; maximum full scale input of $2V_{RMS}$ • Availability: on backplane
Stereo Aux#2 In	• Signal level: ~10 kΩ input impedance; maximum full scale input of $2V_{RMS}$ • Availability: on backplane

Table 3 Audio Interfaces Requirements (cont.)

Interface	Description
Mono In	• Signal level: typical 47 kΩ audio input impedance; nominally $1V_{RMS}$ maximum (centered around 2.1V) input signal level • Availability: as factory option on front panel instead of Micro In and as factory option on backplane instead of Aux#1 In
Mono Out	• Signal level depends on the setting of `OLB` which is a bit in the Codecs Alternate Feature Enable I register (I16) – Maximum $1V_{RMS}$ output (centered around 2.1V) if `OLB` = `1` – Maximum $0.707V_{RMS}$ (centered around 2.1V) if `OLB` = `0` Default is `OLB` = `0`. • Availability: as factory option on backplane instead of Headphone/Line Out

1.2.2 Memory Modules

The main memory capacity is adjustable via installation of the appropriate memory modules. The qualified memory modules depend on the SPARC/CPU-50 processor frequency. They are given in the following table.

Table 4 Qualified Memory Modules

Processor frequency	Memory modules
up to 300 MHz	SPARC/MEM-50x
	SPARC/MEM-50x-5
333 MHz and above	SPARC/MEM-50x-5

Caution

Do not install SPARC/MEM-50x and SPARC/MEM-50x-5 memory modules on the same board, otherwise system malfunction may occur.

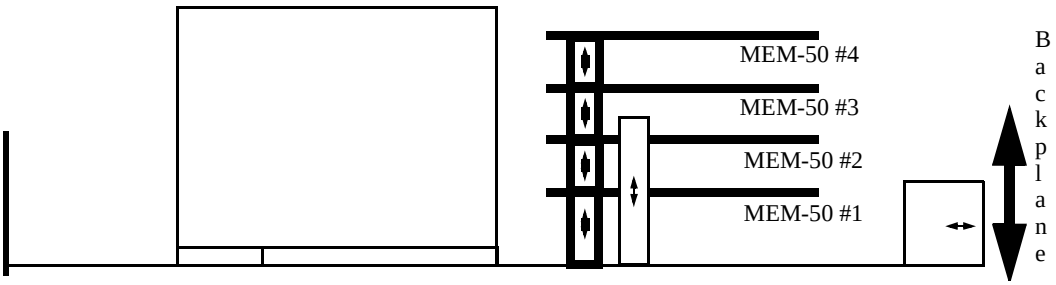
In the following it will be refered to all memory module types as SPARC/MEM-50x.
The Base-50(G) can hold 1 to 4 memory modules providing up to 1 GByte DRAM capacity. 1 memory module can carry 2 memory banks.

Note: **At least 1 lower memory module SPARC/MEM-50L is required.**

See the following figure for the memory module numbering scheme:

- Memory modules #1 and #2 are located facing the first VME slot the SPARC/CPU-50 occupies.
- Memory modules #3 and #4 are located facing the second VME slot the SPARC/CPU-50 occupies.

Figure 5 **MEM-50 – Memory Module Numbering Scheme**



The memory configuration is adjustable to the application's needs via selection of the appropriate memory modules. The memory configuration must fulfill the following requirements:

- The lowest memory module (#1) must be a SPARC/MEM-50L – which is a lower memory module.
- The top memory module (with the greatest number in your configuration given the number scheme in the figure above) can be a SPARC/MEM-50M or SPARC/MEM-50U – which is a middle (M) or upper (U) memory module. The upper module misses the connectors for another memory module to be stacked on top.
- The memory modules between the lowest and the top memory module must be SPARC/ MEM-50M, i.e. middle memory modules.
- If a UPA64S card is installed, at most 2 memory modules can be installed and memory module #2 must be a SPARC/MEM-50U, i.e. an upper memory module.
- Note the limitations given by the SPARC/CPU-50 configuration under consideration (see section 2.2 "Base-50(G) Mechanical Construction" on page 15).

Out of the extensive list of possible configurations the following memory module configurations have been qualified (others may be tested and qualified on request):

Table 5 Qualified Memory Configurations (all data in MByte)

Total capacity	64	128	256	384	512	768	1024
Mem. module #4	–	–	–	–	–	–	256
Mem. module #3	–	–	–	–	–	256	256
Mem. module #2	–	–	–	128	256	256	256
Mem. module #1	64	128	256	256	256	256	256

For installation information see the respective *Installation Guide* delivered together with the memory modules.

1.2.3 Solaris Installation

When installing Solaris, there are some general installation guidelines to be followed before and during Solaris installation and a specific guideline related to Ethernet and SCSI to be followed after Solaris installation (see “” on page 10 and “SCSI” on page 11).

General Installation Guidelines

Note: **Solaris versions and hardware updates prior to 2.5.1 11/97 and 2.6 03/98 are not supported.**

Required Software Packages

The following Solaris software packages must be installed, otherwise Solaris fails to boot. (Applies to Solaris 2.5.1 and 2.6 only.)

Table 6 Required Solaris Packages

Package	Description
`SMEvplr.u`	SME platform links (root)
`SMEvplu.u`	SME platform links (usr)
`SUNWvplr.u`	SMCC sun4u new platform links
`SUNWvplu.u`	SMCC sun4u new usr/platform links

When setting up Solaris interactively, these packages can be installed by selecting the proper software group in the `Software` dialog. Customize the software groups as follows:

Table 7 Customizing Solaris

Software Group	Customization required for		
	Solaris 2.5.1 11/97	**Solaris 2.6 03/98 and later**	**Solaris 2.7 and later**
Entire distribution plus OEM support	No customization is required		No customization required
Entire distribution	Select the following cluster: • SMCC platform links		
Developer system support			
End user system support			
Core system support			

VMEbus Interface

In order to support the Universe IIb, the Solaris Driver Package Release 2.8 or higher and the VMEbus Driver FRCvme V2.4.2 or higher have to be used**.**

Ethernet

When installing Solaris for the first time, the installation program prompts for a default network device (`hme0`, `hme1`, ...). The numbering of the network devices depends on the configuration of the board. However, the numbers in the network device name do not change once Solaris has been set up, even if the hardware configuration is changed.
The following list associates the network devices of a given board configuration with the network device names.

Table 8 Network Device Naming when Installing Solaris

Board configuration	Network device name	Network device
Base board only	`hme0`	Eth. #1 on base board
Base board and I/O board	`hme0`	Eth. #2 on I/O board
	`hme1`	Eth. #1 on base board

Table 8 Network Device Naming when Installing Solaris (cont.)

Board configuration	Network device name	Network device
Base board, I/O board and additional `hme` network devices on PMC modules installed on the I/O board	`hme0`	Eth. #2 on I/O board
	`hme1, .., hme<n>`	*n* `hme` devices on PMC modules
	`hme<n+1>`	Eth. #1 on base board

SCSI

The Solaris SCSI driver may revert wide SCSI devices, which are connected to the front-panel SCSI connector, to asynchronous mode. However, it is possible to operate such a configuration in synchronous mode also by inserting the following line into `/kernel/drv/glm.conf`:
`target`*n*`-scsi-options=0x5f8`
where *n* is the SCSI ID of the wide SCSI device under consideration. In case of several wide SCSI devices insert the respective line per device. Terminate the file with a semicolon `;`.

For further information on SCSI configuration, see section 2.5.4 “SCSI #1 Configuration” on page 29.

1.2.4 Terminal Connection

The SPARC/CPU-50 provides 2 serial interfaces (A and B) which are implemented on the Base-50(G). For the initial power up, a terminal can be connected to interface A via the front-panel 26-pin-MicroD-Sub connector SERIAL A+B. Per default, all serial I/O interfaces provide an RS-232 interface. As factory option the 2 interfaces can be configured as RS-422 interfaces.
For information on the serial interface connector pinout, see section 2.5.5 “Serial I/O Connector Pinout” on page 32.

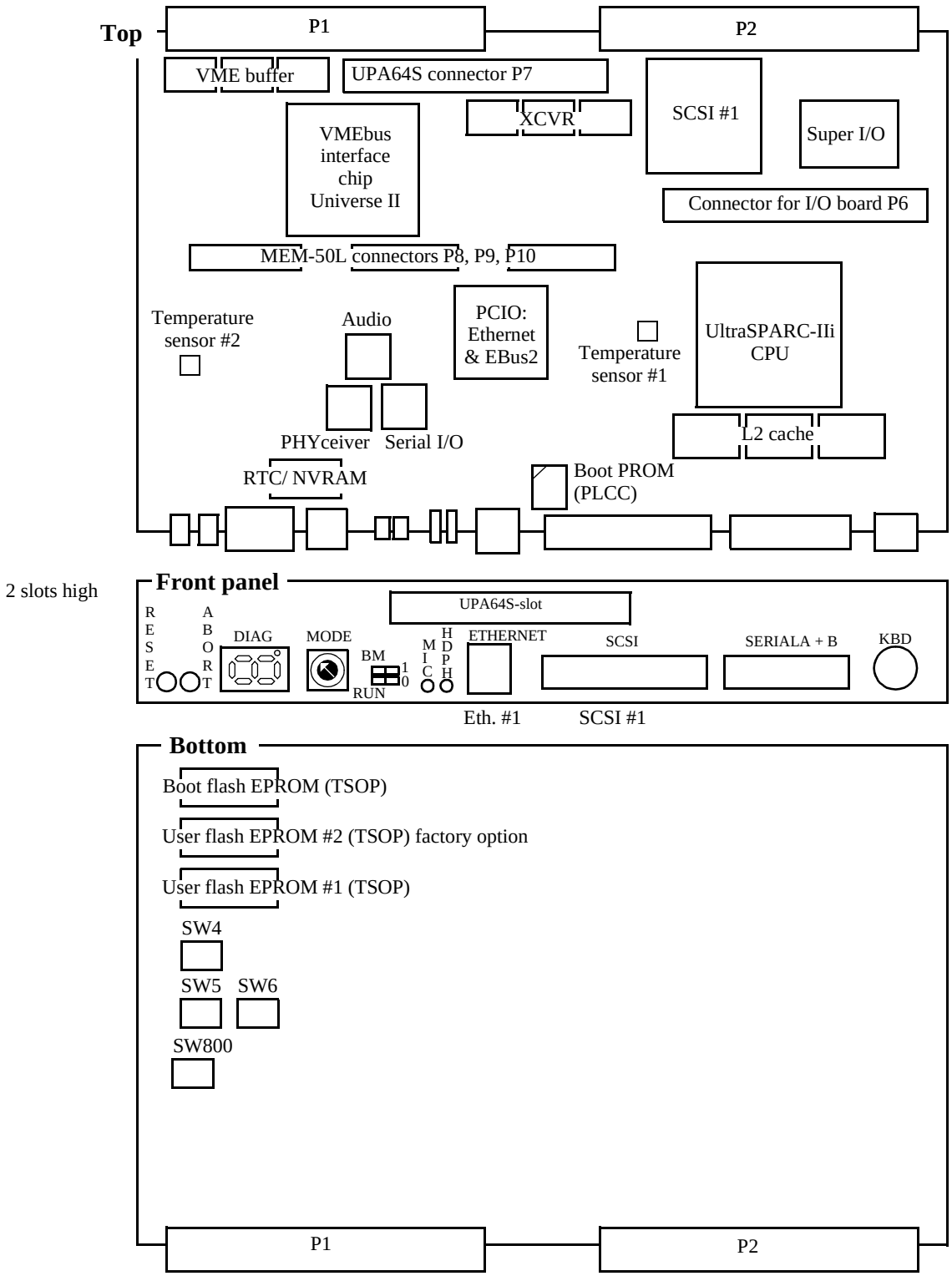
2 Base-50(G) Installation

This section extends **section 1 “Installation” on page 1** by providing the installation information for the Base-50(G) in its various configurations (see section 2.2 “Base-50(G) Mechanical Construction” on page 15).

Note: **Note that there is no need to refer to the installation subsections within section 2.2 “Base-50(G) Mechanical Construction” on page 15 unless you want to change the delivered configuration to upgrade memory, replace a UPA card or the like.**

2.1 Location Overview

Figure 6 Location Diagram of the Base Board (Schematic)



2.2 Base-50(G) Mechanical Construction

The Base-50(G) occupies 2 VMEbus slots and consists of the following major components:

- I/O connector for the VMEbus power module or an I/O-50(G)T
- 3 memory module connectors for up to 4 MEM-50 modules if no UPA64S card is installed or for up to 2 memory modules if a UPA64S card is installed.

The following figures show typical Base-50(G) configurations:

- The Base-50 as used in a 2-slot configuration together with an I/O-50T: see figure 16 “Mechanics of a SPARC/CPU-50T” on page 49.
- The Base-50G in 2-slot configuration with installed VMEbus power module:
  - see figure 7 “Base-50G Mechanical Construction (incl. 4 MEM-50)” on page 15
  - figure 8 “Base-50G Mechanical Construction (incl. 2 MEM-50 and UPA Card)” on page 16.

Figure 7 Base-50G Mechanical Construction (incl. 4 MEM-50)

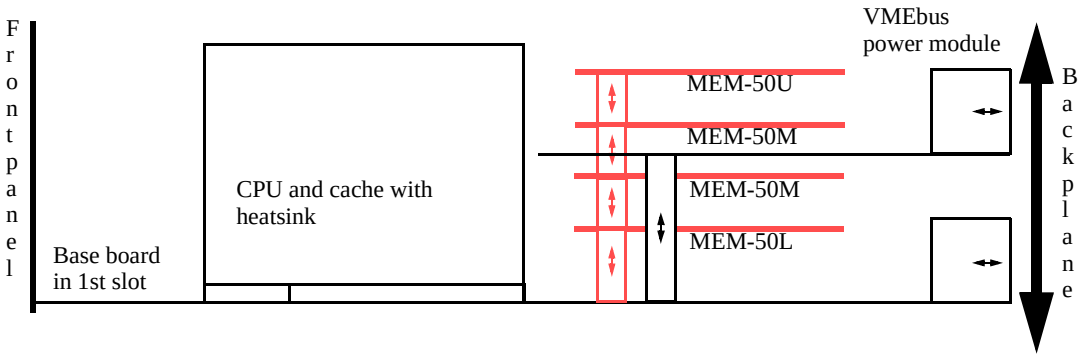
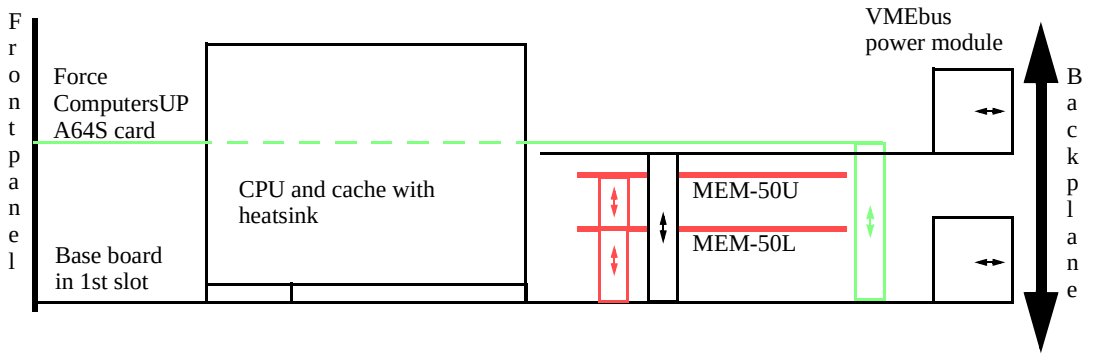
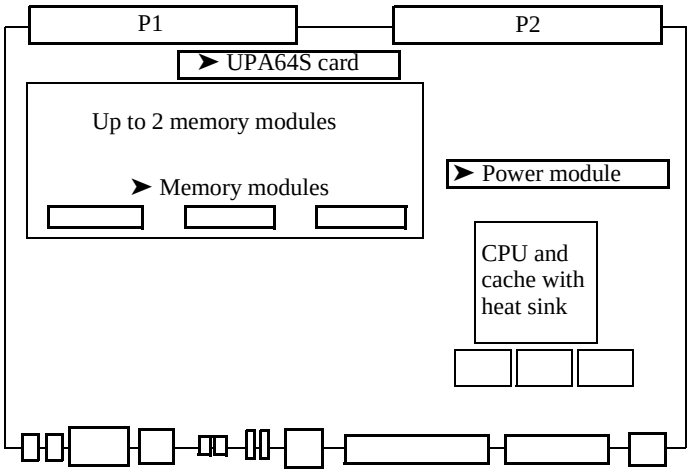


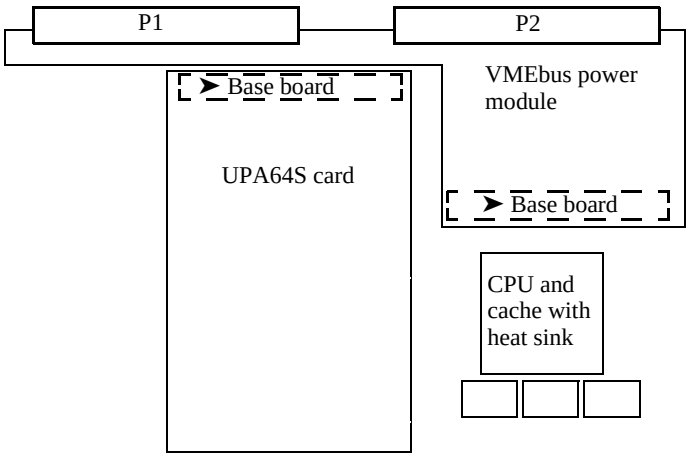
Figure 8 **Base-50G Mechanical Construction (incl. 2 MEM-50 and UPA Card)**



1st of 2 slots
Base board with up to 2 memory modules



2nd of 2 slots
UPA64S card and VMEbus power module

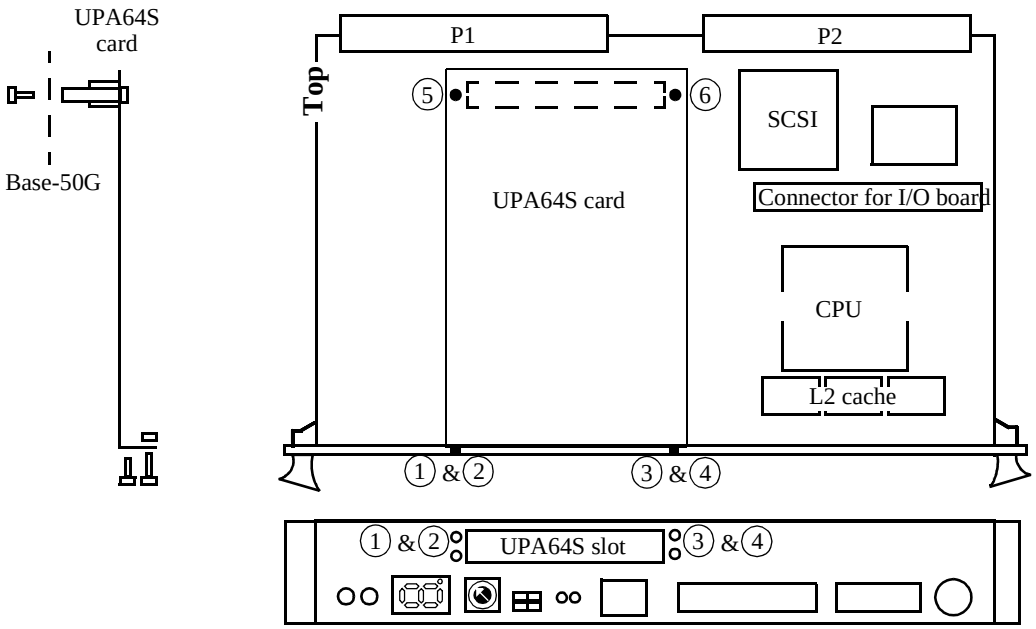


2.2.1 Installing a Force Computers UPA64S Card on a Base-50G

You can only install a Force Computers UPA64S card if you purchased a SPARC/CPU-50 variant with an extra slot for an UPA64S card which is expressed by a G in the product name. The UPA64S card is connected to the Base-50G via the UPA64S connector P7 (see figure 6 “Location Diagram of the Base Board (Schematic)” on page 14).

Note: **Only use UPA64S cards from Force Computers specified to be used with the SPARC/CPU-50.**

Figure 9 Mounting a UPA64S Card



For the locations mentioned in the following description the figure above.

Installation of a UPA64S Card

1. If an I/O-50GT is installed, remove it as described in the I/O-50(G)T installation section.
2. Remove the blind panel fixed in the UPA64S front panel slot of the Base-50G. Store it in a safe place for later use.
3. Plug the UPA64S card to the respective UPA64S connector on the Base-50G.
4. Fix the UPA64S card with 2 screws at location 5 and 6 on the bottom side of the Base-50G.
5. Fix the UPA64S card with the 4 screws and 2 nuts from the blind panel to the front panel of the Base-50G at location 1...4.

Now the UPA64S card is installed.

6. If an I/O-50GT was installed, fix it again as described in the I/O-50(G)T installation section.

Uninstalling a UPA64S Card

1. If an I/O-50GT is installed, remove it as described in the I/O-50(G)T installation section.
2. Remove the 4 screws and 2 nuts on the Base-50G front panel at locations 1...4.
3. Remove the 2 screws at locations 5 and 6 on the bottom side of the Base-520G.
4. Remove the UPA64S card by lifting it.
5. If you do not install the UPA64S card again, fix the blind panel.
6. To install the I/O-50GT again refer to the installation section of the I/O-50(G)T.

2.2.2 Uninstalling the VMEbus Power Module

The SPARC/CPU-50 needs a second VMEbus slot for the heatsink of the UltraSPARC-IIi and for more current. The additional power requirements can be satisfied by

- A separate VMEbus power module which uses the I/O-board connector to provide the base board with +5V-based and +/–12V-based power from a 2nd VMEbus slot
- A separate I/O board I/O-50(G)T satisfying the same power requirements in addition to providing additional interfaces

Caution

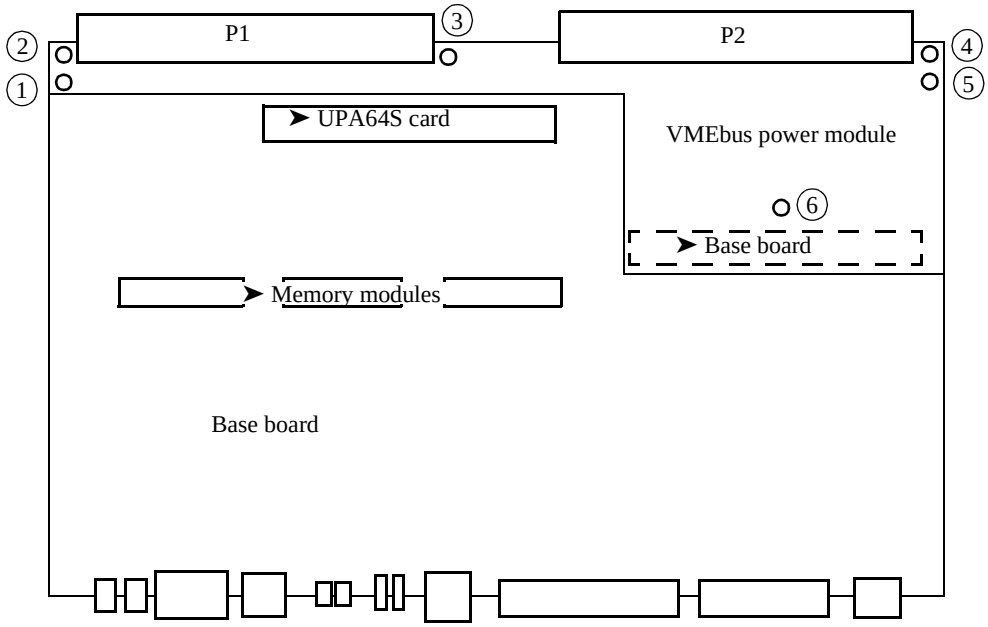
The VMEbus power module must be installed if no I/O-50(G)T is installed.

If you want to extend your Base-50(G) by an I/O-50(G)T you first have to remove the VMEbus power module.

Removing the VMEbus Power Module

To remove the VMEbus power module loosen the 6 screws shown in the figure below and lift the module.

Figure 10 Removing the VMEbus Power Module



2.3 Powering Up

The initial powering up can be done by connecting a terminal to the front panel serial I/O interface A. The advantage of using a terminal is that you do not need any frame buffer, monitor, or keyboard for initial powering up.

VMEbus System Controller

If configured appropriately, the SPARC/CPU-50 recognizes automatically whether it is plugged in slot 1 and 2 of the VMEbus backplane or in any other slot. This auto-configuration feature requires that SW800-1 is set appropriately: OFF (default "OFF", see page 22). Via the auto-configuration the VMEbus system controller is enabled, when the SPARC/CPU-50 is plugged in slot 1, otherwise it is disabled.
If the auto-configuration is disabled, the VMEbus system controller has to be controlled manually by setting SW800-2, see section 2.4 "Switch Settings" on page 21.

Booting

The SPARC/CPU-50 boot PROM consists of a 1 MByte PROM (OTP) PLCC socket device (not writeable). Alternatively a 2 MByte TSOP boot flash EPROM device can be enabled by SW6-2. This boot flash EPROM device is writeable if enabled by SW4-3.

Note: **If an unformated floppy disk resides in a floppy drive connected to the SPARC/CPU-50 during powering up, the SPARC/CPU-50 does not boot and the OpenBoot does not appear. Therefore: Never boot the SPARC/CPU-50 with an unformated floppy disk residing in a floppy drive connected to the SPARC/CPU-50.**

By default the SPARC/CPU-50 is shipped with its boot PROM containing the OpenBoot firmware (see section 2.6 "OpenBoot Firmware" on page 37).

User Application

The SPARC/CPU-50 provides a user flash EPROM to store user applications. For write-protection of the user flash EPROM see SW4-4 in section 2.4 "Switch Settings" on page 21.

2.4 Switch Settings

The following table lists the functions and the default settings of all switches shown in figure 6 “Location Diagram of the Base Board (Schematic)” on page 14.

Note: **Before powering up the board check the current switch settings for consistency. Do not switch during operation.**

Table 9 Default Switch Settings

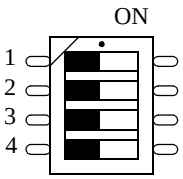
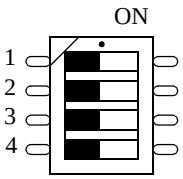
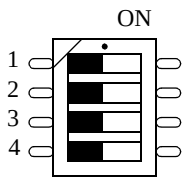
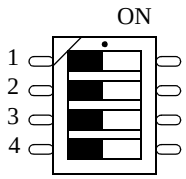
Name and default setting		Function
	SW4-1 OFF	Reset key on front-panel control OFF = RESET key enabled ON = RESET key disabled
	SW4-2 OFF	Abort key control OFF = ABORT key enabled ON = ABORT key disabled
	SW4-3 OFF	Boot flash EPROM write protection – only relevant if SW6-2 = ON OFF = boot flash EPROM write protected ON = boot flash EPROM write enabled
	SW4-4 OFF	User flash EPROM write protection OFF = user flash EPROM write protected ON = user flash EPROM write enabled
	SW5-1 OFF	SCSI Termination for SCSI #1 on front panel OFF = front panel termination automatic ON = front panel termination disabled
	SW5-2 OFF	SCSI Termination for SCSI #1 on P2 OFF = backplane termination disabled ON = backplane termination enabled
	SW5-3 OFF	Reserved, must be OFF
	SW5-4 OFF	Reserved, must be OFF

Table 9 Default Switch Settings (cont.)

Name and default setting		Function
	SW6-1 OFF	Reserved, must be OFF
	SW6-2 OFF	Boot device selection OFF = boot from boot PROM ON = boot from boot flash EPROM
	SW6-3 OFF	VMEbus SYSRESET on power-up OFF = enabled ON = disabled
	SW6-4 OFF	Watchdog enable switch OFF = disabled ON = enabled
	SW800-1 OFF	Automatic VMEbus slot-1 detection OFF = Automatic detection of VMEbus Slot 1 function ON = Automatic detection of VMEbus slot 1 function disabled. Set SW800-2 appropriately.
	SW800-2 OFF	Manual VMEbus slot-1 selection – only relevant if SW800-1 = ON OFF = VMEbus slot 1 function enabled ON = VMEbus slot 1 function disabled
	SW800-3 OFF	External VMEbus SYSRESET OFF = VMEbus SYSRESET generates on-board RESET ON = VMEbus SYSRESET does not generate on-board RESET
	SW800-4 OFF	VMEbus SYSRESET generation OFF = SYSRESET is driven to VMEbus ON = SYSRESET is not driven to VMEbus

2.5 Front Panel, Connectors, and Related Information

Front Panel Features

The features of the front panel are described in the following table. For a location diagram see figure 6 “Location Diagram of the Base Board (Schematic)” on page 14.

Table 10 Front-Panel Features

Device	Description
RESET	Mechanical reset key: When enabled and toggled it instantaneously affects the Base-50(G) by generating a push-button Power On Reset (POR) to the UltraSPARC-IIi. Push-button Power On Reset has the same effect as a Power On Reset from the power supply, with the only difference, that the corresponding status bit (`B_POR`) in the UltraSPARC-IIi `Reset_Control` Register is set and the DRAM refresh is not influenced. For information on disabling the reset key, see “SW4-1” on page 21.
ABORT	Mechanical abort key: When enabled and toggled it instantaneously affects the Base-50(G) by generating a push-button external initiated reset (XIR). Push-button external initiated reset allows a user-reset (abort) of part of the processor without resetting the whole system. UltraSPARC-IIi sets the `B_XIR` bit in the `Reset_Control` Register when a push-button external initiated reset is detected. For information on disabling the abort key, see “SW4-2” on page 21.
DIAG	Software programmable hexadecimal display for diagnostics.
MODE	Hexadecimal rotary switch, decoded with 4 bit. Default setting: F_{16}.
RUN	CPU status LED: green normal operation red the processor is halted or reset is active; it starts blinking to signal a hang-up of the SPARC/CPU-50.

Table 10 Front-Panel Features (cont.)

Device	Description
BM	VMEbus busmaster and SYSFAIL LED: green if the Base-50(G) accesses the VMEbus bus as master red if SYSFAIL is asserted from the Universe II to the VMEbus off otherwise
0, 1	2 software programmable user LEDs. Possible status: off, red, yellow, or green, all colors either permanent or with a blinking frequency of approximately 0.5, 1, or 2 Hz.
MIC	Standard 3.5 mm microphone jack
HDPH	Standard 3.5 mm headphone jack
ETHERNET	Standard Twisted-Pair-Ethernet RJ45 connector for 10BaseT/100BaseTX Ethernet.
SCSI	Standard SCSI 50-pin-fine-pitch connector
SERIAL A+B	26-pin shielded fine-pitch connector for 2 serial interfaces
KBD	Standard 8-pin-mini-DIN connector for keyboard and mouse

On-Board Connectors

In addition to the front-panel connectors, the Base-50(G) provides on-board connectors for memory modules and for the I/O-50(G)T. An overview of the on-board connectors is shown in the following table.

Table 11 On-board Connectors

Connector description and location	Connector type
VMEbus backplane connector P1	VG 96-pin connector male
VMEbus backplane connector P2	VG 160-pin connector male (in case of 3-row factory option VG 96-pin connector male)
I/O-50(G)T connector P6	100-pin MBus connector male

Table 11 On-board Connectors (cont.)

Connector description and location	Connector type
UPA64S interface connector P7	120-pin UPA connector female
Memory module connectors P8, P9, P10	80-pin SMD connector

The next table lists the available signals on the P2 backplane connector. For the P2 connector pinout see “VMEbus P2 Connector Pinout” on page 34.

Table 12 Available signals on P2 Backplane Connector

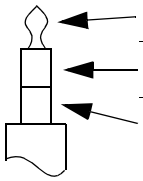
Interface	Backplane connector
Ultra-wide SCSI #1	P2 row A+C
MII Ethernet #1 interface	P2 row D
Floppy interface	P2 row C
Parallel interface	P2 row Z+D
Serial interface A	P2 row A
Serial interface B	P2 row C
Keyboard and mouse	P2 row A
Audio input: Stereo line in, Stereo auxiliary 1 in, Stereo auxiliary 2 in or microphone in (assembly option)	P2 row D
Audio output Stereo headphone out	P2 row D

2.5.1 Audio Interface

The two front panel audio interfaces use standard 3.5-mm-phono jacks supporting

- One single-ended condenser microphone
- One line level signal output, also designed to directly drive low impedance headphones

Table 13 Audio Interface Signals

Connector		Headphone	Microphone
	Tip	Left channel	
	Ring	Right channel	
	Shield	Analog GND	

For further information, see “Audio Interfaces” on page 6.

2.5.2 Ethernet #1 Interfaces, Ethernet Address, and Host ID

The full duplex Ethernet interface is available at the front panel via a 10BaseT/100BaseTx Twisted-Pair-Ethernet connector.

Table 14 Twisted-Pair-Ethernet Connector Pinout

Connector	Pin	Signal
RJ-45 TPE 	1	TX+
	2	TX-
	3	RX+
	4	GND
	5	GND
	6	RX-
	7	GND
	8	GND

The Ethernet #1 interface is also accessible at the 5-row P2 back panel connector via an MII interface. If Ethernet #1 is accessed via I/O panel,

the front-panel connector is disabled automatically. For the connector pinout see figure 14 “Pinout of Row Z and D of a 5-Row P2 Connector” on page 35.

Ethernet Address and Host ID

In order to see the Ethernet address and host ID, enter the following command at theOpenBoot prompt:

```
ok banner
```

The information below explains how the SPARC/CPU-50 Ethernet address and the host ID are determined.

Figure 11 The 48-bit (6-byte) Ethernet Address

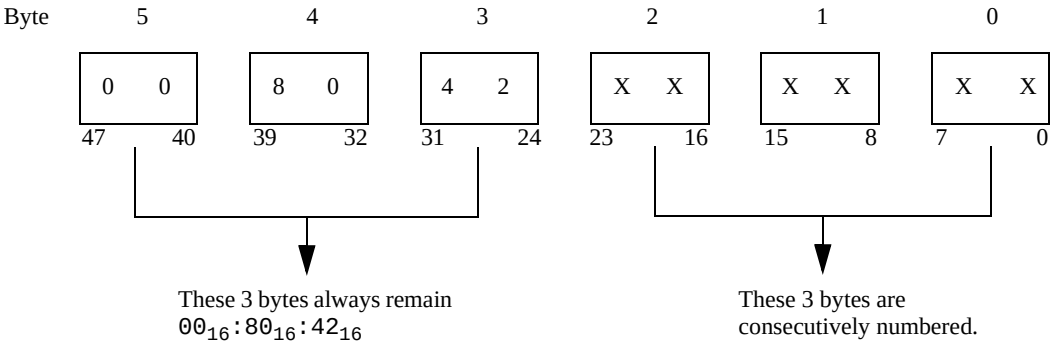
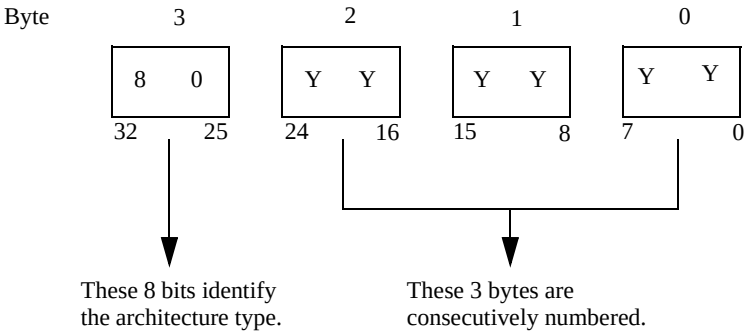


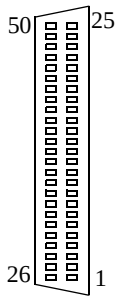
Figure 12 The 32-bit (4-byte) Host ID



2.5.3 SCSI #1 Connector Pinout

The front-panel SCSI #1 interface is single-ended and supports TERMPWR and 8-bit SCSI only. Automatic termination mode means the respective termination is disabled when you connect a standard SCSI cable to the front panel connector. For further information on available SCSI configurations, see section 2.5.4 “SCSI #1 Configuration” on page 29.

Table 15 50-pin SCSI Connector Pinout

Signal	Pin	Connector	Pin	Signal
GND	1		26	D0
GND	2		27	D1
GND	3		28	D2
GND	4		29	D3
GND	5		30	D4
GND	6		31	D5
GND	7		32	D6
GND	8		33	D7
GND	9		34	DP0
GND	10		35	GND
GND	11		36	AUTOTERM
n.c.	12		37	n.c.
n.c.	13		38	TERMPWR
n.c.	14		39	n.c.
GND	15		40	GND
GND	16		41	ATN
GND	17		42	GND
GND	18		43	BSY
GND	19		44	ACK
GND	20		45	RST
GND	21		46	MSG
GND	22		47	SEL
GND	23		48	CD
GND	24		49	REQ
GND	25		50	IO

2.5.4 SCSI #1 Configuration

Note: **Correct SCSI bus selection: The Base-50(G) provides 1 SCSI bus, SCSI #1. A further SCSI controller, SCSI #2 is available on-board the I/O-50(G)T providing access to the SCSI #2 bus which is totally independent from the SCSI #1 bus (see the I/O-50(G)T installation section).**

SCSI #1 Termination

The base board's SCSI #1 bus is accessible via the base board's front-panel SCSI #1 connector providing 8-bit SCSI and via the base board's P2 connector providing wide SCSI. Therefore, the base board holds 2 distinct SCSI bus terminations to enable correct termination of the SCSI #1 bus. Associated to the 2 terminations there are 2 switches – SW5-1 and SW5-2 – which allow easy selection of a valid SCSI #1 bus configuration.

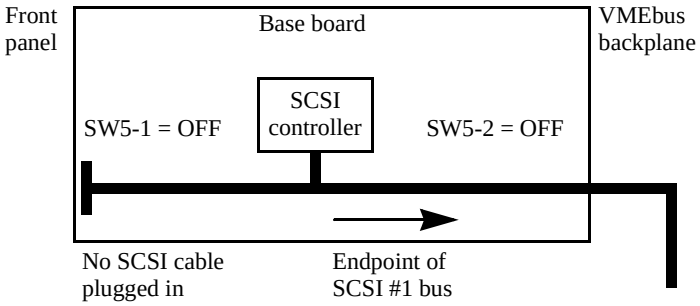
There are 4 valid base board switch settings corresponding to valid SCSI #1 bus configurations. The following factors differentiate the valid SCSI #1 bus configurations:

- The base board's location within the SCSI #1 bus: Is the base board located at an endpoint of the SCSI #1 bus?
- The connector(s) being used from the SCSI #1 bus:
  - Is a SCSI cable plugged into the base board's front-panel SCSI connector?
  - Is the base board's VMEbus P2 connector used by the SCSI #1 bus?
  - Are both base-board connectors used by the SCSI #1 bus?
- The SCSI device type being connected to the SCSI #1 bus: Is a Wide-SCSI device connected to the P2 connector?

Each of the following configuration descriptions starts with identifying the SCSI #1 bus configuration being covered and ends with defining the correct switch setting corresponding to the configuration under consideration.

Default Configuration 1 for 8 bit SCSI

- The default configuration 1 is covered by the default switch setting: The base board is located at an endpoint of the SCSI #1 bus, the SCSI #1 bus is extended via the VMEbus P2 connector, but no SCSI cable is plugged into the front-panel SCSI connector:



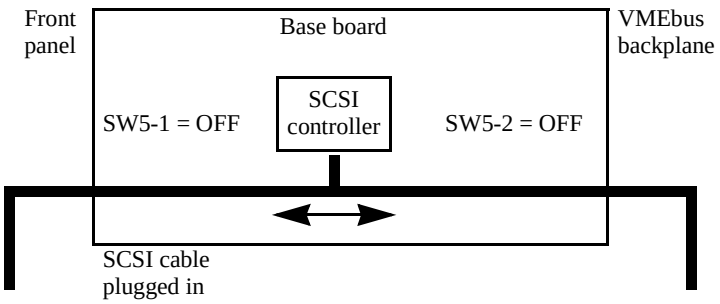
In this configuration (default switch setting):

– SW5-1 must be set to OFF = automatic enabling or disabling of termination by sensing whether a SCSI cable is plugged in

– and SW5-2 must be set to OFF = disabled.

Default Configuration 2 for 8 bit SCSI

- The default configuration 2 is also covered by the default switch setting: the base board is not located at an endpoint of the SCSI #1 bus, the SCSI #1 bus is extended via the VMEbus P2 connector and via the front-panel SCSI connector:



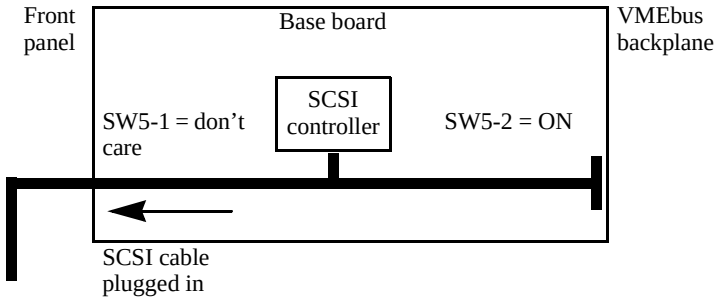
In this configuration (default switch setting):

– SW5-1 must be set to OFF = automatic enabling or disabling of termination by sensing whether a SCSI cable is plugged in

– and SW5-2 must be set to OFF = disabled.

Alternative Configuration for 8 bit SCSI

- Alternative configuration: the base board is located at an endpoint of the SCSI #1 bus and the VMEbus P2 connector is not used for SCSI #1 bus signalling, but the SCSI #1 bus is extended via the front panel connector:



In this configuration

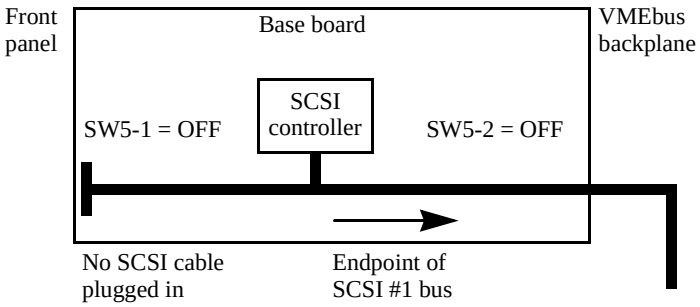
– both settings of SW5-1 are valid

– and SW5-2 must be set to ON = termination enabled.

Default Configuration for Wide-SCSI

Wide SCSI is only available on the P2 VMEbus connector.

- The Wide SCSI configuration is covered by the default switch setting: The base board is located at an endpoint of the SCSI #1 bus, the SCSI #1 bus is extended via the VMEbus P2 connector, but no SCSI cable is plugged into the front-panel SCSI connector:



In this configuration (default switch setting):

– SW5-1 must be set to OFF = automatic enabling or disabling of termination by sensing whether a SCSI cable is plugged in

– SW5-2 must be set to OFF = disabled.

2.5.5 Serial I/O Connector Pinout

Both serial I/O interfaces of the Base-50(G) are independent full-duplex channels. For each of them the 4 signals RXD, TXD, RTS, and CTS are also provided via the respective VMEbus P2 connector (for interfaces A and B see figure 13 “3-Row P2 Connector Pinout” on page 34).
SERIAL A+B on the Base-50(G)’s front panel holds the signals for the 2 serial interfaces A and B.

Table 16 26-Pin Serial A+B Connector Pinout RS232

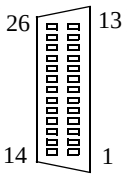
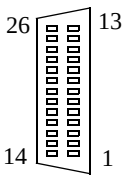
Signal	Pin	Connector	Pin	Signal
n.c.	1		14	TxD_B (Output)
TxD_A (Output)	2		15	RxC_A (Input)
RxD_A (Input)	3		16	RxD_B (Input)
RTS_A (Output)	4		17	RTxC_A (Input)
CTS_A (Input)	5		18	RxC_B (Input)
DSR_A (Input)	6		19	RTS_B (Output)
GND_A (Ground)	7		20	DTR_A (Output)
DCD_A (Input)	8		21	DSR_B (Input)
n.c.	9		22	RTxC_B (Input)
n.c.	10		23	GND_B (Ground)
DTR_B (Output)	11		24	TxC_A (Output)
DCD_B (Input)	12		25	TxC_B (Output)
CTS_B (Input)	13		26	n.c.

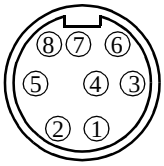
Table 17 26-Pin Serial A+B Connector Pinout RS422 (Factory Option)

Signal	Pin	Connector	Pin	Signal
n.c.	1		14	CTS+_B (Input))
CTS+_A (Input))	2		15	nc
RTS–_A (Output)	3		16	RTS–_B (Output)
RTS+_A (Output)	4		17	nc
CTS–_A (Input)	5		18	nc
nc	6		19	RTS+_B (Output)
RxD–_A (Input)	7		20	RxD+_A (Input)
TxD–_A (Output)	8		21	nc
n.c.	9		22	nc
n.c.	10		23	RxD–_B (Input)
RxD+_B (Input)	11		24	TxD+_A (Output)
TxD–_B (Output)	12		25	TxD+_B (Output)
CTS–_B (Input)	13		26	n.c.

2.5.6 Keyboard/Mouse Connector Pinout

The SUN-type keyboard/mouse interface is available at the front panel via an 8-pin mini-DIN connector.

Table 18 Keyboard/Mouse Connector Pinout

Connector	Pin	Function
	1	GND
	2	GND
	3	+5 V DC
	4	Mouse In
	5	Keyboard Out
	6	Keyboard In
	7	Mouse Out
	8	+5 V DC

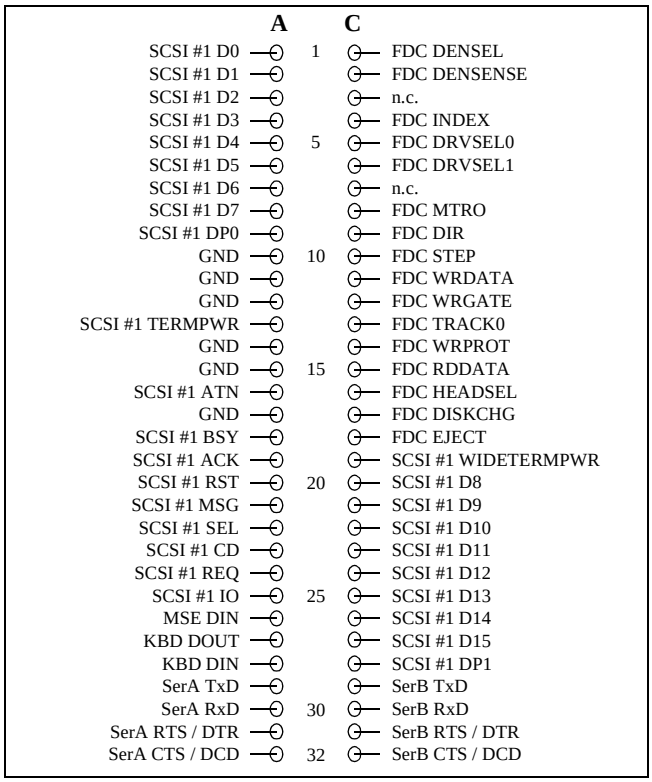
2.5.7 VMEbus P2 Connector Pinout

The pinout shown in the figure below applies to RS-232 configuration of the Base-50(G)'s serial I/O interfaces. Serial I/O interfaces configured for RS-422 (factory option) are only available via the front panel connector. The names used in the following pinouts are given in brackets:
SCSI (`SCSI`), MII (`MII`), parallel (`LPT`), floppy (`FDC`), serial interface A (`SerA`), serial interface B (`SerB`), audio (`AUD`), keyboard (`KBD`), mouse (`MSE`), fused 5 V power for the I/O panel (`VP5`).

The standard Base-50(G) is delivered with 5-row P2 VMEbus connector. However, a 3-row P2 connector variant is also available as factory option.

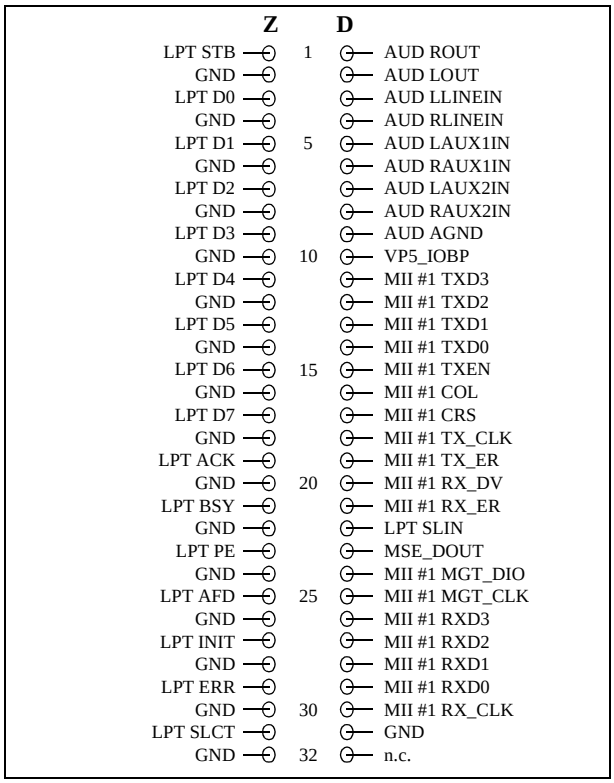
For further information, see "Backplane Configuration" on page 5 and "Slot-1 Function" on page 5.

Figure 13 3-Row P2 Connector Pinout



The signals for rows Z and D (Parallel interface, Ethernet MII interface, Audio) are shown in the following pinout for row D and Z.

Figure 14 Pinout of Row Z and D of a 5-Row P2 Connector



I/O Panel

As a separate price list item an I/O panel is available for the Base-50(G), the SPARC/IOBP-50/*x*. In case of *x*=3 a 3-row backplane connector is supported; in case of *x*=5 a 5-row connector. The corresponding SPARC/CPU-50/AccKit/*x* contains the following cables in addition to the I/O panel itself:

- A serial splitter cable for the front panel and the I/O panel
- A flat ribbon SCSI cable for the I/O panel
- AMicro D-Sub SCSI cable for the front panel
- ATwisted-Pair-Ethernet cable for the front panel

The I/O panel supports the following interfaces:

- SCSI #1
- MII Ethernet #1
- Serial A/B interface
- Audio interface

- Keyboard/mouse
- Parallel interface
- Floppy interface

Danger

The SPARC/IOBP-50/x is especially designed for the Base-50(G). Do not use any other I/O panels on the Base-50(G). In addition note the following:

- **Either use the front-panel or the I/O panel Ethernet interface, not both. Check the configuration of your I/O panel.**
- **SW5-2 on the Base-50(G) must be configured to disable the corresponding backplane SCSI termination. This is necessary because the I/O panel provides automatic termination.**

2.6 OpenBoot Firmware

This chapter describes the use of the OpenBoot firmware. The following tasks will be described in detail:

- Boot the system
- Run diagnostics
- Display system information
- Reset the system
- OpenBoot help

Note: **The examples in this section can differ from the appearance on your monitor according to your device tree (CPU architecture).**

For more information on the OpenBoot firmware see the *Open Boot 3.x Manual Set*.

The OpenBoot firmware is subject to changes. For newest version and how to upgrade refer to the SMART service accessible via the Force Computers World Wide Web site.

2.6.1 Boot the System

The most important function of OpenBoot firmware is the booting of the system. Booting is the process of loading and executing a stand-alone program such as the operating system. After it is powered on, the system usually boots automatically after it has passed the power-on self-test (POST). This occurs without user intervention.
If necessary, you can explicitly initiate the boot process from the Open-Boot command interpreter. Automatic booting uses the default boot device specified in nonvolatile RAM (NVRAM); user initiated booting uses either the default boot device or one specified by the user.
To boot the system from the default boot device, enter the following command at the Forth monitor prompt `ok`:

```
ok boot
```

The boot command has the following format:
`boot [`*`device-specifier`*`] [`*`filename`*`] [-`*`bootoption`*`]`

Optional Boot Parameters

Note: **These options are specific to the operating system and may differ from system to system.**

`[device-specifier]` The name (full path or alias) of the boot device. Typical values are `cdrom`, `disk`, `floppy`, `net`, or `tape`.

[*filename*] The name of the program to be booted. *`filename`* is relative to the root of the selected device. If no filename is specified, the boot command uses the value of *`boot-file`* NVRAM parameter. The NVRAM parameters used for booting are described in the following section.

[-*bootoption*] Boot option may be one of the following:

`[-a]` prompt interactively for the device and name of the boot file.

`[-h]` halt after loading the program.

`[-r]` reconfigure Solaris device drivers after changing hardware configuration.

`[-v]` print verbose information during boot procedure.

Devices to Boot from

To explicitly boot from the internal disk using the Forth monitor enter:

```
ok boot disk
```

To retrieve a list of all device alias definitions, type `devalias` at the Forth Monitor command prompt. The following table lists some typical device aliases:

Table 19 Device Alias Definitions

Alias	Description
	Defined for SCSI
`scsi`	SCSI
`disk`	Default disk SCSI-target-ID 0
`disk6`	disk SCSI-target-ID 6
`disk5`	disk SCSI-target-ID 5
`disk4`	disk SCSI-target-ID 4

Table 19 Device Alias Definitions (cont.)

Alias	Description
`disk3`	disk SCSI-target-ID 3
`disk2`	disk SCSI-target-ID 2
`disk1`	disk SCSI-target-ID 1
`disk0`	disk SCSI-target-ID 0
`tape (or tape0)`	1st tape drive SCSI-target-ID 4
`tape1`	2nd tape drive SCSI-target-ID 5
`cdrom`	CD-ROM partition f, SCSI-target-ID 6
`net`	Defined for Ethernet Ethernet
`floppy`	Floppy disk
`vme`	VME
`audio`	Audio
`keyboard`	Keyboard
`mouse`	Mouse
`ebus`	EBus2
`pci`	primary PCI bus
`flash-prog`	Flash EPROM programming mode
`flash`	Flash EPROM
`ttya`	Serial interface A
`ttyb`	Serial interface B

2.6.2 NVRAM Boot Parameters

The OpenBoot firmware holds its configuration parameters in NVRAM. At the Forth monitor prompt enter `printenv` to see a list of all available configuration parameters.

Note: **Per default the SPARC/CPU-50 boots the OS automatically. If not, ensure that the `auto-boot?` parameter is always set to `true`.**

To Set Parameters

The OpenBoot command `setenv` may be used to set specific parameters in the order below:
`setenv [`*`configuration_parameter`*`] [`*`value`*`]`

The configuration parameters in the following table are involved with the boot process.

Table 20 Setting Configuration Parameters

Parameter	Default value	Description
`auto-boot?`	`true`	If `true`, automatic booting after power on or reset
`boot-device`	`disk`	Device from which to boot
`boot-file`	`empty string`	File to boot
`diag-switch?`	`false`	If `true`, run in diagnostic mode
`diag-device`	`net`	Device from which to boot in diagnostic mode
`diag-file`	`empty string`	File to boot in diagnostic mode

When booting an operating system or another stand-alone program, and neither a boot device nor a filename is supplied, the `boot` command of the Forth monitor takes the omitted values from the NVRAM configuration parameters. If the parameter `diag-switch?` is `false`, `boot-device` and `boot-file` are used. Otherwise, the OpenBoot firmware uses `diag-device` and `diag-file` for booting.

2.6.3 Diagnostics

At Hardware Power On or Button Power On the OpenBoot firmware executes POST. The extent of certain tests executed within the POST depend on the state of the configuration parameter `diag-level.` The operator can choose between minimal or maximal testing by setting this configuration parameter to `min` or `max`. Furthermore an enhanced diagnostic menu is available if setting this parameter to `menu`. If the NVRAM configuration parameter `diag-switch?` is `true` for each test, a message is displayed on a terminal connected to the serial I/O interface A. If the system does not work correctly, error messages are displayed which indicate the problem. After POST the OpenBoot firmware boots an operating system or enters the Forth monitor, if the NVRAM configuration parameter `auto-boot?` is `false`.
The Forth Monitor includes several diagnostic routines. These on-board tests let you check devices such as network controller, SCSI devices, floppy disk system, memory, clock, keyboard and audio. User installed devices can be tested if their firmware includes a self-test routine.

The table below lists several diagnostic routines followed by examples for each of these routines:

Table 21 Diagnostic Routines

Command	Description
`probe-scsi`	Identifies devices connected to the primary SCSI bus
`probe-scsi-all [`*`device-path`*`]`	Performs probe-SCSI on all SCSI buses installed in the system below the specified device tree node. If *`device-path`* is omitted, the root node is used.
`test` *`device-specifier`*	Executes the specified device's self-test method. *`device-specifier`* may be a device path name or a device alias. **Example:** • `test net` – test network connection
`test-all [`*`device-specifier`*`]`	Tests all devices that have a built-in self-test method and that reside below the specified device tree node. If *`device-path`* is omitted, the root node is used.
`watch-clock`	Monitors the clock function.
`watch-net-all`	Monitors network connection via all Ethernet interfaces installed in the system.
`watch-net`	Monitors network connection via primary Ethernet.

Examples:

SCSI Bus

To check the SCSI #1 for connected devices enter:

```
ok probe-scsi
Target 3
Unit 0 Disk FUJITSU M2952ESP SUN2.1G2545
ok
```

All SCSI Buses

To check all the SCSI buses installed in the system enter the following (The actual response depends on the devices on the SCSI buses):

```
ok probe-scsi-all
/pci@1f,0/scsi@2

Target 6
Unit 0 Disk Removable Read Only Device SONY CD-ROM CDU-8012 3.1a

/pci@1f/pci@4,1/scsi@2

Target 3
Unit 0 Disk FUJITSU M2952ESP SUN2.1G2545
ok
```

Note: **The command `probe-scsi-all` can last up to 2 minutes without terminal message.**

Single Device

To test a single installed device enter:

```
ok test device-specifier
```

This executes the `self-test` device method of the specified device node.
`device-specifier` may be a device path name or a device alias as described in Table 19, “Device Alias Definitions,” on page 38. The response depends on the self-test of the device node.

Group of Devices

To test a group of installed devices enter:

```
ok test-all
```

All devices below the root node of the device tree are tested. The response depends on the devices having a self-test routine. If a device specifier option is supplied at the command line, all devices below the specified device tree node are tested.

Clock

To test the clock function enter:

```
ok watch-clock
Watching the ‘seconds’ register of the real time clock
chip.
It should be ‘ticking’ once a second.
Type any key to stop.
22
ok
```

The system responds by incrementing a number once a second. Press any key to stop the test.

Network

To monitor the network connection enter:

```
ok watch-net
Internal loopback test -- succeeded.
Transceiver check -- Using Onboard transceiver -- Link Up.
passed
Using Onboard transceiver -- Link Up.
Looking for Ethernet packets.
‘.’ is a good packet. ‘X’ is a bad packet.
Type any key to stop.
...........X.........................X.............
ok
```

The system monitors the network traffic displaying a dot (`.`) each time it receives a valid packet and displaying an `X` each time it receives a packet with an error which can be detected by the network hardware interface.

2.6.4 Display System Information

The Forth monitor provides several commands to display system information. These commands let you display the system banner, the Ethernet address for the Ethernet controller, the contents of the ID PROM, and the version number of the OpenBoot firmware.
The ID PROM contains specific information to the individual machine, including the serial number, date of manufacture, and assigned Ethernet address.
The following table lists these commands:

Table 22 Commands to Display System Information

Command	Description
`banner`	Displays system banner
`show-pci-devs-all`	Displays list of installed and probed PCI Bus devices
`.enet-addr`	Displays the Ethernet address
`.idprom`	Displays ID PROM contents, formatted
`.traps`	Displays a list of SPARC trap types
`.version`	Displays version and date of the boot PROM
`show-devs`	Displays a list of all device tree nodes
`devalias`	Displays a list of all device aliases

2.6.5 Reset the System

If your system needs to be reset, you either press the reset button on the front panel or, if you are in the Forth Monitor, type **reset** on the command line.

```
ok reset
```

The system immediately begins executing the initialization procedures and executes the POST (not available up to now) if having pressed the reset button. Then the system either boots automatically or enters the Forth Monitor, just as it would have done after a power-on cycle.

2.6.6 OpenBoot Help

The Forth Monitor contains an online help which can be activated by entering:

```
ok help
Enter ‘help command-name’ or ‘help category-name’ for more help
(Use ONLY the first word of a category description)
Examples: help select -or- help line
Main categories are:
Numeric output
Radix (number base conversions)
Arithmetik
Memory access
Line editor
System and boot configuration parameters
Select I/O devices
Floppy eject
Power on reset
Diag (diagnostic routines)
Resume execution
File download and boot
Nvramrc (making new commands permanent)
ok
```

A list of all available help categories is displayed. These categories may also contain subcategories. To get help for special Forth words or subcategories just type `help [name]`.

- The online help shows you the Forth word, the parameter stack before and after execution of the Forth word (before -- after), and a short description.
- The online help of the Forth monitor is located in the boot PROM, that means that there is not an online help for all Forth words.

Example:

How to get help for special Forth words or subcategories:

```
ok help power
reset-all         reset-machine, (simulates power cycling )
power-off         Power Off
ok
```

```
ok help memory
dump ( addr length -- ) display memory at addr for length bytes
fill ( addr length byte -- ) fill memory starting at addr with byte
move ( src dest length -- ) copy length bytes from src to dest address
map? ( vaddr -- ) show memory map information for the virtual address
x? ( addr -- ) display the 64-bit number from location addr
l? ( addr -- ) display the 32-bit number from location addr
w? ( addr -- ) display the 16-bit number from location addr
c? ( addr -- ) display the 8-bit number from location addr
x@ ( addr -- n ) place on the stack the 64-bit data at location addr
l@ ( addr -- n ) place on the stack the 32-bit data at location addr
w@ ( addr -- n ) place on the stack the 16-bit data at location addr
c@ ( addr -- n ) place on the stack the 8-bit data at location addr
x! ( n addr -- ) store the 64-bit value n at location addr
l! ( n addr -- ) store the 32-bit value n at location addr
w! ( n addr -- ) store the 16-bit value n at location addr
c! ( n addr -- ) store the 8-bit value n at location addr
ok
```

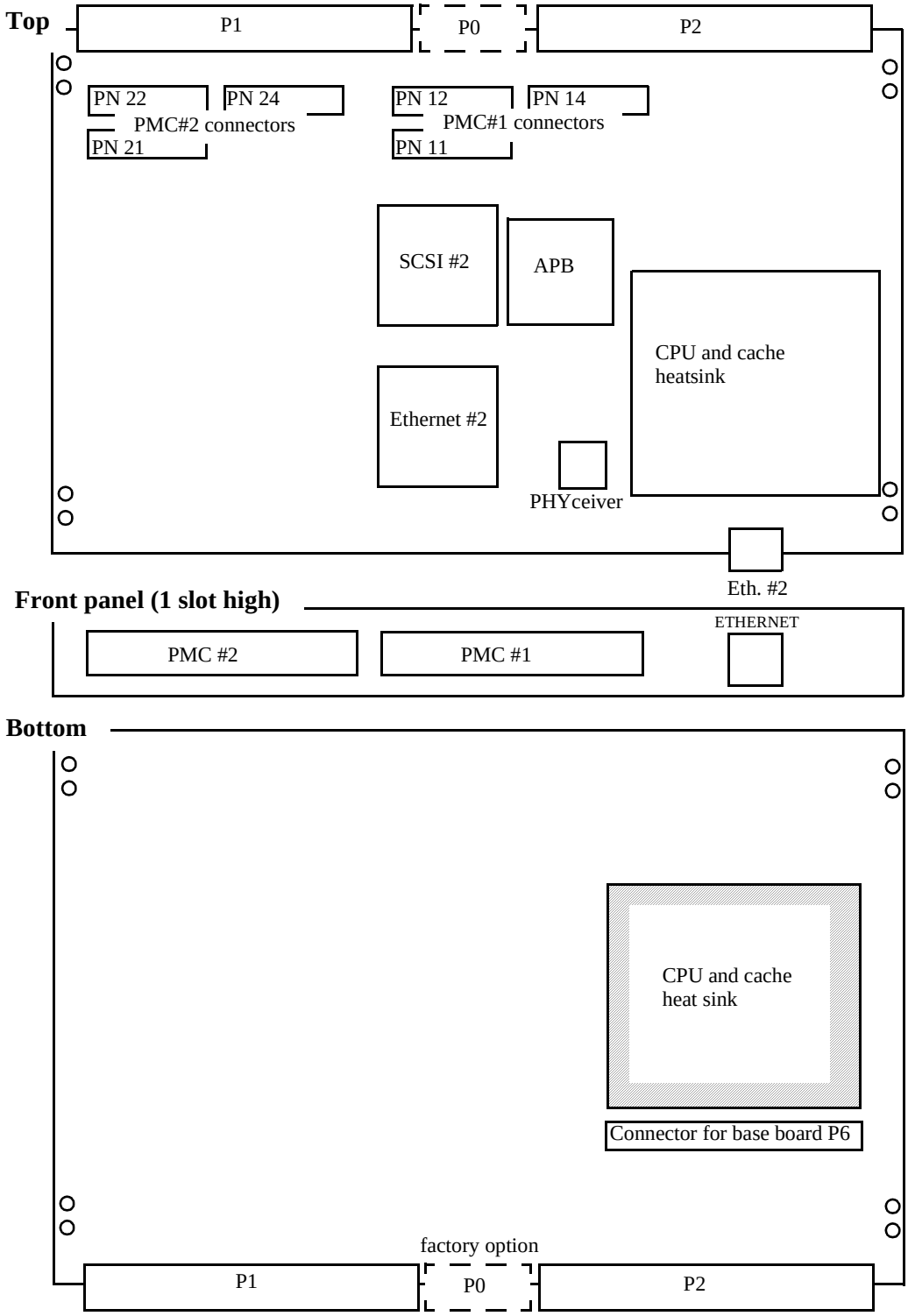
3 I/O-50(G)T Installation

This section extends **section 1 “Installation” on page 1** by providing the installation information for the I/O-50(G)T in its various configurations (see section 3.2 “I/O-50(G)T Mechanical Construction” on page 49).

Note: **Note that there is no need to refer to the installation subsections within section 3.2 “I/O-50(G)T Mechanical Construction” on page 49 unless you want to change the delivered configuration to replace a UPA card or the like.**

3.1 Location Overview

Figure 15 Location Diagram of the I/O-50(G)T (Schematic)



3.2 I/O-50(G)T Mechanical Construction

The I/O-50(G)T is an extension to the Base-50(G). It occupies 1 VMEbus slot and consists of the following major components:

- Two PMC slots
- One SCSI #2 interface
- One Ethernet #2 interface

The following figures show the SPARC/CPU-50 in 2-slot and 3-slot configuration with an I/O-50(G)T.

Figure 16 Mechanics of a SPARC/CPU-50T

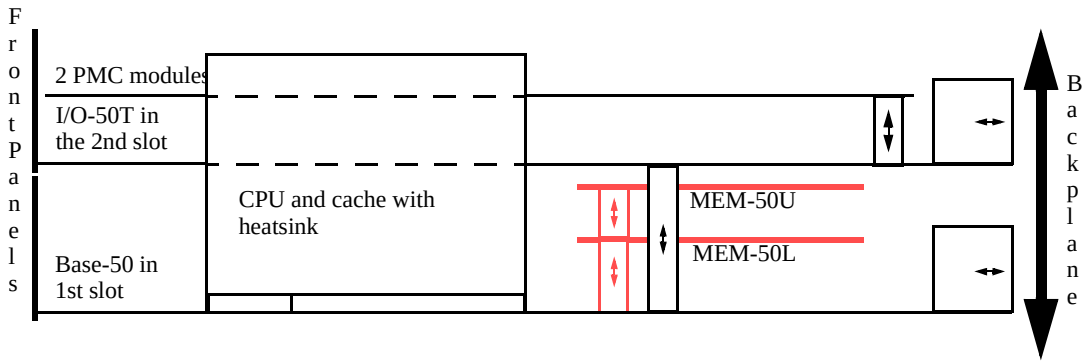


Figure 17 Mechanics of a SPARC/CPU-50GT with UPA64S Card

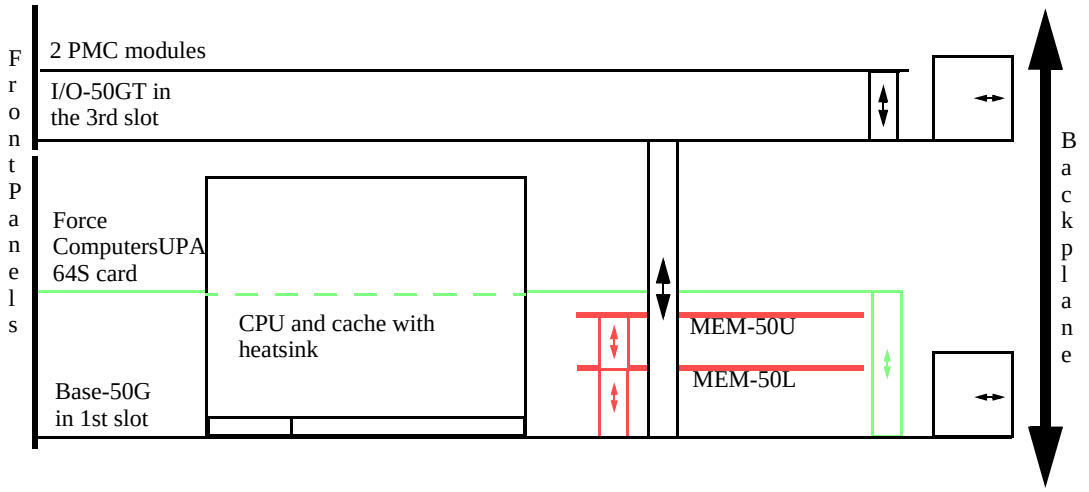
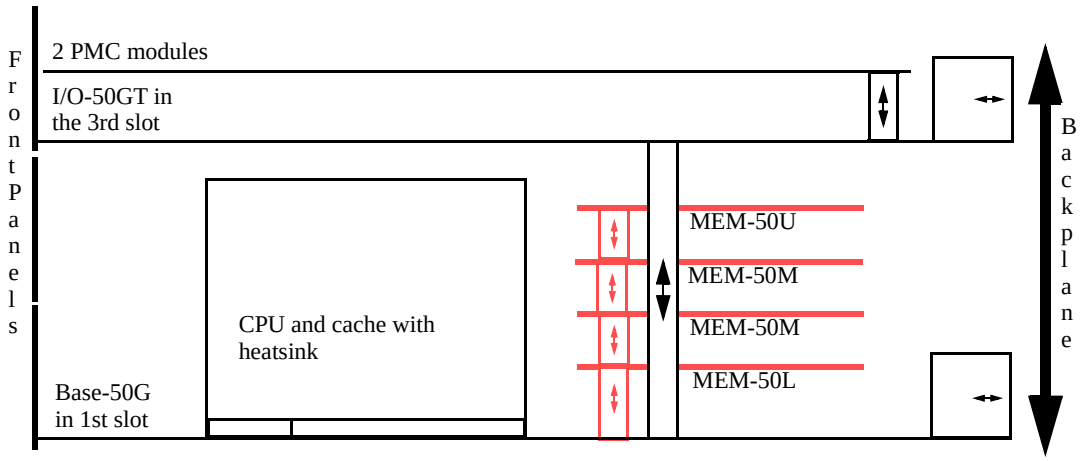


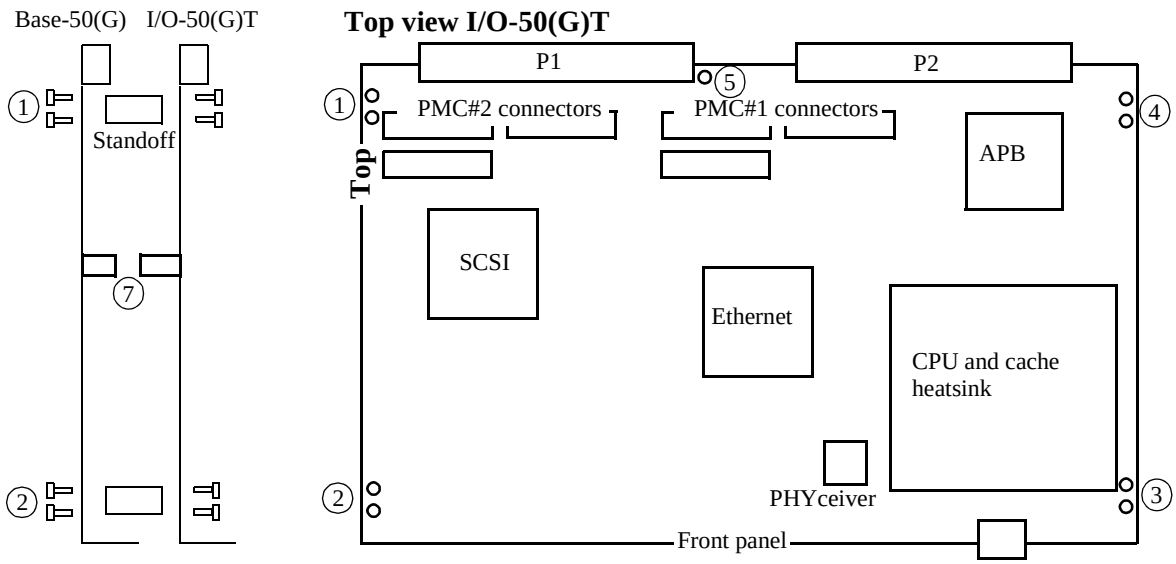
Figure 18 Mechanics of a SPARC/CPU-50GT and four Memory Modules



3.2.1 Installing and Uninstalling the I/O-50(G)T

This section describes how to install or uninstall the I/O-50(G)T. Refer to the figure below to locate the locations mentioned in the description.

Figure 19 Uninstalling the I/O-50(G)T



Uninstalling the I/O-50(G)T

To uninstall the I/O-50(G)T follow the steps below:

1. Remove the 9 screws at location 1…5 on the I/O-50(G)T.
2. Remove the I/O-50(G)T from the Base-50(G) by lifting it.
3. Fix the removed 9 screws on the open ends of the standoffs to have them available when installing the I/O-50(G)T again.

Installing the I/O-50(G)T

To install the I/O-50(G)T follow the steps below:

1. Remove the 9 screws at location 1…5 on the open end of the stand-offs of the Base-50(G).
2. Plug the I/O-50(G)T to the Base-50(G) via the I/O-50(G)T to Base-50(G) connector at position 7.
3. Fix it with the 9 removed screws on the standoffs at location 1…5.

3.3 Front Panel, Connectors, and Related Information

Front Panel Features

The features of the front panel are described in the following table. For a location diagram see figure 15 “Location Diagram of the I/O-50(G)T (Schematic)” on page 48.

Table 23 Front-Panel Features

Device	Description
ETHERNET	Standard Twisted-Pair-Ethernet RJ45 connector for 10BaseT/100BaseTX Ethernet
PMC #1	Hole for the PMC #1 front panel
PMC #2	Hole for the PMC #2 front panel

On-Board Connectors

In addition to the front-panel connectors, the I/O-50(G)T provides on-board connectors for connection to the Base-50(G), to the VMEbus and for 2 PMC modules. An overview is shown in the following table.

Table 24 On-board Connectors

Connector	Description	Connector type
VMEbus P1	–	VG 96-pin male connector
VMEbus P2	SCSI #2 and Ethernet MII #2	VG 160-pin connector male (in case of 3-row factory option VG 96-pin connector male)
VMEbus P0 (factory option)	PMC #1, #2 user I/O	95-pin female connector
P6	I/O-50(G)T extension connector	100-pin MBUS connector female • low: for 2 slot solution SPARC/CPU-50T • high: for 3 slot solution SPARC/CPU-50GT

Table 24 On-board Connectors (cont.)

Connector	Description	Connector type
PN11, PN12, PN14	PMC #1	64-pin SMD connector
PN21, PN22, PN24	PMC #2	64-pin SMD connector

3.3.1 Ethernet #2 Interfaces and Configuration

The full duplex 10BaseT/100BaseTx Ethernet #2 interface is available at the front panel via a Twisted-Pair-Ethernet connector.

Table 25 Twisted-Pair-Ethernet Connector Pinout

Connector	Pin	Signal
RJ-45 TPE 	1	TX+
	2	TX-
	3	RX+
	4	GND
	5	GND
	6	RX-
	7	GND
	8	GND

Ethernet #2 Configuration

The Ethernet #2 interface is also accessible at the 5-row P2 backplane connector via an MII interface. If Ethernet #2 is accessed via the I/O panel, the front panel connector is normally disabled automatically. For other configurations see the respective jumper settings in the *SPARC/IOBP-50 Installation Guide*. For the connector pinout see figure 16 “Pinout of row Z and D of a 5-row P2 connector” on page 52.

Note: **Correct Ethernet selection: The I/O-50(G)T provides 2 Ethernet #2 interfaces: via a TPE #2 interface connected to a front-panel RJ-45 connector or an MII #2 interface available at the VMEbus P2 connector.**

Ethernet address and host ID

For the SPARC/CPU-50 only 1 Ethernet address and host ID exists, see section 2.5.2 “Ethernet #1 Interfaces, Ethernet Address, and Host ID” on

page 26. Use the Ethernet #2 TPE or MII interface of the I/O-50(G)T only in a separate network which is unrelated to the Ethernet #1 network of the Base-50(G).

3.3.2 PMC Slots

The I/O-50(G)T provides 2 PMC slots compliant with IEEE P1386 ("Draft Standard Physical and Environmental Layers for PCI Mezzanine Cards: PMC"). The PCI bus, a high speed local bus compliant with Rev. 2.1., connects different high speed I/O cards with the SPARC/CPU-50. Both PMC slots support 32-bit data bus width with a maximum frequency of 33 MHz.

PMC Voltage Keys

The PCI bus uses a 5V voltage to signal bus levels. The voltage keys prevent 3.3V PMC cards from being plugged into the PMC slots.

Connectors and P0 Factory Option

The 32-bit PCI bus requires 2 PMC connectors. The 3rd PMC connector connects additional user I/O signals of PMC slot 1 and PMC slot 2 to the VMEbus P0 connector (factory option).

– PMC Slot 1

- For the PCI bus: PN11 and PN12
- For 64 user I/O signals: PN14

– PMC Slot 2

- For the PCI bus: PN21 and PN22
- For 32 user I/O signals: PN24

PMC 1/2 Factory Option

As an additional factory option the PMC slot 1 signals can be connected to the PMC slot 2 signals in the following way:

- PMC 1 I/O 1 is connected to PMC 2 I/O 33
- PMC 1 I/O 2 is connected to PMC 2 I/O 34
- …
- PMC 1 I/O 32 is connected to PMC 2 I/O 64

3.3.3 SCSI #2 Configuration

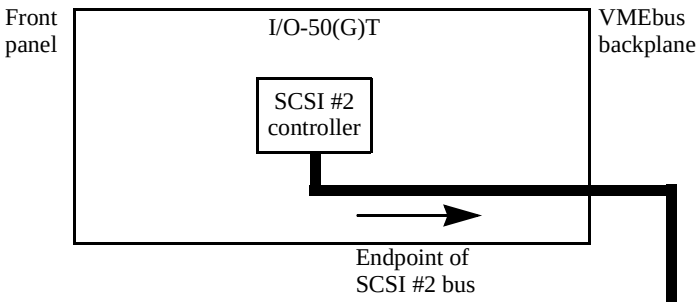
The SCSI #2 bus is only available at the VMEbus P2 connector (see section 3.3.4 “VMEbus P2 Connector Pinout” on page 55).

Note: **Correct SCSI bus selection (see section 2.5.4 “SCSI #1 Configuration” on page 29): The I/O-50(G)T provides a second SCSI bus, SCSI #2. The SCSI #2 bus is always terminated at the SCSI #2 controller.**

Valid Configuration

There is only 1 valid I/O-50(G)T SCSI #2 bus configuration:

- The I/O-50(G)T is located at an endpoint of the SCSI #2 bus, the SCSI #2 bus is extended via the VMEbus P2 connector:

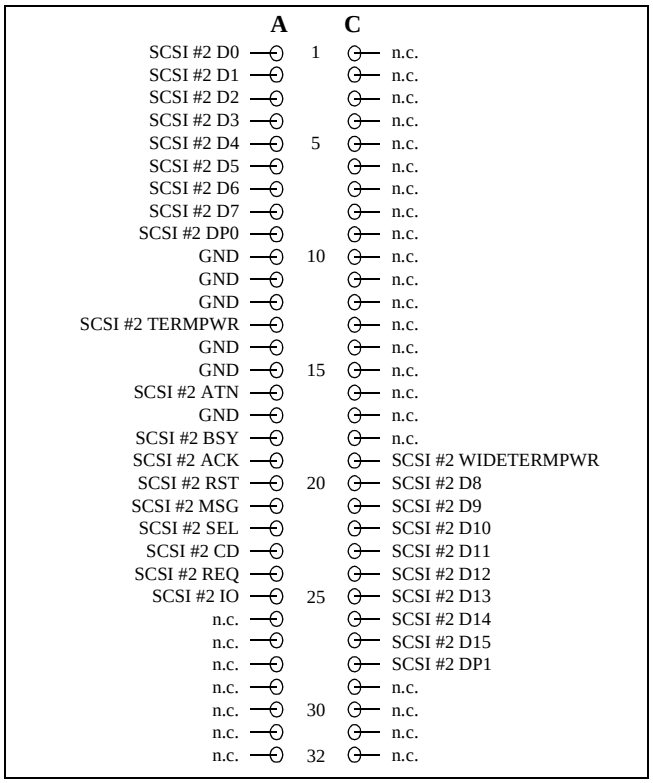


3.3.4 VMEbus P2 Connector Pinout

The standard I/O-50(G)T is delivered with 5-row P2 VMEbus connector. However, a 3-row P2 connector variant is also available as factory option.

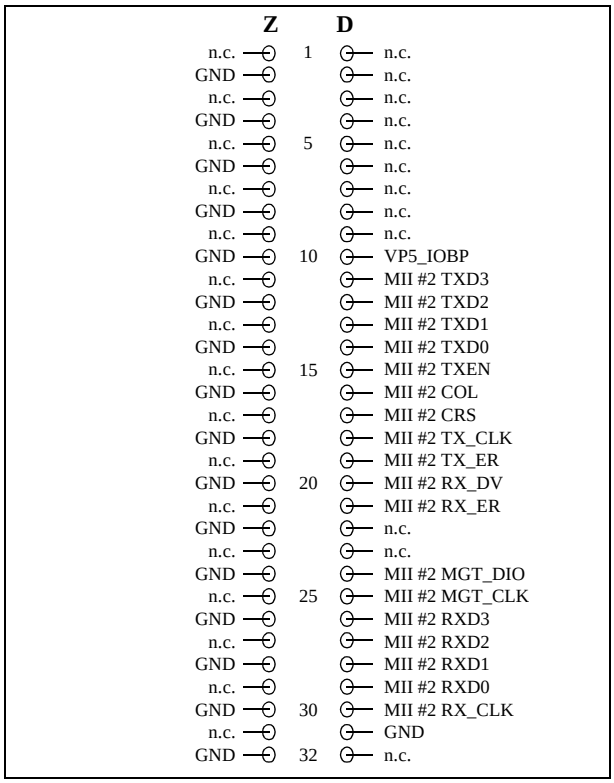
For further information, see “Backplane Configuration” on page 5 and “Slot-1 Function” on page 5.

Figure 20 3-row P2 Connector Pinout



The signals for rows Z and D (Ethernet MII interface) are shown in the following pinout for row Z and D.

Figure 21 **Pinout of Row Z and D of a 5-row P2 Connector**



I/O Panel

As a separate price list item an I/O panel is available for the I/O-50(G)T, the SPARC/IOBP-50/x (x=3 3-row backplane connector; x=5 5-row connector). An extended variant is the SPARC/CPU-50/AccKit/x which contains additionally to the I/O panel the following cables:

- A flat ribbon SCSI cable for the I/O panel
- A Twisted-Pair-Ethernet cable for the front panel.

The I/O panel supports the following interfaces:

- SCSI #2,
- MII #2 Ethernet.

Danger

The SPARC/IOBP-50/x is especially designed for the I/O-50(G)T. Do not use any other I/O panels on the I/O-50(G)T. In addition note:

- **Either use the front-panel or the I/O panel Ethernet interface, not both. Check the configuration of your I/O panel.**

3.3.5 VMEbus P0 Connector Pinout (Factory Option)

Note: **Note that in case of the PMC 1/2 Factory Option, which is described on page 53, half of the PMC 1 user I/O signals is connected to certain PMC 2 user I/O signals.**

Figure 22 **Factory Option P0 (5-row Female 95-pin Metric Connector)**

A	B	C		D	E
PMC 2 I/O 01	PMC 2 I/O 02	PMC 2 I/O 03	19	PMC 2 I/O 04	PMC 2 I/O 05
PMC 2 I/O 06	PMC 2 I/O 07	PMC 2 I/O 08	18	PMC 2 I/O 09	PMC 2 I/O 10
PMC 2 I/O 11	PMC 2 I/O 12	PMC 2 I/O 13	17	PMC 2 I/O 14	PMC 2 I/O 15
PMC 2 I/O 16	PMC 2 I/O 17	PMC 2 I/O 18	16	PMC 2 I/O 19	PMC 2 I/O 20
PMC 2 I/O 21	PMC 2 I/O 22	PMC 2 I/O 23	15	PMC 2 I/O 24	PMC 2 I/O 25
PMC 2 I/O 26	PMC 2 I/O 27	PMC 2 I/O 28	14	PMC 2 I/O 29	PMC 2 I/O 30
PMC 1 I/O 01	PMC 1 I/O 02	PMC 1 I/O 03	13	PMC 1 I/O 04	PMC 1 I/O 05
PMC 1 I/O 06	PMC 1 I/O 07	PMC 1 I/O 08	12	PMC 1 I/O 09	PMC 1 I/O 10
PMC 1 I/O 11	PMC 1 I/O 12	PMC 1 I/O 13	11	PMC 1 I/O 14	PMC 1 I/O 15
PMC 1 I/O 16	PMC 1 I/O 17	PMC 1 I/O 18	10	PMC 1 I/O 19	PMC 1 I/O 20
PMC 1 I/O 21	PMC 1 I/O 22	PMC 1 I/O 23	9	PMC 1 I/O 24	PMC 1 I/O 25
PMC 1 I/O 26	PMC 1 I/O 27	PMC 1 I/O 28	8	PMC 1 I/O 29	PMC 1 I/O 30
PMC 1 I/O 31	PMC 1 I/O 32	PMC 1 I/O 33	7	PMC 1 I/O 34	PMC 1 I/O 35
PMC 1 I/O 36	PMC 1 I/O 37	PMC 1 I/O 38	6	PMC 1 I/O 39	PMC 1 I/O 40
PMC 1 I/O 41	PMC 1 I/O 42	PMC 1 I/O 43	5	PMC 1 I/O 44	PMC 1 I/O 45
PMC 1 I/O 46	PMC 1 I/O 47	PMC 1 I/O 48	4	PMC 1 I/O 49	PMC 1 I/O 50
PMC 1 I/O 51	PMC 1 I/O 52	PMC 1 I/O 53	3	PMC 1 I/O 54	PMC 1 I/O 55
PMC 1 I/O 56	PMC 1 I/O 57	PMC 1 I/O 58	2	PMC 1 I/O 59	PMC 1 I/O 60
PMC 1 I/O 61	PMC 1 I/O 62	PMC 1 I/O 63	1	PMC 1 I/O 64	VP5_IOBP

3.4 OpenBoot Firmware Alias Definitions for I/O-50(G)T

The following table lists alias definitions related to the I/O-50(G)T.

Table 26 Device Alias Definitions

Alias	Description
	Defined for SCSI #2:
scsi-2	SCSI #2
disk26	disk SCSI #2-target-ID 6
disk25	disk SCSI #2-target-ID 5
disk24	disk SCSI #2-target-ID 4
disk23	disk SCSI #2-target-ID 3
disk22	disk SCSI #2-target-ID 2
disk21	disk SCSI #2-target-ID 1
disk20	disk SCSI #2-target-ID 0
tape2 (or tape20)	1st tape drive SCSI #2-target-ID 4
tape21	2nd tape drive SCSI #2-target-ID 5
cdrom2	CD-ROM partition f, SCSI #2-target-ID 6
	Defined for Ethernet #2:
net2	Ethernet #2
pcib-io	secondary PCI Bus B

Product Error Report

PRODUCT:	SERIAL NO.:
DATE OF PURCHASE:	ORIGINATOR:
COMPANY:	POINT OF CONTACT:
TEL.:	EXT.:
ADDRESS: _____ _____ _____	
PRESENT DATE:	
AFFECTED PRODUCT: ❑ HARDWARE ❑ SOFTWARE ❑ SYSTEMS	AFFECTED DOCUMENTATION: ❑ HARDWARE ❑ SOFTWARE ❑ SYSTEMS
ERROR DESCRIPTION: _____ _____ _____ _____ _____ _____ _____ _____ _____ _____	

THIS AREA TO BE COMPLETED BY FORCE COMPUTERS:

DATE:

PR#:

RESPONSIBLE DEPT.: ❑ MARKETING ❑ PRODUCTION
ENGINEERING ➠ ❑ BOARD ❑ SYSTEMS

✉ Send this report to the nearest Force Computers headquarter listed on the back of the title page.