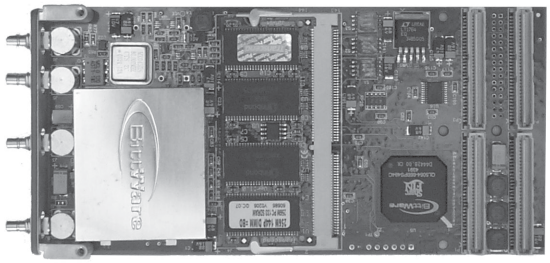
Barracuda-PMC+

High-Speed A/D I/O Card with Reconfigurable FPGA, 64/66 PCI, and SHARC® Link Ports



BittWare's Barracuda-PMC+ (BCPM) board is a high-speed analog input board that provides data capture for two 14-bit, up to 105 MHz A/D channels and streams the data directly to a Xilinx Virtex-II FPGA, which provides A/D control and data distribution and front-end processing capabilities. A 64-bit, 66 MHz PCI interface and four SHARC link ports make the captured data available to the host board, and a bank of up to 512 MB of SDRAM is available for snapshot acquisitions.

High-Speed A/D Interface

The high-speed A/D interface features two 14-bit A/D conversion channels, each sampled at up to 105 MHz. Using high-quality 14-bit A/D converters from Analog Devices, the analog interface provides input bandwidth up to 350 MHz and is available with AC or DC coupled inputs. For clocking options, the board features an internal clock with an on-board programmable clock divider and an external clock and trigger. An optional oven controlled crystal oscillator (OCXO) is available for a high-stability clock in place of the standard on-board oscillator.

Xilinx Virtex-II Reconfigurable FPGA

The Virtex-II reconfigurable FPGA (Xilinx) provides A/D control and data distribution for the Barracuda-PMC+ and is available for configurable preprocessing of high speed A/D data, such as digital filtering, decimation, and digital down conversion. To interface the A/D data to the host, the Virtex-II contains a link port interface for directly accessing ADSP-TS101S or ADSP-2116x DSPs and a local bus interface to access the PCI host and the SDRAM buffer.

SharcFIN ASIC 64-bit, 66 MHz PCI Interface

BittWare's SharcFIN ASIC provides a full 64-bit, 66 MHz bus mastering PCI interface and an SDRAM controller to interface the SDRAM and Virtex-II to the PCI host. The SharcFIN interfaces to the PCI bus at 64 bits, 66 MHz for 528 MB/s burst throughput and provides both bus mastering DMA capability and slave access to the SDRAM and Virtex-II.

PMC+ I/O Interface

The Barracuda-PMC+ is fully compatible with any PMC capable base board. When attached to one of BittWare's PMC+ base boards, it also supports BittWare's PMC+ extensions, which include four link ports directly to the Virtex-II FPGA. The PMC+ link ports are configurable for BittWare's Tiger (ADSP-TS101S) base boards* and are an ideal way to move high-speed data directly to the DSPs.

Available Development Tools

BittWare offers complete software development tools that allow designers to easily develop application code and integrate the Barracuda-PMC+ into their systems. For user-configured pre-processing, XILINX also provides a complete suite of development tools for the Virtex-II. BittWare also offers a Barracuda developer's kit for the Virtex-II that includes the source for the A/D, link port, and local bus interfaces.

** Link ports are not compatible with Hammerhead (ADSP-2116x) base boards.*

Features

- High-performance wideband A/D
  - 2-channel, 14-bit A/D (AD6645 or AD6644)
  - Up to 105 MHz per channel
- Virtex-II 1000 reconfigurable FPGA
  - A/D control and data distribution
  - Configurable pre-processing of high-speed A/D data
- 64-bit, 66 MHz bus mastering PCI interface via SharcFIN ASIC
- 64 - 512 MB SDRAM for snapshot acquisitions
- Four external link ports
  - Configurable for Tiger base boards*
  - Available via PMC+ interface
- Internal/external clock and triggering
- Oven-controlled oscillator for high stability clock (optional)
- Programmable clock divider for on-board clock
- Complete software support
- Virtex-II development and customization support

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Barracuda-PMC+ Specifications

BOARD ARCHITECTURE

A/D Interface

- Two 14-bit A/D converters, each with a single input channel
  - AD6645 at 80 or 105 MHz
  - AD6644 at 65 MHz
- SMA or SMB analog input connectors, terminated in 50 Ohm
- AC or DC coupled inputs

Xilinx Virtex-II FPGA

- 1 million system gates
- A/D control and data distribution
- Configurable pre-processing of high-speed A/D data
- SRAM-based in-system configuration via EPROM or host
- Four SHARC link ports from Virtex-II to PMC+ interface
- 19 digital I/O available via optional DIO connector
- Local parallel bus with high-speed access to SDRAM and SharcFIN ASIC
- FIFOs for storing A/D data
- User-configurable blocks

External Memory

- 64 - 512 MB SDRAM (standard 144-pin SODIMM) available for snapshot data acquisitions (will not support two channels at full speed)

PMC+ Interface

- Compatible with standard PMC modules
- Provides 4 link ports and I^2C, reset, and interrupt connections to BittWare PMC+ carrier boards

SharcFIN™ ASIC

- 64-bit, 66 MHz PCI rev. 2.2 compliant interface
- SDRAM and Virtex-II mapped to PCI memory space
- Universal 5V/3V PCI signaling
- Provides 64-bit, 66 MHz master/slave (528 MB/s peak transfer rate) access
- Backward compatible with 32-bit, 33 MHz PCI interfaces

Clocking Options

- 105 MHz on-board oven controlled crystal oscillator (OCXO) or standard oscillator (XO) with programmable clock divider
- External clock input
- External or internal trigger

Power

- +12V, +5V, and +3.3V required (available via PCI interface)

Size

- 149mm x 74mm (5.9" x 2.9")

SOFTWARE SUPPORT

Host Interface

- BittWare's software development kit for Windows® and Linux contains C-callable libraries for board control and communications routines
- Example software for controlling the board and viewing captured data
- Porting kit available for other operating system platforms

FPGA Development Support

- BittWare developer's kit with source for A/D, link port, and local bus interfaces
- Full customization services available

Ordering Information

BCPM-ABC-XYZ-JKLM

A: Channels
2= 2 Channels

B: ADC Speed
1= 65 MHz (AD6644)
2= 80 MHz (AD6645)
3= 105 MHz (AD6645)

C: Virtex-II Size and Speed
3= Model 1000; Speed grade 4

X: Input Coupling
A= AC coupled
D= DC coupled

M: PMC+ Connector
0= Not populated
1= Populated

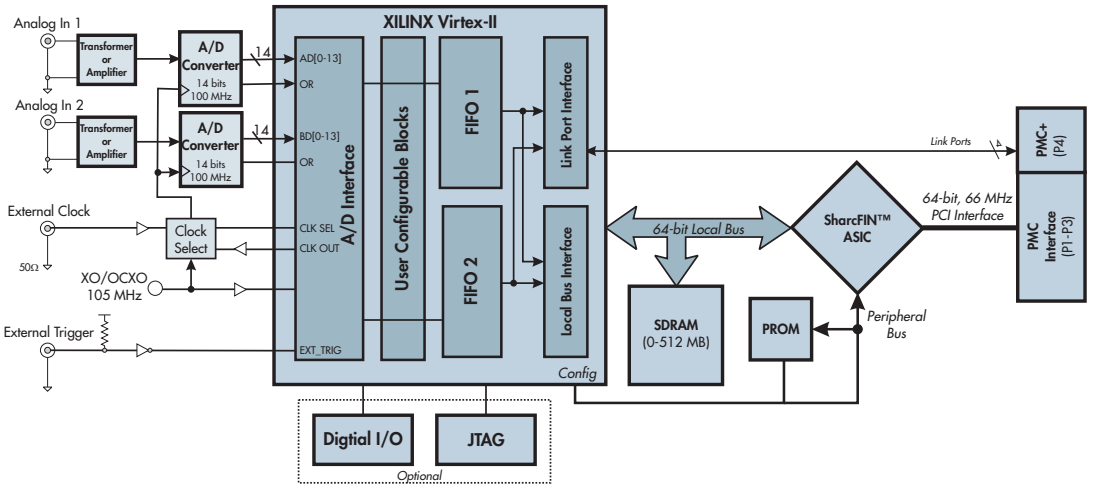
L: Front Panel Connectors
A= SMA
B= SMB

K: DIO Connector
0= Not populated
1= Populated*

J: JTAG Connector
0= Not populated
1= Populated *

Z: SDRAM
5= 64 MB
6= 128 MB
7= 256 MB
8= 512 MB†

Y: Oscillator**
0= No oscillator
1= XO (at speed grade)
2= OCXO (at speed grade)*
3= TCXO (at speed grade)*
S= Special frequency order



* Violates PMC height spec.
† Currently unavailable
** For 65 MHz ADC, oscillator is 64 MHz

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