M4K708

ARINC 708/453

Test and Simulation Module for the
EXC-4000 Family of Carrier Boards

User's Manual

EXCALIBUR SYSTEMS

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Table of Contents

1 Introduction

1.1 Overview 1-1
1.1.1 *M4K708* Module Features 1-2
1.1.2 *M4K708* Module Block Diagram 1-2

1.2 Installation 1-3
1.2.1 Module Installation 1-3
1.2.2 Adding *Software Tools* Drivers 1-3

1.3 *M4K708* General Memory Map 1-4

2 Channel Operation

2.1 Channel Operation 2-2
2.1.1 Channel Receive Operation 2-2
2.1.2 Channel Transmit Operation 2-3

2.2 Global Control Registers and Memory Map 2-4

2.3 Channel Control Registers and Memory Map 2-7

3 Mechanical and Electrical Specifications

3.1 Module Layout 3-1

3.2 LED Indicators 3-2
3.2.1 Factory DIP Switch Settings 3-2

3.3 Connectors 3-3
3.3.1 **EXC-4000** Carrier Board 96-pin Connector 3-3
3.3.2 *M4K708* Module Adapter Cable 3-4

3.4 Power Requirements 3-5

4 Ordering Information

Appendix A ARINC 708 Display Data Bus Word Format

Appendix A-1 ARINC 708 Word Format A-1
Appendix A-2 ARINC 708 Word Bits A-2

1 Introduction

Chapter 1 provides an overview of the *M4K708* avionics communication module. the following topics are covered:

1.1 Overview 1-1
1.1.1 *M4K708* Features 1-2
1.1.2 *M4K708* Module Block Diagram 1-2
1.2 Installation. 1-3
1.2.1 Module Installation 1-3
1.2.2 Adding *Software Tools* Drivers 1-3
1.3 *M4K708* General Memory Map. 1-4

1.1 Overview

The *M4K708* is an interface module for the multimode, multiprotocol Excalibur EXC-4000 family of carrier boards. The module is an ARINC 708/453 2-channel test and simulation module for the Weather Radar Display Databus. The *M4K708* supports two ARINC 708/453 channels, each selectable as transmit or receive. Each channel implements an 64K×16 FIFO and supports polling and/or interrupt driven operation.

The *M4K708* comes complete with Windows software, a C-driver software library including source code. In addition, Excalibur produces adapter cables that convert the carrier board I/O Molex™ connector to two twinax Trompeter CJ70 connectors (or equivalent). The cable may be purchased at an additional cost.

The *M4K708*-E option is an extended temperature (-40º to +85ºC), ruggedized version of the module for industrial or harsh environmental conditions.

1.1.1 *M4K708* Module Features

General Features

Supports 2 ARINC-708/453 channels, each programmable as transmit or receive

64K × 16 FIFO per channel holds up to 655 1600-bit words

Receive Channel

Receive features:
- Word status tagging
- Word time tagging (32-bit)
- Receive count interval trigger

Receive counter [indicates number of words received]

Polling conditions:
- FIFO full
- FIFO half full
- FIFO empty
- '*n*' Words received

Interrupt conditions:
- FIFO full
- '*n*' Words received

Physical Characteristics

Dimensions: 67mm × 48mm
Weight: 20g

Operating Environment

Temperature: 0° to 70°C standard temperature
-40° to +85°C extended temperature [optional]
Humidity: 5%–90% condensing

Optional bus termination

Interrupt and polling modes of operation

Loopback test capability

Transmit Channel

Transmission modes:
- One-shot [one 1600-bit word at a time]
- Continuous [as long as FIFO not empty]
- Continuous FIFO retransmit

Programmable inter word gap time [0–6.5 sec @ 100μsec resolution]

Polling conditions:
- FIFO full
- FIFO half full
- FIFO empty
- '*n*' Words transmitted

Interrupt conditions:
- FIFO empty
- '*n*' Words transmitted

Host Interface

EXC-4000 series of carrier boards
Power:+5V @ 600mA both channels transmitting @ 50% duty cycle

Software Support

C drivers with source code

See **Chapter 4 Ordering Information**, for exact part numbers.

1.1.2 *M4K708* Module Block Diagram

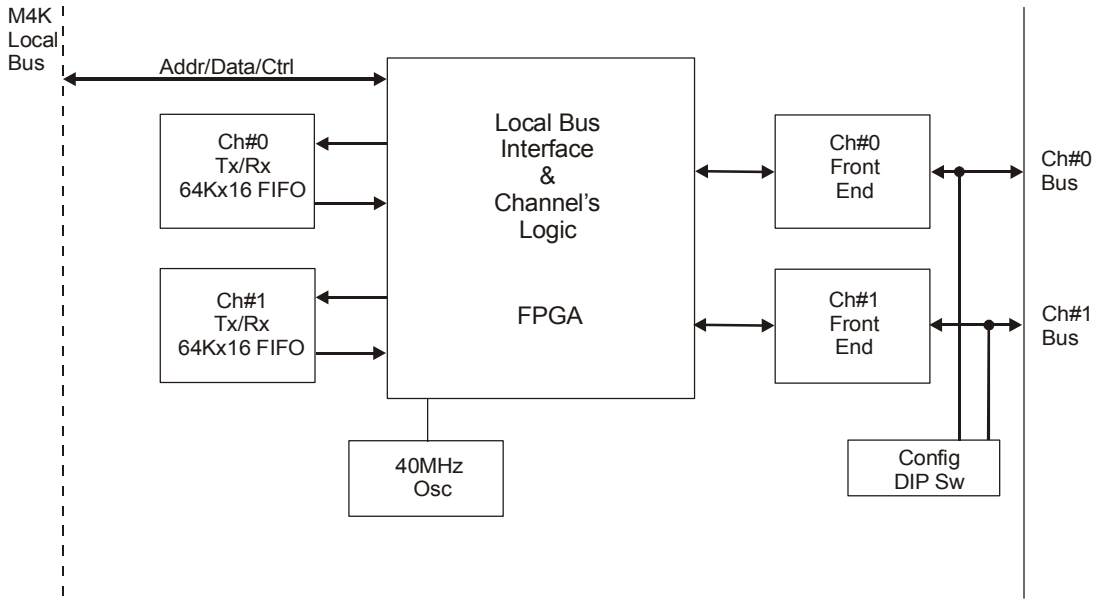

Figure 1-1 *M4K708* Module Block Diagram

1.2 Installation

To operate the *M4K708* module:

1. Install the EXC-4000 carrier board with the module in the computer.
2. Add *Software Tools* drivers to the hard disk.

1.2.1 Module Installation

Warning: Wear a suitably grounded, electrostatic discharge wrist strap whenever handling the *M4K708* module and use all antistatic precautionary measures.

1. If the module is supplied separately from the carrier board, *very carefully*, insert the module on to the desired module location on the carrier EXC-4000 board. The pin #1 marker (marked with a white rectangle) on the module must be aligned with the white rectangles on the carrier board.
2. With the computer power source switched **off**, insert the EXC-4000 carrier board with the *M4K708* module into a slot in the computer.
3. Attach the 708 adapter cable to the carrier board I/O connector and to the bus.

For more information about installing the module, see **Chapter 3 Mechanical and Electrical Specifications**.

1.2.2 Adding *Software Tools* Drivers

The standard software included with the *M4K708* module is for Windows operating systems. Software compatible with other operating systems is available and can be downloaded from our website: www.mil-1553.com.

For information about installing the accompanying software drivers, see the **Readme.pdf** file for the *M4K708* module on the *Excalibur Installation CD* that came with your module.

1.3 *M4K708* General Memory Map

The *M4K708* memory map is divided into four regions – three memory regions and one reserved region:

Region 1 [1 Kbytes] is the Channel #0 memory space;
Region 2 [1 Kbytes] is the Channel #1 memory space;
Region 3 [1 Kbytes] is the Global memory space;
Region 4 – reserved

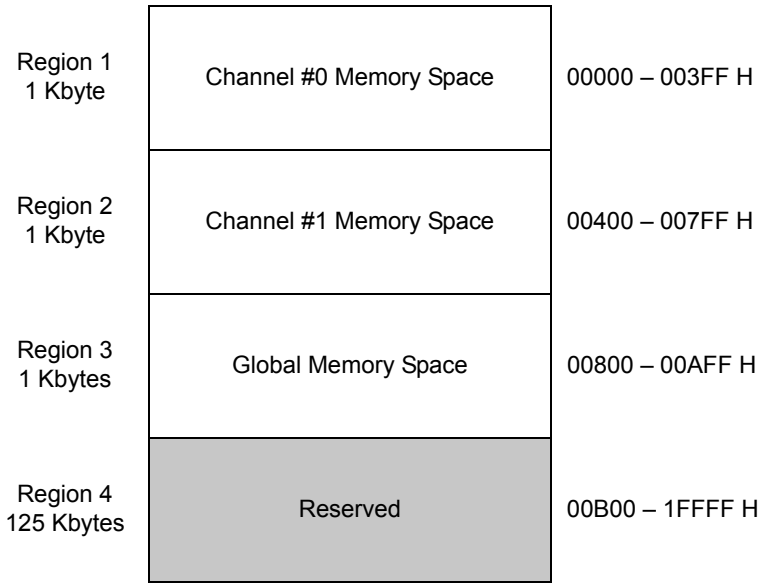

Figure 1-2 *M4K708* General memory Map

For a description of the channel receive and transmit operation as well as Global and Channel Control registers see Chapter 2. Chapter 3 includes details of the Mechanical and Electrical Specifications of the *M4K708* Module.

2 Channel Operation

Chapter 2 describes *M4K708* module operation.

2.1 Channel Operation 2-2
2.1.1 Channel Receive Operation 2-2
2.1.2 Channel Transmit Operation 2-3
2.2 Global Control Registers and Memory Map 2-4
2.2.1 Global Hardware Revision Register 2-4
2.2.2 Global Software Reset Register 2-5
2.2.3 Global Configuration Register 2-5
2.2.4 Global Start Register 2-5
2.2.5 Global Interrupt Status Register 2-6
2.2.6 Global Time Tag Reset Register 2-6
2.2.7 Global Time Tag Counter 2-6
2.3 Channel Control Registers and Memory Map 2-7
2.3.1 Channel Software Reset Register 2-7
2.3.2 Channel Control Register 2-8
2.3.3 Channel Start/Stop Register 2-8
2.3.4 Channel Status Register 2-9
2.3.5 Channel Interrupt Mask Register 2-9
2.3.6 Channel Interrupt Status Register 2-10
2.3.7 Channel Interrupt Clear Register 2-10
2.3.8 Channel Event Frequency Register 2-11
2.3.9 Channel FIFO Counter Register 2-11
2.3.10 Channel Output Trigger Mask Register 2-11
2.3.11 Receive FIFO Read Register 2-13
2.3.12 Receive FIFO Word Type Register 2-14
2.3.13 Receive FIFO Word Count Register 2-14
2.3.14 Transmit FIFO Data / First / Last Write Register 2-14
2.3.15 Transmit Interval Value Register 2-15

2.1 Channel Operation

Each channel's mode of operation, either transmit or receive, is selected through bits in the **Global Configuration Register**. Selecting the mode sets also the direction of the channel's FIFO. Within the channel's Memory space there are three groups of registers:

- The first group is common to transmit and receive modes
- The second group is dedicated to receive mode only
- The third group of registers is dedicated to transmit mode only

Each channel provides interrupts/triggers or polling bits on two occasions. The first occasion (Word Over) is set by the **Channel Event Frequency Register** with the number of 708 Words received/sent between the occasions. The second occasion (FIFO Over) indicates a FIFO overrun/underrun Error condition. In addition the channels can be set up in an Internal loopback configuration. This crosswire connection allows the user to perform a full module's internal self test by transmitting, receiving and comparing in both directions, including interrupts and all other registers functionality.

2.1.1 Channel Receive Operation

In receive mode, after start is activated, each 708 Word is stored in the FIFO as a block of 103 16-bit words (see **Figure 2-3 Received 708 Word Block Structure,** on page 2-12). The first two words in the FIFO block are Time_Tag_Lo (first) and Time_Tag_Hi, indicating the word time stamp, then follow the 100 words comprising the 1600-bits of the 708 Word, and finally comes the Status Word, indicating the word status (valid or not). During the storing process, the Channel FIFO Counter is incremented each write to the FIFO. The **Receive FIFO Word Count Register** is incremented by 1 at the end of receiving the 708 Word. The next received 103 word block is pushed into the FIFO immediately after it. The user can read the FIFO in conjunction with interrupts or polling bits or counters value or **Channel Status Register** bits (FIFO not empty or half full). Each 16-bit word read from the FIFO can be evaluated by reading the **Receive FIFO Word Type Register** immediately after it in order to follow the block structure.

Note: The first bit received from the 708 bus is located at the least significant bit (LSB) of the first data word read from the fifo. In the same way each following 16 bits are shifted in (shift right).

2.1.2 Channel Transmit Operation

In transmit operation the data words are loaded by the user into the FIFO and once start is activated, are transmitted in the run mode selected by the **Channel Control Register** bits. Transmission stops as soon as the FIFO reaches an empty condition. There are three run modes: One-shot, Continuous and Continuous FIFO Retransmit.

Run Mode	Description
One Shot	Transmits one 708 Word and then clears the Start/Stop bit
Continuous	Transmits 708 Words continuously as long as the fifo is not empty
Continuous FIFO Retransmit	The FIFO is preloaded with a set of 708 Words and after start is activated, this set of words is retransmitted continuously

In the continuous modes the 708 Words are sent in time intervals set by the **Transmit Interval Value Register**. The user can write to the FIFO in conjunction with interrupts or polling bits or **Channel FIFO Counter Register** value or **Channel Status Register** bits (FIFO not full or half full or channel in transmit).

Each 708 Word written into the FIFO is a block of 100 16-bit words, which are loaded by the user through three registers. The first word is written to the **Transmit FIFO First Write Register**, the next 98 words are written to the **Transmit FIFO Data Register** and the last word is written to the **Transmit FIFO Last Write Register**. The reason for using three registers is to indicate to the hardware the beginning and end of the block. See **Figure 2-2 Channel Memory Maps,** on page 2-7and **Transmit FIFO Data / First / Last Write Register,** page 2-13.

Note: The least significant bit (LSB) of the first data word written to the FIFO is the first bit transmitted over the 708 bus. In the same way each following 16 bits are shifted out (shift right).

2.2 Global Control Registers and Memory Map

The global memory block contains all the module global functions.

Global Hardware Revision	00800 H
Global Software Reset	00802 H
Global Configuration	00804 H
Global Start	00806 H
Global Interrupt Status	00808 H
Global Time Tag Reset	0080AH
Global Time Tag Counter	0080C – 0080E H
Spare	00810 H
Reserved [Factory test]	00812 H
Reserved	00814 – 1FFFF H

Figure 2-1 Global Registers Memory Map

2.2.1 Global Hardware Revision Register **Address: 00800 (H)**

Read The Global Hardware Revision register indicates the hardware FPGA revision level.

Bit	Bit Name	Description
04-15	Module ID	Hard coded to value 708 H
00-03	FPGA Rev.	1 = Rev 1 2 = Rev 2 3 = Rev 3

Global Hardware Revision Register

2.2.2 Global Software Reset Register — Address: 00802 (H)

Write Writing any value to the Global Software Reset register resets the whole module.

2.2.3 Global Configuration Register — Address: 00804 (H)

Write/ Read The Global Configuration register is used to set the channel configuration and select the self-test configuration.

The internal loopback configuration connects the channel's digital internal input/ output signals. This mode can be used to check the whole channel's logic by transmitting /receiving test words in both directions. No data is transmitted over the 708/453 bus in this mode.

This register is initialized to 0000 (H) at reset.

Bit	Bit Name	Description
04-15	Reserved	Set to 0
03	ST3	Reserved
02	ST	Self-test configuration 0 = No self-test 1 = Internal loopback configuration
01	CG1	Channel 1 Configuration set 0 = Receive 1 = Transmit
00	CG0	Channel 0 Configuration set 0 = Receive 1 = Transmit

Global Configuration Register

2.2.4 Global Start Register — Address: 00806 (H)

Write Writing any value to the Global Start register will start both channels running simultaneously *once* both channels are fully setup.

To start the channels individually, see section **2.3.3 Channel Start/Stop Register,** page 2-8.

2.2.5 Global Interrupt Status Register

Address: 00808 (H)

Read The Global Interrupt register indicates the channel's interrupt status. The **Channel Interrupt Clear Register** resets the status bits.

Bit	Bit Name	Description
02-15	Reserved	Set to 0
01	IS1	Channel 1 Interrupt Status 0 = Bit not active 1 = Interrupt active
00	IS0	Channel 0 Interrupt Status 0 = Bit not active 1 = Interrupt active

Channel Interrupt Status Register

2.2.6 Global Time Tag Reset Register

Address: 0080A (H)

Write Writing any value to the Global Time Tag Reset register reset's the module's Time Tag Counter.

2.2.7 Global Time Tag Counter

Address: 0080C (H)
0080E (H)

Read The two Global Time Tag Counter words represent the current value of the free-running 32-bit Time Tag counter. The counter may be read at any time. Keep the following read sequence:

FIRST: 0080C H (Lo Word - LSB)

LAST: 0080E H (Hi Word - MSB)

The resolution of the counter is 10 µsec. The counter is reset to 0 upon power-up or software reset or through the **Global Time Tag Reset Register**. After the reset operation, the counter starts counting. When the counter reaches the value FFFF FFFF (H), it wraps around to 0 and continues counting.

2.3 Channel Control Registers and Memory Map

The Channel Control Registers must be set for each channel separately.

Register	Channel #0	Channel #1
Channel Software Reset [W]	00000 H	00400 H
Channel Control [W/R]	00002 H	00402 H
Channel Start/Stop [W/R]	00004 H	00404 H
Channel Status [R]	00006 H	00406 H
Channel Interrupt Mask [W/R]	00008 H	00408 H
Channel Interrupt Status [R]	0000A H	0040A H
Channel Interrupt Clear [W]	0000C H	0040C H
Channel Event Frequency [W/R]	0000E H	0040E H
Channel FIFO Counter [R]	00010 H	00410 H
Channel Output Triggers Mask [W/R]	00012 H	00412 H
Reserved	00014 – 00001E H	00414 – 0041E H
Receive FIFO Read [R]	00020 H	00420 H
Receive FIFO Word Type [R]	00022 H	00422 H
Receive FIFO Word Count [R]	00024 H	00424 H
Receive Spare	00026 H	00426 H
Reserved	00028 – 0003E H	00428 – 0043E H
Transmit FIFO Data Write [W]	00040 H	00440 H
Transmit FIFO First Write [W]	00042 H	00442 H
Transmit FIFO Last Write [W]	00044 H	00444 H
Reserved	00046 –00048 H	00446 – 00448 H
Transmit Interval Value [W/R]	0004A H	0044A H
Reserved	0004C – 003FE H	0044C – 007FE H

Figure 2-2 Channel Memory Maps

2.3.1 Channel Software Reset Register **Address: xx000 (H)**

Write Writing any value to the Channel Software Reset register resets the whole channel.

2.3.2 Channel Control Register

Address: xx002 (H)

Write/ Read

The Channel Control register sets the parameters for the Channel Receive and Transmit modes.

This register is initialized to 0000 (H) at reset.

Bit	Bit Name	Description
02–15	Reserved	Set to 0
00-01	RNM	Tx Run Mode 00 = One-shot mode (single word) 01 = Continuous mode (as long as Tx FIFO not empty) 10 = Continuous FIFO retransmit mode 11 = Reserved

Channel Control Register

2.3.3 Channel Start/Stop Register

Address: xx004 (H)

Write/ Read

Writing to the Channel Start/Stop Register starts or stops the channel running.

This register is initialized to 0000 (H) at reset.

Bit	Bit Name	Description
01–15	Reserved	Set to 0
00	STR	Start/Stop 0 = Stop channel transmission/reception at the end of current word processing 1 = Start the channel transmission/reception In transmit one-shot mode this bit is automatically cleared

Channel Start/Stop Register

2.3.4 Channel Status Register

Address: xx006 (H)

Read

The Channel Status register provides various channel status bits and is initialized to 0001 (H) at reset

Bit	Bit Name	Description
05–15	Reserved	Set to 0
04	HCB	Channel FIFO Counter bit 16 [see **Channel FIFO Counter Register,** page 2-11]
03	ITX	Channel in Transmit (Tx mode) 0 = Channel not transmitting 1 = Channel is in Transmit state
02	FUL	Channel FIFO full (Tx mode) 0 = Bit not active 1 = FIFO full (65536 16-bit Words)
01	HFL	Channel FIFO half full (Tx and Rx mode) 0 = Bit not active 1 = FIFO half full (more than 32768 16-bit Words)
00	EMT	Channel FIFO empty (Rx mode) 0 = Bit not active 1 = FIFO empty (0 Words)

Channel Status Register

2.3.5 Channel Interrupt Mask Register

Address: xx008 (H)

Write/ Read

Setting a bit of the Channel Interrupt Mask register enables the corresponding channel interrupt.

Initialized to 0000 (H) at reset.

Bit	Bit Name	Description
02–15	Reserved	Set to 0
01	WOM	Word Over Mask 0 = Disable WOV bit interrupt 1 = Enable WOV bit interrupt
00	FOM	FIFO Over Mask 0 = Disable FOV bit interrupt 1 = Enable FOV bit interrupt

Channel Interrupt Mask Register

2.3.6 Channel Interrupt Status Register

Address: xx00A (H)

Read

Each bit in the Channel Interrupt Status register indicates the corresponding interrupt status. These bits will be set regardless of the state of the Channel Interrupt Mask register bits.

Initialized to 0000 (H) at reset.

Note: After receipt of an interrupt, the user must reset the interrupt condition bit via the **Channel Interrupt Clear Register**

Bit	Bit Name	Description
02–15	Reserved	Set to 0
01	WOV	Word Over [Tx/Rx Interrupt] 0 = Bit not active 1 = Number of 708 Words, set in the **Channel Event Frequency Register**, were transmitted/received.
00	FOV	FIFO Over [Error Interrupt] 0 = Bit not active 1 = All Words in channel were transmitted and the FIFO is empty (in Continuous mode) in Tx mode or the FIFO reached full state in Rx mode.

Channel Interrupt Status Register

2.3.7 Channel Interrupt Clear Register

Address: xx00C (H)

Write

Writing to the Channel Interrupt Clear Register clears the corresponding Channel Interrupt Status register bit.

Bit	Bit Name	Description
02–15	Reserved	Set to 0
01	WOC	Word Over Clear 0 = Bit not active 1 = Clear WOV bit interrupt
00	FOC	FIFO Over Clear 0 = Bit not active 1 = Clear FOV bit interrupt

Channel Interrupt Clear Register

2.3.8 Channel Event Frequency Register

Address: xx00E (H)

Write/ Read

The user sets the Channel Event Frequency Register to the number of ARINC 708 Words to be sent/received between interrupts/triggers.

Bit	Bit Name	Description
10-15	Reserved	Set to 0
00-09	Intrpt_Intrvl	Number of 708 Words to be sent/received between interrupts. Transmit: maximum value = 655 Receive: maximum value = 636 Minimum value = 1 Set to '1' upon power-up or reset

Channel Event Frequency Register

2.3.9 Channel FIFO Counter Register

Address: xx010 (H)

Read

The user reads the Channel FIFO Counter register in order to know the exact quantity of words currently residing within the channel's FIFO. Each write to the FIFO the counter is incremented by 1 and each read it is decremented by 1. The counter is initialized to 0000(H) at reset. While in Continuous FIFO Retransmit mode the counter holds a fixed value with the number of words written to the FIFO before start.

Bit	Bit Name	Description
00-15	FIFO_Cntr	Number of words residing within the FIFO. Bit 16 of this counter resides at bit 04 within the Channel Status register. It is active for one value only when the FIFO is full to represent 65536 [10000 H].

Channel FIFO Counter

2.3.10 Channel Output Trigger Mask Register

Address: xx012 (H)

Write/ Read

Setting a bit of the Channel Output Trigger Mask register enables the corresponding trigger condition to send a pulse over the OUTRIGn output pin (see **3.3.1.1 Module Terminal Stick Pin Assignments And Description** on page 3-4).

The register is initialized to 0000(H) at reset.

Bit	Bit Name	Description
02-15	Reserved	
01	TWOM	Trigger Word Over Mask 0 = Disable WOV bit condition 1 = Enable WOV bit condition
00	TFOM	Trigger FIFO Over Mask 0 = Disable FOV bit condition 1 = Enable FOV bit condition

Channel Output Trigger Mask

See **Channel Interrupt Status Register,** page 2-10.

2.3.11 Receive FIFO Read Register

Address: xx020 (H)

Read

In receive mode this FIFO register contains the received data information and may be read as long as the EMT (Channel FIFO Empty) bit is '0'. The type of each 16-bit Word read from the FIFO, can be verified by reading the Receive FIFO Word Type register immediately after it.

Each received 1600-bit 708 Word block is stored in the FIFO in the following sequence:

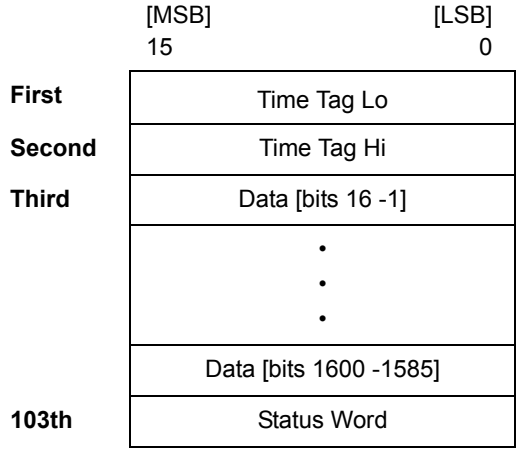

Figure 2-3 Received 708 Word Block Structure

Bit	Bit Name	Description
00-15	Ttag_Lo	Lower 16 bit of the 32 bit Time_tag value [resolution 10 μsec]

708 Word Receive Block - Time Tag Lo word

Bit	Bit Name	Description
00-15	Ttag_Hi	Upper 16 bit of the 32 bit Time_tag value

708 Word Receive Block - Time Tag Hi word

Bit	Bit Name	Description
01-15	Reserved	Set to 0
00	VW	Valid Word 0 = Not valid (Manchester/bit count error) 1 = Valid

708 Word Receive Block - Status word

2.3.12 Receive FIFO Word Type Register

Address: xx022 (H)

Read The Receive FIFO Word Type Register provides the currently read FIFO 16-bit word type. It can be read, every time, immediately after reading the Receive FIFO Read Register to review the current Word type.

Bit	Bit Name	Description
02-15	Reserved	Set to 0
00-01	RFWT	Receive FIFO Word Type 10 = Time Tag Lo 11 = Time Tag Hi 00 = Data 01 = Status

Receive FIFO Word Type Register

2.3.13 Receive FIFO Word Count Register

Address: xx024 (H)

Read The Receive Word FIFO Count register indicates the number of 708 Words received (0 – 65535). The register wraps around to 0 after reaching the maximum value of FFFF (H).

Initialized to 0000 (H) after reset

2.3.14 Transmit FIFO Data / First / Last Write Register

Address: xx040 (H), xx042 (H), xx044 (H)

Write In Transmit mode these FIFO registers contain the data to be transmitted and are written as long as the FUL (Channel FIFO Full) bit is '0'. Each 1600-bit 708 Word block is comprised of 100 16-bit words and must be written in the following sequence:

Register	Sequence	Content	Address
First	First write	Data bits [16 - 1]	xx042 H
Data	Next 98 writes	Data bits [1584 - 17]	xx040 H
Last	Last write	Data bits [1600 - 1585]	xx044 H

The block is written in separate addresses in order to indicate to the hardware the beginning and end of the 708 Word block.

2.3.15 Transmit Interval Value Register

Address: xx04A (H)

Write/ Read

In continuous modes the Transmit Interval Value Register sets the interval time between the start of each of the contiguous 708 words.

Bit	Bit Name	Description
00-15	Intrvl_Val	Interval Value Resolution = 0.1msec/bit. Minimum interval time = 1.6msec [0010 H value in register] for no gap between words Maximum interval time ≅ 6.5 sec.[FFFF H] Set to 0037 (H) upon power-up or reset for a default value of 5.5 msec

Transmit Interval Value Register

3 Mechanical and Electrical Specifications

Chapter 3 describes the mechanical and electrical specification of the *M4K708* module.

3.1 Module Layout 3-1
3.2 LED Indicators 3-2
3.2.1 Factory DIP Switch Settings 3-2
3.3 Connectors 3-3
3.3.1 **EXC-4000** Carrier Board 96-pin Connector 3-3
3.3.2 *M4K708* Module Adapter Cable 3-4
3.4 Power Requirements 3-5

3.1 Module Layout

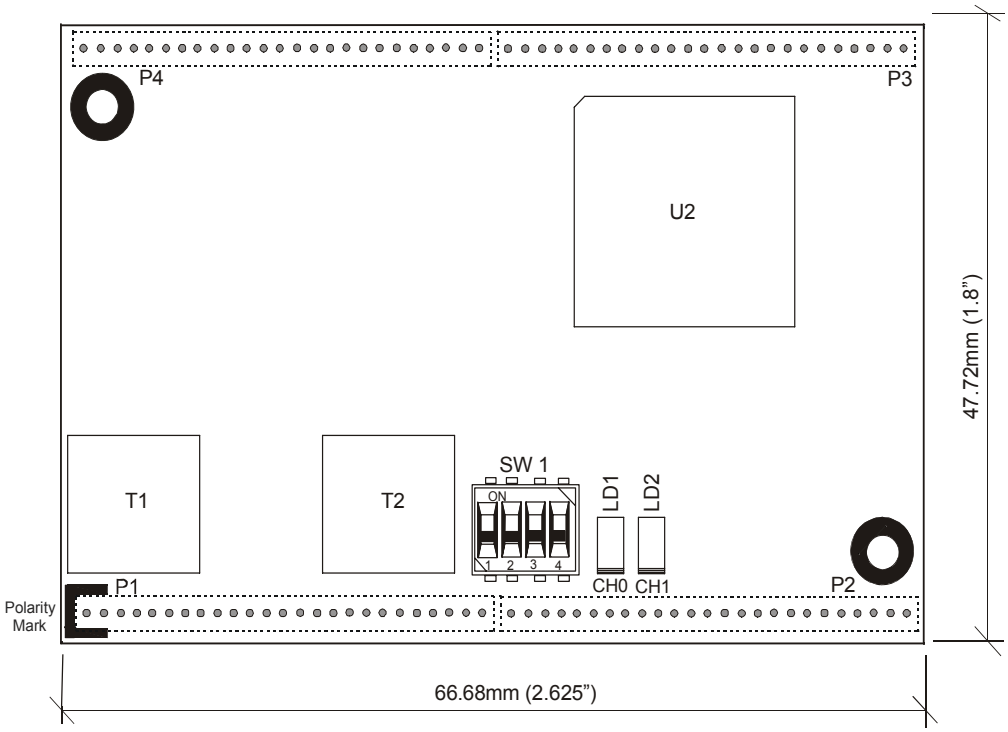

Figure 3-1 *M4K708* Module Layout – top view

3.2 LED Indicators

The *M4K708* contains two LEDS:

LED	Indications
LD1	Activity on channel 0
LD2	Activity on channel 1

LED Indicators

The *M4K708* SW1 DIP Switch sets the channel termination.

SW1 Switch #	Function	Position Assignment
1	Channel 0 Reserved	ON = Reserved OFF = Reserved
2	Channel 0 Termination Select	ON = 78 Ohm termination OFF = None
3	Channel 1 Reserved	ON = Reserved OFF = Reserved
4	Channel 1 Termination Select	ON = 78 Ohm termination OFF = None

Table 3-1 Channel Termination DIP Switch SW1

3.2.1 Factory DIP Switch Settings

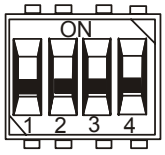

Figure 3-2 DIP Switch: top view

Dip Switch	Switch Position	Description
SW1	All segments to ON	Channels set to 78 Ohm termination

Table 3-2 Factory Default DIP Switch Settings

3.3 Connectors

The *M4K708* contains four 25-pin, 0.05" spacing strips (P1 – P4), which comprise a total of 100 pins for all module connections. These pins mate with the carrier board socket strips. Out of these 100 pins, 24 pins are assigned for the communication I/O signals. On the EXC-4000 carrier board all the module's 24 I/O signals are wired to a 96-pin female connector. This connector is divided into 4 rows (or terminal sticks) of 24 pins each. Each terminal stick is intended for a specific module location. See Figure 3-3.

3.3.1 EXC-4000 Carrier Board 96-pin Connector

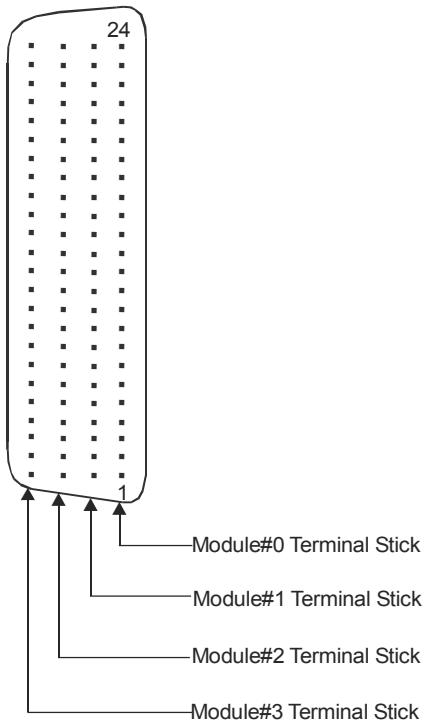

Figure 3-3 EXC-4000 Carrier Board 96-pin Connector Layout: Front View

3.3.1.1 Module Terminal Stick Pin Assignments And Description

Pin #	Signal Name	Description
1	SHIELD	Provided for the cables shield connection. This signal is connected to the computer's case through the carrier board's bracket or panel.
2	BUS0L	Channel 0 Lo connection
3	BUS0H	Channel 0 Hi connection
4–9	Reserved	Reserved pins - no connections
10	BUS1L	Channel 1 Lo connection
11	BUS1H	Channel 1 Hi connection
12	SHIELD	Provided for the cables shield connection. This signal is connected to the computer's case through the carrier board's bracket or panel.
13–22	Reserved	Reserved pins - no connections
23	OUTRIGn	Output trigger low active output. Provides trigger pulses of approximately 500 nsec. width and is activated upon the same conditions as interrupts. See **2.3.10 Channel Output Trigger Mask Register** on page 2-11.This output is an open-collector type pulled up with a 330-Ohm resistor to 5V.
24	GND	Provides ground reference for the OUTRIGn output.

Table 3-3 Module Terminal Stick Pin Assignments and Description

3.3.2 *M4K708* Module Adapter Cable

Excalibur will provide at an extra cost a standard adapter cable which converts the Molex® terminal stick to two female twinax connectors [Trompeter CJ70 or equivalent] for Channel 0 and Channel 1.

The twinax connectors mate, for example, with Trompeter PL75 male twinax connectors. These connectors are not supplied by Excalibur.

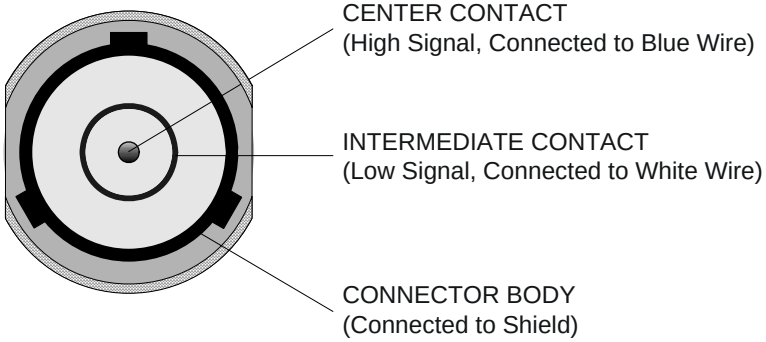

Figure 3-4 Twinax Connector– Front View

3.3.2.1 M4K708 Adapter Cable Connectors Pin Assignments

	Twinax Connector Pin Position	Signal Name	Description
Channel 0	CENTER PIN	BUS0H	Channel 0 connection Hi
	INNER SHEATH	BUS0L	Channel 0 connection Lo
	BODY ASSEMBLY	SHIELD	Cables shield connection
Channel 1	CENTER PIN	BUS1H	Channel 1 connection Hi
	INNER SHEATH	BUS1L	Channel 1 connection Lo
	BODY ASSEMBLY	SHIELD	Cables shield connection

Table 3-4 Adapter Cable Twinax Connectors Pin Assignments

For more information refer to **Ordering Information** in the EXC-4000 carrier board *User's Manual*.

3.4 Power Requirements

The *M4K708* maximum power requirements:

Requirement	Condition
+5V@150mA	Two channels receive
+5V@400mA	One receive, one transmit @ 50% duty cycle
+5V@600mA	One receive, one transmit @ 100% duty cycle
+5V@650mA	Both transmit @ 50% duty cycle
+5V@1050mA	Both transmit @ 100% duty cycle

4 Ordering Information

Chapter 4 explains the options to indicate when ordering a *M4K708* module.

Basic Part Number	Option	Description
M4K708		ARINC 708/453 interface module for the EXC-4000 family of carrier boards. Supports 2 channels.
	-E	Same as above with extended temperature option: -40° to +85°C
Optional Adapter cable		
X4KCx		*M4K708* adapter cable, 0.5 meter length with 2 twinax female connectors. See **M4K708 Module Adapter Cable** on page 3-4.

Appendix A ARINC 708 Display Data Bus Word Format

Appendix A-1 ARINC 708 Word Format

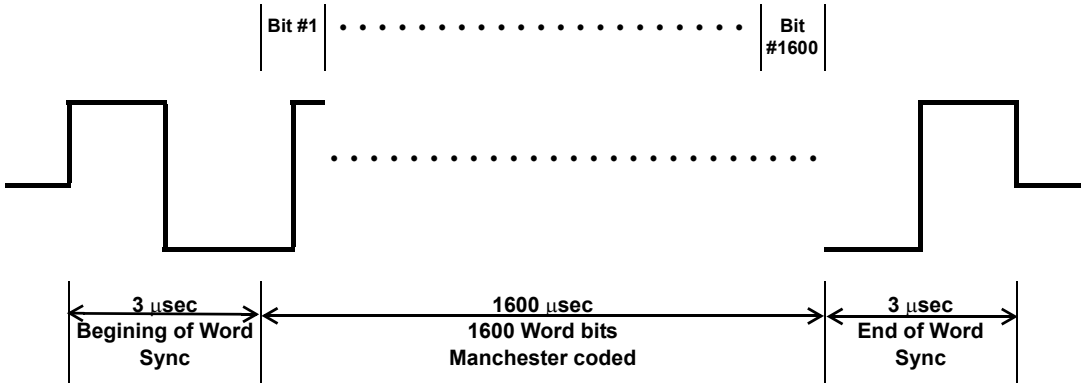

Figure A-1 ARINC 708 Waveform Pattern

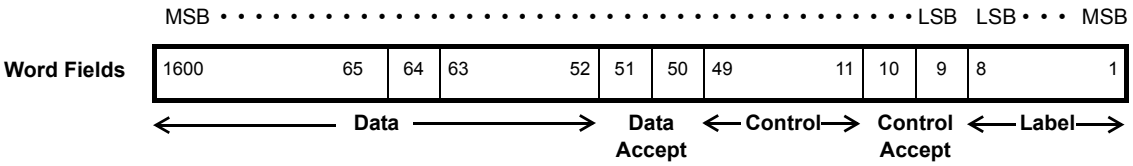

Figure A-2 ARINC 708 Word Fields

Bits	Data Display	Function details	page
01– 08	Label	055 (octal)	
09 – 10	Control Accept	see **Table A-2 Control Accept Functions**	A-2
11	Slave	0 = Master (Normal) 1 = Slave	
12 – 13	Spare		
14 – 18	Mode Annunciation	see **Table A-3 Mode Annunciation**	A-2
19 – 25	Faults	see **Table A-5 Faults**	A-3
26	Stabilization	0 = Stabilization OFF 1 = Stabilization ON	
27 – 29	Mode	see **Table A-6 Operating mode**	A-3
30 – 36	Tilt	see **Table A-7 Tilt data**	A-4
37 – 42	Gain	see **Table A-8 Gain data**	A-4
43 – 48	Range	see **Table A-9 Range Data**	A-4
49	Spare		
50 – 51	Data Accept	see **Table A-10 Data accept**	A-5
52 – 63	Scan Angle	see **Table A-11 Scan angle**	A-5
64	Spare		
65 – 67	Bin 1		
. . .	. . .	see **Table A-12 Weather Condition / Reflectivity Data**	A-5
1598 – 1600	Bin 512		

Table A-1 Display Data Bus Word Format

Note: The lowest order bit is referred to as bit 8 for the **Label** field while for the other fields it is referred to as bit 9.

Appendix A-2 ARINC 708 Word Bits

Control Accept Function

Matrix Code	Bit 10	Bit 9	Function
0	0	0	Do not accept control
1	0	1	IND 1 accept control
2	1	0	IND 2 accept control
3	1	1	All INDs accept control

Table A-2 Control Accept Functions

Mode Annunciation

Bit	18	17	16	15	14	Function
	0	0	0	0	0	Normal
	1	0	0	0	0	Antenna stability limits
	0	1	0	0	0	Sector scan
	0	0	1	0	0	Anti clutter
	0	0	0	1	0	Weather alert
	0	0	0	0	1	Turbulence alert

Table A-3 Mode Annunciation

Bits 14 – 18 should be independently coded to indicate (when to set to 1) to the display or other receiver device the following:

Bit	Code indicator
14	Automatic sensing of a **Turbulence alert** has occurred
15	Automatic sensing of a reflectivity **Weather alert** has occurred
16	Clutter elimination circuitry is in operation
17	Reduced **Sector scan** is in operation
18	Aircraft attitude and /or tilt control exceeds the system's design limits.

Table A-4 Mode annunciation code indicator

Faults - coded independently

Bit	25	24	23	22	21	20	19	LRU Failure Indication
	0	0	0	0	0	0	0	No detected faults
	1	0	0	0	0	0	0	Transmitter/receiver Fault
	0	1	0	0	0	0	0	Antenna fault
	0	0	1	0	0	0	0	Control fault
	0	0	0	1	0	0	0	Altitude input fault
	0	0	0	0	1	0	0	Calibration fault [T–R]
	0	0	0	0	0	1	0	Display fault
	0	0	0	0	0	0	1	Cooling fault

Table A-5 Faults

Operating Mode

Matrix Code	Bit 29	Bit 28	Bit 27	Operating Mode
0	0	0	0	Standby
1	0	0	1	Weather [only]
2	0	1	0	Map
3	0	1	1	Contour
4	1	0	0	Test
5	1	0	1	Turbulence [only]
6	1	1	0	Weather & turbulence
7	1	1	1	Reserved [Calibration annunciation]

Table A-6 Operating mode

Note: Weather (only) Reflectivity (Weather) only data should be transmitted on all azimuth addresses.

Turbulence (only) Turbulence only data should be transmitted on all azimuth addresses.

Weather & turbulence Turbulence data combined with reflectivity data is allowed as a means to transmit both weather only and weather plus turbulence words when Weather & turbulence mode is selected.

Tilt Data

Bit	Tilt in degrees
36	–16
35	+8
34	+4
33	+2
32	+1
31	+0.5
30	+0.25

Table A-7 Tilt data

Note: TWO's complement tilt

Gain Data

Bit	42	41	40	39	38	37	Value
	1	1	1	1	1	1	Cal
	0	0	0	0	0	0	Max
	0	0	0	1	0	1	-5
	0	0	1	0	1	1	-11
	1	1	1	1	1	0	-62

Table A-8 Gain data

Range Data

Bit	48	47	46	45	44	43	Range in NM
	0	0	0	0	0	1	5
	0	0	0	0	1	0	10
	0	0	0	1	0	0	20
	0	0	1	0	0	0	40
	0	1	0	0	0	0	80
	1	0	0	0	0	0	160
	1	1	1	1	1	1	315
	0	0	0	0	0	0	320

Table A-9 Range Data

Data Accept

Bit	51	50	Function
	0	0	Do not accept data
	0	1	Accept data 1
	1	0	Accept data 2
	1	1	Accept any data

Table A-10 Data accept

Scan Angle

Bit	Angle (in degrees)	Bit	Angle (in degrees)
63	180	57	2.8125
62	90	56	1.40625
61	45	55	0.703125
60	22.5	54	0.3415625
59	11.25	53	0.17578125
58	5.625	52	0.087890625

Table A-11 Scan angle

Weather Conditions/Reflectivity Data

Matrix code [Pixel Value 3 bits]	Weather Condition	Bin *N* Bit *n2*	Bit *n1*	Bit *n0*	Display Color Example
0	No precipitation [< Z2]	0	0	0	Black
1	Light precipitation [Z2 to Z3]	0	0	1	Green
2	Moderate precipitation [Z3 to Z4]	0	1	0	Yellow
3	Heavy precipitation [Z4 to Z5]	0	1	1	Red
4	Very heavy precipitation [> Z5]	1	0	0	Magenta
5	Reserved[1]	1	0	1	
6	Medium turbulence	1	1	0	
7	Heavy turbulence	1	1	1	

Table A-12 Weather Condition / Reflectivity Data

1. Out of Calibration Indication

March 2010, Rev A-3