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Document # PE3308

This file provides information on P&E's Cable16/32 Background Debug Mode (BDM) cable.

1.0 Introduction

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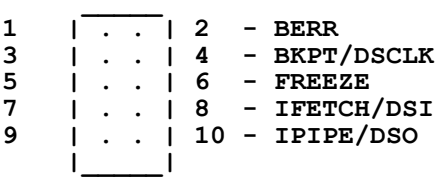
P&E's ICD Interface Cable provides access to the Background Debug Mode (BDM) on Motorola CPU16 and CPU32 microcontrollers. It is the hardware interface between a standard IBM PC parallel port (DB25 Female Connector) and a standard 10 pin "Berg" connector (J1 header) . The pinouts of the connector are specified by Motorola as:



Initially, Motorola specified an 8 pin connector. The cable will work with the 8 pin configuraton by using the bottom 8 pins in the flat ribbon cable provided.

2.0 Startup Sequence

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In order to use the Background Debug Mode of the microcontroller, it must be initialized coming out of reset. This is accomplished by P&E's ICD (In Circuit Debugger) software on the host PC by generating the following reset sequence:

1. **BKPT/DSCLK is pulled low. (to processor)**
2. **Delay ~1ms.**
3. **RESET is pulled low. (to processor)**
4. **Delay ~20ms.**
5. **RESET is released (tri state, should be pulled up on target).**
6. **Wait for FREEZE (out of processor).**
7. **Shifting activity appears on DSCLK, DSI and DSO.**

Note that if FREEZE is not returned(High) from the processor, then it did not enter the Background Debug Mode. If this happens, the ICD debuggers issue the error message "Can not enter background mode".
If you get the message "Can not enter background mode", you should check your+ hardware with a scope, logic analyzer or logic probe. First check for power on. Then check to make sure the processor oscillator is running. Finally, look for the startup sequence given above.

3.0 Speed Considerations

The shift clock (DSCLK) is used to serially shift data in and out of the processor BDM interface. This clock is generated in P&E's software on the PC. The faster the PC (actually the faster the IO cycles) the faster the shift clock. The shift frequency is limited by the target processor clock. Hence, it is possible to shift data too fast for the interface. P&E's software packages provide a command line parameter IO_DELAY_COUNT which can be used to slow down the shift clock.

4.0 Hardware Breakpoint

The BDM interface cable has provision to do an external hardware breakpoint. The breakpoint is caused by shorting together the two pins (labeled J2, pins 1 and 2) which are next to the flat ribbon cable in the connector housing. The pin furthest from the flat ribbon cable (J2-2) is ground. The other pin (J2-1) is a TTL sense input with an internal pull up resistor. In the original cable (Rev. A), this pin is sensed by PC based software which then forces the target processor into the background mode. This causes a software delay between a breakpoint signal and the entering of the background mode. In the Rev. B cable, the breakpoint is generated in hardware and causes the
break to occur at the end of the current target instruction.

5.0 Pullup Options

Revision A of the cable does not have pull up resistors on the BKPT/DSCLK and IFETCH/DSI connections of the BGDM interface. However, revisions B and on do.