IP-HSPIO

Option 95112C

16-bit Buffered High Speed Parallel Input Output IndustryPack®

User's Manual

Manual Revision: iv

Hardware Revision: A

IP-HSPIO

16-bit
Buffered High Speed
Parallel Input Output
IndustryPack®

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Manual Revision iv. Revised 2/16/96.

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Product Description

The IP-HSPIO is part of the IndustryPack® family of modular I/O components and provides FIFO buffered, 16 bit wide I/O capability between its carrier board and an external peripheral device. A block diagram of the IP-HSPIO is shown below in Figure 1. The input FIFO and output FIFO are each 8K words deep. The IP-HSPIO provides a 7 bit control register (output) and a 7 bit status register (input). These registers are available for controlling and monitoring the peripheral device connected to the IP-HSPIO. All peripheral device interface signals use RS-422 Differential Drivers and Receivers. All resources on the IP-HSPIO are mapped into the Industry Pack I/O space.

This IP-HSPIO includes Option 95112C. This option uses bit 4 (PCTRL4) of the Peripheral Control Register (OUTCNTRL – Offset 0xC) to implement a software controlled driver enable for the RS-422 drivers on the XFREQ_IN, XFREQ_OUT, PCTRL0 and PCTRL1 signals. The default state for this bit is '0' after power on or master reset. When Bit 4 is '0', the RS-422 drivers on the XFREQ_IN, XFREQ_OUT, PCTRL0 and PCTRL1 signals are disabled. Bit 4 of the Peripheral Control Register must be set to '1' to enable these RS-422 drivers.

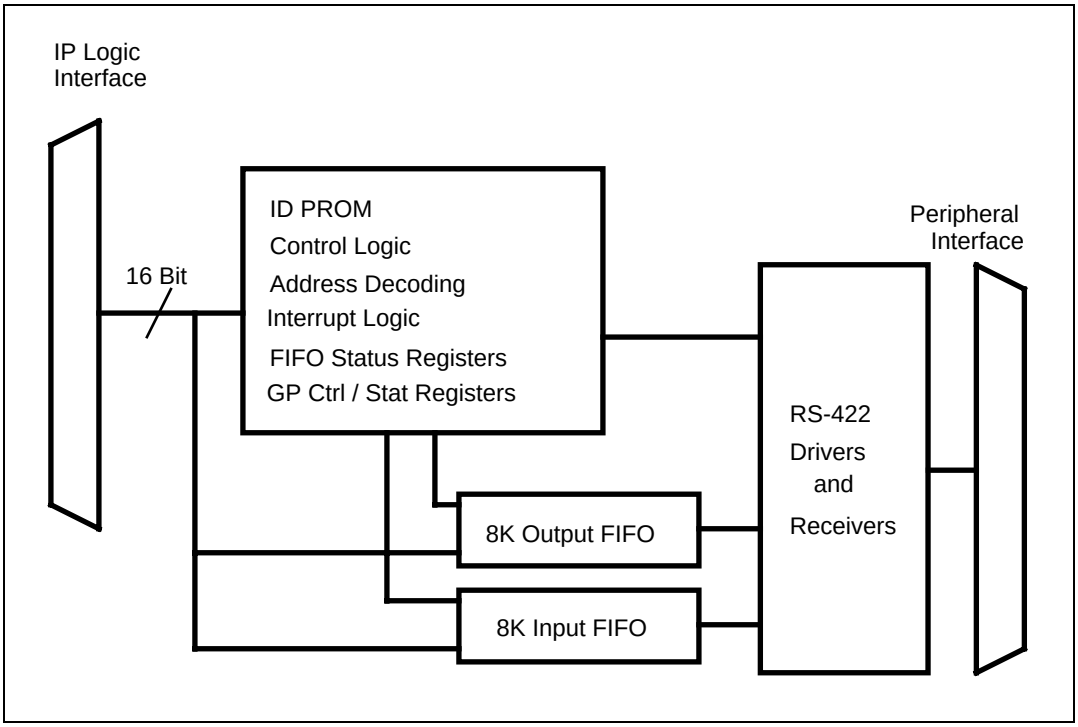

Figure 1 IP-HSPIO Block Diagram

Industry Pack Interface

All the registers of the IP-HSPIO are located in the I/O space of the Industry Pack. All I/O space access cycles are completed with no wait states. As required by the IP Interface Specification, all interface signals are synchronize with the 8 MHz clock from the Industry Pack interface.

Reset Condition

The reset signal from the Industry Pack Interface is used as the hardware reset and the entire IP-HSPIO is initialized when reset is activated. Upon reset, the IP-HSPIO is initialized to the state listed below in Figure 2.

Register	Reset State
Master Reset Bit	1 (active)
FIFO Reset Bit	1 (active)
Interrupt Mask	All 1
FIFO Word Count	All 0
Input FIFO Interrupt Interval Count	0
Interrupt Vector	All '1'
Input FIFO	Empty
Output FIFO	Empty
XFREQ_IN	Asserted
XFREQ_OUT	Deasserted

Figure 2 Reset Initialization State

All of the control logic on the IP-HSPIO is contained in an Xilinx FPGA. After a system reset the FPGA undergoes a programming process that requires 330 milliseconds. During this programming time the IP will not respond to Carrier board accesses which results in a Bus Error. The errors can be eliminated by designing the system software so that the IP is not accessed during the first 330 milliseconds after a system reset.

The following is the recommended initialization sequence:

1. Write a '0' to the Master Reset and FIFO Reset bits to enable the FIFO control logic.
2. Program the desired Input FIFO Interrupt Interval value
3. Program the Interrupt Vector register.
4. Enable the desired interrupt by writing a '0' to the appropriate mask register bit.

Refer to the I/O Register Definition section below for register details.

Interrupt Generation

The IP-HSPIO can be programmed to issue an interrupt under the conditions listed below in Figure 3

Interrupt Condition	Interrupt Signal
Input FIFO is Full	IP Slot A, Interrupt Request 0
Input FIFO Interrupt Interval	IP Slot A, Interrupt Request 1
Output FIFO is Full	IP Slot B, Interrupt Request 0

Figure 3 Interrupting Conditions

When the interrupting condition occurs and the interrupt mask bit for that conditions is programmed to enable the interrupt, the interrupt signal listed in Figure 3 is asserted. The interrupt signal is not automatically reset by the interrupt acknowledge cycle. The interrupt service software is required to toggle the mask bit of that particular interrupt to reset the interrupt condition. The least significant two bits of the interrupt vector returned during the acknowledge cycle are encoded to indicate the interrupting condition. The coding is listed in Figure 4 on the next page.

Interrupt Condition	V1-V0
Input FIFO Full	0 0
Input FIFO Word Count	0 1
Output FIFO Full	1 0

Figure 4 Interrupting Vector Encoding

FIFO Operation

The operation of the FIFOs on the IP-HSPIO is very simple. After the IP-HSPIO has been initialized, the FIFO is enabled by the software writing a '0' to the FIFO Reset bit. The program can then check the FIFO status to determine the FULL and EMPTY state of each FIFO. The FIFO word count register can also be read to determine the exact number of words stored in the FIFO. The maximum size of the Input FIFO and the output FIFO is 8K word each.

Up/Down counters are used to implemented the word count registers for the Input FIFO and the Output FIFO. The Input FIFO word count register is increment by 1 whenever data is written into the input FIFO by the peripheral device. This counter is then decrement by 1 whenever data is read out of the FIFO by the carrier board. Similarly, the output FIFO word count register is increment by 1 whenever data is a written into the output FIFO by the carrier board. The counter is decrement by 1 whenever data is read out of the FIFO by the peripheral device.

Peripheral Interface

The peripheral interface logic is synchronized to a 16 MHz clock derived from the 8 MHz Industry Pack Interface clock. This implementation provides the high performance timing of the Transfer Request handshaking on the peripheral device interface. The DEVFLG input signal (DEV_IN) from the peripheral device is synchronized to the 16 MHz clock. The XFREQ pulse (XFREQ_IN) is generated from the trailing edge of DEV_IN.

When the last word is written into the input FIFO, the Input FIFO status becomes FULL and XFREQ_IN remains in the deasserted state. Similarly, when the last word is read out of the output FIFO, the Output FIFO status becomes EMPTY and XFREQ_OUT remains in the deasserted state.

TIMING

The IP-HSPIO interface is synchronous to the 8 MHz clock from the IP Logic Interface. The timing diagram below shows a typical FIFO read and write Cycle.

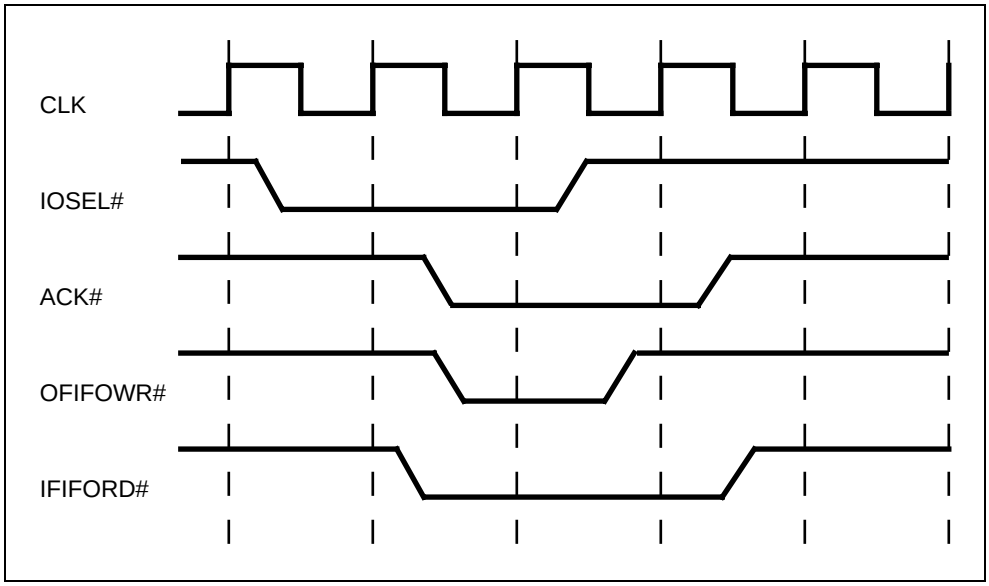

Figure 5 HSPIO FIFO Read/Write Cycle

Parameter	Timing (nanoseconds)
XFREQ_OUT high to OFIFO Data Valid	50 Max.
DEV_OUT high pulse width	125 Min.
DEV_OUT negative edge to XFREQ_OUT negative edge	62.5 Max.
XFREQ_OUT low pulse width	62.5 Min.
Output Data Hold	62.5 Min.
Input Data to DEV_IN setup	40 Min.
Input Data to DEV_IN hold	20 Min.
DEV_IN high pulse width	125 Min.
DEV_IN negative edge to XFREQ_IN negative edge	62.5 Max.
XFREQ_IN low pulse width	62.5 Min.

Figure 6 HSPIO Peripheral Interface Time Requirements

The transfer of data over the Peripheral Interface is controlled by the XFREQ and DEV signals. The signals XFREQ_IN and DEV_IN control the writing of data to the Input FIFO by the peripheral device. The signals XFREQ_OUT and DEV_OUT control the reading of data from the Output FIFO by the peripheral device.

Once there is at least one word of data written to the Output FIFO, the IP-HSPIO drives XFREQ_OUT high to indicate to the peripheral device that data is available. Activating XFREQ_OUT also asserts OFIFORD# to read data from the FIFO to the interface drivers. This data is valid within a maximum of 50 nanoseconds. The peripheral device drives DEV_OUT high to indicate that it is reading the data. The signal DEV_OUT must be high for a minimum of 125 nanoseconds. When the peripheral device drives DEV_OUT low, the IP-HSPIO drives

XFREQ_OUT low within 62.5 nanoseconds for a minimum of 62.5 nanoseconds. The IP-HSPIO continues to drive the output data until XFREQ_OUT is driven low by the IP-HSPIO to provide data hold time to the peripheral device. If this read makes the Output FIFO empty, then the IP-HSPIO continues to drive XFREQ_OUT low until the host processor writes a word to the Output FIFO. The diagram in Figure 7 shows typical Peripheral Interface read cycle.

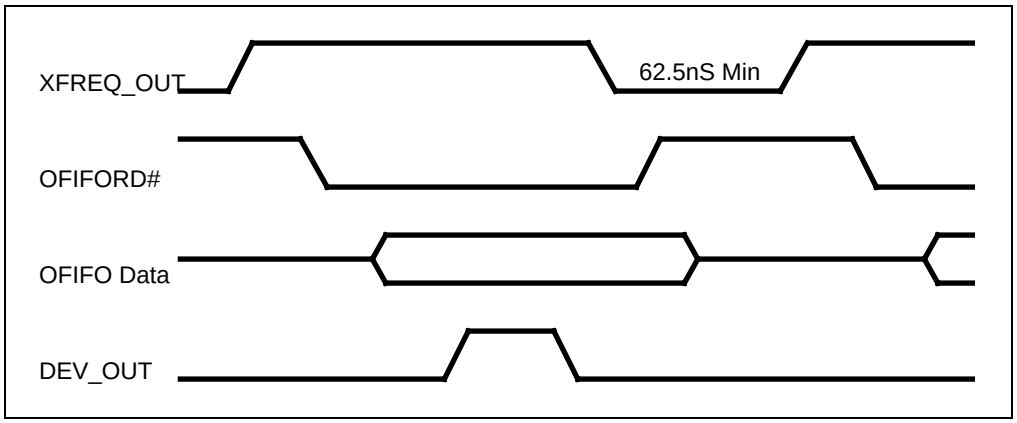

Figure 7 Output FIFO Read Cycle by Peripheral

As long as there is room for one more word in the Input FIFO, the IP-HSPIO drives XFREQ_IN high to indicate to the peripheral device that data can be written into the FIFO. The peripheral device must drive the data line for a minimum of 40 nanoseconds before asserting DEV_IN. The signal DEV_IN must remain active for a minimum of 125 nanoseconds. The signal DEV_IN is used to generate the write strobe to the Input FIFO. The peripheral device must continue to drive the input data for a minimum of 20 nanoseconds after it drives DEV_IN low. When the peripheral device drives DEV_IN low, the IP-HSPIO drives XFREQ_IN low within 62.5 nanoseconds for a minimum of 62.5 nanoseconds. If this write makes the Input FIFO full, then the IP-HSPIO continues to drive XFREQ_IN low until the host processor has read a word from the Input FIFO. The diagram in Figure 8 shows a typical Peripheral Interface write cycle.

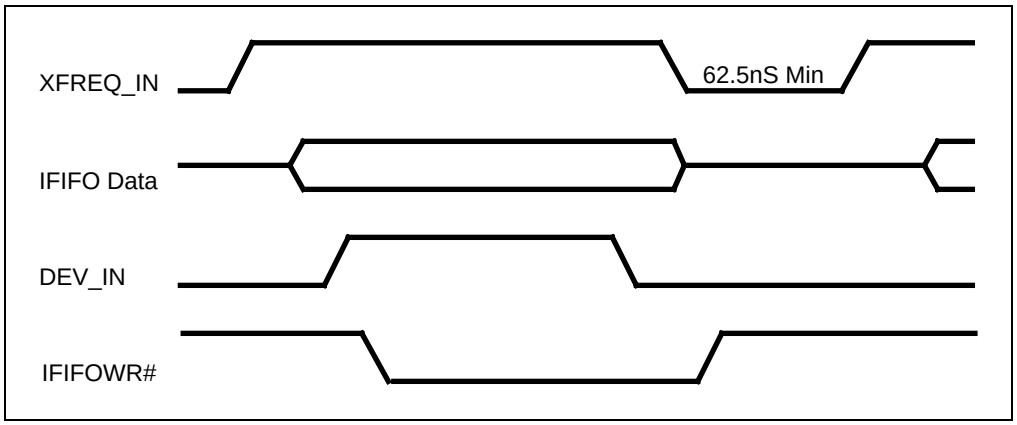

Figure 8 Input FIFO Write Cycle by Peripheral

VMEbus Addressing

All the registers and FIFOs of the IP-HSPIO are all located in the I/O space of the Industry Pack. Only 16 bit word access to these registers is supported. The address offset of each register is shown in Figure 9. The IP-HSPIO is a double size Industry Pack with all the addresses based on the IP carrier board base address for the P1 connector of the double pack. Typically this is either the IP slot A or IP slot C base address.

Word accesses on the VMEbus are on data lines D15..D0.

Byte accesses are on data lines D7..D0. A byte address is the even byte in Intel family host architectures, and the odd byte in Motorola 68K host architectures. Byte accesses are not supported by the IP-HSPIO.

Function	Description	Offset (A0 - A5)	Access	Type
INCNT	Input FIFO Word Count	$00	Word	Read Only
OUTCNT	Output FIFO Word Count	$02	Word	Read Only
IRQ_INTERVAL	Input FIFO IRQ Interval	$04	Word	Read/Write
IFIFO_RD	Input FIFO Read	$08	Word	Read Only
OFIFO_WR	Output FIFO Write	$0A	Word	Write Only
OUTCTRL	Peripheral Control	$0C	Word	Read/Write
INSTATUS	Peripheral Status	$0E	Word	Read Only
VECTOR	Interrupt Vector	$10	Word	Read/Write
Interrupt Mask	Interrupt Mask	$12	Word	Read/Write
MASTER_RESET	System Reset	$14	Word	Read/Write
FIFO_RESET	FIFO Reset	$16	Word	Read/Write
FIFO_STATUS	Read FIFO Status	$18	Word	Read Only

Figure 9 VMEbus Address Map

See the I/O Register Definition section below for register details.

NuBus Addressing

Word addresses on the NuBus are the same as for VMEbus. Word accesses are on data lines D15..D0.

NuBus addressing requires computing the address from the byte addresses given above under VMEbus Addressing. The formula is:

NuBus byte address = (VMEbus byte address * 2) – 1

All byte data is still transferred on data lines D0..D7. Byte accesses are not supported by the IP-HSPIO.

See the I/O Register Definition section below for register details.

Interrupt mapping is a function of the selected carrier board. See your IP carrier board User Manual for more information.

ISA (PC-AT) Bus Addressing

Word addresses on the ISA Bus are the same as for VMEbus. Word accesses are on data lines D15..D0.

Byte accesses are on data lines D7..D0. A byte address is the even byte in Intel family host architectures, and the odd byte in Motorola 68K host architectures. Byte accesses are not supported by the IP-HSPIO.

See the I/O Register Definition section below for register details.

Interrupt mapping is a function of the selected carrier board. See your IP carrier board User Manual for more information.

I/O Register Definition

INCNT — Offset 0x0
(Input FIFO Word Count — Read Only)

This read only I/O register contains the 13 bit word representing the number of words currently present in the Input FIFO in binary format. The maximum FIFO word count is 1FFF hex. The FIFO full condition causes the word count to wrap around and become 0. Therefore, the FIFO full condition should be determine by reading the FIFO status register. Bits 13 through 15 are ignored on a write and are undefined on a read.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Figure 10 Input FIFO Word Count Register

OUTCNT — Offset 0x2
(Output FIFO Word Count — Read Only)

This read only I/O register contains the 13 bit word representing the number of words currently present in the Output FIFO in binary format. The maximum FIFO word count is 1FFF hex. The FIFO full condition causes the word count to wrap around and become 0. Therefore, the FIFO full condition should be determine by reading the FIFO status register. Bits 13 through 15 are ignored on a write and are undefined on a read.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}

Figure 11 Output FIFO Word Count Register

IFIFO_RD — Offset 0x8
(Input FIFO — Read Only)

This is the 16 bit read port for the Input FIFO. Whenever it is read, data is transferred from the input FIFO to the IP Carrier board and the Input FIFO Word Count Register is decremented.

OFIFO_WR — Offset 0xA
(Output FIFO — Write Only)

This is the 16 bit write port for the Output FIFO. Whenever it is written, data is transferred from the IP Carrier board to the Output FIFO and the Output FIFO word count is incremented.

OUTCTRL — Offset 0xC
(Peripheral Control — Read/Write)

This is the read/write register for the 7 control bits which drive the peripheral interface control lines. Bits 7 through 15 are ignored on a write and are undefined on a read. The default state for the bits of this register is '0' after power on or master reset.

Option 95112C, included on this IP-HSPIO uses bit 4 of the Peripheral Control Register to implement a driver enable for the RS-422 drivers on the XFREQ_IN, XFREQ_OUT, PCTRL0 and PCTRL1 signals. Bit 4 of the Peripheral Control Register must be set to '1' to enable these RS-422 drivers.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	6	5	4	3	2	1	0

Figure 12 Peripheral Control Register

INSTATUS — Offset 0xE
(Peripheral Status — Read Only)

This is the read only port of the 7 status bits which monitor the peripheral interface status lines. Bits 7 through 15 are ignored on a write and are undefined on a read.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	6	5	4	3	2	1	0

Figure 13 Peripheral Status Register

IRQ_INTERVAL — Offset 0x4
(Input FIFO Interrupt Word Count — Read/Write)

This is the read/write register for the word count value, in binary format, that determines the number of words that are written into the Input FIFO by the peripheral device before an interrupt is generated to the IP Carrier board. For a value of N in this register, an interrupt will be generated each time the Input FIFO Word Count is equal to N. A value of '0' in this register disables Input FIFO Interval interrupts**.** Bits 13 through 15 are ignored on a write and are undefined on a read.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0

Figure 14 Interrupt Word Count Register

Interrupt VECTOR — Offset 0x10
(Interrupt Vector — Read/Write)

This is the read/write register that contains the six most significant bits of the interrupt vector. The least significant two bits are encoded to indicate the interrupting condition. This register is set to all '1's by the system or hardware reset. Bits 8 through 15 are ignored on a write and are undefined on a read.

Bits 0 and 1 are set to '00' on an Input FIFO Full Interrupt.
Bits 0 and 1 are set to '01' on an Input FIFO Word Count Interrupt
Bits 0 and 1 are set to '10' on an Output FIFO Full interrupt.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	V7	V6	V5	V4	V3	V2	X	X

Figure 15 Interrupt Vector Register

Interrupt MASK — Offset 0x12
(Interrupt Mask — Read/Write)

This is the read/write register that contains the interrupt mask. All mask bits are set to '1' by the system or hardware reset. Bits 3 through 15 are ignored on a write and are undefined on a read. Writing a '0' in bits 0 through 2 unmasks the corresponding interrupt.

M0 is used to mask the Input FIFO Full Interrupt.
M1 is used to mask the Input FIFO Word Count Interrupt
M2 is used to mask the Output FIFO Full interrupt.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	X	X	X	X	M2	M1	M0

Figure 16 Interrupt Mask Register

MASTER_RESET — Offset 0x14
(Master Reset — Read/Write)

This read/write register accesses the Master Reset bit. Writing a '1' to the least significant bit of this register generates a Master Reset to the IP-HSPIO. During a hardware reset, the R bit is set to '1'. The software is always required to write a '0' back into this bit to resume operation after either reset condition. Bits 1 through 15 are ignored on a write and are undefined on a read.

A Master Reset has the following effect:

Reset the Input FIFO and the Output FIFO.
Reset the Input FIFO and the Output FIFO word counters.
Set all bits of the Interrupt Mask.
Reset the Interrupt Vector to all '1's.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	R

Figure 17 Master Reset Register

FIFO_RESET — Offset 0x16
(FIFO Reset — Read/Write)

This read/write register accesses the FIFO Reset bit. Writing a '1' to the least significant bit of this register generates a FIFO Reset to both the Input FIFO and the Output FIFO. During a hardware reset, the R bit is set to '1'. The software is always required to write a '0' back into this bit to resume operation after either reset condition. Bits 1 through 15 are ignored on a write and are undefined on a read.

A FIFO Reset has the following effect:

Reset the Input FIFO and the Output FIFO.
Reset the Input FIFO and the Output FIFO word counters.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	R

Figure 18 FIFO Reset Register

FIFO Status — Offset 0x18
(FIFO Status — Read Only)

This is a read only register reflecting the actual status of the Input FIFO and the Output FIFO. Bits 4 through 15 are ignored on a write and are undefined on a read.

3	2	1	0
OUT EMPTY	IN EMPTY	OUT FULL	IN FULL

Figure 19 FIFO Status Register

ID PROM

Every IP contains an ID PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires a particular revision IP, it may check for it directly.

Standard data in the ID PROM on the IP-HSPIO is shown in Figure 20 below. For more information on IP ID PROMs refer to the IndustryPack Logic Interface Specification, available from GreenSpring Computers. The ID PROM is implemented on the IP-HSPIO as part of the XILINX field programmable gate array.

The location of the ID PROM in the host's address space is dependent on the carrier used. Normally for VMEbus carriers the ID PROM space is directly above the IP's I/O space, or at IP-base + $80. Macintosh drivers use the ID PROM automatically. RM1260 address may be derived from Figure below by multiplying the addresses given by two, then subtracting one. RM1270 addresses may be derived by multiplying the addresses given by two, then adding one.

3F 19	(available for user)	
17	CRC for bytes used	(EA)
15	No of bytes used	(0C)
13	Driver ID, high byte	(00)
11	Driver ID, low byte	(01)
0F	Reserved	(00)
0D	Revision	(A1)
0B	Model No IP-HSPIO	(4C)
09	Manufacturer ID GreenSpring	(F0)
07	ASCII "C"	(43)
05	ASCII "A"	(41)
03	ASCII "P"	(50)
01	ASCII "I"	(49)

Figure 20 ID PROM Data (hex)

I/O Pin Wiring

This section gives the Peripheral Device Interface pin assignments for IP-HSPIO. This interface uses connectors P2 and P4. The IP Logic Interface uses connectors P1 and P3 and is listed in the next section.

The pin numbers given in Figures 21 and 22 below correspond to numbers on the 50-pin IndustryPack I/O connector, to the wires on a 50-pin flat cable plugged into a standard IP carrier board, and to the screw terminal numbers on the IP-Terminal block.

Connector P2

Pin Number	Signal Name	Function	Level
1	ID0	Input Data 0	RS-422 +
2	ID0#	Input Data 0 #	RS-422 -
3	ID1	Input Data 1	RS-422+
4	ID1#	Input Data 1 #	RS-422 -
5	ID2	Input Data 2	RS-422 +
6	ID2#	Input Data 2#	RS-422 -
7	ID3	Input Data 3	RS-422 +
8	ID3#	Input Data 3#	RS-422 -
9	ID4	Input Data 4	RS-422 +
10	ID4#	Input Data 4#	RS-422 -
11	ID5	Input Data 5	RS-422+
12	ID5#	Input Data 5#	RS-422 -
13	ID6	Input Data 6	RS-422+
14	ID6#	Input Data 6#	RS-422-
15	ID7	Input Data 7	RS-422+
16	ID7#	Input Data 7#	RS-422-
17	ID8	Input Data 8	RS-422+
18	ID8#	Input Data 8#	RS-422-
19	ID9	Input Data 9	RS-422+
20	ID9#	Input Data 9#	RS-422-
21	ID10	Input Data 10	RS-422
22	ID10#	Input Data 10#	RS-422-
23	ID11	Input Data 11	RS-422+
24	ID11#	Input Data 11#	RS-422-
25	ID12	Input Data 12	RS-422+
26	ID12#	Input Data 12#	RS-422-
27	ID13	Input Data 13	RS-422+
28	ID13#	Input Data 13#	RS-422-
29	ID14	Input Data 14	RS-422+
30	ID14#	Input Data 14#	RS-422+
31	ID15	Input Data 15	RS-422+
32	ID15#	Input Data 15#	RS-422-
33	DEV_IN	Device Flag In	RS-422+
34	DEV_IN#	Device Flag In#	RS-422-
35	XFREQ_IN	Transfer Req In	RS-422+
36	XFREQ_IN#	Transfer Req In#	RS-422-
37	PCTRL5	Control 5	RS-422+
38	PCTRL5#	Control 5#	RS-422-
39	PCTRL6	Control 6	RS-422+
40	PCTRL6#	Control 6#	RS-422-
41	ISTAT0	Status 0	RS-422+
42	ISTAT0#	Status 0#	RS-422-
43	ISTAT1	Status 1	RS-422+
44	ISTAT1#	Status 1#	RS-422-
45	ISTAT2	Status 2	RS-422+
46	ISTAT2#	Status 2#	RS-422-
47	ISTAT3	Status 3	RS-422+
48	ISTAT3#	Status 3#	RS-422-
49	ISTAT4	Status 4	RS-422+
50	ISTAT4#	Status 4#	RS-422-

Figure 21 I/O Pin Assignment First Half

Connector P4

Pin Number	Signal Name	Function	Level
1	ISTAT5	Status 5	RS-422 +
2	ISTAT5#	Status 5#	RS-422 -
3	ISTAT6	Status 6	RS-422+
4	ISTAT6#	Status 6#	RS-422 -
5	PCTRL0	Control 0	RS-422 +
6	PCTRL0#	Control 0#	RS-422 -
7	PCTRL1	Control 1	RS-422 +
8	PCTRL1#	Control 1#	RS-422 -
9	PCTRL2	Control 2	RS-422 +
10	PCTRL2#	Control 2#	RS-422 -
11	PCTRL3	Control 3	RS-422+
12	PCTRL3#	Control 3#	RS-422 -
13	PCTRL4	Control 4	RS-422+
14	PCTRL4#	Control 4#	RS-422-
15	DEV_OUT	Device Flag Out	RS-422+
16	DEV_OUT#	Device Flag Out#	RS-422-
17	XFREQ_OUT	Transfer Req Out	RS-422+
18	XFREQ_OUT#	Transfer Req Out#	RS-422-
19	OD0	Output Data 0	RS-422+
20	OD0#	Output Data 0#	RS-422-
21	OD1	Output Data 1	RS-422
22	OD1#	Output Data 1#	RS-422-
23	OD2	Output Data 2	RS-422+
24	OD2#	Output Data 2#	RS-422-
25	OD3	Output Data 3	RS-422+
26	OD3#	Output Data 3#	RS-422-
27	OD4	Output Data 4	RS-422+
28	OD4#	Output Data 4#	RS-422-
29	OD5	Output Data 5	RS-422+
30	OD5#	Output Data 5#	RS-422-
31	OD6	Output Data 6	RS-422+
32	OD6#	Output Data 6#	RS-422-
33	OD7	Output Data 7	RS-422+
34	OD7#	Output Data 7#	RS-422-
35	OD8	Output Data 8	RS-422+
36	OD8#	Output Data 8#	RS-422-
37	OD9	Output Data 9	RS-422+
38	OD9#	Output Data 9#	RS-422-
39	OD10	Output Data 10	RS-422+
40	OD10#	Output Data 10#	RS-422-
41	OD11	Output Data 11	RS-422+
42	OD11#	Output Data 11#	RS-422-
43	OD12	Output Data 12	RS-422+
44	OD12#	Output Data 12#	RS-422-
45	OD13	Output Data 13	RS-422+
46	OD13#	Output Data 13#	RS-422-
47	OD14	Output Data 14	RS-422+
48	OD14#	Output Data 14#	RS-422-
49	OD15	Output Data 15	RS-422+
50	OD15#	Output Data 15#	RS-422-

Figure 22 I/O Pin Assignment Second Half

IndustryPack Logic Interface Pin Assignment

Figures 23 and 24 below give the pin assignments for the IndustryPack Logic Interface on the IP-HSPIO. Pins marked n/c below are defined by the specification, but not used on IP-HSPIO. See also your User Manual for your IP Carrier board for more information.

Connector P1

GND	GND	1	26
CLK	+5V	2	27
Reset*	R/W*	3	28
D0	IDSel*	4	29
D1	n/c	5	30
D2	n/c	6	31
D3	n/c	7	32
D4	INTSel*	8	33
D5	n/c	9	34
D6	IOSel*	10	35
D7	n/c	11	36
D8	A1	12	37
D9	n/c	13	38
D10	A2	14	39
D11	n/c	15	40
D12	A3	16	41
D13	IntReq0*	17	42
D14	A4	18	43
D15	IntReq1*	19	44
n/c	A5	20	45
n/c	n/c	21	46
n/c	n/c	22	47
n/c	Ack*	23	48
+5V	n/c	24	49
GND	GND	25	50

Note 1: The no-connect (n/c) signals above are defined by the IndustryPack Logic Interface Specification, but not used by this IP. See the Specification for more information.

Note 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IndustryPack.

Figure 23 Logic Interface Pin Assignment First Half

Connector P3

GND	GND	1	26
n/c	+5V	2	27
n/c	n/c	3	28
D0	n/c	4	29
D1	n/c	5	30
D2	n/c	6	31
D3	n/c	7	32
D4	INTSel*	8	33
D5	n/c	9	34
D6	n/c	10	35
D7	n/c	11	36
D8	A1	12	37
D9	n/c	13	38
D10	n/c	14	39
D11	n/c	15	40
D12	n/c	16	41
D13	IntReq0*	17	42
D14	n/c	18	43
D15	n/c	19	44
n/c	n/c	20	45
n/c	n/c	21	46
n/c	n/c	22	47
n/c	Ack*	23	48
+5V	n/c	24	49
GND	GND	25	50

Note 1: The no-connect (n/c) signals above are defined by the IndustryPack Logic Interface Specification, but not used by this IP. See the Specification for more information.

Note 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IndustryPack.

Figure 24 Logic Interface Pin Assignment Second Half

Construction and Reliability

IndustryPacks were conceived and engineered for rugged industrial environments. The IP-HSPIO is constructed out of 0.062 inch thick FR4 V0 material. The six copper layers consist of two signal layers on the top and bottom, and four internal layers. Two internal layers are dedicated to power and ground planes. Two additional layers are used for signal wiring.

Through hole and surface mounting of components is used. IC sockets use gold plated, screw-machine pins. High insertion and removal forces are required, which assists in keeping components in place. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the four corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IndustryPack connectors are keyed, shrouded and gold plated on both contacts and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured to the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IndustryPack provides a low temperature coefficient of 0.89 W/°C for uniform heat. This is based on the temperature coefficient of the base FR4 material of 0.31 W/m-°C, and taking into account the thickness and area of the IP. This coefficient means that if 0.89 Watts is applied uniformly on the component side, that the temperature difference between the component and the solder side is one degree Celsius.

Warranty and Repair

GreenSpring Computer warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, GreenSpring Computer's sole responsibility shall be to repair, or at GreenSpring Computer's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to GreenSpring Computers. All replaced products become the sole property of GreenSpring Computers.

GreenSpring Computer's warranty of and liability for defective products is limited to that set forth herein. GreenSpring Computers disclaims and excludes all other product warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchandisability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

GreenSpring's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of GreenSpring Computers, Inc.

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. GreenSpring Computers will not be responsible for damages due to improper packaging of returned items. For service on GreenSpring Products not purchased directly from GreenSpring Computers contact your reseller. Products returned to GreenSpring Computers for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
GreenSpring Computers
1204 O'Brien Drive
Menlo Park, CA 94025
(415) 327-1200
(415) 327-3808 fax

Specifications IP-HSPIO

This section gives the technical specification for the standard grade IP-HSPIO.

Size	Double-high IndustryPack
Dimensions	3.6 x 3.9 x 0.340 inches max
Reset Recovery Time:	330 milliseconds
Number of Lines	16 bit parallel data input lines, 16 bit parallel data output lines, 4 data transfer control line, 7 bit parallel control output 7 bit parallel status input
Data Transfer Modes	16 bit FIFO buffered input, 16 bit FIFO buffered output
Electrical Interface	All I/O use RS-422 differential drivers and receivers
Data Buffers	8K by 16 bit input FIFO, 8K by 16 bit Output FIFO
I/O Interconnect	Two 50-pin cables, 100 lines
Interrupts	Three uniquely vectored interrupts
Wait States	Zero on all IP Interface cycles
Power Requirements:	+5 VDC, 630 mA typical
Environmental	Operating temperature: 0 to 70°C Humidity: 5 - 95% non-condensing Storage temperature: –10 to +85°C

Order Information

IP-HSPIO	16 bit parallel FIFO buffered data input lines, 16 bit parallel FIFO buffered data output lines, 4 data transfer control line, 7 bit parallel control output 7 bit parallel status input
Eng Kit—IP-HSPIO	Engineering Kit includes: 6 foot data cable, 50-pin screw terminal block, Technical Documentation, Data sheet reprints

***Note**: The Engineering Kit is strongly recommended for first time IP-HSPIO buys.*

Schematics

Schematics are provided here for customer *reference only*. This information was current at the time the printed circuit board was last revised. This revision letter is shown on the front of this manual as "Corresponding Hardware Revision." This information is not necessarily current or complete manufacturing data, nor is it part of the product specification.

Current manufacturing information, including schematics, programmed device listings, bills-of-material, and assembly diagrams are available from GreenSpring Computers as part of the Engineering Kit option or from your international distributor.