# Model cPCI-75SD1 (3U)

Eight (8) Synchro/Resolver-to-Digital Channels

## EIGHT (8) SYNCHRO/RESOLVER-to-DIGITAL TRACKING CONVERTERS

**Single Speed or Two-Speed Programmable Encoder, Velocity, & Commutation Outputs**
**Continuous Self-Test; On-Board Programmable Reference**
**Both Commercial & Extended Temperature Ranges**

**FEATURES:**

- 16-bit resolution for single-speed (up to 24 bits for two-speed configuration)
- Accuracy: 1 arc minute for single-speed. 1 arc minute divided by gear ratio for two-speed
- Continuous background testing with Reference and Signal loss detection
- Power-On Self-Test (POST)
- **Self-calibrating. Does not require removal for calibration**
- **Automatically supports either 5V or 3.3V PCI bus**
- Synchro/Resolver programmable
- Either two-speed or single speed configurable
- Watchdog timer and soft reset
- Accurate Digital Velocity outputs
- Angle change alert
- 47 Hz to 10 Khz options available
- Transformer isolated
- Synthetic reference compensates for ±60° phase shift
- Latch feature
- No adjustments or trimming required
- Part number, S/N, Date code, & Rev. in non-volatile memory
- Conducted cooled versions available

**DESCRIPTION:**

This single slot 3U card offers **eight (8) transformer isolated Synchro/Resolver-to-Digital tracking converters that are programmable for either single speed or two-speed mode, extensive diagnostics, velocity outputs, angle change alert, and optional programmable reference supply. Each channel also produces differential incremental encoder (A&B) outputs (with programmable resolution) and a zero degree marker pulse. Commutation outputs are available for 4, 6, or 8 pole brushless DC motors that eliminate the need for Hall Effect sensors on the motor thus eliminating processor time and reducing bus traffic. In the two-speed configuration any ratio between 2 and 255 can be selected.** Ambiguity circuits maintain monotonic outputs by compensating for variations of the zero positions between the Coarse and Fine synchros. The card also checks the angle difference between the Coarse and Fine synchros and will set a flag when the max. allowable angle difference of 90°/n is exceeded. The S/D channels, even when large accelerations are encountered, never lose tracking, because they incorporate the unique capability to automatically shift to higher bandwidths. The shifting is smooth and continuous with no glitches. Tracking rates are only limited to bandwidth restrictions, up to 150 RPS, at 16-bit resolution. The “Latch” feature permits user to read all channels at the same time. Reading will unlatch that channel. The **angle alert** monitors each channel for the programmed angle difference and sets an interrupt as soon as that threshold is reached. Thus, no polling of the angle registers is required until an angle has reached the specified difference. Programmable Synchro/Resolver capability can be specified (see P/N). The use of Type II servo loop processing techniques enables tracking, at full accuracy, up to the specified rate. A step input will not cause any hang-up condition. Intermediate transparent latches, on all angle and velocity outputs, assure that valid data is always available without interrupts or waiting time. Our synthetic reference compensates for ±60° phase shifts, thus eliminating the need for individual compensation networks. Each channel can be specified for a different voltage or frequency. A watchdog timer is provided to monitor the processor. Part #, S/N, Date code, & Rev. are in non-volatile memory.

**Major diagnostics are incorporated** that offer substantial improvements to system reliability because user is immediately alerted to malfunctions. This approach also reduces bus traffic because the Status registers do not require constant polling. Power-On, (POST) diagnostic can immediately initiate (D3) test. Three different tests (one on-line and two off-line) can be selected:

**The (D2) test** initiates automatic background BIT testing. Each channel is checked every 5° to a testing accuracy of 0.05° and each Signal and Reference are always monitored. For two-speed applications, a flag will be set when the max. allowable angle difference of 90°/n is exceeded. Any failure triggers an Interrupt (if enabled) and the results are available in status registers. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus.

**The (D3) or POST test,** if enabled, starts an initiated bit test that disconnects all channels from the outside world and connects them across an internal stimulus that generates and tests 72 different angles to a test accuracy of 0.05° and results can be read from registers. External reference is not required. Any failure triggers an Interrupt (if enabled). The testing is totally transparent to the user, requires no external programming, and can be enabled or disabled via the bus. Power-On (POST) test can be enabled or disabled via the bus.

**The (D0) test** is used to check the card and the interface. All channels are disconnected from the outside world allowing user to write any number of input angles to the card and then read the data from the interface. External reference is not required.

## SPECIFICATIONS:

| | |
|---|---|
| Resolution: | 16 bits |
| Accuracy: | ±1 arc minute for single speed inputs<br>1 arc minute divided by the gear ratio for two-speed inputs |
| Tracking Rate: | 18.5 rps for 60 Hz versions; 150 rps max. for 360Hz or greater versions. Referred to Fine for two-speed configuration |
| Bandwidth: | Normal is 10 Hz for 60 Hz version; 40 Hz for 400 Hz versions, and 100 Hz for greater than 1 kHz versions. Can be readily customized |
| Input format: | Synchro or Resolver, (See part number) |
| Gear ratio: | Each channel pair is programmable from 2 to 255 |
| Input voltage: | Resolver : 2-28 $V_{L-L}$, Autoranging, or 90 $V_{L-L}$.<br>Synchro : 11.8 $V_{L-L}$ , or 90 $V_{L-L}$<br>Resolver and Synchro inputs are transformer isolated<br>Other input options available; consult factory. |
| Input Impedance: | 26 $V_{L-L}$ or less: 40 kΩ min. 90 $V_{L-L}$: 100 kΩ min. |
| Reference/Input: | 2-26 Vrms, Autoranging or 115 Vrms fixed. Transformer Isolated, (See part number) |
| Reference Zin | 100 kΩ min. |
| Frequency: | 47 Hz to 10 kHz (See part number) |
| Encoder outputs: | Either 12,13,14,15, or 16 bit resolution, (field programmable) and Index marker. 12 bit resolution is equivalent to 1,024 cycles (4,096 transitions) etc. Differential outputs. The encoder resolution is fixed and does not change with speed. (Optional, see P/N). |
| Commutation outputs: | Equivalent to the A, B, C outputs from Hall Effect Sensors for 4, 6 or 8 pole motors |
| Angle change alert: | Each channel can be set to a different angle differential. When that differential is exceeded, an interrupt (if enabled) is triggered. Default: “Ch. disabled”. Msb=180°; Min. differential is 0.05°. |
| Phase shift: | The synthetic reference circuit automatically compensates for phase shifts between the transducer excitation and output up to ±60°. |
| Velocity, Digital: | 16 bit resolution; Linearity: 0.1%. |
| Wrap around Self Test: | The three different powerful test methods are detailed in the Description section and further described in the Programming Instructions. |
| Signal Logic Level: | Automatically supports either 5V or 3.3V PCI bus. |
| Power: | + 5 VDC: 0.80 A + 1A ( 3A peak ) @ 5VA Load on optional Reference Supply<br>±12 VDC: 0.08 A |
| Temperature, operating: | "C" 0°C to +70°C; "E" -40°C to +85°C (See part number) |
| Storage temperature: | -55°C to +105°C. |
| Size: | 3U (3.94") height, 4HP (0.8") width. 100 mm x 20.3 mm x 160 mm deep |
| Weight: | 18 oz. |

**REFERENCE SUPPLY:** Optional (see part number)

Voltage: 2.0 - 28Vrms programmable, resolution 0.1Vrms, or 115Vrms fixed. Accuracy ±2%

Frequency: 360 Hz to 10 kHz +/- 1 % with 1 Hz resolution

Regulation: 10 % max. no load to full load

Output Power: 5 VA max. at 40°min. load inductive
190mA RMS @ 2-26VAC, 45mA RMS @ 115VAC
Note: Power is reduced linearly as the Reference Voltage

## PROGRAMMING INSTRUCTIONS:

This card can be programmed for either single-speed or two-speed applications. Thus, for ease of usage, all channels are referred to as 1 to 8. For two-speed applications we generally refer to Coarse and Fine inputs. Therefore, channel becomes 1 Coarse, channel 2 becomes 1 Fine, channel 3 becomes 2 Coarse, channel 4 becomes 2 Fine etc. Should further clarification be required, please contact Customer Service.

## MEMORY MAP

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 00 | Ch.1 Data Hi | read | 4C | Ratio Ch. 7/8 | read/write | 98 | Interrupt Enable | read/write | E4 | Velocity scale Ch.7 | read/write |
| 04 | Ch.2 Data Hi | read | 50 | Angle Δ Ch.1 | read/write | 9C | Interrupt Status | read | E8 | Velocity scale Ch.8 | read/write |
| 08 | Ch.3 Data Hi | read | 54 | Angle Δ Ch.2 | read/write | A0 | Synchro/Resolver | read/write | F0 | Ch.2 Data Lo | read |
| 0C | Ch.4 Data Hi | read | 58 | Angle Δ Ch.3 | read/write | A4 | (POST) Enable | read/write | F4 | Ch.4 Data Lo | read |
| 10 | Ch.5 Data Hi | read | 5C | Angle Δ Ch.4 | read/write | A8 | Two speed lock loss | read | F8 | Ch.6 Data Lo | read |
| 14 | Ch.6 Data Hi | read | 60 | Angle Δ Ch.5 | read/write | AC | (A & B) res. Ch.1 | read/write | FC | Ch.8 Data Lo | read |
| 18 | Ch.7 Data Hi | read | 64 | Angle Δ Ch.6 | read/write | B0 | (A & B) res. Ch.2 | read/write | 100 | Freq. (Ref. Supply) | read/write |
| 1C | Ch.8 Data Hi | read | 68 | Angle Δ Ch.7 | read/write | B4 | (A & B) res. Ch.3 | read/write | 104 | Eo (Ref. Supply) | read/write |
| 20 | Velocity 1 | read | 6C | Angle Δ Ch.8 | read/write | B8 | (A & B) res. Ch.4 | read/write | 108 | Watchdog timer | read/write |
| 24 | Velocity 2 | read | 70 | Angle Δ initiate | read/write | BC | (A & B) res. Ch.5 | read/write | 10C | Soft reset | write |
| 28 | Velocity 3 | read | 74 | Active channels | read/write | C0 | (A & B) res. Ch.6 | read/write | 110 | Part Number | read |
| 2C | Velocity 4 | read | 78 | Test (D2) verify | read/write | C4 | (A & B) res. Ch.7 | read/write | 114 | Serial Number | read |
| 30 | Velocity 5 | read | 7C | Test Enable | read/write | C8 | (A & B) res. Ch.8 | read/write | 118 | Date code | read |
| 34 | Velocity 6 | read | 80 | Status, Signal | read | CC | Velocity scale Ch.1 | read/write | 11C | PC Board rev. | read |
| 38 | Velocity 7 | read | 84 | Status, Reference | read | D0 | Velocity scale Ch.2 | read/write | 120 | Software rev. | read |
| 3C | Velocity 8 | read | 88 | Status, Test | read | D4 | Velocity scale Ch.3 | read/write | 124 | Interface FPGA rev. | read |
| 40 | Ratio Ch. 1/2 | read/write | 8C | Latch | write | D8 | Velocity scale Ch.4 | read/write | 128 | FPGA rev. | read |
| 44 | Ratio Ch. 3/4 | read/write | 90 | Test angle | write | DC | Velocity scale Ch.5 | read/write | 140 | (reserved) | |
| 48 | Ratio Ch. 5/6 | read/write | 94 | Angle Δ Change Alert | read | E0 | Velocity scale Ch.6 | read/write | | | |

## Register Bit Map

| | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Data (angle)° Hi [1] | 180 | 90 | 45 | 22.5 | 11.25 | 5.625 | 2.813 | 1.406 | .703 | .352 | .176 | .088 | .044 | .022 | .011 | .0055 |
| Data (angle)° Lo [1] | .00274 | .00137 | .00068 | .00034 | .00017 | .00008 | .00004 | .00002 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Active channels | X | X | X | X | X | X | X | X | SD8 | SD7 | SD6 | SD5 | SD4 | SD3 | SD2 | SD1 |
| Latch outputs | X | X | X | X | X | X | X | X | X | X | X | X | X | X | 1 | X |
| Two-speed lock loss | X | X | X | X | X | X | X | X | Ch7/8 | X | Ch5/6 | X | Ch3/4 | X | Ch1/2 | X |
| Synchro/Resolver | X | X | X | X | X | X | X | X | SD8 | SD7 | SD6 | SD5 | SD4 | SD3 | SD2 | SD1 |
| Test Enable | X | X | X | X | X | X | X | X | X | X | X | X | D3 | D2 | X | D0 |
| Status, Test | X | X | X | X | X | X | X | X | SD8 | SD7 | SD6 | SD5 | SD4 | SD3 | SD2 | SD1 |
| Status, Signal | X | X | X | X | X | X | X | X | SD8 | SD7 | SD6 | SD5 | SD4 | SD3 | SD2 | SD1 |
| Status, Reference | X | X | X | X | X | X | X | X | SD8 | SD7 | SD6 | SD5 | SD4 | SD3 | SD2 | SD1 |
| Angle Δ Alert | X | X | X | X | X | X | X | X | SD8 | SD7 | SD6 | SD5 | SD4 | SD3 | SD2 | SD1 |
| Interrupt Enable/Status | X | X | X | X | X | X | X | X | X | X | X | X | #4 | #3 | #2 | #1 |
| (A&B) resolution/poles | D15 | X | X | X | X | X | X | X | X | X | X | X | X | **D2** | **D1** | **D0** |

↑ "0"= Encoder
"1"= Commutation

Note 1 –Values are rounded off.

**TABLE 3**

| | | | | |
|---|---|---|---|---|
| **4 pole** | **16 bit** | 0 | 0 | 0 |
| **6 pole** | **15 bit** | 0 | 0 | 1 |
| **8 pole** | **14 bit** | 0 | 1 | 0 |
| | **13 bit** | 0 | 1 | 1 |
| | **12 bit** | 1 | 0 | 0 |

**Commutation outputs** ↑

**Encoder outputs** ↑

## INTERRUPT ENABLE & STATUS REGISTERS

**#1 = S/D Signal Loss** **#2 = S/D Reference Loss** **#3 = S/D Angle Change Alert** (Global **–** Read *Angle Change Al*ert *Register* for particular channel ) **#4 = S/D Test Accuracy Error**

## S/D FUNCTIONS:

**Power-On Self-Test (POST):** The unit will initiate the D3 Test upon power-on, if POST is enabled and saved. Enable by writing "1" to *POST Register*. Disable by writing "0" to *POST Register* and then save setup.

**Active Channels:** Set the bit corresponding to each channel to be monitored during BIT testing in the *Active Channel Register* ("1"=active; "0"=not used). **Omitting this step will produce errors on unused channels causing false alarms**; hence unused channels will set faults, i.e. status bits, interrupts, etc.

**Optional Synchro/Resolver Mode:** Where applicable, write a "1" or "0" (Synchro = 1; Resolver = 0) to each bit, representing a channel, of *Synchro/Resolver Register*.

**Ratio:** Enter the desired ratio, as an integer number, in the *Ratio Register* corresponding to the pair of channels to be used for a two-speed channel. Example: Single speed = 1; 36:1 = integer 36.

**Read:** For single speed applications (Ratio=1), read individual channels 1,2,3,4,etc. For two-speed applications, read only channels (2,4,6,8,etc.) for the combined output of 16 bits. For resolution up to 24 bits, read Data Lo word, then Data Hi word. Data Lo word, when read, latches high word.

**Two-Speed Lock-Loss:** The card monitors misalignment between Coarse and Fine angles during two-speed operation. A two-speed lock loss condition exists if the maximum allowable misalignment between the Coarse and Fine angles of 90°/ratio is exceeded. The corresponding bit for that channel pair in the *Two-Speed Lock-Loss Register* will be set to "0".

**Two-Speed Connectivity:** In two-speed S/D applications, the single speed information (coarse) from the synchro should be connected to the odd channel of the pair. The N-speed information (multi-speed, fine) from the synchro should be connected to the even channel of the pair. The pairs are defined as: CH1 & 2, CH3 & 4, CH5 & 6, or CH7 & 8.

**Latch:** Writing the integer 2 to the *Latch Register* will cause the angle data of all channels to be latched. Reading a particular channel will disengage the latch for that channel. Writing 0 to this register will disengage latch on all channels.

**Velocity Output:** Read Velocity Registers of each channel as a 2's complement word, with 7FFFh being maximum CW rotation, and 8000h being maximum CCW rotation.

When max. velocity is set to 152.5878 RPS, an actual speed of 10 RPS CW would be read as 0863h.
When max. velocity is set to 152.5878 RPS, an actual speed of 10 RPS CCW would be read as F79Ch.
When max. velocity is set to 50.8626 RPS, an actual speed of 10 RPS CW would be read as 192Ah.
When max. velocity is set to 50.8626 RPS, an actual speed of 10 RPS CCW would be read as E6D5h.

To convert a velocity word to RPS: **Velocity in RPS = Maximum x Output / Full Scale**

If Velocity Output were E6D5h, and maximum velocity were 50.8626 RPS, then
Velocity in RPS = 50.8626 x E6D5h / 32,768 = 50.8626 x -6,442 / 32,768 = -10 RPS

**Velocity Scale Factor:** The velocity scale factor is used to achieve a greater resolution at lower rotational speeds (RPS). The scale factor is: **4095(152.5878RPS/max RPS),** where the max RPS is selected by the user to achieve the maximum resolution for a desired RPS. Enter the scale factor as an integer to the corresponding *Velocity Scale Register* for that particular channel.

To scale the Max Velocity word for 152.5878 RPS, set Velocity Scale Factor = 4095 (max velocity word of +32,767 (7FFFh) being 152.5878 RPS for CW rotation, and –32,768 (8000h) being 152.5878 RPS for CCW rotation). Scaling effects only the Velocity output word and not the dynamic performance.

To get a maximum velocity word (32,767) @ 152.5878 RPS, Scale Factor = 4095(152.5878/152.5878) = 4095 = 0FFFh;
This results in a velocity resolution of: (152.5878 RPS/32,767) x 360°/RPS = 1.676°/sec (factory default)

To get a maximum velocity word (32,767) @ 50.8626 RPS, Scale Factor = 4095(152.5878/50.8626) = 12,285 = 2FFDh);
This is a velocity resolution of: (50.8626 RPS/32,767) x 360°/RPS = 0.5588°/sec

For 9.5367 RPS max, Scale Factor = 4095(152.5878/9.5367) = 65,520 = FFF0h; 0.10477 °/sec resolution (lowest setting)

**D2 Test Enable:** Writing “1” to the D2 bit of the *Test Enable Register* initiates automatic background BIT testing that checks each channel every 5° to a test accuracy of 0.05°. The result of an accuracy error is available in the *Test Status Register* and if enabled, an interrupt will be generated (See *Interrupt Register*). A “0” deactivates this test. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled. The card will write 55h to the *Test (D2) Verify Register*, every 30 seconds, when the D2 Test is enabled. User can periodically clear the *Test (D2) Verify Register* by writing 00h, waiting 30 seconds, then reading the register again to verify that background BIT testing is activated.

In addition, each S/D Signal and Reference input is continually monitored. Any failure triggers an Interrupt (if enabled) and the results are available in the *Signal* and *Reference Status Registers*.

**D3 Test Enable:** Writing “1” to the D3 bit of the *Test Enable Register* initiates a BIT test that disconnects all channels from the outside world and connects them across an internal stimulus that generates and tests 72 different angles to a test accuracy of 0.05°. External reference is not required. The test cycle is completed within 45 seconds and results can be read from the *Test Status Registers* when D3 bit changes from “1” to “0” and if enabled, an interrupt will be generated if a BIT failure is detected (See *Interrupt Register*). The testing can be terminated at any time by writing "0" to D3 bit of the *Test Enable Register*.

Signal and Reference monitoring is disabled during D3 test.

**D0 Test Enable:** Used to check card and PC interface. Writing “1” to the D0 bit of the *Test Enable Register* disconnects all channels from the outside world and connects them to internal test signals, enabling the user to generate any test angle by writing an integer value, to the *Test Angle Register*. Data is then read through the interface (after writing, allow 400 ms before reading). External reference is not required. (e.g. 330° = angle/$(360/2^{16})$ ).

Signal and Reference monitoring is disabled during D0 test.

**Status, Test:** Check the channel’s corresponding bit of the *Test Status Register* for status of BIT testing for each active channel. A ”1” means accuracy passes; A “0” indicates a failure on an active channel. Channels that are inactive are also set to “0”. (Test cycle takes 45 seconds for accuracy error). Any Test status failure, transient or intermittent will latch the *Test Status Register*. Reading will unlatch register.

**Status, Reference:** Check the channel’s corresponding bit of the *Reference Status Register* for status of the reference input for each active channel. A ”1” means Reference ON, a “0” means Reference Loss on active channels. (Reference loss is detected within 2 seconds). Channels that are inactive are also set to “0”. Reference monitoring is disabled during D3 or D0 Test. Any Reference status failure, transient or intermittent will latch the *Reference Status Register*. Reading will unlatch register.

**Status, Signal:** Check the corresponding bit of the *Signal Status Register* for status of the input signals for each active channel. A "1" means Signal is valid (level must be a minimum of 2V), a “0” means Signal loss on active channels. (Signal loss is detected after 2 seconds). Channels that are inactive are also set to “0”. Signal monitoring is disabled during D3 and D0 test. Any Signal status failure, transient or intermittent will latch the *Signal Status Register*. Reading will unlatch register.

Now, let us consider what happens when a status bit changes before registers are read. For example, if a reference loss was detected and latched into registers and subsequent scans find that the reference was reconnected, then this status change will be held in background until registers are read. Within 250ms, registers will be updated with the background data. Allow 250 ms to scan all channels.

**Angle Change Alert:** Write a 16-bit word to the appropriate *Angle Change Register* for a given channel, to represent the minimum differential change required. MSB=180°; Minimum differential is 0.05°, setting to zero disables the Angle Change Alert for a given channel. Initiate monitoring by writing “1” to *Angle Change Initiate Register*.

When that differential is exceeded, on any monitored channel, the bit corresponding to that channel is set in *Angle Change Alert Register* ("0" = no change, "1" = change).

**Optional (A&B) Encoder Resolution:** To set Encoder Mode, write a "0" to the D15 bit and the appropriate code for the desired resolution to the D2, D1 & D0 bits of the corresponding channel (*A&B) Resolution/Poles Register*. Changing the resolution for any channel can be done on the fly. The default is a 12 bit resolution encoder output. See Table 3.
**Note**: Encoder/Commutation outputs are optional; see part ordering information.

**Optional Commutation Outputs (A,B,C):** To set Commutation Mode, write a "1" to the D15 bit and the appropriate code for the required motor poles to the D2, D1 & D0 bits of the corresponding channel *(A&B) Resolution/Poles Register*. See Register Bit map table.
**Note**: Encoder/Commutation outputs are optional; see part ordering information.

**Optional Reference Supply:** For frequency, write a 16-bit integer to the *Frequency Ref Supply Register*. (Ex: 400 Hz = 0190h) with LSB= 1Hz. For voltage, write a 16-bit integer to the *Voltage Ref Supply Register*. (Ex: 26Vrms =0104h) with LSB=0.1Vrms. It is recommended that the user program the required frequency before setting the output voltage.

**Interrupt Registers:** Interrupts can be enabled to relay specific problems/failures detected by the card. The problem/failures that generate these interrupts are:

S/D Signal Loss, S/D Reference Loss, S/D Angle Change Alert, S/D Test Accuracy Error,

Each external interrupt can be enabled individually. This is accomplished by writing a "1" to the bit corresponding to desired interrupts to the *Interrupt Enable Register* and a "0" to disable those interrupts not used. Refer to Table 3.

**Interrupt Status Registers:** When an interrupt is initiated via a problem/failure, the *Interrupt Status Register* can be interrogated by a read to identify, which interrupt occurred. Refer to Table 3. Register is latched when interrupt is generated and unlatched when read.

Note: This register is typically read and cleared by the device driver. Subsequent readings of this register will give clear status.

## ADDITIONAL FUNCTIONS:

**Soft Reset:** Write an integer "1" to *Soft Reset Register*, then clear to 0 before 50ms elapses. **CAUTION: Register is level sensitive and for proper card operation, the logic level "1", or pulsewidth, must be <= 50ms**. Considering minimum and maximum, 1 µs < pulsewidth <= 50ms. Processor reboots in about 400 ms, after which calibration procedures begin. This function is equivalent to a power-on reset.

**Watchdog Timer:** This feature monitors the *Watchdog Timer Register*. When it detects that a code has been received, that code will be inverted within 100 µsec. The inverted code stays in the register until replaced by a new code. The user should look for the inverted code, after 100 µsec, to confirm that the processor is operating.

**Part Number:** Read as a 16-bit binary word from the *Part Number Register*. A unique 16 bit code is assigned to each model number.

**Serial Number:** Read as a 16-bit binary word from the *Serial Number Register*. This is the serial number of that particular board.

**Date Code:** Read as decimal number from the *Date Code Register*. Four digits represent YYWW (Year, Year, Week, Week)

**Rev Levels:** There are a total of 4 *Revision Level Registers*, which are listed below. Each register is defined as 16 bits. The integer value of that particular register corresponds to the actual revision.

Rev level PCB
Rev level S/D DSP
Rev level S/D FPGA
Rev level Interface FPGA

## Software - PCI Programming

This section provides programmers the information needed for developing drivers other than those supplied. The following information resides in the PCI configuration registers:

| | | |
|---|---|---|
| Device ID | = 7501 | (hex) |
| Vendor ID | = 15AC | (hex) |
| Rev | = 01 | (hex) |
| Subsystem ID | = 000115AC | (hex) |
| Base Address | = Assigned by the PCI BIOS. Interrogate the PCI BIOS for this information. | |
| Required Address space | = 1K for each card. | |

### Front panel Connector:

DD-50P, Mate: DD-50S (not supplied)

| Pin | Ch. 1 | Pin | Ch. 2 | Pin | Ch. 3 | Pin | Ch. 4 | Pin | Ch. 5 | Pin | Ch. 6 | Pin | Ch. 7 | Pin | Ch. 8 | Pin | Ref. output |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 25 | S1 | 22 | S1 | 2 | S1 | 42 | S1 | 43 | S1 | 45 | S1 | 31 | S1 | 49 | S1 | 1 | Ref Hi Out |
| 8 | S2 | 5 | S2 | 19 | S2 | 37 | S2 | 26 | S2 | 28 | S2 | 30 | S2 | 32 | S2 | 34 | Ref Lo Out |
| 9 | S3 | 6 | S3 | 3 | S3 | 41 | S3 | 27 | S3 | 29 | S3 | 47 | S3 | 33 | S3 | | |
| 24 | S4 | 21 | S4 | 18 | S4 | 38 | S4 | 10 | S4 | 12 | S4 | 14 | S4 | 16 | S4 | | |
| 7 | RHi | 20 | RHi | 35 | RHi | 39 | RHi | 11 | RHi | 13 | RHi | 15 | RHi | 17 | RHi | | |
| 23 | RLo | 4 | RLo | 36 | RLo | 40 | RLo | 44 | RLo | 46 | RLo | 48 | RLo | 50 | RLo | | |

### Rear panel J2 connector

| Pin | Ch. 1 | Pin | Ch. 2 | Pin | Ch. 3 | Pin | Ch. 4 | Pin | Ch. 5 | Pin | Ch. 6 | Pin | Ch. 7 | Pin | Ch. 8 | Pin | Ref. output |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| D20 | S1 | D17 | S1 | D15 | S1 | D12 | S1 | D2 | S1 | D5 | S1 | D7 | S1 | D10 | S1 | E1 | Ref Hi Out |
| E21 | S2 | E18 | S2 | E16 | S2 | E13 | S2 | E3 | S2 | E6 | S2 | E8 | S2 | E11 | S2 | D1 | Ref Lo Out |
| E20 | S3 | E17 | S3 | E15 | S3 | E12 | S3 | E2 | S3 | E5 | S3 | E7 | S3 | E10 | S3 | | |
| D21 | S4 | D18 | S4 | D16 | S4 | D13 | S4 | D3 | S4 | D6 | S4 | D8 | S4 | D11 | S4 | | |
| E19 | RHi | C19 | RHi | E14 | RHi | C14 | RHi | E4 | RHi | C4 | RHi | E9 | RHi | C9 | RHi | | |
| D19 | RLo | B19 | RLo | D14 | RLo | B14 | RLo | D4 | RLo | B4 | RLo | D9 | RLo | B9 | RLo | | |
| C21 | A Hi | C18 | A Hi | C16 | A Hi | C13 | A Hi | C11 | A Hi | C8 | A Hi | C6 | A Hi | C3 | A Hi | | |
| B21 | A Lo | B18 | A Lo | B16 | A Lo | B13 | A Lo | B11 | A Lo | B8 | A Lo | B6 | A Lo | B3 | A Lo | | |
| C20 | B Hi | C17 | B Hi | C15 | B Hi | C12 | B Hi | C10 | B Hi | C7 | B Hi | C5 | B Hi | C2 | B Hi | | |
| B20 | B Lo | B17 | B Lo | B15 | B Lo | B12 | B Lo | B10 | B Lo | B7 | B Lo | B5 | B Lo | B2 | B Lo | | |
| A21 | IDX Hi | A18 | IDX Hi | A16 | IDX Hi | A13 | IDX Hi | A11 | IDX Hi | A8 | IDX Hi | A6 | IDX Hi | A3 | IDX Hi | | |
| A20 | IDX Lo | A17 | IDX Lo | A15 | IDX Lo | A12 | IDX Lo | A10 | IDX Lo | A7 | IDX Lo | A5 | IDX Lo | A2 | IDX Lo | | |

S4 pins used only with Resolvers. Do not connect to any undesignated pins

As of June 1, 2004 High and Low Reference Signal outputs have been moved from E22 and D22 to E1 and D1 respectively to support cPCI Geographical Addressing.

## Code Table

| Code | Frequency (Hz) | Input ($V_{L-L}$) | Input ($Z_{in}$) | Ref Vrms | Comments |
|---|---|---|---|---|---|
| 01 | 400 | 11.8 | 40K | 26 | |
| 02 | 400 | 90 | 100K | 115 | |
| 03 | 50/400 | 90 | 100K | 115 | |
| 04 | 400 | 2-26 | 40K | 2-26 | |
| 06 | 10K | 2-26 | 40K | 2-26 | |

See code list addendum for descriptions of code 50 and above.

**IMPORTANT: Bandwidth can easily be customized to meet your specific requirements.**

## PART NUMBER DESIGNATION

**75SD1- XX X X X X - XX**

**TOTAL NUMBER OF CHANNELS**
02 – 2 S/D Channels
04 – 4 S/D Channels
08 – 8 S/D Channels

**ENVIRONMENTAL**
C = 0°C to +70°C
E = -40°C to +85°C
H = E With Removable Conformal Coating
K = C With Removable Conformal Coating
contact factory for other temperature requirements

**FORMAT**
S = Synchro
R = Resolver
M = Mixed (See Code Table)
P = Synchro/Resolver Programmable

**MECHANICAL**
F = Front Panel I/O only
B = Front Panel I/O and J2 I/O
P = J2 I/O only
W= P with Wedgelocks (cPCI only, not PXI)
only available on 4 channel versions.

**Note**: J2 connections can not be used for Analog signals in a PXI chassis. Analog Outputs must be via the front panel I/O only

**CODE** (See Code Table)

**ENCODER/COMMUTATION**
- = Without Encoder/Commutation option
E = With Encoder/Commutation option

Encoder/Commutation outputs are via the J2 connector **only**

**OPTIONAL REFERENCE SELECTION**
0 = No "On Board Reference"
A = 2-28 VRMS output
C = 115 VRMS fixed output

# Revision Page

| Revision | Description of Change | Engineer | Date |
|---|---|---|---|
| Rev 2.0 | Original | JWP | 09/21/01 |
| Rev 2.1 | Changed temperature references from “M” to E” | FH/BC | 10/16/01 |
| Rev 2.2 | Added codes 51-53 to Code Table | BC | 12/04/01 |
| Rev 2.3 | “(POST)… can be enable disabled…” to “…(POST)… can be enabled or disabled…”<br>D2 Test section “bit” reference changed to “BIT”.<br>Memory Map 12ch Save is read/write | GS | 01/01/02 |
| Rev 2.4 | See code list addendum for descriptions of code 50 and above. Part Number: contact factory for other temp requirements. Non-volatile, not permanent memory. Automatically supports either 5V or 3.3V logic levels. Changed S/D Read 1spd/2spd text. | GS | 02/04/02 |
| Rev 2.5 | Memory Map SAVE address is 140 | GS | 02/25/02 |
| Rev 2.6 | Changes Front Panel Connector pin 38 to 32 | GS | 03/21/02 |
| Rev 2.7 | Max Vel Out is 152.5878 | GS | 05/30/02 |
| 2.8 | For proper Soft Reset operation, 1µ < pulsewidth <=50ms. | GS | 06/27/02 |
| 2.9 | Removed 2-13.5 volt reference option (from spec, and PN) | GS | 06/28/02 |
| 3.0 | Two-Speed Read: read Data Lo word, then Data Hi word. Data Lo word, when read, latches high word. | GS | 08/06/03 |
| 3.1 | As of June 1, 2004 High and Low Reference Signal outputs have been moved from E22 and D22 to E1 and D1 respectively to support cPCI Geographical Addressing. | GS | 06/04/04 |
| 3.2 | Adds Mechanical Option W. | GS | 06/09/04 |
| 3.3 | Conducted cooled versions available. | GS | 07/07/04 |
| 3.4 | Wedgelock option is only available for 4 channel versions | GS | 04/19/05 |
| 3.5 | Changed Address | DD | 05/07/07 |
| 3.6 | Initial Agile release. Removed reference to “Save Setup” feature (retroactive clarification) | AS | 02/26/14 |