IPM429-E-16T-0R
IPM429-EI-16T-0R
IPM429-ELB-16T-0R
IPM429-ELBI-16T-0R

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IPM429-E-16T-0R™

User Manual

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IPM429-E-16T-0R REVISION CROSS REFERENCE

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* Refer to MAX Technologies Product History documents for a full hardware history of all MAX Technologies products. More details on software compatibility, product revision, global modification revision, PCB revision and firmware revision are available in the Product History documents.

Table of content

List of tables

1. INTRODUCTION

This document describes the operation of the IPM429-E-16T-0R Module. The IP module has the following characteristics:

- 16 ARINC 429 transmitters.
- Single size, 16-bit Industry Pack interface at 32 MHz.
- Meets or exceeds ARINC 429 electrical and timing specifications.
- Data transfer controlled by interruptions or pooling.
- 32 ARINC words buffer per port.
- The exact transmission time of every ARINC word can be locally controlled by a 16 bit, 1 us resolution timer.
- Buffer Overflow detection and error generation.
- Programmable parity (odd, even or none).
- Word length selection (25 or 32 bits).
- Two programmable bit rate generators (from 8 to 256 us / bit with .5us increments).
- 8 general usage TTL compatible IO lines.
- Each TX port may generate a synchronization pulse when an ARINC word is transmitted on the IO lines.
- 2 Event capture systems on IO lines with a resolution of 1 us.
- Programmable gap length.
- TX lines interfaces continuous diagnostics (LB option).
- Industrial temperature range available (I option).
- On-board IRIG-B decoder (rev.B1 and higher).

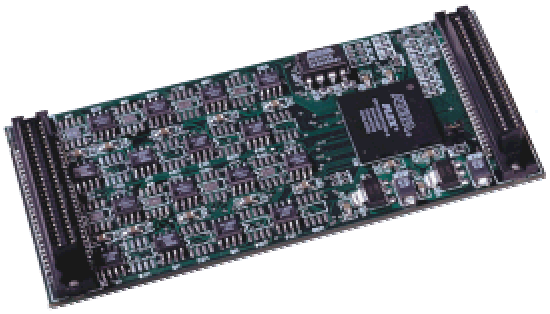


Figure 1-1 : IPM429-E-8T-8R

2. HARDWARE SPECIFICATION

2.1 The Main Controller

The main controller on the IP includes 7 sections:

- IP Bus interface controller.
- IP ID ROM emulation block.
- A set of control and status registers.
- The SRAM data buffers.
- The DATA buffer controller (16 FIFOs within the SRAM).
- Two bit rate generators.
- 16 ARINC 429 transmitter controller blocks

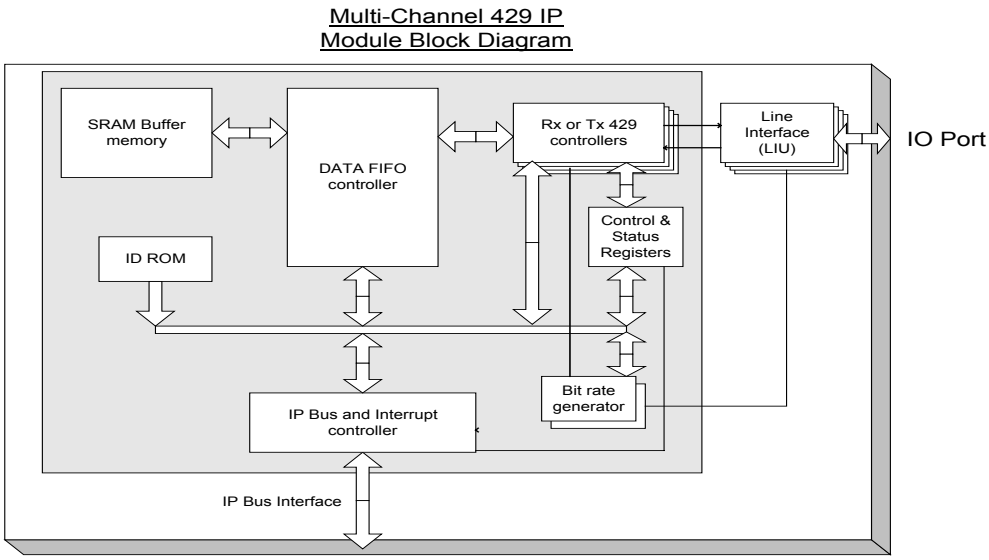


Figure 2-1: IPM429 Block Diagram

2.1.1 The IP Bus Interface Controller

The host uses this interface to configure the module, read statuses and to transfer the data transmitted and received.

2.1.2 The Data Buffers

The FIFO buffers are implemented with an internal SRAM, shared between the IP interface and the ports. A 128 words deep FIFO 16 bits wide is implemented for each port (32 ARINC words per port). Every time an ARINC word and the associated TX_TIME and control word are written from the IP interface, they are saved in the transmitter port FIFO. See chapter 4 for details on data transfer structure.

2.1.3 The Main Timer

A 32 bit, 1 us resolution timer is implemented in the main controller. It is primary used for precise data transmission for TX ports and IO event capture.

2.1.4 Data Transmission

To accomplish precise time transmission, a 16 bit word (TX_TIME) may be associated with ARINC data word. The transmission of the ARINC word is then delayed until the timer's 16 LSB reaches the TX_TIME value. The precise time transmission feature may be used or not, depending on the application.

2.1.5 The Bit Rate Generators

Two bit-rate generator registers are provided to program the low and high speed rate of every port. Each port is programmed to operate at the high or the low rate. Each transmitter has a 9 bit programmable counter used to generate his own bit rate. This independent bit rate generator for each TX port permits to achieve the 1us timing precision. These counters decrement every .5 us and are re-loaded with the value contained in the HIGH_RATE or LOW_RATE registers when it reaches zero. Selecting the bit rate generator also fixes the rise and fall time of the transmitter ports (1 us for high rate ports, 10us for low rate ports).

2.1.6 The TX Diagnostic (LB option only)

This feature allows testing of the line interface for the TX port. Each transmitter has its own diagnostic circuit that verify every single bit transmitted. When a failure is detected in the bit transmission an error may be issued from the IP to the host card. The diagnostic circuitry is a dedicated ARINC line interface receiver HI-8588 for each TX and connected directly to the IP IO pin.

2.1.7 The Time Captures

A falling or rising edge on IOs 0 and 1 may generate an interrupt and be time stamped. There is a separate time capture register and interrupt control register for both IOs. The time capture may be used whenever the IO is configured as an input or an output.

2.1.8 The IRIG-B decoder

An IRIG-B decoder on the module can optionally provide IRIG-B time code to user application and synchronize the IPM-429E to them for true real-time critical applications. Since the module have a 32bit 1us Time tag precision and the IRIG-B time code have a one second resolution, we‘ve implemented an algorithm to precisely correlate the 1us timer to the Pr point of the IRIG-B (start of the time code) or the 1PPS signal if available. (see 3.4.23 IRIGB_SEL Register)

The decoder logic accepts both TTL and standard amplitude-modulated (AM) IRIG-B signal. When using the TTL input, the 1us synchronicity is exact since the rising edge of the TTL output corresponds exactly to the Pr point. When using an AM IRIG-B signal, the decoder circuitry and logic will synchronize on the zero crossing of the beginning of the Pr point of the AM modulated signal. This zero crossing of the low frequency AM modulated signal is not as accurate as the TTL or 1PPS signal. So the user may use a 1PPS signal on the TTL input to improve synchronicity when using the IRIG-B AM signal or compensate. (See application Note: <Calibration process for MAX Technologies product with IRIG.pdf>)

2.2 Electrical Interfaces

2.2.1 Output Interfaces

The output line interfaces are the integrated circuit HOLT HI-8585 that are compliant with the ARINC-429 output specification:

- Differential 10V +/- 0.5V.
- Bipolar (RZ) coding.
- Controlled rising and falling edge
- 75 ohms differential output impedance.
- Short-circuit tolerant.

2.2.2 Input Interfaces (LB option only)

The input line interfaces, used for the TX diagnostic (LB option only), are the integrated circuit HOLT HI-8588 that are compliant with the ARINC-429 input specification:

- Differential input Threshold 5 +/-0.5V.
- Bipolar (RZ) coding.
- Differential Input Impedance > 100 Kohm

3. MEMORY MAP

3.1 The IP ID ROM region

The IP identification ROM is implemented in one of the ALTERA memory cells. It is preloaded with the proper device definition during the programming phase of the ALTERA.

IP Region	Address	Description	Value (hex)
ID	0	ASCII "VI"	0x5649
	2	ASCII "TA"	0x5441
	4	ASCII "4 "	0x3420
	6	Manufacturer ID high 8 bit	0x0000
	8	Manufacturer ID low 16 bit	0x0000
	A	Model #	0x0009 (E) or 0x000C (ELB)
	C	Revision #	0x00B1
	E	Reserved	0x0000
	10	Driver ID LSB	0x10E8
	12	Driver ID MSB	0x0008 => OPTION*
	14	16-bit flag	0x0004
	16	Number of byte used in the ROM	0x0030
	18	CRC of the byte used in the ROM	0xXXXX
	1A	Active TX PORT	0xFFFF (port 0 to 15 are TX)
	1C	Active RX PORT	0x0000 (no RX)
	1E	Not Used	0x0000
	20	Not Used	0x0000
	22	Last Compatible Model	0x0001
	24	ASCII "IP"	0x4950
	26	ASCII "M4"	0x4D34
	28	ASCII "29"	0x3239
	2A	ASCII "E "	0x4520
	2C	ASCII " " or ASCII "LB" (LB option)	0x2020 or 0x4C42
	2E	ASCII " " or ASCII "I " (I option)	0x2020 or 0x4920

Table 3-1: IP ID ROM map

* : Included option bit definition :
  bit 0 : Future use
  bit 1 : Future use
  bit 2 : Future use
  bit 3 : IRIG-B decoder included (Option D)

3.2 The IP IO region

IP Region	Address	IP Bus Bits	Access	Name	RESET Value (hex)
IO	00	[15:0]	R/W	PORT_ENABLE	0x0000
	02	[15:0]	R	BUFFER_STATUS	0xFFFF
	04	[15:0]	R/W	BUFFER_OVERFLOW	0x0000
	06	[15:0]	R/W	INTERRUPT_ENABLE	0x0000
	08	[15:0]	R/W	PARITY_ENABLE	0x0000
	0A	[15:0]	R/W	WORD_LENGTH	0x0000
	0C	[15:0]	R/W	RATE SELECT	0x0000
	0E	[8:0]	R/W	HIGH_RATE	0x0013
	10	[8:0]	R/W	LOW_RATE	0x009F
	12	[7:0]	R/W	IO_DATA	0x00FF
	14	[7:0]	R/W	IO_DIR	0x0000
	16			N.U.	0x0000
	18	[15:0]	R/W	TX_INT_CONFIG	0x0102
	1A			N.U.	0x0000
	1C	[15:0]	R	TIMER[31:16]	0x0000
	1E	[15:0]	R	TIMER[15:0]	0x0000
	20	[15:0]	W	TX #0 BUFFER	Empty
	22	[15:0]	W	TX #1 BUFFER	Empty
	24	[15:0]	W	TX #2 BUFFER	Empty
	26	[15:0]	W	TX #3 BUFFER	Empty
	28	[15:0]	W	TX #4 BUFFER	Empty
	2A	[15:0]	W	TX #5 BUFFER	Empty
	2C	[15:0]	W	TX #6 BUFFER	Empty
	2E	[15:0]	W	TX #7 BUFFER	Empty
	30	[15:0]	W	TX #8 BUFFER	Empty
	32	[15:0]	W	TX #9 BUFFER	Empty
	34	[15:0]	W	TX #10 BUFFER	Empty
	36	[15:0]	W	TX #11 BUFFER	Empty
	38	[15:0]	W	TX #12 BUFFER	Empty
	3A	[15:0]	W	TX #13 BUFFER	Empty
	3C	[15:0]	W	TX #14 BUFFER	Empty
	3E	[15:0]	W	TX #15 BUFFER	Empty
	40	[15:0]	R/W	TX_RX_ERROR	0x0000
	42	[15:0]	R/W	TX_RX_ERROR_MASK	0x0000
	44	[5:0]	R/W	GAP_LENGTH	0x0010
	46	[15:0]	R/W	GAP_LENGTH _SEL	0x0000
	48	[5:0]	R/W	EDGE_CAPTURE_CTRL	0x0000
	4A	[15:0]	R	CAPTURE_TIME0	0x0000
	4C	[15:0]	R	CAPTURE_TIME1	0x0000
	4E-72			N.U.	
	74	[15:0]	R	IRIG_CTT_LOW	0000
	76	[15:0]	R	IRIG_CTT_HIGH	0000
	78	[15:0]	R	IRIG_DATA_LOW	0000
	7A	[13:0]	R	IRIG_DATA_HIGH	0000
	7C	[15:11]	R/W	IRIGB_SEL	0000
	7E		R	Reserved for internal use	0004

Table 3-2: IP IO map.

3.3 Registers Definition and usage

3.3.1 The PORT_ENABLE Register (IO Addr: 0x00)

This register is used to enable or disable each PORT.

Bit	Function	Reset value
0	TX #0 enable	0 (port disabled)
1	TX #1 enable	0 (port disabled)
2	TX #2 enable	0 (port disabled)
3	TX #3 enable	0 (port disabled)
4	TX #4 enable	0 (port disabled)
5	TX #5 enable	0 (port disabled)
6	TX #6 enable	0 (port disabled)
7	TX #7 enable	0 (port disabled)
8	TX #8 enable	0 (port disabled)
9	TX #9 enable	0 (port disabled)
10	TX #10 enable	0 (port disabled)
11	TX #11 enable	0 (port disabled)
12	TX #12 enable	0 (port disabled)
13	TX #13 enable	0 (port disabled)
14	TX #14 enable	0 (port disabled)
15	TX #15 enable	0 (port disabled)

Table 3-3: PORT_ENABLE Register

3.3.2 The BUFFER_STATUS Register (IO Addr: 0x02)

This register contains the status of the data buffers of every port on the module. When set, the status bit indicates that a transmitter buffer is almost empty.

For transmitters:

IF (TransmitterBuffer[PORT] contains TX_FIFO_AE[1] ARINC words) then
    BUFF_STAT[PORT] goes to '1'
ELSE IF(TransmitterBuffer[PORT] contains TX_FIFO_AF words) then
    BUFF_STAT[PORT] return to '0'
END IF

Bit	Function		Reset
0	TX #0 Buffer status	TX: 0 => Buffer NOT almost empty 1 => buffer almost empty	1
1	TX #1 Buffer status	"	1
2	TX #2 Buffer status	"	1
3	TX #3 Buffer status	"	1
4	TX #4 Buffer status	"	1
5	TX #5 Buffer status	"	1
6	TX #6 Buffer status	"	1
7	TX #7 Buffer status	"	1
8	TX #8 Buffer status	"	1
9	TX #9 Buffer status	"	1
10	TX #10 Buffer status	"	1
11	TX #11 Buffer status	"	1
12	TX #12 Buffer status	"	1
13	TX #13 Buffer status	"	1
14	TX #14 Buffer status	"	1
15	TX #15 Buffer status	"	1

Table 3-4: BUFFER_STATUS Register

[1] TX_FIFO_AE, TX_FIFO_AF is configurable threshold values defined in section 3.4.12.

3.3.3 The BUFFER_OVERFLOW Register (IO Addr: 0x04)

This register indicates if any of the data buffers has overflowed. The IP_Error* is asserted when there is an overflow condition on at least one port. To reset an overflow condition, there must be a one written to the associated bit (sticky bit).

Bit	Function	Reset
0	TX #0 Buffer OV	0 (no overflow)
1	TX #1 Buffer OV	0
2	TX #2 Buffer OV	0
3	TX #3 Buffer OV	0
4	TX #4 Buffer OV	0
5	TX #5 Buffer OV	0
6	TX #6 Buffer OV	0
7	TX #7 Buffer OV	0
8	TX #8 Buffer OV	0
9	TX #9 Buffer OV	0
10	TX #10 Buffer OV	0
11	TX #11 Buffer OV	0
12	TX #12 Buffer OV	0
13	TX #13 Buffer OV	0
14	TX #14 Buffer OV	0
15	TX #15 Buffer OV	0

Table 3-5: BUFFER_OVERFLOW Register

3.3.4 The INT_ENABLE Register (IO Addr: 0x06)

This register enables or disables the interrupt at each port as a possible interrupt source. When the buffer status bit of a port and the corresponding bit in the interrupt mask register are set, the IntReq0* signal is asserted.

Bit	Function	Reset value
0	TX #0 interrupt enable	0 (INT disabled)
1	TX #1 interrupt enable	"
2	TX #2 interrupt enable	"
3	TX #3 interrupt enable	"
4	TX #4 interrupt enable	"
5	TX #5 interrupt enable	"
6	TX #6 interrupt enable	"
7	TX #7 interrupt enable	"
8	TX #8 interrupt enable	"
9	TX #9 interrupt enable	"
10	TX #10 interrupt enable	"
11	TX #11 interrupt enable	"
12	TX #12 interrupt enable	"
13	TX #13 interrupt enable	"
14	TX #14 interrupt enable	"
15	TX #15 interrupt enable	"

Table 3-6: INT_ENABLE Register

3.3.5 The PARITY_ENABLE Register (IO Addr: 0x08)

This register enables or disables the automatic parity generation. Note that the control word receive with each ARINC word is used to select the parity (even or odd).

Bit #	Function	Description	Reset value
0	TX #0 parity enable	0 => parity generation disabled 1 => parity generation enabled	0 (no parity generation)
1	TX #1 parity enable	"	"
2	TX #2 parity enable	"	"
3	TX #3 parity enable	"	"
4	TX #4 parity enable	"	"
5	TX #5 parity enable	"	"
6	TX #6 parity enable	"	"
7	TX #7 parity enable	"	"
8	TX #8 parity enable	"	"
9	TX #9 parity enable	"	"
10	TX #10 parity enable	"	"
11	TX #11 parity enable	"	"
12	TX #12 parity enable	"	"
13	TX #13 parity enable	"	"
14	TX #14 parity enable	"	"
15	TX #15 parity enable	"	"

Table 3-7: PARITY_ENABLE Register

3.3.6 The WORD_LENGTH Register (IO Addr: 0x0A)

Each port can be programmed to work on 25 or 32 bit ARINC words.

Bit	Function	Reset value
0	TX #0 word length select 0 => 25 bit word 1 => 32 bit word	0 (25 bit word)
1	"	"
2	"	"
3	"	"
4	"	"
5	"	"
6	"	"
7	"	"
8	"	"
9	"	"
10	"	"
11	"	"
12	"	"
13	"	"
14	"	"
15	"	"

Table 3-8: WORD_LENGTH Register

3.3.7 The RATE_SELECT Register (IO Addr: 0x0C)

This register selects which of the two rate generators is assigned to every port. This register also controls the rise and fall time of the transmitters (10us rise and fall time for the low speed ports, 1 us for the high speed ports).

Bit	Function	Reset value
0	TX #0 Rate select	0 (Low Rate,10us rise/fall time)
1	TX #1 Rate select	“
2	TX #2 Rate select	“
3	TX #3 Rate select	“
4	TX #4 Rate select	“
5	TX #5 Rate select	“
6	TX #6 Rate select	“
7	TX #7 Rate select	“
8	TX #8 Rate select	“
9	TX #9 Rate select	“
10	TX #10 Rate select	“
11	TX #11 Rate select	“
12	TX #12 Rate select	“
13	TX #13 Rate select	“
14	TX #14 Rate select	“
15	TX #15 Rate select	“

Table 3-9: RATE_SELECT Register

3.3.8 The HIGH_RATE Register (IO Addr: 0x0E)

This 9 bits register contains the bit rate used by the ports programmed to operate at the high rate (see the RATE_SELECT register). The rate should never be less than 8 us per bit.

RATE = (HIGH_RATE + 1) * 0.5us

Example:

HIGH_RATE Value (Hex)	Corresponding bit rate
1FF	3906.25 bits / s
09F (low rate reset value)	12.5 Kbit / sec
014	95.238Kbit / sec
013 (high rate reset value)	100 Kbit / sec
00F	125 Kbit / sec

Table 3-10: HIGH_RATE Register

3.3.9 The LOW_RATE Register (IO Addr: 0x10)

This register is identical to the HIGH_RATE register, but is used by ports configured to operate at the low rate.

3.3.10 The IO_DATA Register. (IO Addr: 0x12)

Depending on the data direction chosen for each IO/SYNC signal, this register returns the value of signals configured as inputs or controls the level on signals configured as outputs.

Bit	Function	Reset value
0	IO/SYNC #0	1
1	IO/SYNC #1	1
2	IO/SYNC #2	1
3	IO/SYNC #3	1
4	IO/SYNC #4	1
5	IO/SYNC #5	1
6	IO/SYNC #6	1
7	IO/SYNC #7	1

Table 3-11: IO_DATA Register

3.3.11 The IO_DIR Register. (IO Addr: 0x14)

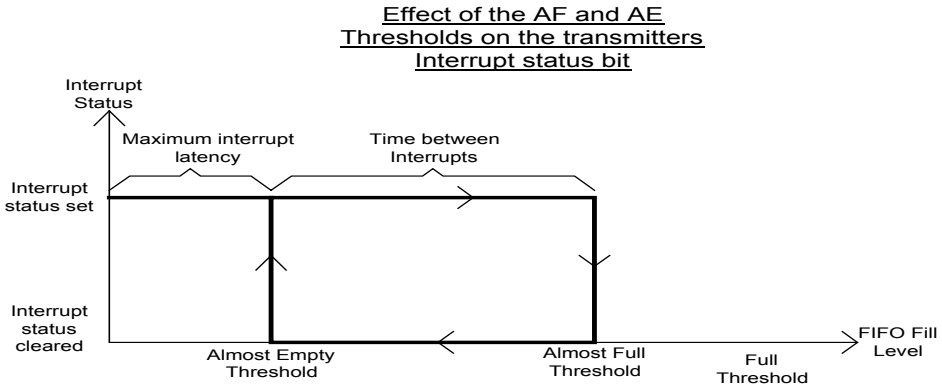
Controls whether the IO/Sync[7:0] signals are input or output signals. When an IO/SYNC signal is configured as an input, the level present on the line is reflected in the corresponding bit of the IO_DATA register. When configured as an output, the IO_DATA register controls the level present on the corresponding IO/SYNC signal.

Bit	Function	Reset value
0	0 => IO/SYNC0 is an input 1 => IO/SYNC0 is an output	0
1	0 => IO/SYNC1 is an input 1 => IO/SYNC1 is an output	0
2	0 => IO/SYNC2 is an input 1 => IO/SYNC2 is an output	0
3	0 => IO/SYNC3 is an input 1 => IO/SYNC3 is an output	0
4	0 => IO/SYNC4 is an input 1 => IO/SYNC4 is an output	0
5	0 => IO/SYNC5 is an input 1 => IO/SYNC5 is an output	0
6	0 => IO/SYNC6 is an input 1 => IO/SYNC6 is an output	0
7	0 => IO/SYNC7 is an input 1 => IO/SYNC7 is an output	0

Table 3-12: IO_DIR Register

3.3.12 The TX_INT_CONFIG Register (IO Addr: 0x18)

Contains the almost empty (AE) and almost full (AF) threshold. The AF threshold fixes the level at which the interrupt status bit of transmitter is cleared when the host fills a transmitter FIFO. The AE threshold fixes the level at which the interrupt status bit of a transmitter is asserted when a transmitter empties its buffer.
The following figure graphically presents the effect of the AE and AF thresholds on the receivers and transmitters interrupt status bit.



Bit	NAME	Description	Reset value
[5:0]	TX_FIFO_AE	Fifo Almost Empty threshold	02h
[11:6]	TX_FIFO_AF	Fifo Almost Full threshold	04h

Table 3-13: TX_INT_CONFIG Register

Note that 32 is the maximum quantity of ARINC words that the TX buffer may contain. Values greater than 32 will result in an unreachable threshold.

3.3.13 The TIMER Register (IO Addr: 0x1C & 0x1E)

This register is a latch of the 32 bit main timer. When reading the MSB (address 1C), the latch will freeze until the LSB (address 1E) is read. The IP_Strobe* signal from the carrier board is used to reset this timer. As an example, the IP_Strobe* signal could be asserted simultaneously to all IP modules in order to reset and thus synchronize the timers present on every MAX Technologies IP modules that support this feature.

3.3.14 The TX_RX_ERROR Register (IO Addr: 0x40)

This register sets a flag when a transmitter does not transmit correctly (LB Option only). If the associated mask in the TX_RX_ERROR_MASK_REG register is set to one for transmitter, the IP_ERROR* line will be asserted. To reset an error condition, there must be a 1 written to the associated bit (sticky bit).

Bit #	Function	Description	Reset value
0	TX #0 diag. flag	Set to one when an error occurs on transmitter	0
1	TX #1 diag. flag	Set to one when an error occurs on transmitter	0
2	TX #2 diag. flag	Set to one when an error occurs on transmitter	0
3	TX #3 diag. flag	Set to one when an error occurs on transmitter	0
4	TX #4 diag. flag	Set to one when an error occurs on transmitter	0
5	TX #5 diag. flag	Set to one when an error occurs on transmitter	0
6	TX #6 diag. flag	Set to one when an error occurs on transmitter	0
7	TX #7 diag. flag	Set to one when an error occurs on transmitter	0
8	TX #8 diag. flag	Set to one when an error occurs on transmitter	0
9	TX #9 diag. flag	Set to one when an error occurs on transmitter	0
10	TX #10 diag. flag	Set to one when an error occurs on transmitter	0
11	TX #11 diag. flag	Set to one when an error occurs on transmitter	0
12	TX #12 diag. flag	Set to one when an error occurs on transmitter	0
13	TX #13 diag. flag	Set to one when an error occurs on transmitter	0
14	TX #14 diag. flag	Set to one when an error occurs on transmitter	0
15	TX #15 diag. flag	Set to one when an error occurs on transmitter	0

Table 3-14: TX_RX_ERROR Register

3.3.15 The TX_RX_ERROR_MASK Register (IO Addr: 0x42)

This register enables/disables the error notification on line IP_Error* from a defective or shorted transmitter (LB Option only). When TX diagnostic mask bit is set, the transmitter is disabled if a TX failure happens on this transmitter.

Bit #	Function	Description	Reset value
0	TX #0 diag. mask	Enable/disable the error on IP_ERROR*	0
1	TX #1 diag. mask	Enable/disable the error on IP_ERROR*	0
2	TX #2 diag. mask	Enable/disable the error on IP_ERROR*	0
3	TX #3 diag. mask	Enable/disable the error on IP_ERROR*	0
4	TX #4 diag. mask	Enable/disable the error on IP_ERROR*	0
5	TX #5 diag. mask	Enable/disable the error on IP_ERROR*	0
6	TX #6 diag. mask	Enable/disable the error on IP_ERROR*	0
7	TX #7 diag. mask	Enable/disable the error on IP_ERROR*	0
8	TX #8 diag. mask	Enable/disable the error on IP_ERROR*	0
9	TX #9 diag. mask	Enable/disable the error on IP_ERROR*	0
10	TX #10 diag. mask	Enable/disable the error on IP_ERROR*	0
11	TX #11 diag. mask	Enable/disable the error on IP_ERROR*	0
12	TX #12 diag. mask	Enable/disable the error on IP_ERROR*	0
13	TX #13 diag. mask	Enable/disable the error on IP_ERROR*	0
14	TX #14 diag. mask	Enable/disable the error on IP_ERROR*	0
15	TX #15 diag. mask	Enable/disable the error on IP_ERROR*	0

Table 3-15: TX_RX_ERROR_MASK Register

3.3.16 The GAP_LENGTH Register (IO Addr: 0x44)

This register sets the gap length time between two words with a resolution of a quarter of a bit.
Ex: Lets suppose a bit time of 10us, hence, writing 3 to the register sets the gap length to 7.5us .

Bit #	Function	Description	Reset value
[0:5]	GAP_LENGTH	Gap length value between words	10h

Table 3-16: GAP_LENGTH Register

Performances of the gap length:

Resolution : 0.25 bit time
Precision : Limited by rise/fall time as per ARINC specification and HI-8585 transceiver. (typ.: 100ns)

3.3.17 The GAP_LENGTH_SEL register. (IO Addr: 0x46)

This register selects the gap length value written in the GAP_LENGTH register.

Bit #	Function	Description	Reset value
0	TX #0 gap length selection	0 => Gap length value of 4 bits 1 = >Gap length from gap length reg	0
1	TX #1 gap length selection	“	0
2	TX #2 gap length selection	“	0
3	TX #3 gap length selection	“	0
4	TX #4 gap length selection	“	0
5	TX #5 gap length selection	“	0
6	TX #6 gap length selection	“	0
7	TX #7 gap length selection	“	0
8	TX #8 gap length selection	“	0
9	TX #9 gap length selection	“	0
10	TX #10 gap length selection	“	0
11	TX #11 gap length selection	“	0
12	TX #12 gap length selection	“	0
13	TX #13 gap length selection	“	0
14	TX #14 gap length selection	“	0
15	TX #15 gap length selection	“	0

Table 3-17: GAP_LENGTH_SEL Register

3.3.18 The EDGE_CAPTURE_CTRL Register (IO Addr: 0x48)

This register controls the edge type and holds the interrupt masks and flags.

Bit	NAME	Description	Reset value	Access
0	EDGE0	1 : Rising edge on IO0 will set EFLAG0 0 : Falling edge on IO0 will set EFLAG0	0	R/W
1	EDGE1	1 : Rising edge on IO1 will set EFLAG1 0 : Falling edge on IO1 will set EFLAG1	0	R/W
2	EFLAG0	Set when EDGE0 occurred	0	R/WC[1]
3	EFLAG1	Set when EDGE1 occurred	0	R/WC[1]
4	EMASK0	When set and EFLAG0 is set an interrupt is issued on IntReq0*	0	R/W
5	EMASK1	When set and EFLAG1 is set an interrupt is issued on IntReq0*	0	R/W

[1] R/WC is write 1 clear type. Writing 1 to this bit clears this bit.

Table 3-18: EDGE_CAPTURE Register

3.3.19 The TIME_CAPTUREx register. (IO Addr: 0x4Ah and 0x4C)

These 16 bit registers hold the TIMER LSBs copied when the first EDGEx that triggered the EFLAGx occurred. Here are the characteristics of the captured time:

- Resolution : 1 us (LSB weight)
- Precision : + 0.075us (time capture delay)

3.3.20 The IRIGB_CTT register. (IO Addr: 0x74 and 0x76)

When the IRIG-B is enabled, IRIG_CTT is used as a correlation time-tag with the IRIG-B time. When the IRIG-B second is reached, the internal 32-bit microsecond timer is latched, which gives the correlation between the IRIG-B time and microsecond time. In that case, when reading the IRIG_CTT LSB (0x18), the IRIG_CTT MSB and the IRIG_DATA are latched, and will only be latched again after the IRIG_DATA is accessed.

Bit	**Description**	**Reset**	**Access**
[31..0]	IRIG_CTT	0x00000000	R

3.3.21 The IRIGB_DATA register. (IO Addr: 0x78 and 0x7A)

This register shows the last set of information the IRIG-B decoder has captured. If no IRIG-B signal is fed into the decoder circuit, these registers will remain at their reset value. The following table describes the content of the registers (bits 16 to 31 represent bits 0 to 15 of the second register). These registers are read-only. Note: IRIG-B signals often give Greenwich Mean Time (GMT+00:00).

Bit	Description	Reset value
0-3	Units of seconds	0000
6-4	Tens of seconds	000
10-7	Units of minutes	0000
13-11	Tens of minutes	000
17-14	Units of hours	0000
19-18	Tens of hours	00
23-20	Units of days	0000
27-24	Tens of days	0000
29-28	Hundreds of days	00

3.3.22 The IRIGB_SEL register. (IO Addr: 0x7C)

Bit	Name	Description	Reset value
0..13	Reserved		0
14	IRIGB_TTL_EN	When set to one, the DIO6 is used as a TTL IRIG-B signal. 1 => IRIG-B TTL enable	0
15	IRIGB_TTL_CONFIG	Gives the option between IRIG-B TTL entry or 1PPS signal used in correlation with IRIG-B AM signal. 0 => IRIG-B TTL digital 1 => IRIG-B 1PPS signal	0

The IRIGB_TTL_EN gives the possibility to use the TTL entry. When TTL enabled, the IRIGB_TTL_CONFIG is used to choose between an IRIG-B digital input and a 1PPS digital input, which is a 1 Hz TTL signal, with the rising edge precisely on the IRIG second (used in conjunction with the AM IRIG-B signal). When the IRIG-B digital input is used, the AM IRIG-B input is ignored. (See application note: <Q&A IRIG-B correlation.pdf> for more details on how to correlate Time Tag with IRIG-B Time code).

Note that to use the IRIG-B feature, jumpers of JP1 must be set on pins 4-6 and pins 3-5. When these are set, the IOSYNC6 and the IOSYNC7 cannot be used.

4. DATA TRANSFER

4.1 Data transfer to the Transmitters

Each ARINC word is sent with a 16 bit control word (see section 4.2.1) and a 16 bit time tag that specifies the transmission time. The following table presents the order in which the data is transferred to the IP module.

Data transfer sequence to the transmitters:

Write order	Word written to the TX FIFO
1 (first)	CONTROL[15:0]
2	TIME_TAG[15:0]
3	ARINC_DATA[32:17]
4 (last)	ARINC_DATA[16:1]

Table 4-1: Data Write Order

Performances of time controlled transmission :

Resolution : 1us
Precision: Limited by rise/fall time as per ARINC specification and HI-8585 transceiver. Deterministic delay are specified for each TX port before the beginning of an edge on the ARINC line.

TX0 : + 1.82 us	TX8 : + 2.30us
TX1 : + 1.88 us	TX9 : + 2.36 us
TX2 : + 1.94 us	TX10 : + 2.42 us
TX3 : + 2.0 us	TX11 : + 2.48 us
TX4 : + 2.06 us	TX12 : + 2.54 us
TX5 : + 2.12 us	TX13 : + 2.60 us
TX6 : + 2.18 us	TX14 : + 2.66 us
TX7 : + 2.24 us	TX15 : + 2.72 us

4.1.1 TX control word definition

The control word sent with each ARINC word is used to:

- Control the 8 external trigger signals
- Control the parity bit.
- Enable or disable the utilization of the time tag (useful to transmit unscheduled words)
- Control the number of bits to send

Bit #	Name	Description
[1:0]	WORD_SIZE	Word Size: 00 => Word length 01 => Word length - 1 10 => Word length + 1 11 => not used
2	N.U.	
3	N.U.	
4	N.U.	
5	N.U.	
6	N.U.	
7	N.U.	
8	EXT_SYNC	When this bit is set and the IO/SYNC corresponding to the port is configured as output, the IO/SYNC output will reverse for the ARINC word transfer duration. Note that this functionality is only available on the TX0 to TX7.
9	N.U.	
10	N.U.	
11	N.U.	
12	N.U.	
13	N.U.	
14	ODD_PARITY	0 => EVEN parity 1 => ODD parity
15	TX_NOW	When set, the ARINC word is transmitted immediately. When cleared, the transmission of the ARINC word is delayed until the internal timer becomes equal to the time tag (scheduled words)

Table 4-2: TX Control Word Description

4.1.2 Word size

When the word length is a standard word length –1, the bit removed is the bit before the parity bit (24 or 31). The last bit sent is a parity bit calculated on the 23 or 30 previously transmitted bits. When the word length is a standard word length +1, a bit is inserted before the parity bit. Parity is calculated on the 25 or 32 previously transmitted bits. The inserted bit value is the same as the 17th bit for a 32 bits word length and is the 25 th for a 25 bits word length.

5. Hardware Configuration

5.1 IP IO Connector Definition

The IO connector pin-out is given in the following table:

PIN #	Function
1	GND
2	TX_0A
3	TX_0B
4	TX_1A
5	TX_1B
6	GND
7	TX_2A
8	TX_2B
9	TX_3A
10	TX_3B
11	GND
12	TX_4A
13	TX_4B
14	TX_5A
15	TX_5B
16	GND
17	TX_6A
18	TX_6B
19	TX_7A
20	TX_7B
21	GND
22	TX_8A
23	TX_8B
24	TX_9A
25	TX_9B
26	GND
27	TX_10A
28	TX_10B
29	TX_11A
30	TX_11B
31	GND
32	TX_12A
33	TX_12B
34	TX_13A
35	TX_13B
36	GND
37	TX_14A
38	TX_14B
39	TX_15A
40	TX_15B
41	GND
42	Not Used
43	IO/SYNC0
44	IO/SYNC1
45	IO/SYNC2
46	IO/SYNC3
47	IO/SYNC4
48	IO/SYNC5
49	IO/SYNC6 / IRIG-B TTL
50	IO/SYNC7 / IRIG-B AM

Table 5-1: IO Connector Definition

5.2 IP Signal Connector Definition

The IP signal connector pin-out is given in the following table:

PIN #	Signal
1	GND
2	IP_CLK
3	IP_RESET*
4	IP_D0
5	IP_D1
6	IP_D2
7	IP_D3
8	IP_D4
9	IP_D5
10	IP_D6
11	IP_D7
12	IP_D8
13	IP_D9
14	IP_D10
15	IP_D11
16	IP_D12
17	IP_D13
18	IP_D14
19	IP_D15
20	IP_BS0*
21	IP_BS1*
22	- 12 V
23	+ 12 V
24	+ 5 V
25	GND
26	GND
27	+ 5 V
28	IP_R/W*
29	IP_IDSEL*
30	N.U.
31	IP_MEMSEL*
32	N.U.
33	N.U.
34	N.U.
35	IP_IOSEL*
36	IP_RESERVED
37	IP_A1
38	N.U.
39	IP_A2
40	IP_ERROR*
41	IP_A3
42	IP_INTREQ0*
43	IP_A4
44	N.U.
45	IP_A5
46	IP_STROBE*
47	IP_A6
48	IP_ACK*
49	IP_RESERVED
50	GND

N.U. = Not Used

Table 5-2: IP Connector Definition

5.3 Jumpers configuration

J3 is a shunt may be used to disconnect the IP_STROBE* signal to the IP module main controller. This permits to use the IPM429-E-16T-0R on a host board that does not support the IP_STROBE* feature or that has a definition for this signal that is not compatible with the IPM429-E-16T-0R.

J4, J5 and J6 are reserved for future use and shall not have a shunt installed on them.

6. SPECIFICATIONS

6.1 IP specifications

IPM429-E-16T-0R is fully compliant to the Industry Pack module single size type II mechanical specifications (See VITA 4-1995 Draft 1.0.d.0 April 7, 1995).

6.2 Environmental Specifications

Operation Temperature (natural convection)	0-55 º C -40-85 º C (I option)
Relative Humidity (non-condensing)	0-95%
Storage Temperature	-55 to 125 º C

Table 6-1: Environmental Specifications

6.3 Electrical Specifications

ARINC 429 input-output :

- Fully compliant, see Holt Hi-8585 and HI-8588 for detailed specification

IO Input characteristics :

- TTL compatible
- On board 10K pull-up to +5V
- Under/over shoot diode protection.

IO Output characteristics :

- TTL compatible
  - I_{OH} = +25 mA
  - I_{OL} = -25 mA
- Not current limited *

***WARNING:** Be careful not to switch to an output mode (see next section 3.4.11) if the IO pin is physically connected to another source of voltage (possibly intended for the IO in input mode).

Consumption :

+5V	31mA Full Tx bus loaded
+12V	240mA Full Tx bus loaded
-12V	235mA Full Tx bus loaded

Table 6-2: Electrical Specifications