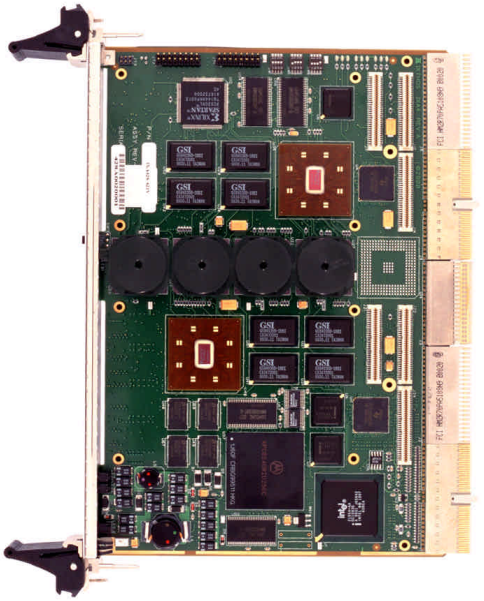
Compact CHAMP-AV

High Performance DSP with Concurrent Multi-Processing Architecture

Features

- Processors
  - Four MPC7400/7410 PowerPC™ processors with AltiVec ™ at 400–500 MHz
  - Over 16 GFLOPS peak floating point performance (Four G4's at 500MHz)
  - 200 MHz MPC8240 PowerPC core processor provides an additional 6.1 SPECint95
- Enhanced I/O
  - Support for two industry standard PMC I/O expansion modules, 5 V
  - Three 10/100 BaseTX Ethernet ports, compliant with PICMG 2.16
  - Supports up to 2.5 Gbps I/O with Switched Fabric Technology - PMC via front panel or rear panel (PICMG 2.17)
  - Advanced CHAMP (Common Heterogeneous Architecture for Multi-Processing) architecture allows for simultaneous transfers between (i) each PMC and dual 7400/7410 processors and (ii) the 8240 and the Compact PCI backplane
  - Bridges support up to 400 Mbytes/sec of cumulative, on-board, simultaneous I/O data movement
  - Six independent DMA controllers balance the DSP processing power with the I/O bandwidth, allowing for optimum application-specific trade-offs
  - Multi-channel interrupt multiplexer provides flexibility when controlling real-time processor-to-processor events
- Onboard Memory
  - Global SDRAM – 64 Mbytes, 64 bits wide, 100 MHz
  - Local SDRAM – 64 to 256 Mbytes per PowerPC pair, 64 bits wide, 100 MHz
  - L2 cache – 2 Mbytes per PowerPC
- Flash
  - 16 or 32 Mbytes
- Front Panel
  - Reset switch
  - Red System LED
  - Blue Hot Swap LED
  - 4 green user LED's
- Hot Swap support
- Software Support
  - VxWorks® BSP with Shared Memory Networking
  - IXLibs-AV optimized AltiVec DSP function library
  - IOPlus with SmartDMA embedded runtime kernel
  - IXAbsp O/S board support libraries
  - HostAPI utilities



Overview

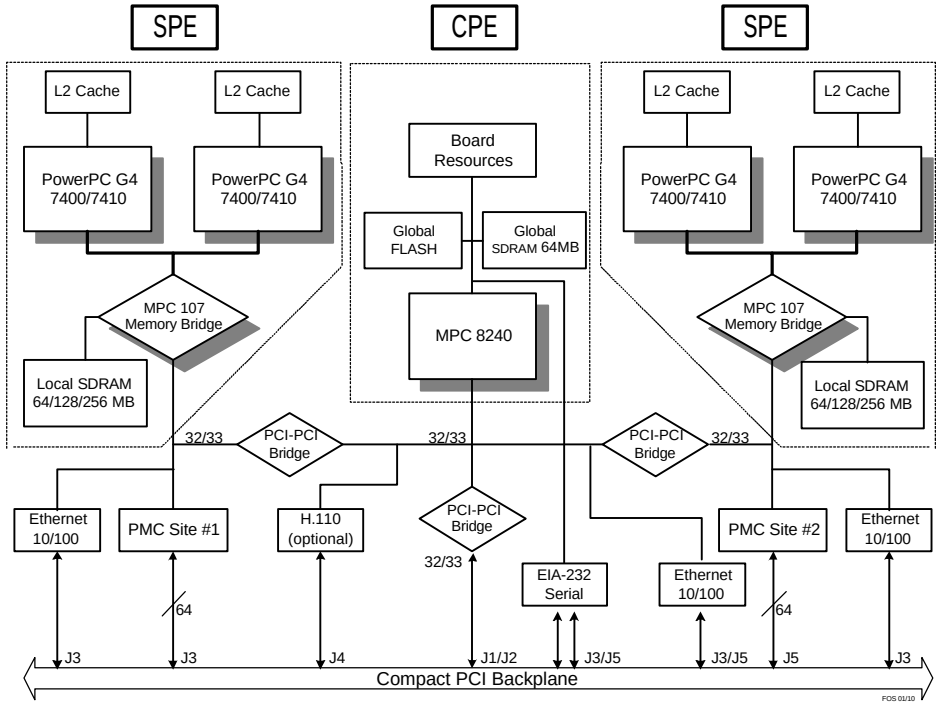
The Compact CHAMP-AV is the latest Dy4 Systems offering in the growing line of high-performance Digital Signal Processing (DSP) solutions. The Compact CHAMP-AV provides over 16 GFLOPS of floating point performance in a single Compact PCI slot. Supporting various high speed/high performance versions of the PowerPC™ G4 (with AltiVec™) microprocessors from Motorola®, the Compact CHAMP-AV is ideal for a diverse range of real-time signal processing applications. The Compact CHAMP-AV architecture supports two industry-standard PCI-based Mezzanine Cards (PMCs) providing a flexible and powerful I/O architecture that enables very high throughput.

The heart of the Compact CHAMP-AV is its advanced, optimized data flow architecture (see Figure 1). The Compact CHAMP-AV board is segmented into three isolated 32-bit, 33MHz PCI bus sections allowing the PowerPC processor (MPC8240) access to the Compact PCI bus concurrently with I/O data transfer operations between each dual 7400/7410 G4 Signal Processing Element (SPE) and its associated PMC site. The internal 32-bit/33 MHz PCI bridges allow concurrent and efficient data transfers between the independent DSP Signal Processing Elements (SPEs) and the PCI bus sections. The embedded MPC8240 Control Processing Element (CPE) has access to the Compact PCI bus, PMC I/O sites, and each SPE's local memory, allowing for flexible, free data flow and real-time control path implementations.

Every real time system requires a high bandwidth, low latency I/O mechanism to move data on and off the board. The Compact CHAMP-AV can accomplish this with it's included I/O ports via the rear panel connectors, and also through the use of industry standard PMC modules. Connectivity through the backplane includes three 10/100 Mbps Ethernet interfaces, two EIA-232 serial ports and PMC routing for a standard 2.5 Gbps Switched Fabric interface. Additionally there is an optional ECTF H.110 Computer Telephony interface which can handle up to 4096 simultaneous voice channels. The PMC sites can also be used to support Fibre channel, digital radio, Gigabit Ethernet, and A/D or D/A interfaces. The PMC I/O is accessible through a front panel connection or through the 64 user I/O pins provided on the J3/J5 connectors, all of which are routed to the rear panel. By leveraging PMC technology, the Compact CHAMP-AV is ideally suited for highly reliable, demanding, high data throughput telecommunications, multimedia broadband server/router, smart antenna, Voice-over-IP, Radar and Sonar applications.

Dy 4 Systems provides a comprehensive suite of software development and debug tools, signal processing libraries, and real-time operating systems, including VxWorks/Tornado from Wind River.

Figure 1: Compact CHAMP-AV block diagram



The CHAMP Architecture

The Compact CHAMP-AV supports the Dy 4 Common Heterogeneous Architecture for Multi-Processing (CHAMP). The CHAMP architecture (see Figure 2) organizes the processing resources as two independent clusters of Signal Processor Elements (SPE's), each with the ability to have dedicated access to its PMC module for tightly coupled I/O resources. PCI-to-PCI isolation bridges allow for concurrent data movement on each isolated section of the PCI bus. The CHAMP architecture allows each processing cluster to perform I/O operations to its PMC module independently of other on-board data transfer operations. The MPC8240 embedded processor is also capable of performing I/O operations concurrently with the DSP clusters. The isolated triple PCI bus organization allows for up to 400 Mbytes/sec peak cumulative data transfer throughput.

Digital Signal Processors

The Compact CHAMP-AV may be equipped with either two or four G4 PowerPC processors, which form the heart of the Signal Processing Elements. The board supports either MPC7400 or MPC7410 processors (400 and 500 MHz). Every processor has access to all memory and I/O resources on the board including local SDRAM arrays, global SDRAM, PMC sites and the Compact PCI bus. This simplifies programming as there are no restrictions on where application functions reside.

DSP Memory

The Compact CHAMP-AV utilizes fast Synchronous Burst SRAM (SBSRAM) for the backside L2 cache and Synchronous DRAM (SDRAM) for local cluster memory. The SBSRAM interface supports up to 2 Mbytes of L2 cache memory per processor. The local SDRAM supports 64 to 256 Mbytes per SPE node with 100 MHz SDRAM speeds.

Independent I/O Processor

The Compact CHAMP-AV is equipped with a Core Processing Element (CPE) comprised of an MPC8240 integrated embedded processor/bridge device to handle I/O and general processing applications.

Running at 200 MHz, the MPC8240 provides 6.1 SPECint95 of computing performance. The MPC8240 can access up to 64 Mbytes of SDRAM, which may be used for I/O operations, data buffering, or general processing requirements. The board contains up to 32 Mbytes of on-board, user-programmable Flash.

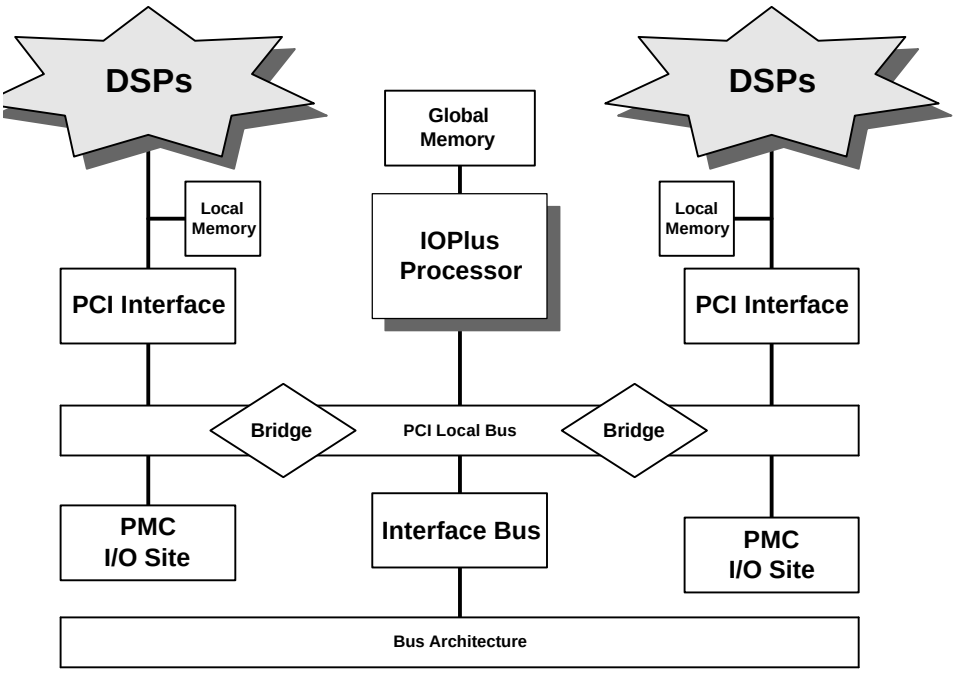
The MPC8240 may be used in either of two ways, embedded or user-programmed. When functioning as an embedded processor, the 8240 executes Dy4's SmartDMA firmware to provide data movement services independently of the G4 processors. SmartDMA works by utilizing the DMA controllers within the 8240. A DSP application can send command messages to the SmartDMA firmware by using the supplied interface library. (This is part of the IXATools software suite.) SmartDMA can move data between any of the on-board memories, and also between memory and the Compact PCI bus.

The other option is for the user to develop custom software to run on the 8240. This mode is fully supported with a VxWorks BSP (optional). This method affords the user the flexibility and power of isolating DSP tasks to the G4's, and keeping all I/O software running on the 8240. This can simplify the design of the DSP software, as it is not subject to asynchronous interrupts needed to service I/O devices. This is particularly relevant when special-purpose PMC cards are employed.

DMA Controllers

A key aspect of maximizing the performance of a DSP application is to make optimum use of the various data buses on the card, so that data processing is balanced with data movement. The Compact CHAMP-AV utilizes six independent DMA controllers to move data on or off the board, or between processor memories while the processors themselves are involved in other tasks. This enhances the performance of the Compact CHAMP-AV by allowing processor CPU cycles to be used to process data rather than moving data around the board. Each MPC107 PCI-PowerPC bridge provides two DMA engines, which operate in single or chained modes, and the 8240 processor contains two more DMA engines.

Figure 2: The CHAMP Architecture



PMC Sites

The Compact CHAMP-AV is equipped with two fully independent IEEE 1386.1 D2.0/VITA 32 D0.21 compatible PMC/PPMC sites. The PMC interfaces support 32-bit, 33MHz transfers to their associated pair of G4 processors. I/O is supported on both the front panel as well as through the rear panel. 64 bits from each PMC are routed to the J3 and J5 connectors. The rear-panel interface supports both single-ended and high-speed Low Voltage Differential Signaling (LVDS) for implementing PICMG 2.17 switched fabric networks.

The two PMC sites provide industry-standard I/O mezzanine expansion for system developers. A large variety of standard modules are available from dozens of third parties to provide I/O, memory and processing expansion. PMCs can be used to provide interfaces such as Fibre channel, Gigabit Ethernet, Switched Fabric, digital receiver, graphics, A/D, D/A, and proprietary interfaces.

Through Dy 4's Embedded Partners Program, Dy 4 offers a number of pre-configured PMC I/O system solutions ideal for telecom I/O, digital radio, sonar, radar, and high speed serial interconnect and fabric applications. Contact Dy 4 for assistance and suggestions in configuring other compatible PMC modules.

Inter-processor Messaging Interrupts

A multi-processor application needs to coordinate events between processors. The Compact CHAMP-AV provides a mechanism to configure the hardware to suit any software/dataflow methodology. This is done with a sophisticated, multi-channel interrupt multiplexer that services interrupts from many on-board and off-board sources and, under software control, routes them to each of the four PowerPCs and the MPC8240. This allows interrupt sources from the Compact PCI bus, PowerPCs, PMCs and other sources to be individually routed to the PowerPC's and the MPC8240. Two input signals are provided on the J3/J5 connectors to accept interrupts from external sources.

Compact PCI Bus Interface

The Compact CHAMP-AV is equipped with a 32-bit, 33 MHz Hot Swap compliant Compact PCI bus interface. The interface is designed as a peripheral interface, meaning that it must reside in a chassis that contains a Compact PCI System Controller board. The board is fully compliant with the Compact PCI Core Specification (PICMG 2.0) and the Hot Swap Specification (PICMG 2.1).

The Compact PCI interface is supported on J1 and J2. (J2 is used only for power.) J3, J4 and J5 are defined as user I/O. The PCI Industrial Computer Manufacturer's Group (PICMG) is the consortium that defines and publishes specifications related to Compact PCI. They have defined several specifications that use the J3 through J5 connectors. The Compact CHAMP-AV supports an optional H.110 Computer Telephony interface on J4 (PICMG 2.5) and the Compact PCI Packet Switching Backplane interface on J3 (PICMG 2.16). Through the use of a StarFabric PMC, J3 also supports the basic node configuration (two links) defined in PICMG 2.17.

The Compact CHAMP-AV draws both 5 V and 3.3 V power from the Compact PCI backplane. Advanced on-board power management circuitry isolates input power until both the 3.3V and 5V power rails stabilize within proper tolerances upon system power up. This ensures proper power sequencing protection for all on-board devices and eliminates the requirements for sequencing or synchronizing within the system power-supply.

Ethernet Interfaces

The Compact CHAMP-AV provides three IEEE 802.3-compliant 10BASE-T/100BASE-TX Ethernet interfaces, implemented with Intel 82559ER controllers. The Ethernet controllers are distributed among the three PCI segments of the board. See Figure 1. The interfaces are presented on the J3 and J5 connectors. An optional rear transition module is available which provides three standard RJ-45 connectors to access the Ethernet ports. The card is also compliant with the PICMG 2.16 Packet Switching Backplane specification. There are corresponding backplanes and Ethernet switches available from other industry suppliers, that permit systems to be easily constructed that are networked together with Ethernet.

EIA-232 Serial Ports

Two EIA-232 serial ports are accessible on the J3/J5 connectors. The serial ports are implemented with an Exar 16C2550 UART. The device supports asynchronous communication at baud rates between 50 baud and 115.2 Kbaud. The baud rate of each port can be set independently. Each port provides Tx, Rx, CTS, RTS and DCD signals. The UART is accessed from the 8240 processor. The software interface to the serial ports is normally through an operating system BSP, which should be referenced to determine the supported modes of operation, baud rates etc.

Software Support

The Compact CHAMP-AV is supported with an extensive array of software items, which cover all facets of developing application code for the board.

- A VxWorks Board Support Package (BSP) is available that supports both the 8240 and 7400/7410 processors. Users have the option of using VxWorks on the 8240 alone, or on all five processors. The VxWorks BSP supports development of multi-tasking, AltiVec-enabled applications using either Tonado 2.0 or 2.1. The BSP also supports VxWorks Shared Memory Networking. This allows the user to share a single network connection between multiple processors on one or many boards. In development, users can connect to a single Ethernet port and then make TCP/IP connections to any processor in the system. An extension of this concept is that multiple software developers can share one connection into a rack of DSP cards and independently debug application code. For deployed systems, the shared network is especially beneficial, as only a single Ethernet port must be cabled in the chassis to support in-system upgrades of software. The VxWorks BSP is delivered as part of the IXATools software suite. See the IXATools data sheet for detailed information.
- IXLibs-AV is a library of fully optimized DSP functions that take advantage of the AltiVec instruction unit. By using IXLibs-AV the user is spared the complexity of programming the AltiVec instruction unit. For customers with AltiVec expertise, the library includes assembly language macros and an open vector data storage format to support mixed user and library functions in an application. See the IXLibs-AV data sheet for detailed information.
- The Board Resource Library contains C functions to access both hardware and software features of the Compact CHAMP-AV, including interrupts, semaphores, the Compact PCI backplane, SmartDMA functions, Flash, and indicator LED's. The Board Resource Library is self-contained code that be can used without an operating system, or it can be used with VxWorks.
- The IOPlus software runs on the 8240 to provide the SmartDMA capability, which allows the G4's to command the 8240 to perform data movement operations. The IOPlus software is delivered as firmware for the 8240, and as a linkable library for users writing applications for the 8240. The IOPlus firmware also includes power-on diagnostics.
- The Board Configuration Utility is a Windows-based program that is used to program the on-board Flash EPROM with configuration parameters and user application software.
- The HostAPI library is a set of functions that may be used on a Single Board Computer that is co-resident on the Compact PCI bus with Compact CHAMP-AV DSP cards. It provides functions to remotely load and start programs, check status, and program the Compact CHAMP-AV on-board Flash. Contact Dy4 for a list of supported SBCs.

The Compact CHAMP-AV also supports the use of EST JTAG emulators to provide JTAG connections to the 8240 and the 7400/7410 processors for code development.

Options

Rear Transition Module

The following are optional items that are available for use with the Compact CHAMP-AV.

- A Rear Transition Module (RTM) is available to provide standard connectors for the on-board interfaces which exit the backplane connectors. The RTM inserts into the backside of a Compact PCI mid-plane chassis. The Compact CHAMP-AV RTM has three RJ-45 modular jacks for direct connections to the three Ethernet ports, two DB-9 serial port connectors and a pair of high-density I/O connectors for the 64 I/O signals from each of the two PMCs.

Specifications

Table 1: Specifcations

DIMENSIONS	
Height: 233.4 mm (9.2 in)	Depth: 160.0 mm (6.3 in)
Front Panel Height: 261.8 mm (10.3 in)	Width: 19.8 mm (.8 in)
POWER REQUIREMENTS	
5V	6.2 A typical *
3.3V	3 A typical
+12V	Not used by the base card, routed to the PMC sites
-12V	Not used by the base card, routed to the PMC sites
ENVIRONMENTAL	
Operating Temperature: 0C to +55C;	Non operating: -40C to +85C)
Operating Altitude: 5,000 m;	Non operating: 15,000 m
Operating Humidity (NC): 10% to 80%	Non operating: 10% to 90%

* detailed power consumption characterization report available

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