Advance Data Sheet
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microelectronics group

Lucent Technologies
Bell Labs Innovations

Ambassador™ T8100A, T8102, and T8105 H.100/H.110 Interfaces and Time-Slot Interchangers

1 Product Overview

1.1 Features

- Complete solution for interfacing board-level circuitry to the H.100 telephony bus
- H.100 compliant interface; all mandatory signals
- Programmable connections to any of the 4096 time slots on the H.100 bus
- Up to 16 local serial inputs and 16 local serial outputs, programmable for 2.048 Mbits/s, 4.096 Mbits/s, and 8.192 Mbits/s operation per CHI specifications
- Programmable switching between local time slots, up to 1024 connections
- Subrate switching of nibbles, dibits, or bits
- Backward compatible to T8100 through software
- Programmable switching between local time slots and H.100 bus, up to 512 (T8102, T8105 only) connections
- Choice of frame integrity or minimum latency switching on a per-time-slot basis
  — Frame integrity to ensure proper switching of wideband data
  — Minimum latency switching to reduce delay in voice channels
- On-chip phase-locked loop (PLL) for H.100, *MVIP**, or SC-Bus clock operation in master or slave clock modes
- Serial TDM bus rate and format conversion between most standard buses
- Optional 8-bit parallel input and/or 8-bit parallel output for local TDM interfaces
- High-performance microprocessor interface
  — Provides access to device configuration registers and to time-slot data
  — Supports both *Motorola*† nonmultiplexed and *Intel*‡ multiplexed/nonmultiplexed modes
- Two independently programmable groups of up to 12 framing signals each
- Devices available in 0.25 micron technology
- 3.3 V supply with 5 V tolerant inputs and TTL-compatible outputs
- Boundary-scan testing support
- 208-pin, plastic SQFP package
- 217-ball BGA package (industrial temperature range)

1.2 Description

These products in the *Ambassador* T8100 family provide a complete time-slot switch and an interface for the H.100/H.110 time-division multiplexed (TDM) buses. The T8100 family includes devices with hierarchical switching as well as a capacity of up to 512 local to H.100 connections. The hierarchical switching allows up to 1024 local connections without using H.100 bus bandwidth. The family also includes the T8102 device for a low-cost solution in nonhierarchical systems.

All three TSI chips are backward compatible with the bus standards *MVIP*-90 and *Dialogic*'s§ SC-Bus, as well as supporting the newer standards, H-*MVIP* and ECTF H.100. Other features include a built-in PLL for H.100, *MVIP*, or SC-Bus clock operation in master or slave clock modes and two independently programmable groups of up to 12 framing signals each. Packaged in both a 208-pin SQFP and a 217-ball BGA, the T8100 TSI devices provide an economic solution for the computer telephony market.

* *MVIP* is a registered trademark of GO-MVIP, Inc.
† *Motorola* is a registered trademark of Motorola, Inc.
‡ *Intel* is a registered trademark of Intel Corporation.
§ *Dialogic* is a registered trademark of Dialogic Corporation.