SYCARD TECHNOLOGY

# *CF test 222*

## *Technical Reference Manual*

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*Preliminary*

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# 1. Introduction

The CF test 222 is designed to provide manufacturers of CompactFlash based hosts a quick method of testing and verifying the operation of the CompactFlash sockets.

The CF test is enclosed in a standard 3.3mm thick card that plugs into a standard CompactFlash socket. The board is designed for both automated GO/NO-GO testing and component level debug. Test software is required on the host system.

A custom ASIC is the core of the CF test 222. All testing logic is contained in this ASIC. The CF test contains an on-board A/D to provide accurate measurement of Vcc voltages.

Sycard Technology provides a DOS application to test Intel 82365SL compatible socket controllers. Simple command line invocation allows tests to be embedded into batch test files. OEMs that wish to use the CF test on a non-DOS platform can use this specification to develop custom test applications.

## 1.1 Differences between the CF test 222 and the CF test 220

Although the CF test 220 and the 222 appear to be the same, there are slight differences that make the model 222 suitable for certain applications. The CF test 222 was created to solve a problem with socket controllers that do not support 8 bit I/O windows (e.g. StrongArm SA-1100). On power-up the CF test 220 and 222 will put the WP/IOIS16# signal into a low state. Socket controllers that do not support 8 bit windows will use the IOIS16# signal to determine if the register is 16-bit or 8-bit. These socket controllers will not be able to access the odd numbered registers in the CF test 220. Since the control of the WP/IOIS16# is located in an odd numbered register (in the CF test 220) it is impossible to put the card into 8-bit mode. The CF test 222 solves this problem by placing the WP/IOIS16# control in an even numbered register. Table 1.1-1 illustrates the differences between the CF test 220 and 222.

| Control Bit | CF test 220 | CF test 222 |
|---|---|---|
| WP/IOIS16# | MISC Register (offset 3) bit 6 | CNTL Register (offset 4) bit 0 |
| RDY/BSY/IREQ# | MISC Register (offset 3) bit 7 | CNTL Register (offset 4) bit 1 |
| ADCCE | CNTL Register (offset 4) bit 0 | MISC Register (offset 3) bit 6 |
| ADCLK | CNTL Register (offset 4) bit 1 | MISC Register (offset 3) bit 7 |

**Table 1.1-1 CF test 220 and 222 differences**

In addition to register changes, the CF test 222 CIS (tuples) have been modified to identify the model. See appendix B for the tuple listing.

# 2.0 Architecture of the CF test

Figure 2.0-1 Illustrates the architecture of the CF test model 222. The functional blocks can be partitioned into the following major sub-sections:

- Tester ASIC (Test ASIC)
- A/D Converter and Logic

All interface to the CF test unit are via eight registers contained in the test ASIC. These eight registers control the various test functions contained within the CF test unit. The location at which these registers are accessed depends on which mode the CF test unit is in. On power-up, these test registers are located in attribute memory space. The test software can then enable I/O and/or common memory modes to test the various access modes of the CompactFlash interface.

There are two major types of tests performed by the CF test unit, those implemented by the Test ASIC and the A/D tests. The Test ASIC based tests are designed to test the basic functionality of the interface. These tests will verify the basic operation of the interface including access strobes, data bus and address bus. Once these basic access modes are verified, the A/D test verifies the Vcc and Vpp levels.

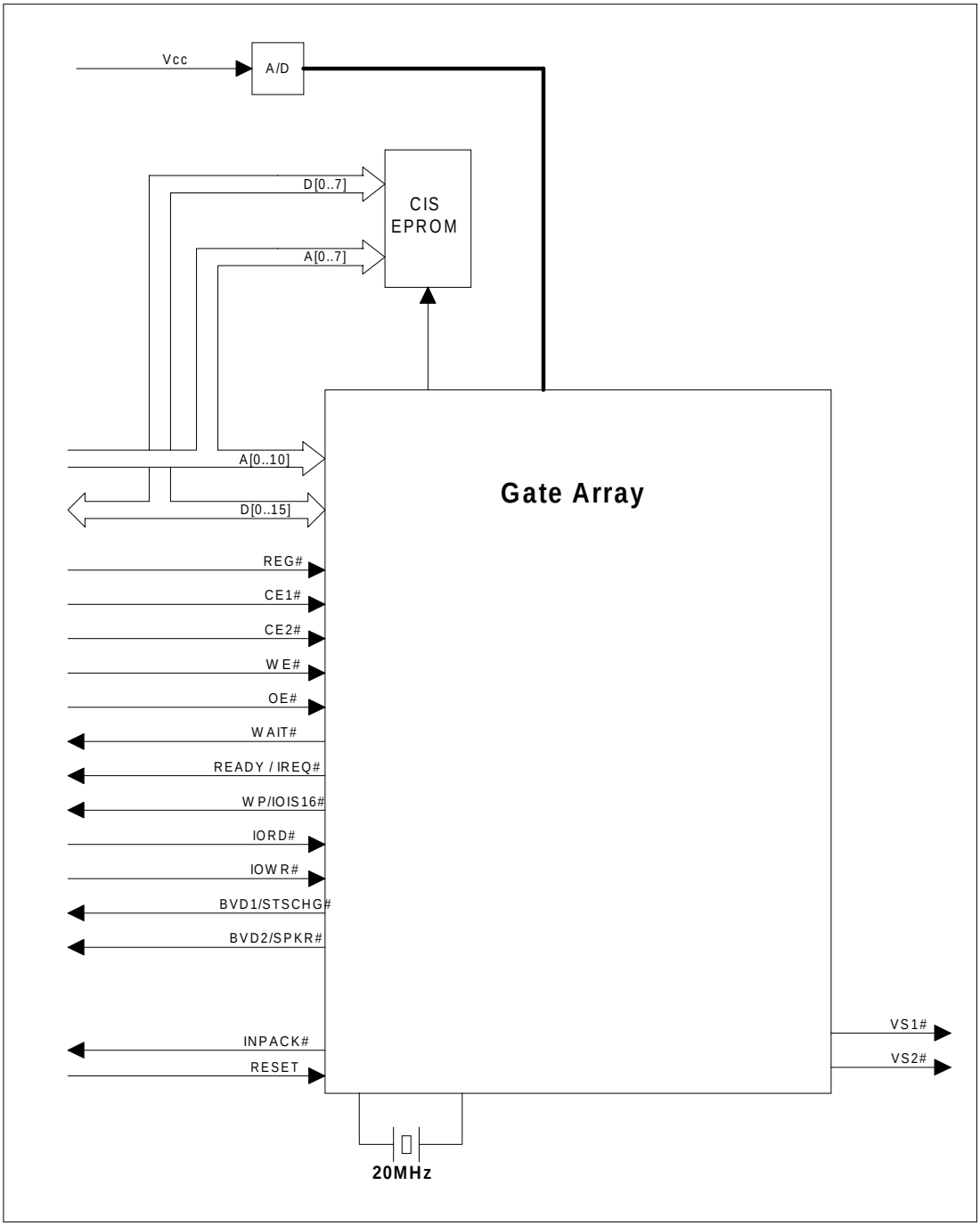



**Figure 2.0-1 CF test 222 block diagram**

# *3.0 Testing the CompactFlash Interface*

Most of the basic interface tests are handled in the Test ASIC. Eight registers control the operation of the Test ASIC. Appendix A lists the Test ASIC's register description. Note that most write registers cannot be read back. It is up to the programmer to maintain an image of the write registers, since a read/modify/write operation is not possible for most of the register bits. Testing the CompactFlash interface involves writing various test patterns to the CF test unit through the host socket controller. Status read back through these registers verify the functionality of the various portions of the interface.

## *3.1 Initializing the CF test*

The CF test must be powered through the host socket before any test operations can begin. The CF test model 222 can be powered to 3.3 or 5.0 Volts. All CF test units require a power-on reset to initialize the internal operating circuitry. Care must be taken when switching operating voltages on the CF test . Do not switch from 3.3V to 5.0V or 5.0V to 3.3V without allowing the power to go to first to 0V. The CF test on-board circuitry requires a minimum of 1200ms after Vcc is stable to initialize.

## *3.2 Opening a Memory and I/O Window to the CF test*

In order to access the test resources in the CF test an 8-bit attribute memory and an 8-bit I/O window must be opened to the CF test . Both an I/O and memory window are required to fully test the CompactFlash interface. The CF test contains eight 8-bit registers. These registers are accessed as 8 consecutive bytes.

***Note**: For information on opening an I/O window, consult your socket controller chip user's manual.*

A memory window with a length of at least 8 bytes is required to test the interface's memory interface. Most socket controllers provide a minimum window length of 4K bytes.

### *3.2.1 CF test Memory and I/O Map*

The CF test 222 supports all three address spaces defined in the CompactFlash Specification. On power-up the CF test 222 responds to attribute memory accesses. Attribute memory reads from address 0H-FFH access the on-board Card Information Structure (CIS). The CIS contains tuples that identify the CF test 222. Appendix B contains a listing of the tuples contained in the CIS. Attribute Memory addresses 100H-107H contains the control registers used to test the CompactFlash Interface. The function of these registers are described in Appendix A.

| Attribute Space | Description |
|---|---|
| 0H – 0FFH | Card Information Structure |
| 100H – 107H | Control Registers |
| 108H-3FFH | Control Registers (mirrored) |

**Table 3.2-1 Attribute Memory Space**

The MODE register (offset 6) controls, which address spaces the CF test responds to. Once the CF test unit it programmed out of its power-on mode, the control registers are accessed through I/O or common memory space. When accessing these registers in I/O or common memory mode these registers appear at offset 0. Since there is no address decode for common memory or I/O mode, these registers are accessible on any 8-bit boundary. The following table describes the various CF test modes.

| MODE.2 | MODE.1 | MODE.0 | CF test Mode | CF test operating mode |
|---|---|---|---|---|
| 0 | 0 | 0 | MODE 0 | Attribute memory space enabled, I/O and common memory accesses disabled |
| 0 | 0 | 1 | MODE 1 | I/O space enabled, attribute and common memory space disabled |
| 0 | 1 | 0 | MODE 2 | I/O space at 1F0H-1F7H enabled, attribute and common memory space disabled |
| 0 | 1 | 1 | MODE 3 | I/O space at 170H-177H enabled, attribute and common memory space disabled |
| 1 | 0 | 0 | MODE 4 | Common memory and attribute space enabled, I/O space disabled |
| 1 | 0 | 1 | MODE 5 | Common memory and I/O space enabled. Attribute space disabled. |

**Table 3.2-2 CF test modes accessed through MODE register**

***Note**: Once the Mode 1,2,3 or 5 is enabled, all access to attribute memory space is disabled. Access to the CF test 's internal registers should be made through the enabled memory or I/O space.*

***Note**: The RESET signal will NOT put the CF test into its power-on state. To reset the CF test unit, cycle power to the slot.*

## *3.3 Preliminary Tests*

Before accessing the CF test hardware, the test software should verify the basic operation of the socket controller and that the CF test is properly inserted into the socket. This will avoid any unnecessary delays or erroneous error messages.

1. Verify that socket controller is present by executing a simple register test.
2. Power-up socket.
3. Verify that the socket controller has powered up the slot (through the socket controller status)
4. Wait 1200ms for CF test to initialize.
5. Verify that card detects are active (CD1# and CD2# are low)

If any of these tests fail, further testing is not possible.

## *3.4 Basic Tests*

Once the socket controller has been verified and card detects are active, the CF test 's functions can be accessed. This part of the test procedure verifies the basic read/write operation of the card. If any failures are detected in the basic test, more advanced tests may return erroneous results. In order to run the first set of tests, an attribute memory window to the card must be opened.

a. Read the CIS and compare with values contained in Appendix B.
a. Basic 8-bit attribute memory read/write to the DATALO register - Verify basic 8 bit memory read.
b. Basic 16-bit attribute memory read/write to the DATALO/DATAHI register - Verify basic 16 bit memory read.

Once these tests pass, further more detailed tests can be run.

*Note: Basic 8-bit operation of the CF test requires the following signals to be working:*

D[7:0]
OE#
WE#
CE1#
A[2:0]

## *3.5 Data Tests*

The CompactFlash data bus may be tested through several methods. When the CF test 222 is in MODE 0 the host writes data to the data latches DATALO at attribute memory offset 100H or DATAHI at 101H. Both 8 and 16 bit accesses are allowed. Data is latched into these registers on an attribute memory write to the DATALO and DATAHI registers. Once data is written, it can be read back to verify that all data bits that have been written are correct.

The data pattern test can be run via I/O or common memory accesses. The test software must enable I/O or common memory accesses via the MODE register at offset 106H. See table 3.2-2 for the valid modes. Data pattern tests can be run through attribute memory, common memory or I/O space depending on the setting of the MODE register. Common and attribute memory data pattern tests can be accomplished by accessing the same DATALO and DATAHI registers starting at offset 0 in I/O or common memory space. After a power-on reset the CF test is reset to Mode 0 and the can be accessed through the attribute memory space only.

Prior to running the data test, the lower 8 bits of the data bus can be verified by reading the CIS data. A listing of the CIS is contained in Appendix B.

## *3.6 Address and REG# Tests*

Writing various address patterns to the CF test unit can test the CompactFlash 11-bit address bus. All address bits can be latched and read through the CompactFlash host interface. The address latching circuit must be armed prior to the access that triggers the latching circuitry. Addresses are latched on the falling edge of the control strobes, WE#, OE#, IORD#, or IOWR#.

***Note**: The latching signal is a logical OR of the OE#, WE#, IORD# and IOWR# strobes qualified by either CE1# or CE2#.*

Arming of the address latches is accomplished through the ALAT bit in CNTL register (offset 4). A low to high transition of this bit will arm the latch. Any access after this arm will result in the latching of all 11 address signals on the interface. The following C code is used to arm the address latch:

```
outportb(tester_addr+4,reg4_image & 0xfb);
outportb(tester_addr+4,reg4_image | 0x04);
```

The latched values of the address and REG- signal may be read directly from the registers

| Signal | Register | Offset | Description |
|---|---|---|---|
| A[7:0] | LADDRLO | 4 | A0-A7 |
| A[10:8] | LADDMID | 5 | A8-A10 |
| CE1# | STBLAT.2 | 7 | Latched CE1# |
| CE2# | STBLAT.3 | 7 | Latched CE2# |
| OE# | STBLAT.0 | 7 | Latched OE# |
| WE# | STBLAT.1 | 7 | Latched WE# |
| IORD# | STBLAT.4 | 7 | Latched IORD# |
| IOWR# | STBLAT.5 | 7 | Latched IOWR# |
| REG# | LATMISC.5 | 3 | Attribute Memory Select |

**Table 3.6-1 Address Latch Locations**

The following procedure is used to latch the address and read the data from the address latches to create a 11-bit address.

1. Clear the ALAT bit in CNTL register at offset 4.
2. Set the ALAT bit in the CNTL register. The address latch is now armed.
3. Access the card with IORD#, IOWR#, OE# or WE# strobe. The address of the access is latched on the falling edge of the strobe.
4. Read the lower 8 bits A[7:0] from the LADDRLO register at offset 4.
5. Read the contents of the A[10:8] latch from the LADDMID register at offset 5.
6. Read the contents of the REG# latch from the LATMISC register at offset 3.
7. Read the contents of the CE1#, CE2#, WE#,OE#, IORD# and IOWR# latch from the STBLAT register at offset 7.

## *3.7 Timing Measurements*

The CF test provides a flexible timing measurement circuit providing 50ns resolution. This circuit can measure from the rising/falling edge of any of the control strobes to the rising falling edge of the same set of signals. The following table lists the various control strobes that can be measured:

| Signal | Description | TCR Value |
|---|---|---|
| OE# | Memory Read Strobe | 08H |
| WE# | Memory Write Strobe | 19H |
| IORD# | I/O Read Strobe | 6EH |
| IOWR# | I/O Write Strobe | 7FH |
| CE1# | Chip Enable 1 | 2AH |
| CE2# | Chip Enable 2 | 3BH |

**Table 3.7-1 Common Strobe Measurements TCR Values**

The signal and polarity that start the timer is selected via the STR[2:0] and the STRPOL bits in the TCR register. The STP[2:0] and STPPOL bits determine the signal that stops the timer. The following examples illustrate the values programmed into the TCR register (offset 2) for various timing measurements:

| Timing Measurement | TCR Value |
|---|---|
| Falling edge of CE1# to rising edge of OE# | A0H |
| Pulse width of IORD# | 6EH |
| Pulse width of IOWR# | 7FH |
| Rising edge of CE1# to rising edge of OE# | 20H |
| Pulse width of WE# | 19H |

**Table 3.7-2 Various Strobe Measurements TCR Values**

As with the address latching circuit, the timing logic is armed and the next access to the card is measured. The timing measurement is armed through an I/O write to the TRST register (offset 5). Once armed, the timer will start on first instance of the value programmed into the STR[2:0] register. The value can be read from the TIM register (offset 6). The value read from the TIM register is multiplied by the sample rate (50ns) to obtain the strobe width.

## *3.8 Testing RESET*

The RESET signal is an input to the CF test unit. RESET is only monitored by the CF test and will not reset the CF test. The current state of the RESET signal can be read from RESET bit in the LATMISC register (offset 3, bit 4). Testing of RESET involves forcing the state of RESET and reading the status in the LATMISC register.

In some socket controllers when RESET is asserted, the CompactFlash interface is tri-stated or disabled. In systems such as these, the previously described method of testing RESET will not work. With socket controllers such as these, the CF test 222 contains a RESET latch that stores the fact that a transition occurred RESET. The status of this latch can be read from LRESET bit in the STBLAT register (offset 7 bit 7). This latch is armed by setting, then clearing, the CLR_RST bit the CNTL register (offset 4 bit 4). Once the reset latch is armed the test software will then strobe the RESET signal from high to low. The latch will capture the low to high transition of the reset signal. Software can verify this by reading the LRESET bit in the STBLAT register

## *3.9 INPACK# Tests*

CF test can generate INPACK# on all I/O reads. Most socket controllers can use INPACK# to gate the CompactFlash data on to the host system data bus. Setting the INPKEN bit in the CNTL control register (offset 4 bit 3) enables INPACK# generation on all I/O reads.

## *3.10 Testing WAIT#*

A programmable wait state generator is used to generate wait states to simulate slow I/O or memory devices. The wait state generator is capable of generating wait states up to 3160ns. This covers the full range of CompactFlash access times. Used in conjunction with the pulse measuring circuits, this can result in accurate measurement of read/write strobe widths. Timing for the wait state generator is based on the CF test ’s main crystal (20Mhz).

The wait state generator is accessed through WAIT[0:2] bits in the MISC control register at offset 3 bits [0:2]. In addition to the WAIT[0:2] bits, the WAITEN bit at offset 3 bit 3 must be set to enable wait states.

| WAIT2 | WAIT1 | WAIT0 | Time in ns |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 50 |
| 0 | 1 | 0 | 100 |
| 0 | 1 | 1 | 200 |
| 1 | 0 | 0 | 400 |
| 1 | 0 | 1 | 800 |
| 1 | 1 | 0 | 1650 |
| 1 | 1 | 1 | 3160 |

**Table 3.10-1 Wait state delays**

## *3.11 Testing BVD1 and BVD2*

The BVD1 and BVD2 signal are outputs from the CF test card. They are implemented as parallel port bits in the CNTL register at offset 4. The host software writes various patterns to these bits and verifies continuity by checking the state of these bits through the socket controller's status registers. There are four bits used to control the BVD1 and BVD2 outputs. BVD1_EN# and BVD2_EN# must be set to 0 to enable the BVD1 and BVD2 tri-state outputs. The BVD1_OUT and BVD2_OUT bits control the state of the corresponding outputs.

## *3.12 Testing Ready and WP*

The RDY/BSY/IREQ# and WP/IOIS16# signal are outputs from the CF test card. They are implemented as parallel port bits in the CNTL register (offset 4, bits 0 and 1). The host software writes various patterns to these bits and verifies continuity by reading the status through the socket controller's status registers.

## *3.13 Testing Card Interrupts*

1. De-assert IREQ# by clearing RDY/BSY/IREQ# bit in MISC register (offset 4 bit 1).
2. Configure interrupt routing in host socket controller for desired interrupt.
3. Insert interrupt handler for desired interrupt.
4. Assert interrupt by setting RDY/BSY/IREQ# bit in MISC register (offset 4 bit 1).
5. Interrupt Service routine clears RDY/BSY/IREQ# bit to disable interrupt.
6. Disable interrupt routing in host socket controller.

## *3.14 Testing Status Change (STSCHG#) Interrupts*

1. Enable the BVD1 output by clearing BVD1_EN# in the CNTL register (offset 4 bit 4).
2. De-assert STSCHG# by setting BVD1(STSCHG#) bit in CNTL register (offset 4 bit 5).
3. Configure interrupt routing in host socket controller for desired interrupt.
4. Insert interrupt handler for desired interrupt.
5. Clear BVD1(STSCHG#) bit in CNTL register (offset 4 bit 5).
6. Interrupt Service routine sets BVD1(STSCHG#) bit to disable interrupt.
7. Disable interrupt routing in host socket controller.

## *3.15 Testing Voltage Sense (VS1# and VS2#)*

The CF test model 222 support testing of the VS1# and VS2# signals. On card initialization, VS1# and VS2# are both set inactive (high). VS1# and VS2# can be independently forced active (low) through the TCR register at offset 2. VS1# can be forced active (low) by setting STP[2:0] equal to 101. VS2# can be forced active (low) by setting STR[2:0] to 101. The test software is required to verify the state of VS1# and VS2# through the host controller’s status registers.

## *3.16 Speaker (SPKR#) Testing*

The CompactFlash's digital audio output (SPKR#) can be tested by enabling the host socket controller's speaker out signal. The host test software can then toggle the BVD2_OUT bit (offset 4, bit 2) at an audible frequency to verify the signal path between the CF test and the systems audio subsystem. In addition, the BVD2_EN# control (offset 4, bit 6) must be low to enable the SPKR# output. The test software is responsible for enabling the host socket controller's speaker output pin and any other hardware required to enable the speaker drivers.

## *3.17 Identifying the CF test*

Test software can identify that a CF test unit has been inserted by reading the Card Information Structure (CIS). The CIS contains an ID string identifying the CF test along with the version of CF test hardware. Appendix B contains a listing of the CF test 's CIS.

## *3.18 Measuring Vcc.*

The CF test unit contains an on-board 10-bit A/D converter. An input analog multiplexer selects which voltage is to be measured. Figure 3.18-1 details the A/D converter subsystem.

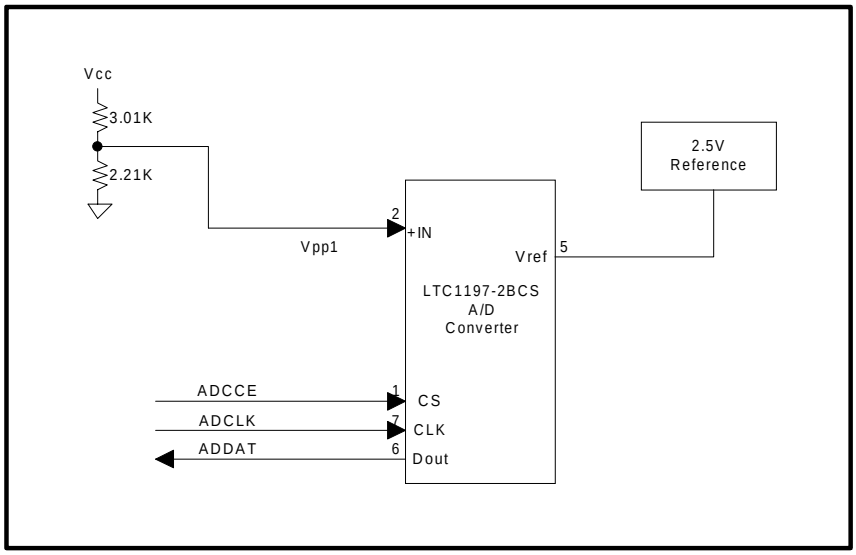



**Figure 3.18-1 - CF test 222 A/D Subsystem**

The A/D converter I/O pins are controlled via internal register bits. The following control bits are tied to the A/D converter:

| Register Location | Register Bit | Description |
|---|---|---|
| MISC.7 | ADCLK | Controls the A/D clock signal |
| MISC.6 | ADCCE | Controls the A/D chip enable signal |
| LATMISC.1 | ADDAT | A/D data output |

**Table 3.18-1 A/D Control Bits**

The A/D converter is implemented using the Linear Technology LTC1197. The programming interface to the A/D converter is contained in the LTC1197 data sheet. A copy of the LTC1197 datasheet is contained in Appendix C.

# *Appendix A - Register Description*

This section describes the configuration of the CF test registers on initial power up. All CF test registers are written via attribute, memory or I/O write commands depending on the setting of the MODE register. There are eight writable 8-bit registers within the CF test unit. A[2:0] will select which register is written by the write strobe. The following table describes at which offset the CF test registers are located in each CF test mode.

| Mode | Space | Register Offset |
|---|---|---|
| 0 | Attribute | 100H |
| 1 | I/O | 0 |
| 2 | I/O | 1F0H |
| 3 | I/O | 170H |
| 4 | Attribute | 100H |
| 4 | Common | 0 |
| 5 | Common | 0 |
| 5 | I/O | 0 |

**0 - DATALO - Low Data Byte to CompactFlash bus**

Any memory write (WE#) qualified with a valid CE1# and A[0:2] = 000 will cause the DATALO register to be updated with contents of the CompactFlash data bus (D[7:0]). In addition, an I/O write qualified with CE1# and A[0:2] = 000 will also cause a write to this register

Any memory read qualified with a valid CE1# will cause the value of the DATALO register to gated onto the CompactFlash data bus (D[7:0]). An I/O read qualified with CE1# and A[0:2] = 000 will gate the contents of DATALO onto the CompactFlash data bus.

**1 - DATAHI - High Data Byte to CompactFlash bus**

Any memory write memory qualified with a valid CE2# will cause the DATAHI register to be updated with contents of the CompactFlash data bus (D[15:7]).

> ***Note**: An 8 bit I/O write to the DATAHI register is not possible.*

A memory read qualified with a valid CE2# will cause the value of the DATAHI register to be gated onto the CompactFlash data bus (D[15:8]). An 8 bit I/O read qualified by CE1# and A[0:2] = 001 will gate the contents of DATAHI onto the CompactFlash data bus D[7:0].

**2 - LADRHI – Address latch for A[23:16] (read)**

Not used in CF test 222.

**2 - TCR - Timer control register (write)**

The TCR is a write-only register that controls the operation of the strobe measurement circuitry. STR[2:0] selects the strobe that will cause the measurement to start. STRPOL selects which edge of the signal will start the timer. STP[2:0] selects the strobe that will stop the timer. STPPOL selects which edge terminates the timer.

| Bit | Name | Description | | | |
|---|---|---|---|---|---|
| D[2:0] | STR[2:0] | Start Pulse select | | | |
| | | STR2 | STR1 | STR0 | Signal |
| | | 0 | 0 | 0 | OE# |
| | | 0 | 0 | 1 | WE# |
| | | 0 | 1 | 0 | CE1# |
| | | 0 | 1 | 1 | CE2# |
| | | 1 | 0 | 0 | Not Used |
| | | 1 | 0 | 1 | Force VS2# Low |
| | | 1 | 1 | 0 | IORD# |
| | | 1 | 1 | 1 | IOWR# |
| D3 | STRPOL | Start polarity<br>0 - Start timer on positive edge<br>1 - Start timer on negative edge | | | |
| D[6:4] | STP[2:0] | End Pulse Select | | | |
| | | STP2 | STP1 | STP0 | Signal |
| | | 0 | 0 | 0 | OE# |
| | | 0 | 0 | 1 | WE# |
| | | 0 | 1 | 0 | CE1# |
| | | 0 | 1 | 1 | CE2# |
| | | 1 | 0 | 0 | Not Used |
| | | 1 | 0 | 1 | Force VS1# Low |
| | | 1 | 1 | 0 | IORD# |
| | | 1 | 1 | 1 | IOWR# |
| D7 | STPPOL | Stop polarity<br>0 - Stop timer on positive edge<br>1 - Stop timer on negative edge | | | |

**Table A-1: TCR Register - Timer Control Register (Offset 2)**

**3 - LATMISC – Misc Latched Bits (Read)**

The LATMISC register contains various realtime and latched status signals from the CompactFlash interface.

| Bit | Name | Description |
|---|---|---|
| D0 | LA24 | Not Used on CF test |
| D1 | ADC Data | A/D Data |
| D2 | BVD1_RB | BVD1 Readback |
| D3 | BVD2_RB | BVD2 Readback |
| D4 | RESET | Unlatched Reset status |
| D5 | LREG# | Latched REG# Signal |
| D6 | WP/IOIS16# | WP/IOIS16# Readback |
| D7 | LA25 | Not Used on CF test |

**Table A-2: LATMISC Register - Misc Latched Bits (Offset 3)**

### 3 - MISC - Control Register (write)

The MISC Control register is a read/write register that contains various control bits for the CF test unit.

| Bit | Name | Description | | | |
|---|---|---|---|---|---|
| D[0:2] | WAIT[0:2] | Wait State Select – control the number of wait states that are inserted for any I/O or memory access. The wait state generator must be enabled through bit 3 of this register. | | | |
| | | WAIT2 | WAIT1 | WAIT0 | Wait States |
| | | 0 | 0 | 0 | No wait states |
| | | 0 | 0 | 1 | 50ns wait |
| | | 0 | 1 | 0 | 100ns wait |
| | | 0 | 1 | 1 | 200ns wait |
| | | 1 | 0 | 0 | 400ns wait |
| | | 1 | 0 | 1 | 800ns wait |
| | | 1 | 1 | 0 | 1600ns wait |
| | | 1 | 1 | 1 | 3200ns wait |
| D3 | ENWAIT | Enable Wait State Generator | | | |
| D4 | CIS Enable | 0 = CIS ROM Enabled (Default)<br>1 = CIS ROM Disabled | | | |
| D5 | AMUX0 | A/D Mux Control bit 0 | | | |
| D6 | ADCCE | A/D Converter Chip Enable | | | |
| D7 | ADCLK | A/D Converter Clock | | | |

**Table A-3: MISC Register - Misc Control bits (offset 3)**

### 4 - LADRLO – Address latch for A[7:0] (read)

A read of this register returns the value of the specified latched address bits. Addresses are latched after the address latch circuitry is armed through the ALAT bit located in the CNTL control register at offset 4.

### 4 - CNTL – Control Register (write)

CNTL is a write only register.

| Bit | Name | Description |
|---|---|---|
| D0 | WP/IOIS16# | WP/IOIS16# Output |
| D1 | RDY/BSY/IREQ# | RDY/BSY/IREQ# Output (inverted) |
| D2 | ALAT | Address Latch Enable |
| D3 | INPKEN | INPACK# Enable<br>0 = INPACK# not generated<br>1 = INPACK# generated on all IORD# access |
| D4 | BVD1_EN#<br><br>CLR_RST | 0 = Enable BVD1/STSCHG# output<br>1 = Tri-state BVD1/STSCHG# output<br>1 = Clear LRESET bit in STBLAT.7.<br>0 = Arm reset latch |
| D5 | BVD1_OUT | 0 = Force BVD1/STSCHG# output low<br>1 = Force BVD1/STSCHG# output high |
| D6 | BVD2_EN# | 0 = Enable BVD2/SPKR# output<br>1 = Tri-state BVD2/SPKR# output |
| D7 | BVD2_OUT | 0 = Force BVD2/SPKR# output low<br>1 = Force BVD2/SPKR# output high |

**Table A-4: CNTL Register - Control Signal Latch (offset 4)**

**5 - LADRMID – Address latch for A[10:8] (read)**

A read of this register returns the value of the specified latched address bits. Addresses are latched after the address latch circuitry is armed through the ALAT bit located in the CNTL control register (offset 4).

**5 - TRST - Reset strobe to pulse counter (write)**

A write to the TRST register will arm the strobe timer circuitry. Once a write to the TRST register is complete, the counter will be armed and waiting for the selected CompactFlash strobe.

**6 - TIM[0..7] - Timer Register (read)**

The Timer Register is a read-only register containing the results of the strobe timer. An 8 bit value represents the number of clocks that occurred between the selected start transition and the end transition specified in the TCR register. The actual value in nanoseconds can be calculated by multiplying the count by the sample clock period. The sample clock period for the CF test 222 is 50nS. The timer is armed by a write to the TRST register (offset 5).

**6 - MODE – Mode Control Register (write)**

The mode control register is used to enable the various CF test test modes. Bits in this register enable common memory and I/O modes.

| **Bit** | **Name** | **Description** | | | |
|---|---|---|---|---|---|
| D[0:2] | MODE [0:2] | Mode Control | | | |
| | | MODE2 | MODE1 | MODE0 | Description |
| | Mode 0 | 0 | 0 | 0 | Attribute memory enabled, I/O space and common memory not enabled |
| | Mode 1 | 0 | 0 | 1 | I/O space enabled, common and attribute memory disabled |
| | Mode 2 | 0 | 1 | 0 | I/O space at 1F0H-1F7H enabled, common and attribute memory disabled |
| | Mode 3 | 0 | 1 | 1 | I/O space at 170H-177H enabled, common and attribute memory disabled |
| | Mode 4 | 1 | 0 | 0 | Common and attribute space enabled, I/O space disabled |
| | Mode 5 | 1 | 0 | 1 | Common memory space enabled, I/O space enabled, attribute memory space disabled. |
| D3 | N.A. | Not Used | | | |
| D4 | N.A. | Not Used | | | |
| D5 | N.A. | Not Used | | | |
| D6 | N.A. | Not Used | | | |
| D7 | N.A. | Not Used | | | |

**Table A-5: MODE Register - Mode Control Register (Offset 6)**

**7 - STBLAT – Latched Control Bits (read)**

The STBLAT register is a read only register that contains the latched status of various control signals on the CompactFlash interface. All latched signal, except LRESET, are latched using the same mechanism at the address latch.

| Bit | Name | Description |
|---|---|---|
| D0 | LOE# | Latched OE# |
| D1 | LWE# | Latched WE# |
| D2 | LCEL# | Latched CEL# |
| D3 | LCEH# | Latched CEH# |
| D4 | LIORD# | Latched IORD# |
| D5 | LIOWR# | Latched IOWR# |
| D6 | N.A. | Not Used |
| D7 | LRESET | Latched RESET status. Cleared by setting bit 4 in the CNTL register |

**Table A-6: STBLAT Register - Latched Status Bits (read)**

# *Appendix B – CF test 222 Rev 1.02 CIS*

This section describes the CF test 222 Card Information Structure (CIS) stored in the attribute memory space of the CF test 222 Rev 1.02.

| Addr | Byte | Description |
|---|---|---|
| 00H | 01H | CISTPL_DEVICE |
| 02H | 03H | Tuple link |
| 04H | D1H | Device Info Field 1 - Function Specific Memory type 16K buffer @250nS |
| 06H | 0AH | 2 units of 8K = 16K |
| 08H | 0FFH | End of tuple |
| | | |
| 0AH | 15H | CISTPL_VERS_1 |
| 0CH | 30H | Tuple link |
| 0EH | 05H | TPLLV1_MAJOR |
| 10H | 00H | TPLLV1_MINOR |
| 12H | 53H | 'S' |
| 14H | 79H | 'y' |
| 16H | 63H | 'c' |
| 18H | 61H | 'a' |
| 1AH | 72H | 'r' |
| 1CH | 64H | 'd' |
| 1EH | 20H | ' ' |
| 20H | 54H | 'T' |
| 22H | 65H | ‘e' |
| 24H | 63H | 'c' |
| 26H | 68H | 'h' |
| 28H | 6EH | 'n' |
| 2AH | 6FH | 'o' |
| 2CH | 6CH | 'l' |
| 2EH | 6FH | 'o' |
| 30H | 67H | 'g' |
| 32H | 79H | 'y' |
| 34H | 00H | 00H |
| 36H | 43H | 'C' |
| 38H | 46H | 'F' |
| 3AH | 74H | 't' |
| 3CH | 65H | 'e' |
| 3EH | 73H | 's' |
| 40H | 74H | 't' |
| 42H | 20H | ' ' |
| 44H | 00H | 00H |
| 46H | 4DH | 'M' |
| 48H | 6FH | 'o' |
| 4AH | 64H | 'd' |
| 4CH | 65H | 'e' |
| 4EH | 6CH | 'l' |
| 50H | 20H | ' ' |
| 52H | 32H | '2' |
| 54H | 32H | '2' |
| 56H | 32H | '2' |

| Addr | Byte | Description |
|---|---|---|
| 58H | 00H | 00H |
| 5AH | 52H | 'R' |
| 5CH | 65H | 'e' |
| 5EH | 76H | 'v' |
| 60H | 20H | ' ' |
| 62H | 31H | '1' |
| 64H | 2EH | '.' |
| 66H | 30H | '0' |
| 68H | 32H | '2' |
| 6AH | 00H | 00H |
| 6CH | 0FFH | |
| 6EH | 20H | CISTPL_MFG_ID |
| 70H | 04H | Tuple Link |
| 72H | 16H | Manufacturer ID - LSB |
| 74H | 02H | Manufacturer ID - MSB |
| 76H | 22H | Product Number - LSB |
| 78H | 02H | Product Number - MSB |
| 7AH | 21H | CISTPL_FUNC_ID |
| 7CH | 02H | Tuple Link |
| 7EH | FEH | TPFID_FUNCTION - Vendor Specific Function |
| 80H | 00H | |
| 82H | 1AH | CISTPL_CONFIG |
| 84H | 05H | Tuple Link |
| 86H | 01H | TPCC_SZ - Specify 2 byte address field |
| 88H | 01H | TPCC__LAST Index value of last table entry tuple |
| 8AH | 00H | TPCC_RADR(LSB) Config register base address (0x200) |
| 8CH | 02H | TPCC_RADR(MSB) Config register base address (0x200) |
| 8EH | 01H | TPCC_RMSK - Register Mask |
| 90H | 1BH | TPCC_CFTABLE_ENTRY |
| 92H | 07H | TPL_LINK |
| 94H | C1H | TPL_INDEX |
| 96H | 01H | TPCE_IF - Interface Definition Byte |
| 98H | 18H | TPCE_FS - Feature Selection Byte |
| 9AH | 63H | TPCE_IO - I/O Window 8,16 bit, 3 address lines |
| 9CH | 30H | TPCE_IR - Interrupt Request Description (Level and Mask) |
| 9EH | FFH | TPCE_IR - Interrupt Mask 1 (All interrupts allowed) |
| A0H | FFH | TPCE_IR - Interrupt Mask 2 (All interrupts allowed) |
| A2H | 14H | CISTPL_NO_LINK |
| A4H | 00H | |
| A6H | 0FFH | CISTPL_END - That’s all folks |

# *Appendix C – Linear Technology LTC-1197 A/D Converter*

# 10-Bit, 500ksps ADCs in MSOP with Auto Shutdown

## FEATURES

- **8-Pin MSOP and SO Packages**
- 10-Bit Resolution at 500ksps
- Single Supply: 5V or 3V
- Low Power at Full Speed:
  25mW Typ at 5V
  2.2mW Typ at 2.7V
- Auto Shutdown Reduces Power Linearly at Lower Sample Rates
- 10-Bit Upgrade to 8-Bit LTC1196/LTC1198
- SPI and MICROWIRE™ Compatible Serial I/O
- **Low Cost**

## APPLICATIONS

- High Speed Data Acquisition
- Portable or Compact Instrumentation
- Low Power or Battery-Operated Instrumentation

## DESCRIPTION

The LTC®1197/LTC1197L/LTC1199/LTC1199L are 10-bit A/D converters with sampling rates up to 500kHz. They have 2.7V (L) and 5V versions and are offered in 8-pin MSOP and SO packages. Power dissipation is typically only 2.2mW at 2.7V (25mW at 5V) during full speed operation. The automatic power down reduces supply current linearly as sample rate is reduced. These 10-bit, switched-capacitor, successive approximation ADCs include a sample-and-hold. The LTC1197/LTC1197L have a differential analog input with an adjustable reference pin. The LTC1199/LTC1199L offer a software-selectable 2-channel MUX.

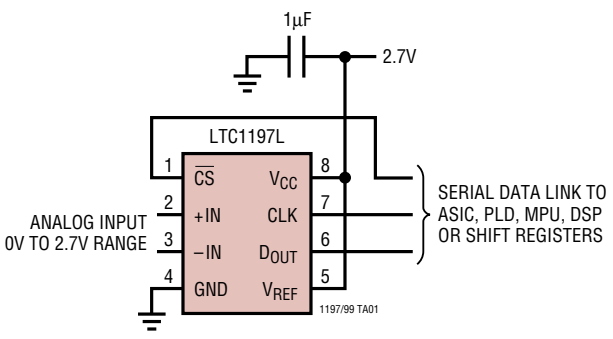
The 3-wire serial I/O, MSOP and SO-8 packages, 2.7V operation and extremely high sample rate-to-power ratio make these ADCs ideal choices for compact, low power high speed systems.

These circuits can be used in ratiometric applications or with external references. The high impedance analog inputs and the ability to operate with reduced spans below 1V full scale (LTC1197/LTC1197L) allow direct connection to signal sources in many applications, eliminating the need for gain stages.

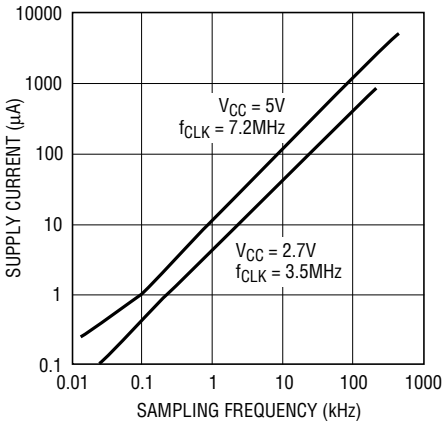


## TYPICAL APPLICATION

**Single 2.7V Supply, 250ksps, 10-Bit Sampling ADC**




**Supply Current vs Sampling Frequency**

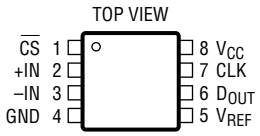


## ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage ($V_{CC}$) ..... 12V
Voltage
  Analog Input ..... GND – 0.3V to $V_{CC}$ + 0.3V
  Digital Input ..... GND – 0.3V to 12V
  Digital Output ..... GND – 0.3V to $V_{CC}$ + 0.3V
Power Dissipation ..... 500mW
Storage Temperature Range ..... –65°C to 150°C

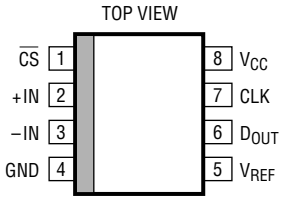
Operating Temperature Range
  LTC1197C/LTC1197LC
  LTC1199C/LTC1199LC ..... 0°C to 70°C
  LTC1197I/LTC1197LI
  LTC1199I/LTC1199LI ..... –45°C to 85°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

## PACKAGE/ORDER INFORMATION



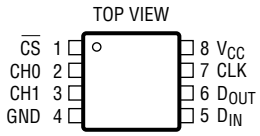

MS8 PACKAGE
8-LEAD PLASTIC MSOP
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 210°C/W

| ORDER PART NUMBER |
|---|
| LTC1197LCMS8 |
| **MS8 PART MARKING** |
| LTBL |



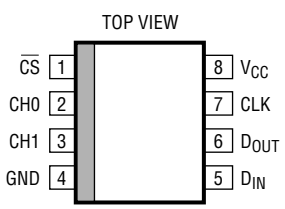

S8 PACKAGE
8-LEAD PLASTIC SO
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 175°C/W

| ORDER PART NUMBER |
|---|
| LTC1197CS8<br>LTC1197IS8<br>LTC1197LCS8<br>LTC1197LIS8 |
| **S8 PART MARKING** |
| 1197 1197L<br>1197I 1197LI |




MS8 PACKAGE
8-LEAD PLASTIC MSOP
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 210°C/W

| ORDER PART NUMBER |
|---|
| LTC1199LCMS8 |
| **MS8 PART MARKING** |
| LTCM |




S8 PACKAGE
8-LEAD PLASTIC SO
$T_{JMAX}$ = 150°C, $\theta_{JA}$ = 175°C/W

| ORDER PART NUMBER |
|---|
| LTC1199CS8<br>LTC1199IS8<br>LTC1199LCS8<br>LTC1199LIS8 |
| **S8 PART MARKING** |
| 1199 1199L<br>1199I 1199LI |

Consult factory for Military grade parts.

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | | LTC1197 MIN | LTC1197 TYP | LTC1197 MAX | LTC1199 MIN | LTC1199 TYP | LTC1199 MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | | 4 | | 9 | 4 | | 6 | V |
| **$V_{CC}$ = 5V Operation** | | | | | | | | | | |
| $f_{CLK}$ | Clock Frequency | | ● | 0.05 | | 7.2 | 0.05 | | 7.2 | MHz |
| $t_{CYC}$ | Total Cycle Time | | | 14 | | | 16 | | | CLK |
| $t_{SMPL}$ | Analog Input Sampling Time | | | 1.5 | | | 1.5 | | | CLK |
| $t_{h\overline{CS}}$ | Hold Time $\overline{CS}$ Low After Last CLK↑ | | | 13 | | | 13 | | | ns |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | | LTC1197 MIN | LTC1197 TYP | LTC1197 MAX | LTC1199 MIN | LTC1199 TYP | LTC1199 MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| **$V_{CC}$ = 5V Operation** | | | | | | | | | | |
| $t_{su\overline{CS}}$ | Setup Time $\overline{CS}\downarrow$ Before First CLK↑ (See Figures 1, 2) | | | 26 | | | 26 | | | ns |
| $t_{hDI}$ | Hold Time $D_{IN}$ After CLK↑ | LTC1199 | | | | | 26 | | | ns |
| $t_{suDI}$ | Setup Time $D_{IN}$ Stable Before CLK↑ | LTC1199 | | | | | 26 | | | ns |
| $t_{WHCLK}$ | CLK High Time | $f_{CLK} = f_{CLK(MAX)}$ | | 40% | | | 40% | | | $1/f_{CLK}$ |
| $t_{WLCLK}$ | CLK Low Time | $f_{CLK} = f_{CLK(MAX)}$ | | 40% | | | 40% | | | $1/f_{CLK}$ |
| $t_{WH\overline{CS}}$ | $\overline{CS}$ High Time Between Data Transfer Cycles | | | 32 | | | 32 | | | ns |
| $t_{WL\overline{CS}}$ | $\overline{CS}$ Low Time During Data Transfer | | | 13 | | | 15 | | | CLK |

| SYMBOL | PARAMETER | CONDITIONS | | LTC1197L MIN | LTC1197L TYP | LTC1197L MAX | LTC1199L MIN | LTC1199L TYP | LTC1199L MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | | 2.7 | | 4 | 2.7 | | 4 | V |
| **$V_{CC}$ = 2.7V Operation** | | | | | | | | | | |
| $f_{CLK}$ | Clock Frequency | | ● | 0.01 | | 3.5 | 0.01 | | 3.5 | MHz |
| $t_{CYC}$ | Total Cycle Time | | | 14 | | | 16 | | | CLK |
| $t_{SMPL}$ | Analog Input Sampling Time | | | 1.5 | | | 1.5 | | | CLK |
| $t_{h\overline{CS}}$ | Hold Time $\overline{CS}$ Low After Last CLK↑ | | | 40 | | | 40 | | | ns |
| $t_{su\overline{CS}}$ | Setup Time $\overline{CS}\downarrow$ Before First CLK↑ (See Figures 1, 2) | | | 78 | | | 78 | | | ns |
| $t_{hDI}$ | Hold Time $D_{IN}$ After CLK↑ | LTC1199L | | | | | 78 | | | ns |
| $t_{suDI}$ | Setup Time $D_{IN}$ Stable Before CLK↑ | LTC1199L | | | | | 78 | | | ns |
| $t_{WHCLK}$ | CLK High Time | $f_{CLK} = f_{CLK(MAX)}$ | | 40% | | | 40% | | | $1/f_{CLK}$ |
| $t_{WLCLK}$ | CLK Low Time | $f_{CLK} = f_{CLK(MAX)}$ | | 40% | | | 40% | | | $1/f_{CLK}$ |
| $t_{WH\overline{CS}}$ | $\overline{CS}$ High Time Between Data Transfer Cycles | | | 96 | | | 96 | | | ns |
| $t_{WL\overline{CS}}$ | $\overline{CS}$ Low Time During Data Transfer | | | 13 | | | 15 | | | CLK |

## CONVERTER AND MULTIPLEXER CHARACTERISTICS

**$V_{CC}$ = 5V, $V_{REF}$ = 5V, $f_{CLK} = f_{CLK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.**

| PARAMETER | CONDITIONS | | LTC1197 MIN | LTC1197 TYP | LTC1197 MAX | LTC1199 MIN | LTC1199 TYP | LTC1199 MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Offset Error | | ● | | | ±2 | | | ±2 | LSB |
| Linearity Error | (Note 3) | ● | | | ±1 | | | ±1 | LSB |
| Gain Error | | ● | | | ±4 | | | ±4 | LSB |
| No Missing Codes Resolution | | ● | 10 | | | 10 | | | Bits |
| Analog Input Range | | | | −0.05V to $V_{CC}$ + 0.05V | | | | | V |
| Reference Input Range | LTC1197, $V_{CC} \le 6V$<br>LTC1197, $V_{CC} > 6V$ | | 0.2<br>0.2 | | $V_{CC}$ + 0.05V<br>6 | | | | V<br>V |
| Analog Input Leakage Current | (Note 4) | ● | | | ±1 | | | ±1 | µA |

## CONVERTER AND MULTIPLEXER CHARACTERISTICS

**$V_{CC}$ = 2.7V, $V_{REF}$ = 2.5V (LTC1197L), $f_{CLK}$ = $f_{CLK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.**

| PARAMETER | CONDITIONS | | LTC1197L MIN | LTC1197L TYP | LTC1197L MAX | LTC1199L MIN | LTC1199L TYP | LTC1199L MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| Offset Error | | ● | | | ±2 | | | ±2 | LSB |
| Linearity Error | (Note 3) | ● | | | ±1 | | | ±1 | LSB |
| Gain Error | | ● | | | ±4 | | | ±4 | LSB |
| No Missing Codes Resolution | | ● | 10 | | | 10 | | | Bits |
| Analog Input Range | | | | −0.05V to $V_{CC}$ + 0.05V | | | | | V |
| Reference Input Range | LTC1197L | | 0.2 | | $V_{CC}$ + 0.05V | | | | V |
| Analog Input Leakage Current | (Note 4) | ● | | | ±1 | | | ±1 | µA |

## DYNAMIC ACCURACY

**$V_{CC}$ = 5V, $V_{REF}$ = 5V, $f_{CLK}$ = $f_{CLK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | LTC1197 MIN | LTC1197 TYP | LTC1197 MAX | LTC1199 MIN | LTC1199 TYP | LTC1199 MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| S/(N + D) | Signal-to-Noise Plus Distortion Ratio | 100kHz Input Signal | | 60 | | | 60 | | dB |
| THD | Total Harmonic Distortion First 5 Harmonics | 100kHz Input Signal | | −64 | | | −64 | | dB |
| | Peak Harmonic or Spurious Noise | 100kHz Input Signal | | −68 | | | −68 | | dB |
| IMD | Intermodulation Distortion | $f_{IN1}$ = 97.046kHz, $f_{IN2}$ = 102.905kHz | | | | | | | |
| | | 2nd Order Terms | | −65 | | | −65 | | dB |
| | | 3rd Order Terms | | −70 | | | −70 | | dB |

**$V_{CC}$ = 2.7V, $V_{REF}$ = 2.5V, $f_{CLK}$ = $f_{CLK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | LTC1197L MIN | LTC1197L TYP | LTC1197L MAX | LTC1199L MIN | LTC1199L TYP | LTC1199L MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| S/(N + D) | Signal-to-Noise Plus Distortion Ratio | 50kHz Input Signal | | 58 | | | 58 | | dB |
| THD | Total Harmonic Distortion First 5 Harmonics | 50kHz Input Signal | | −60 | | | −60 | | dB |
| | Peak Harmonic or Spurious Noise | 50kHz Input Signal | | −63 | | | −63 | | dB |
| IMD | Intermodulation Distortion | $f_{IN1}$ = 48.5kHz, $f_{IN2}$ = 51.5kHz | | | | | | | |
| | | 2nd Order Terms | | −60 | | | −60 | | dB |
| | | 3rd Order Terms | | −65 | | | −65 | | dB |

# DIGITAL AND DC ELECTRICAL CHARACTERISTICS

**$V_{CC}$ = 5V, $V_{REF}$ = 5V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | LTC1197 MIN | LTC1197 TYP | LTC1197 MAX | LTC1199 MIN | LTC1199 TYP | LTC1199 MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | $V_{CC}$ = 5.25V | ● | 2.4 | | | 2.4 | | | V |
| $V_{IL}$ | Low Level Input Voltage | $V_{CC}$ = 4.75V | ● | | | 0.8 | | | 0.8 | V |
| $I_{IH}$ | High Level Input Current | $V_{IN}$ = $V_{CC}$ | ● | | | 2.5 | | | 2.5 | µA |
| $I_{IL}$ | Low Level Input Current | $V_{IN}$ = 0V | ● | | | –2.5 | | | –2.5 | µA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = 4.75V, $I_O$ = 10µA<br>$V_{CC}$ = 4.75V, $I_O$ = 360µA | ●<br>● | 4.5<br>2.4 | 4.74<br>4.72 | | 4.5<br>2.4 | 4.74<br>4.72 | | V<br>V |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = 4.75V, $I_O$ = 1.6mA | ● | | | 0.4 | | | 0.4 | V |
| $I_{OZ}$ | Hi-Z Output Leakage | $\overline{CS}$ = High | ● | | | ±3 | | | ±3 | µA |
| $I_{SOURCE}$ | Output Source Current | $V_{OUT}$ = 0V | | | –25 | | | –25 | | mA |
| $I_{SINK}$ | Output Sink Current | $V_{OUT}$ = $V_{CC}$ | | | 45 | | | 45 | | mA |
| $I_{REF}$ | Reference Current (LTC1197) | $\overline{CS}$ = $V_{CC}$<br>$f_{SMPL}$ = $f_{SMPL(MAX)}$ | ●<br>● | | 0.001<br>0.5 | 3<br>1 | | | | µA<br>mA |
| $I_{CC}$ | Supply Current | $\overline{CS}$ = $V_{CC}$<br>$f_{SMPL}$ = $f_{SMPL(MAX)}$ | ●<br>● | | 0.001<br>4.5 | 3<br>8 | | 0.001<br>5 | 3<br>8.5 | µA<br>mA |
| $P_D$ | Power Dissipation | $f_{SMPL}$ = $f_{SMPL(MAX)}$ | | | 22.5 | | | 25 | | mW |

**$V_{CC}$ = 2.7V, $V_{REF}$ = 2.5V, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | LTC1197L MIN | LTC1197L TYP | LTC1197L MAX | LTC1199L MIN | LTC1199L TYP | LTC1199L MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage | $V_{CC}$ = 3.6V | ● | 1.9 | | | 1.9 | | | V |
| $V_{IL}$ | Low Level Input Voltage | $V_{CC}$ = 2.7V | ● | | | 0.45 | | | 0.45 | V |
| $I_{IH}$ | High Level Input Current | $V_{IN}$ = $V_{CC}$ | ● | | | 2.5 | | | 2.5 | µA |
| $I_{IL}$ | Low Level Input Current | $V_{IN}$ = 0V | ● | | | –2.5 | | | –2.5 | µA |
| $V_{OH}$ | High Level Output Voltage | $V_{CC}$ = 2.7V, $I_O$ = 10µA<br>$V_{CC}$ = 2.7V, $I_O$ = 360µA | ●<br>● | 2.3<br>2.1 | 2.60<br>2.45 | | 2.3<br>2.1 | 2.60<br>2.45 | | V<br>V |
| $V_{OL}$ | Low Level Output Voltage | $V_{CC}$ = 2.7V, $I_O$ = 400µA | ● | | | 0.3 | | | 0.3 | V |
| $I_{OZ}$ | Hi-Z Output Leakage | $\overline{CS}$ = High | ● | | | ±3 | | | ±3 | µA |
| $I_{SOURCE}$ | Output Source Current | $V_{OUT}$ = 0V | | | –6.5 | | | –6.5 | | mA |
| $I_{SINK}$ | Output Sink Current | $V_{OUT}$ = $V_{CC}$ | | | 11 | | | 11 | | mA |
| $I_{REF}$ | Reference Current (LTC1197L) | $\overline{CS}$ = $V_{CC}$<br>$f_{SMPL}$ = $f_{SMPL(MAX)}$ | ●<br>● | | 0.001<br>0.250 | 3.0<br>0.5 | | | | µA<br>mA |
| $I_{CC}$ | Supply Current | $\overline{CS}$ = $V_{CC}$<br>$f_{SMPL}$ = $f_{SMPL(MAX)}$ | ●<br>● | | 0.001<br>0.8 | 3<br>2 | | 0.001<br>0.8 | 3<br>2 | µA<br>mA |
| $P_D$ | Power Dissipation | $f_{SMPL}$ = $f_{SMPL(MAX)}$ | | | 2.2 | | | 2.2 | | mW |

## AC CHARACTERISTICS

**$V_{CC}$ = 5V, $V_{REF}$ = 5V, $f_{CLK}$ = $f_{CLK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | LTC1197 MIN | LTC1197 TYP | LTC1197 MAX | LTC1199 MIN | LTC1199 TYP | LTC1199 MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{CONV}$ | Conversion Time (See Figures 1, 2) | | ● | | | 1.4 | | | 1.4 | µs |
| $f_{SMPL(MAX)}$ | Maximum Sampling Frequency | | ● | 500 | | | 450 | | | kHz |
| $t_{dDO}$ | Delay Time, CLK↑ to $D_{OUT}$ Data Valid | $C_{LOAD}$ = 20pF | <br>● | | 68 | 78<br>100 | | 68 | 78<br>100 | ns<br>ns |
| $t_{dis}$ | Delay Time, $\overline{CS}$↑ to $D_{OUT}$ Hi-Z | | ● | | 75 | 150 | | 75 | 150 | ns |
| $t_{en}$ | Delay Time, CLK↓ to $D_{OUT}$ Enabled | $C_{LOAD}$ = 20pF | ● | | 40 | 68 | | 40 | 68 | ns |
| $t_{hDO}$ | Time Output Data Remains Valid After CLK↑ | $C_{LOAD}$ = 20pF | ● | 25 | 55 | | 25 | 55 | | ns |
| $t_r$ | $D_{OUT}$ Rise Time | $C_{LOAD}$ = 20pF | ● | | 10 | 20 | | 10 | 20 | ns |
| $t_f$ | $D_{OUT}$ Fall Time | $C_{LOAD}$ = 20pF | ● | | 10 | 20 | | 10 | 20 | ns |
| $C_{IN}$ | Input Capacitance | Analog Input On Channel<br>Analog Input Off Channel<br>Digital Input | | | 20<br>5<br>5 | | | 20<br>5<br>5 | | pF<br>pF<br>pF |

**$V_{CC}$ = 2.7V, $V_{REF}$ = 2.5V, $f_{CLK}$ = $f_{CLK(MAX)}$ as defined in Recommended Operating Conditions, unless otherwise noted.**

| SYMBOL | PARAMETER | CONDITIONS | | LTC1197L MIN | LTC1197L TYP | LTC1197L MAX | LTC1199L MIN | LTC1199L TYP | LTC1199L MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|
| $t_{CONV}$ | Conversion Time (See Figures 1, 2) | | ● | | | 2.9 | | | 2.9 | µs |
| $f_{SMPL(MAX)}$ | Maximum Sampling Frequency | | ● | 250 | | | 210 | | | kHz |
| $t_{dDO}$ | Delay Time, CLK↑ to $D_{OUT}$ Data Valid | $C_{LOAD}$ = 20pF | <br>● | | 130 | 180<br>250 | | 130 | 180<br>250 | ns<br>ns |
| $t_{dis}$ | Delay Time, $\overline{CS}$↑ to $D_{OUT}$ Hi-Z | | ● | | 120 | 250 | | 120 | 250 | ns |
| $t_{en}$ | Delay Time, CLK↓ to $D_{OUT}$ Enabled | $C_{LOAD}$ = 20pF | ● | | 100 | 200 | | 100 | 200 | ns |
| $t_{hDO}$ | Time Output Data Remains Valid After CLK↑ | $C_{LOAD}$ = 20pF | ● | 45 | 120 | | 45 | 120 | | ns |
| $t_r$ | $D_{OUT}$ Rise Time | $C_{LOAD}$ = 20pF | ● | | 15 | 40 | | 15 | 40 | ns |
| $t_f$ | $D_{OUT}$ Fall Time | $C_{LOAD}$ = 20pF | ● | | 15 | 40 | | 15 | 40 | ns |
| $C_{IN}$ | Input Capacitance | Analog Input On Channel<br>Analog Input Off Channel<br>Digital Input | | | 20<br>5<br>5 | | | 20<br>5<br>5 | | pF<br>pF<br>pF |

The ● denotes specifications which apply over the full operating temperature range.

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

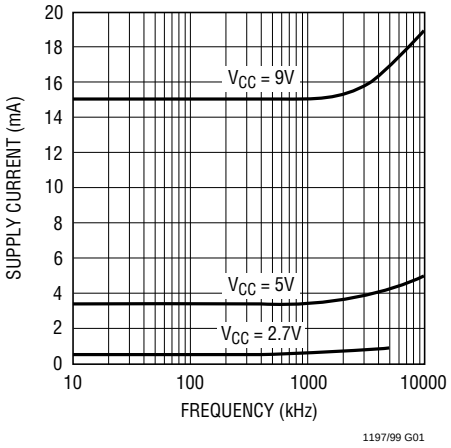
**Note 2:** All voltage values are with respect to GND.

**Note 3:** Integral nonlinearity is defined as deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

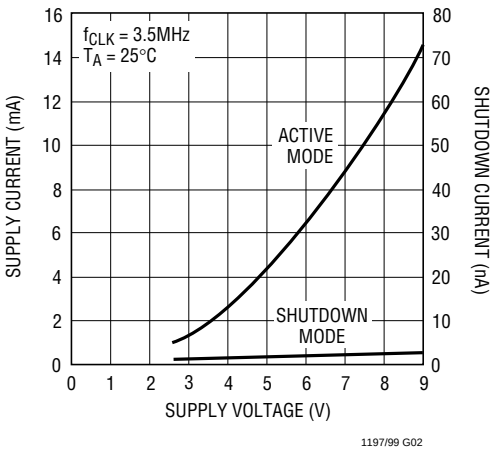
**Note 4:** Channel leakage current is measured after the channel selection.

# TYPICAL PERFORMANCE CHARACTERISTICS

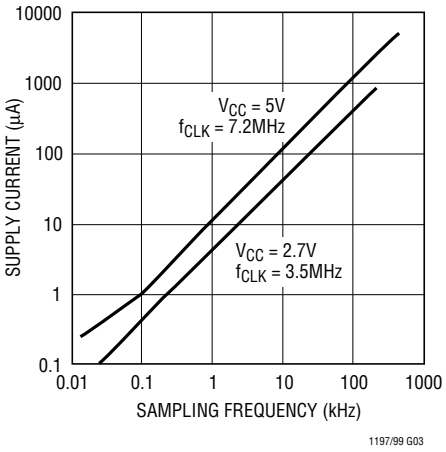
### Supply Current vs Clock Rate*



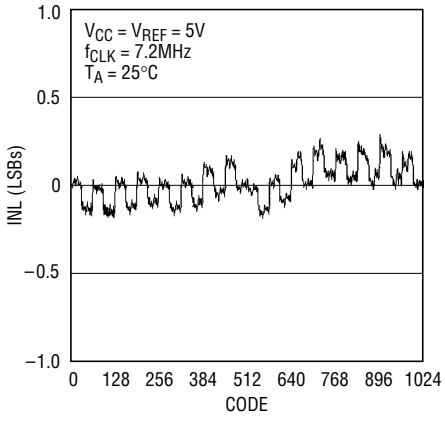

### Supply Current vs Supply Voltage



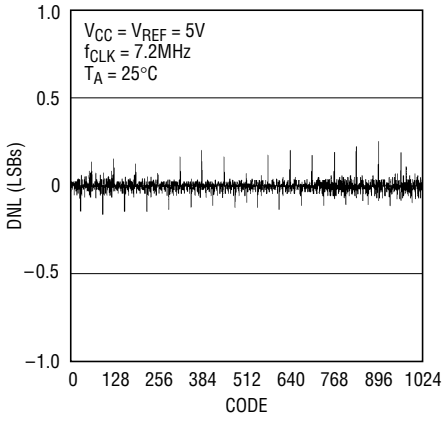

### Supply Current vs Sampling Frequency



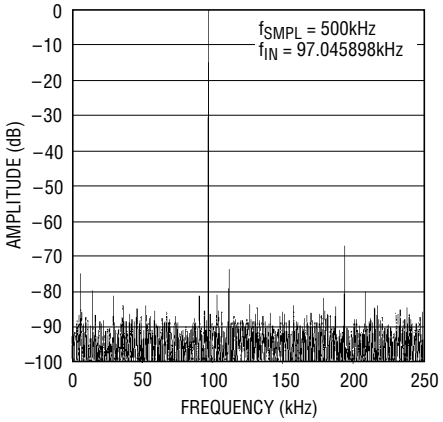

### INL Plot



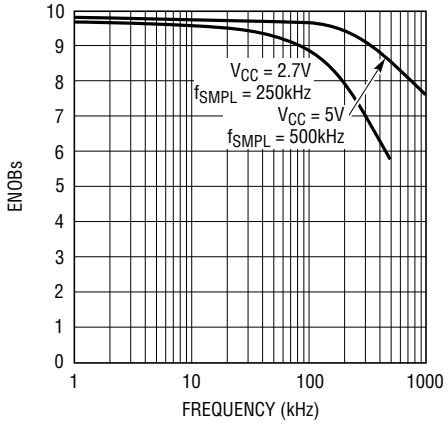

### DNL Plot



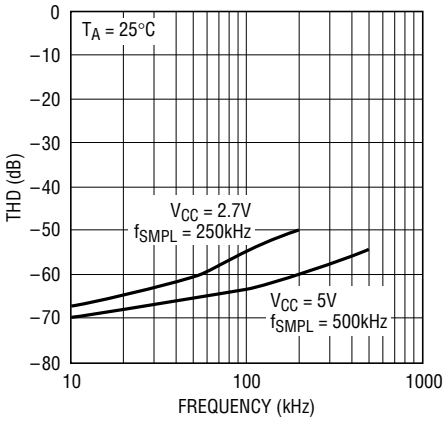

### LTC1197 4096 Point FFT



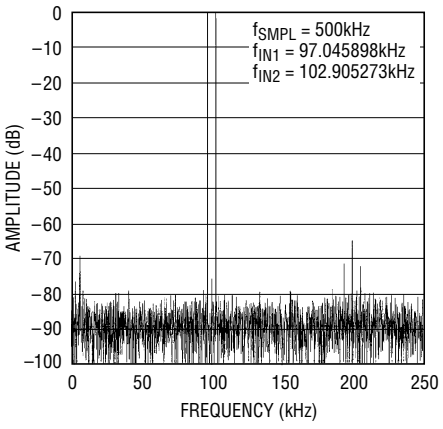

### ENOBs vs Frequency




### THD vs Frequency



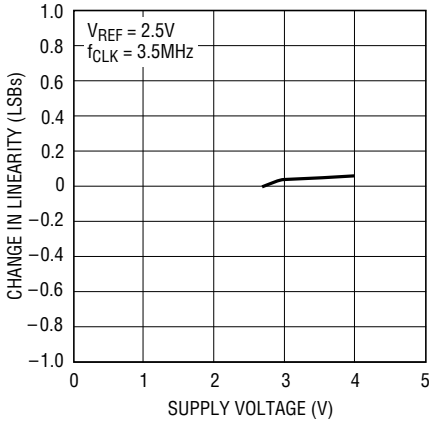

### Intermodulation Distortion Plot




*Part is continuously sampling, spending only a minimum amount of time in shutdown.

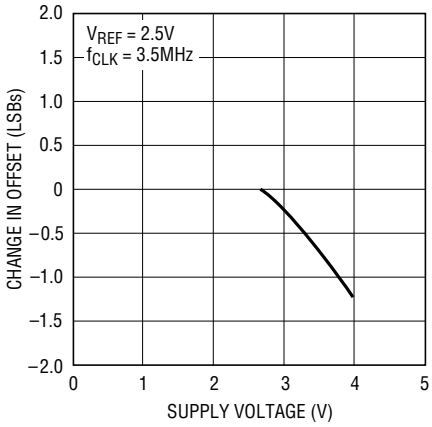
## TYPICAL PERFORMANCE CHARACTERISTICS

**LTC1197L Change in Linearity vs Supply Voltage**



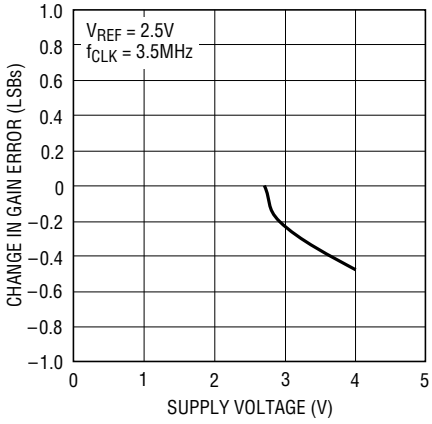

1197/99 G10

**LTC1197L Change in Offset vs Supply Voltage**



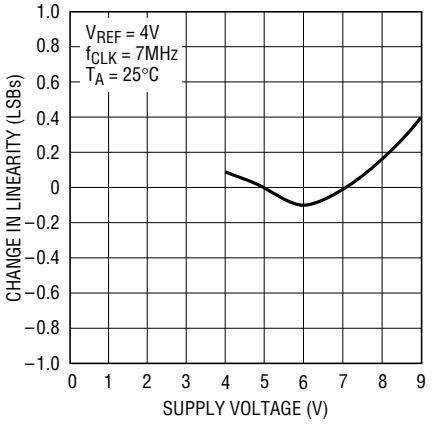

1197/99 G11

**LTC1197L Change in Gain Error vs Supply Voltage**



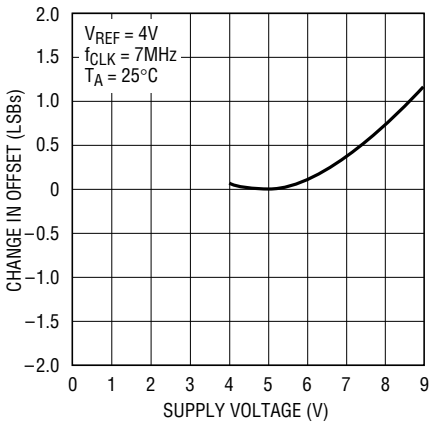

1197/99 G12

**LTC1197 Change in Linearity vs Supply Voltage**



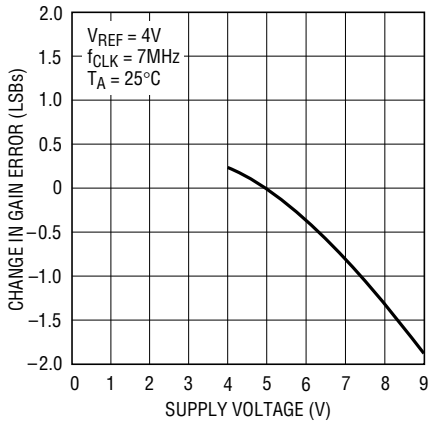

1197/99 G13

**LTC1197 Change in Offset vs Supply Voltage**



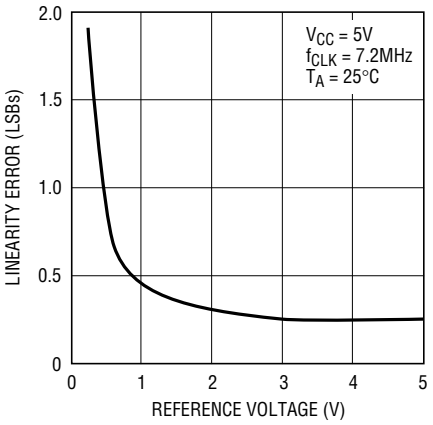

1197/99 G14

**LTC1197 Change in Gain Error vs Supply Voltage**



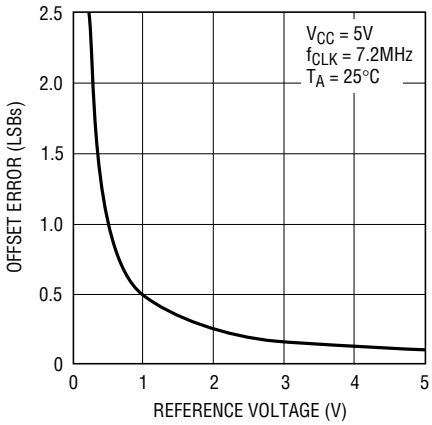

1197/99 G15

**LTC1197 Linearity Error vs Reference Voltage**



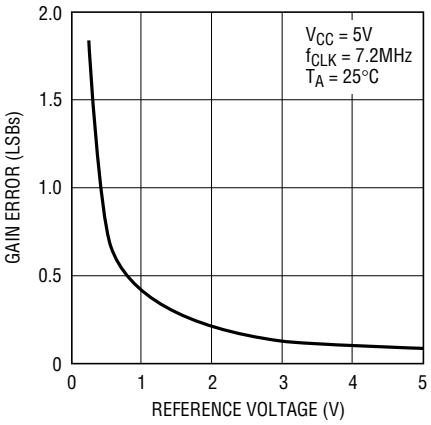

1197/99 F16

**LTC1197 Offset Error vs Reference Voltage**




1197/99 G17

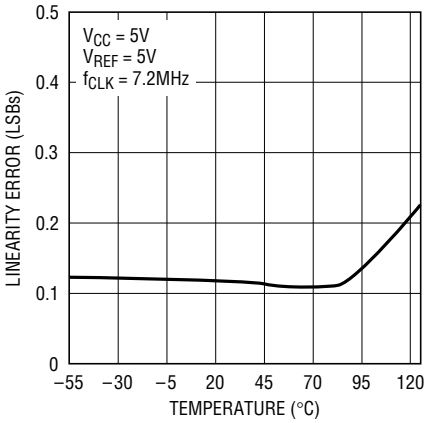
**LTC1197 Gain Error vs Reference Voltage**




1197/99 F18

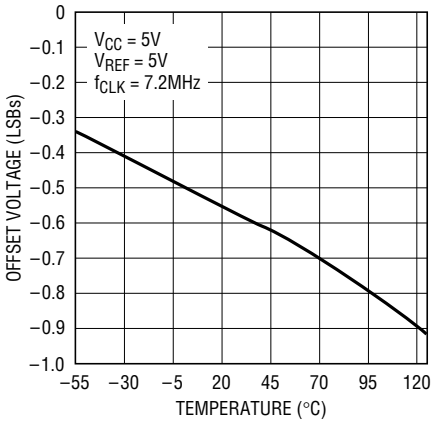
# TYPICAL PERFORMANCE CHARACTERISTICS

### Linearity vs Temperature



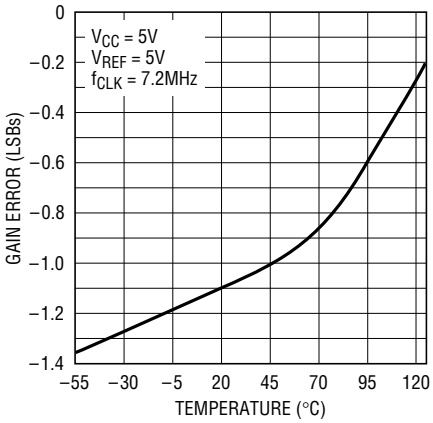

1197/99 G19

### Offset vs Temperature



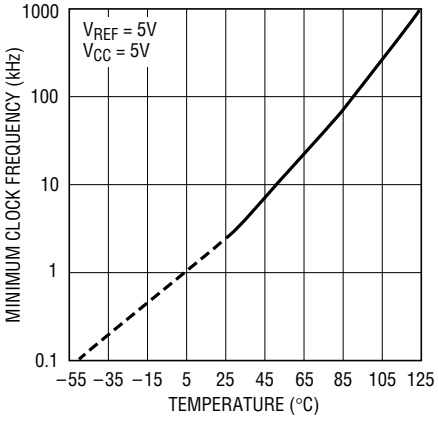

1197/99 G20

### Gain Error vs Temperature



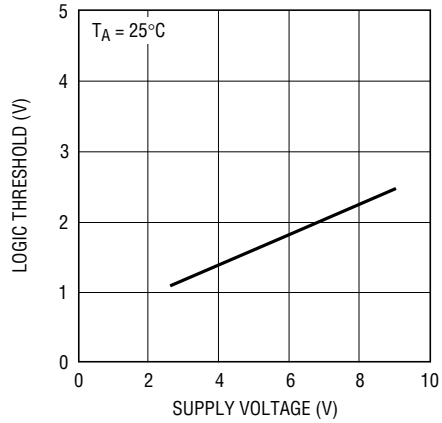

1197/99 G21

### Minimum Clock Frequency for 0.1LSB Error* vs Temperature



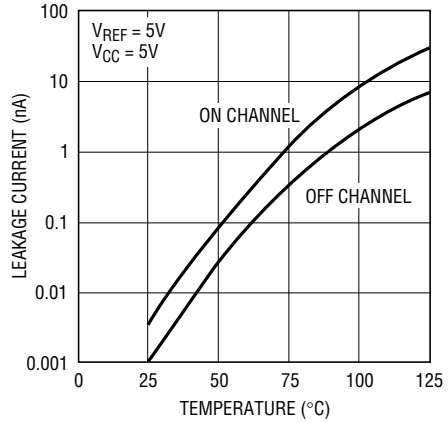

1197/99 G22

### Digital Input Threshold vs Supply Voltage



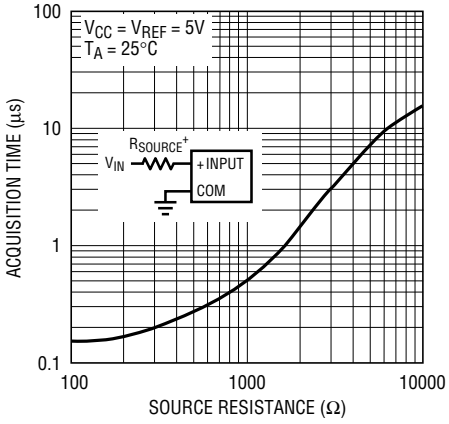

1197/99 G23

### Input Channel Leakage Current vs Temperature



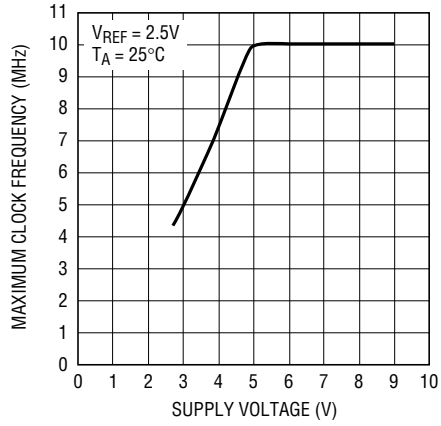

1197/99 G24

### Acquisition Time vs Source Resistance



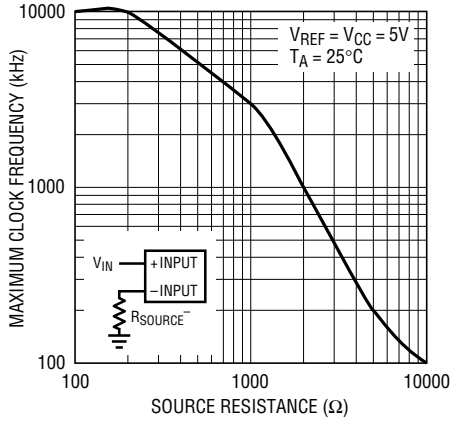

1197/99 G25

### Maximum Clock Frequency vs Supply Voltage




1197/99 G26

### Maximum Clock Frequency† vs Source Resistance




1197/99 G27

*As the CLK frequency is decreased from 2MHz, minimum CLK frequency (Δerror ≤ 0.1LSB) represents the frequency at which a 0.1LSB shift in any code translation from its 2MHz value is first detected.

†Maximum CLK frequency represents the clock frequency at which a 0.1LSB shift in the error at any code transition from its 3.5MHz value is first detected.

## PIN FUNCTIONS

**$\overline{CS}$ (Pin 1):** Chip Select Input. A logic low on this input enables the LTC1197/LTC1197L/LTC1199/LTC1199L. Power shutdown is activated when $\overline{CS}$ is brought high.

**+IN, CH0 (Pin 2):** Analog Input. This input must be free of noise with respect to GND.

**–IN, CH1 (Pin 3):** Analog Input. This input must be free of noise with respect to GND.

**GND (Pin 4):** Analog Ground. GND should be tied directly to an analog ground plane.

**$V_{REF}$ (Pin 5):** LTC1197/LTC1197L Reference Input. The reference input defines the span of the A/D converter and must be kept free of noise with respect to GND.

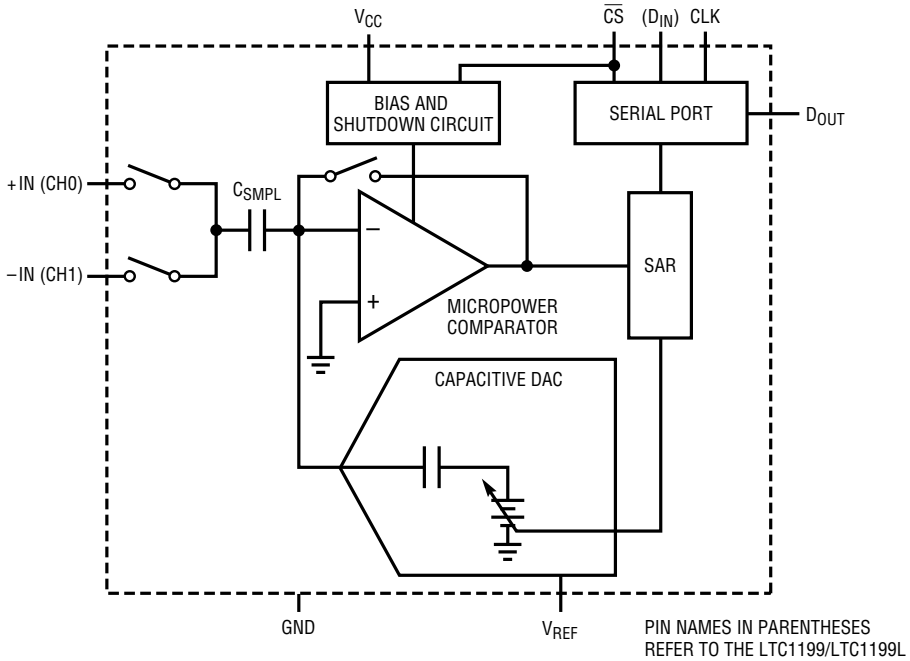
**$D_{IN}$ (Pin 5):** LTC1199/LTC1199L Digital Data Input. The A/D configuration word is shifted into this input.

**$D_{OUT}$ (Pin 6):** Digital Data Output. The A/D conversion result is shifted out of this output.

**CLK (Pin 7):** Shift Clock. This clock synchronizes the serial data transfer.

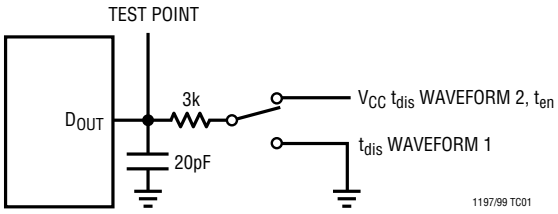
**$V_{CC}$ (Pin 8):** Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane. For LTC1199/LTC1199L, $V_{REF}$ is tied internally to this pin.

## BLOCK DIAGRAM

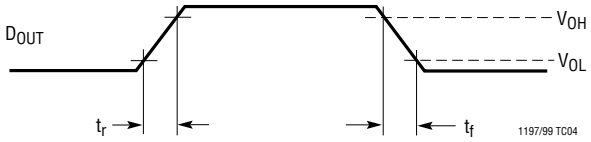


# TEST CIRCUITS

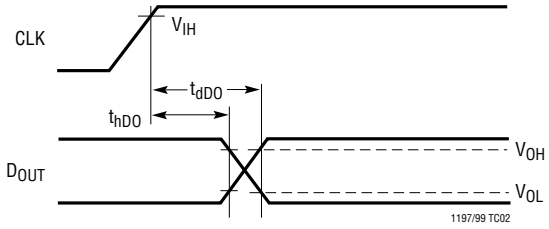
### Load Circuit for $t_{dDO}$, $t_r$, $t_f$, $t_{dis}$ and $t_{en}$



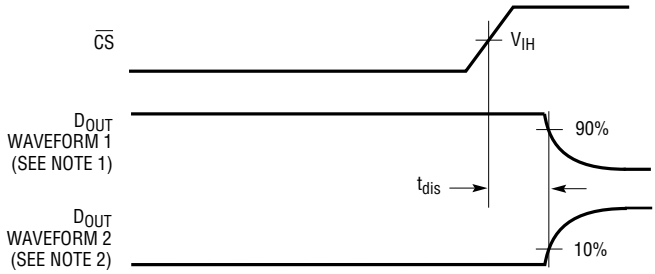

### Voltage Waveforms for $D_{OUT}$ Rise and Fall Times, $t_r$, $t_f$




### Voltage Waveforms for $D_{OUT}$ Delay Time, $t_{dDO}$




### Voltage Waveforms for $t_{dis}$




NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL

NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL

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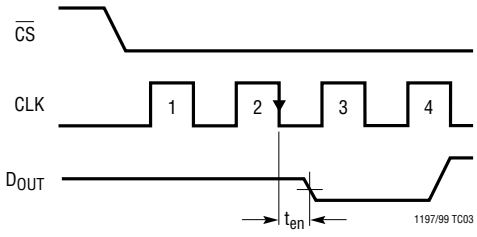
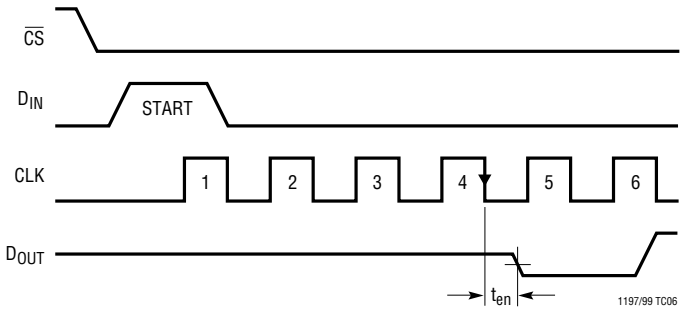
### LTC1197/LTC1197L $t_{en}$ Voltage Waveforms




### LTC1199/LTC1199L $t_{en}$ Voltage Waveforms



# APPLICATIONS INFORMATION

## OVERVIEW

The LTC1197/LTC1197L/LTC1199/LTC1199L are 10-bit switched-capacitor A/D converters. These sampling ADCs typically draw 5mA of supply current when sampling up to 500kHz (800µA at 2.7V sampling up to 250kHz). Supply current drops linearly as the sample rate is reduced (see Supply Current vs Sample Rate in the Typical Performance Characteristics). The ADCs automatically power down when not performing a conversion, drawing only leakage current. They are packaged in 8-pin MSOP and SO packages. The LTC1197L/LTC1199L operate on a single supply ranging from 2.7V to 4V. The LTC1197 operates on a single supply ranging from 4V to 9V while the LTC1199 operates from 4V to 6V.

These ADCs contain a 10-bit, switched-capacitor ADC, a sample-and-hold and a serial port (see Block Diagram). Although they share the same basic design, the LTC1197/LTC1197L and LTC1199/LTC1199L differ in some respects. The LTC1197/LTC1197L have a differential input and have an external reference input pin. They can measure signals floating on a DC common mode voltage and can operate with reduced spans down to 200mV. Reducing the span allows it to achieve 200µV resolution. The LTC1199/LTC1199L have a 2-channel input multiplexer with the reference connected to the supply ($V_{CC}$) pin. They can convert the input voltage of either channel with respect to ground or the difference between the voltages of the two channels.

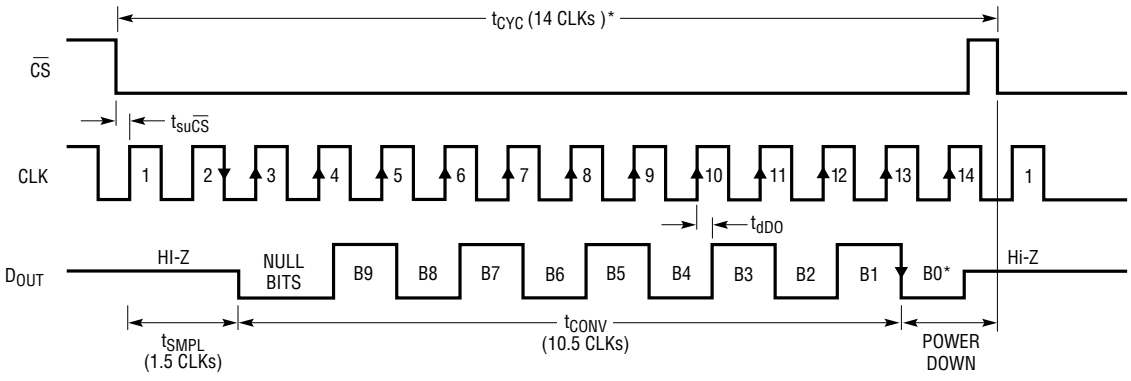
## SERIAL INTERFACE

The LTC1199/LTC1199L communicate with microprocessors and other external circuitry via a synchronous, half duplex, 4-wire serial interface while the LTC1197/LTC1197L use a 3-wire interface (see Operating Sequence in Figures 1 and 2). These interfaces are compatible with both SPI and MICROWIRE protocols without requiring any additional glue logic (see MICROPROCESSOR INTERFACES: Motorola SPI).

## DATA TRANSFER

The CLK synchronizes the data transfer with each bit being transmitted and captured on the rising CLK edge in both transmitting and receiving systems. The LTC1199/LTC1199L first receives input data and then transmits back the A/D conversion result (half duplex). Because of the half-duplex operation, $D_{IN}$ and $D_{OUT}$ may be tied together allowing transmission over just three wires: $\overline{CS}$, CLK and DATA ($D_{IN}/D_{OUT}$).

Data transfer is initiated by a falling chip select ($\overline{CS}$) signal. After $\overline{CS}$ falls the LTC1199/LTC1199L look for a start bit on the $D_{IN}$ input. After the start bit is received, the 3-bit input word is shifted into the $D_{IN}$ input which configures the LTC1199/LTC1199L and starts the conversion. After two null bits, the result of the conversion is output on the $D_{OUT}$ line in MSB-first format. At the end of the data exchange $\overline{CS}$ should be brought high. This resets the LTC1199/LTC1199L in preparation for the next data exchange. Bringing $\overline{CS}$ high after the conversion also minimizes supply current if CLK is left running.




*AFTER COMPLETING THE DATA TRANSFER, IF FURTHER CLOCKS ARE APPLIED WITH $\overline{CS}$ LOW, THE ADC WILL OUTPUT ZEROS INDEFINITELY

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**Figure 1. LTC1197/LTC1197L Operating Sequence**

## APPLICATIONS INFORMATION

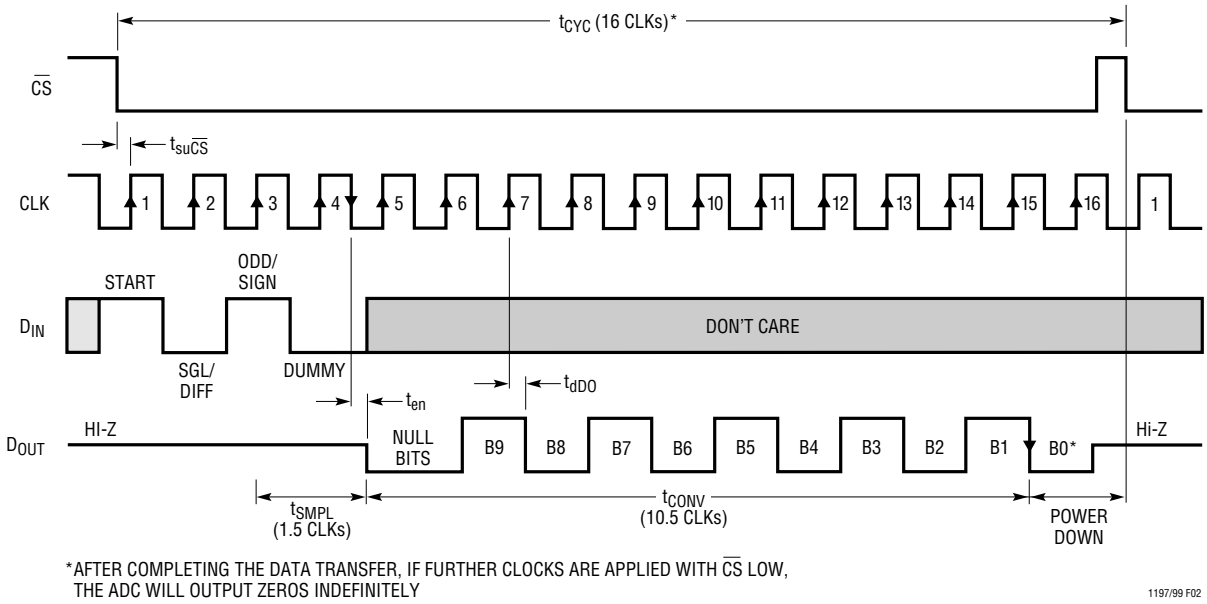
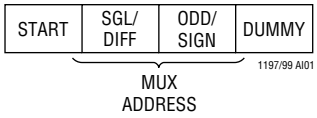



**Figure 2. LTC1199/LTC1199L Operating Sequence**

The LTC1197/LTC1197L do not require a configuration input word and have no $D_{IN}$ pin. A falling $\overline{CS}$ initiates data transfer as shown in the LTC1197/LTC1197L operating sequence. After $\overline{CS}$ falls, the second CLK pulse enables $D_{OUT}$. After two null bits, the A/D conversion result is output on the $D_{OUT}$ line in MSB-first format. Bringing $\overline{CS}$ high resets the LTC1197/LTC1197L for the next data exchange and minimizes the supply current if CLK is continuously running.

### INPUT DATA WORD (LTC1199/LTC1199L ONLY)

The LTC1199 4-bit data word is clocked into the $D_{IN}$ input on the rising edge of the clock after $\overline{CS}$ goes low and the start bit has been recognized. Further inputs on the $D_{IN}$ pin are then ignored until the next $\overline{CS}$ cycle. The input word is defined as follows:




### Start Bit

The first "logical one" clocked into the $D_{IN}$ input after $\overline{CS}$ goes low is the start bit. The start bit initiates the data transfer and all leading zeros that precede this logical one will be ignored. After the start bit is received the remaining bits of the input word will be clocked in. Further inputs on the $D_{IN}$ pin are then ignored until the next $\overline{CS}$ cycle.

### Multiplexer (MUX) Address

The bits of the input word following the start bit assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the "+" and "–" signs in the selected row of the following table. In single-ended mode, all input channels are measured with respect to GND. Only the + inputs have sample-and-holds. Signals applied at the – inputs must not change more than the required accuracy during the conversion.

**Multiplexer Channel Selection**

| MUX ADDRESS | | CHANNEL # | | |
|---|---|---|---|---|
| SGL/DIFF | ODD/SIGN | 0 | 1 | GND |
| 1 | 0 | + | | – |
| 1 | 1 | | + | – |
| 0 | 0 | + | – | |
| 0 | 1 | – | + | |

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## APPLICATIONS INFORMATION

### Dummy Bit

The dummy bit is a placeholder that extends the acquisition time of the ADC. This bit can be either high or low and does not affect the conversion of the ADC.

### Operation with $D_{IN}$ and $D_{OUT}$ Tied Together

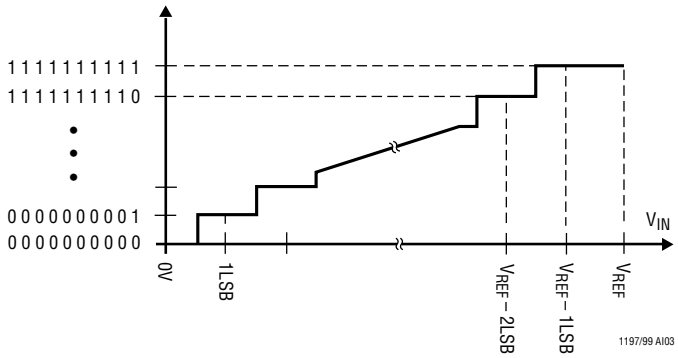
The LTC1199/LTC1199L can be operated with $D_{IN}$ and $D_{OUT}$ tied together. This eliminates one of the lines required to communicate to the microprocessor (MPU). Data is transmitted in both directions on a single wire. The processor pin connected to this data line should be configurable as either an input or an output. The LTC1199/LTC1199L will take control of the data line and drive it low on the 4th falling CLK edge after the start bit is received (see Figure 3). Therefore the processor port line must be switched to an input before this happens to avoid a conflict.

In the Typical Applications section, there is an example of interfacing the LTC1199/LTC1199L with $D_{IN}$ and $D_{OUT}$ tied together to the Intel 8051 MPU.

### Unipolar Transfer Curve

The LTC1197/LTC1197L/LTC1199/LTC1199L are permanently configured for unipolar only. The input span and code assignment for this conversion type are shown in the following figures for a 5V reference.

**Unipolar Transfer Curve**




**Unipolar Output Code**

| OUTPUT CODE | INPUT VOLTAGE | INPUT VOLTAGE ($V_{REF}$ = 5.000V) |
|---|---|---|
| 1111111111 | $V_{REF}$ – 1LSB | 4.99512V |
| 1111111110 | $V_{REF}$ – 2LSB | 4.99023V |
| • | • | • |
| • | • | • |
| 0000000001 | 1LSB | 4.88mV |
| 0000000000 | 0V | 0V |

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### ACHIEVING MICROPOWER PERFORMANCE

With typical operating currents of 5mA (LTC1197/LTC1199) at 5V and 0.8mA (LTC1197L/LTC1199L) at 2.7V it is possible for these ADCs to achieve true micropower performance by taking advantage of the automatic shutdown between conversions. In systems

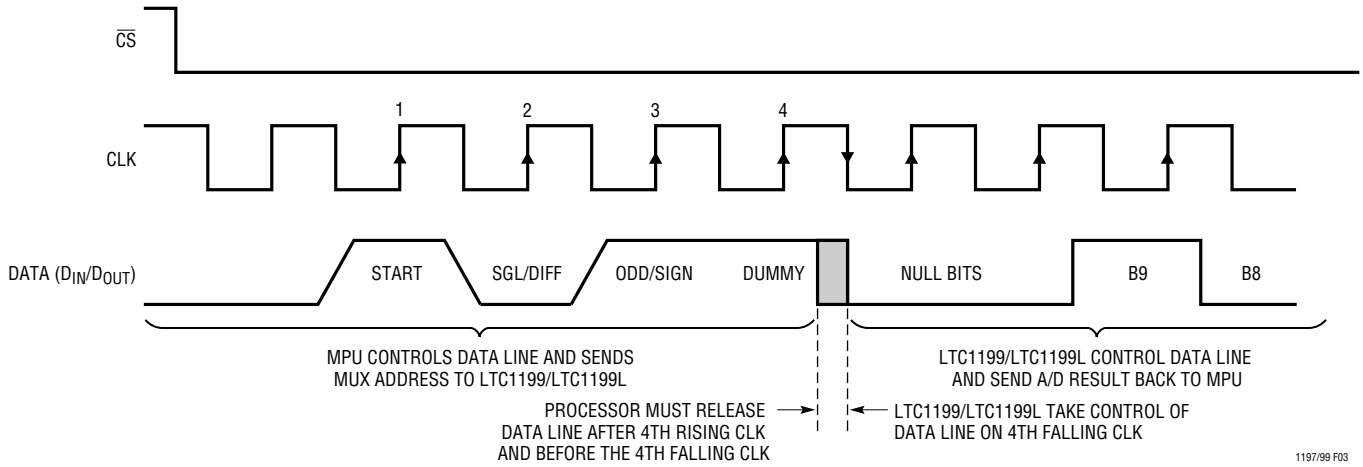


**Figure 3. LTC1199/LTC1199L Operation with $D_{IN}$ and $D_{OUT}$ Tied Together**

## APPLICATIONS INFORMATION

that convert continuously, the LTC1197/LTC1197L/LTC1199/LTC1199L will draw their normal operating power continuously. Several things must be taken into account to achieve micropower operation.

### Shutdown

Figures 1 and 2 show the operating sequence of the LTC1197/LTC1197L/LTC1199/LTC1199L. The converter draws power when the $\overline{CS}$ pin is low and powers itself down when that pin is high. If the $\overline{CS}$ pin is not taken all the way to ground when it is low and not taken to $V_{CC}$ when it is high, the input buffers of the converter will draw current. This current may be tens of microamps. It is worthwhile to bring the $\overline{CS}$ pin all the way to ground when it is low and all the way to $V_{CC}$ when it is high to obtain the lowest supply current.

When the $\overline{CS}$ pin is high (= supply voltage), the converter is in shutdown mode and draws only leakage current. The status of the $D_{IN}$ and CLK inputs have no effect on supply current during this time. There is no need to stop $D_{IN}$ and CLK with $\overline{CS}$ = high, except the MPU may benefit.

### Minimize $\overline{CS}$ Low Time

In systems that have significant time between conversions, lowest power drain will occur with the minimum $\overline{CS}$ low time. Bringing $\overline{CS}$ low, transferring data as quickly as possible, and then returning $\overline{CS}$ high will result in the lowest possible current drain. This minimizes the amount of time the device draws power. Even though the device draws more power at high clock rates, the net power is less because the device is on for a shorter time.

### $D_{OUT}$ Loading

Capacitive loading on the digital output can increase power consumption. A 100pF capacitor on the $D_{OUT}$ pin can add 200μA to the supply current at a 7.2MHz clock frequency. The extra 200μA goes into charging and discharging the load capacitor. The same goes for digital lines driven at a high frequency by any logic. The C•V•f currents must be evaluated and the troublesome ones minimized.

### Lower Supply Voltage

For lower supply voltages, LTC offers the LTC1197L/LTC1199L. These pin compatible devices offer specified performance to 2.7V supplies.

### OPERATING ON OTHER THAN 5V SUPPLIES

The LTC1197 operates from 4V to 9V supplies and the LTC1199 operates from 4V to 6V supplies. The LTC1197L/LTC1199L operate from 2.7V to 4V supplies. To use these parts at other than 5V supplies a few things must be kept in mind.

### Bypassing

At higher supply voltages, bypass capacitors on $V_{CC}$ and $V_{REF}$ if applicable, need to be increased beyond what is necessary for 5V. For a 9V supply a 10μF tantalum in parallel with a 0.1μF ceramic is recommended.

### Input Logic Levels

The input logic levels of $\overline{CS}$, CLK and $D_{IN}$ are made to meet TTL threshold levels on a 5V supply. When the supply voltage varies, the input logic levels also change. For the ADC to sample and convert correctly, the digital inputs have to meet logic low and high levels relative to the operating supply voltage (see typical curve of Digital Input Logic Threshold vs Supply Voltage). If achieving micropower consumption is desirable, the digital inputs must go rail-to-rail between $V_{CC}$ and ground (see ACHIEVING MICROPOWER PERFORMANCE section).

### Clock Frequency

The maximum recommended clock frequency is 7.2MHz for the LTC1197/LTC1199 running off a 5V supply and 3.5MHz for the LTC1197L/LTC1199L running off a 2.7V supply. With the supply voltage changing, the maximum clock frequency for the devices also changes (see the typical curve of Maximum Clock Rate vs Supply Voltage). If the maximum clock frequency is used, care must be taken to ensure that the device converts correctly.

# APPLICATIONS INFORMATION

### Mixed Supplies

It is possible to have a microprocessor running off a 5V supply and communicate with the ADC operating on 3V or 9V supplies. The requirement to achieve this is that the outputs of $\overline{CS}$, CLK and $D_{IN}$ from the MPU have to be able to trip the equivalent inputs of the ADC and the output of the ADC must be able to toggle the equivalent input of the MPU (see typical curve of Digital Input Logic Threshold vs Supply Voltage). With the LTC1197 operating on a 9V supply, the output of $D_{OUT}$ may go between 0V and 9V. The 9V output may damage the MPU running off a 5V supply. The way to solve this problem is to have a resistor divider on $D_{OUT}$ (Figure 4) and connect the center point to the MPU input. It should be noted that to get full shutdown, the $\overline{CS}$ input of the ADC must be driven to the $V_{CC}$ voltage. This would require adding a level shift circuit to the $\overline{CS}$ signal in Figure 4.

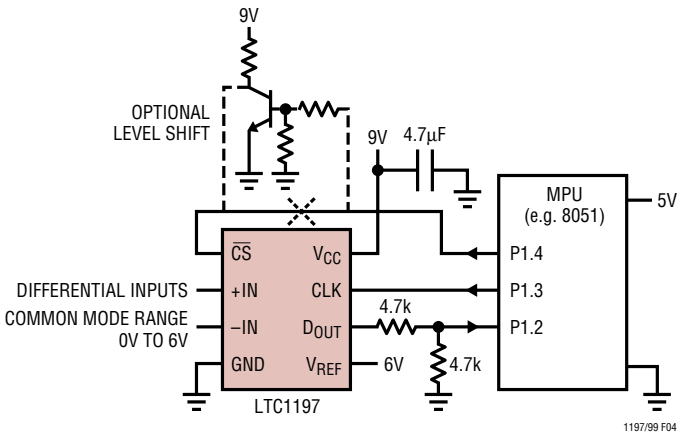


**Figure 4. Interfacing a 9V-Powered LTC1197 to a 5V System**

## BOARD LAYOUT CONSIDERATIONS

### Grounding and Bypassing

The LTC1197/LTC1197L/LTC1199/LTC1199L should be used with an analog ground plane and single point grounding techniques. The GND pin should be tied directly to the ground plane. The $V_{CC}$ pin should be bypassed to the ground plane using a 1µF tantalum capacitor with leads as short as possible. All analog inputs should be referenced directly to the single point ground. Digital inputs and outputs should be shielded from and/or routed away from the reference and analog circuitry.

### SAMPLE-AND-HOLD

The LTC1197/LTC1197L/LTC1199/LTC1199L provide a built-in sample-and-hold (S/H) function to acquire signals. The S/H of the LTC1197/LTC1197L acquires input signals for the "+" input relative to the "–" input during the $t_{SMPL}$ time (see Figure 1). However the S/H of the LTC1199/LTC1199L can sample input signals from the "+" input relative to ground and from the "–" input relative to ground in addition to acquiring signals from the "+" input relative to the "–" input (see Figure 5) during $t_{SMPL}$.

### Single-Ended Inputs

The sample-and-hold of the LTC1199/LTC1199L allows conversion of rapidly varying signals. The input voltage is sampled during the $t_{SMPL}$ time as shown in Figure 5. The sampling interval begins as the ODD/SGN bit is shifted in and continues until the falling CLK edge after the dummy bit is received. On this falling edge, the S/H goes into hold mode and the conversion begins.

### Differential Inputs

With differential inputs, the ADC no longer converts just a single voltage but rather the difference between two voltages. In this case, the voltage on the selected "+" input is still sampled and held and therefore may be rapidly time varying just as in single-ended mode. However, the voltage on the selected "–" input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the differencing operation may not be performed accurately. The conversion time is 10.5 CLK cycles. Therefore, a change in the "–" input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the "–" input this error would be:

$$V_{ERROR\ (MAX)} = V_{PEAK} \bullet 2 \bullet \pi \bullet f(\text{"–"}) \bullet 10.5/f_{CLK}$$

Where f("–") is the frequency of the "–" input voltage, $V_{PEAK}$ is its peak amplitude and $f_{CLK}$ is the frequency of the CLK. In most cases $V_{ERROR}$ will not be significant. For a 60Hz signal on the "–" input to generate a 1/4LSB error (1.22mV) with the converter running at CLK = 7.2MHz, its peak value would have to be 2.22V.

## APPLICATIONS INFORMATION

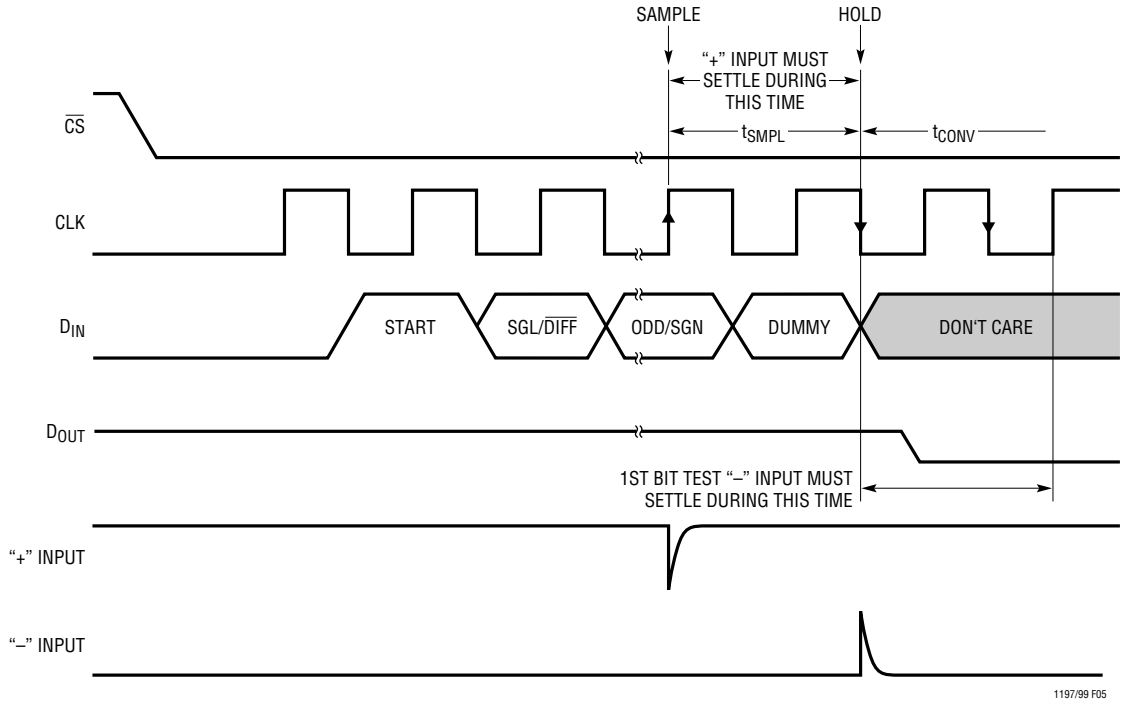


**Figure 5. LTC1199/LTC1199L "+" and "–" Input Settling Windows**

### ANALOG INPUTS

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1197/LTC1197L/LTC1199/LTC1199L have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem if source resistances are less than 200Ω or high speed op amps are used (e.g., the LT®1224, LT1191, LT1226 or LT1215). However, if large source resistances are used or if slow settling op amps drive the inputs, take care to ensure that the transients caused by the current spikes settle completely before the conversion begins.

#### "+" Input Settling

The input capacitor of the LTC1197/LTC1197L is switched onto the "+" input in the falling edge of $\overline{CS}$ and the sample time continues until the second falling CLK edge (see Figure 1). However, the input capacitor of the LTC1199/LTC1199L is switched onto "+" input after ODD/SGN is clocked into the ADC and remains there until the fourth falling CLK edge (see Figure 5). The sample time is 1.5 CLK cycles before conversion starts. The voltage on the "+" input must settle completely within $t_{SMPL}$ for the ADC to perform an accurate conversion. Minimizing $R_{SOURCE}^+$ and C1 will improve the input settling time (see Figure 6). If a large "+" input source resistance must be used, the sample time can be increased by using a slower CLK frequency.

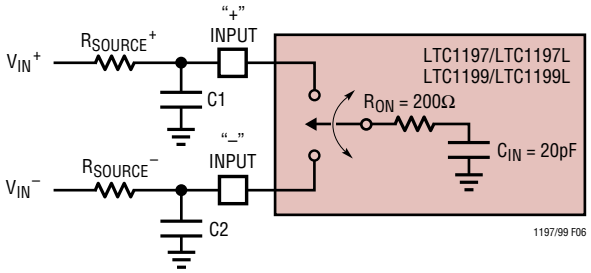


**Figure 6. Analog Equivalent Circuit**

#### "–" Input Settling

At the end of $t_{SMPL}$, the input capacitor switches to the "–" input and conversion starts (see Figures 1 and 5). During the conversion the "+" input voltage is effectively "held" by the sample-and-hold and will not affect the

## APPLICATIONS INFORMATION

conversion result. However, it is critical that the "–" input voltage settles completely during the first CLK cycle of the conversion time and be free of noise. Minimizing $R_{SOURCE}^-$ and C2 will improve settling time (see Figure 6). If a large "–" input source resistance must be used, the time allowed for settling can be extended by using a slower CLK frequency.

### Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figure 5). Again, the "+" and "–" input sampling times can be extended as described above to accommodate slower op amps. High speed op amps such as the LT1224, LT1191, LT1226 or LT1215 can be made to settle well even with the minimum settling window of 200ns which occurs at the maximum clock rate of 7.2MHz.

### Source Resistance

The analog inputs of the LTC1197/LTC1197L/LTC1199/LTC1199L look like a 20pF capacitor ($C_{IN}$) in series with a 200Ω resistor ($R_{ON}$) as shown in Figure 6. $C_{IN}$ gets switched between the selected "+" and "–" inputs once during each conversion cycle. Large external source resistors and capacitors will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle within the allowed time.

### RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 7. For large values of $C_F$ (e.g., 1µF), the capacitive input switching currents are averaged into a net DC current. Therefore, a filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 20pF(V_{IN}/t_{CYC})$ and is roughly proportional to $V_{IN}$. When running at the minimum cycle time of 2µs, the input current equals 50µA at $V_{IN}$ = 5V. In this case a filter resistor of 10Ω will cause 0.1LSB of full-scale error. If a larger filter resistor must be used, errors can be eliminated by increasing the cycle time.

### Input Leakage Current

Input leakage currents can also create errors if the source resistance gets too large. For instance, the maximum input leakage specification of 1µA (at 85°C) flowing through a source resistance of 1k will cause a voltage drop of 1mV or 0.2LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical curve of Input Channel Leakage Current vs Temperature).

### REFERENCE INPUTS

The voltage on the reference input of the LTC1197/LTC1197L defines the voltage span of the A/D converter. The reference input transient capacitive switching currents are due to the switched-capacitor conversion technique used in these ADCs (see Figure 8). During each bit test of the conversion (every CLK cycle), a capacitive current spike will be generated on the reference pin by the ADC. These current spikes settle quickly and do not cause a problem.

### Reduced Reference Operation

The minimum reference voltage of the LTC1199 is 4V and the minimum reference voltage of the LTC1199L is 2.7V because the $V_{CC}$ supply and reference are internally tied together. However, the LTC1197/LTC1197L can operate with reference voltages below 1V.

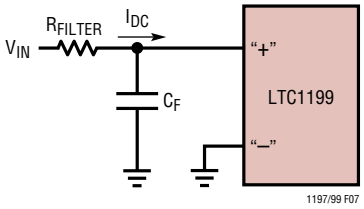


Figure 7. RC Input Filtering

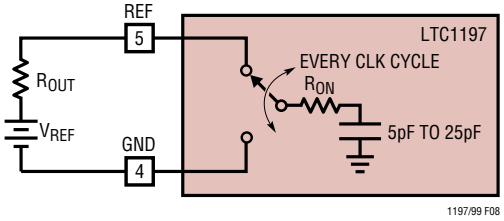


Figure 8. Reference Input Equivalent Circuit

## APPLICATIONS INFORMATION

The effective resolution of the LTC1197/LTC1197L can be increased by reducing the input span of the converter. The LTC1197/LTC1197L exhibits good linearity and gain over a wide range of reference voltages (see typical curves of Linearity and Full-Scale Error vs Reference Voltage). However, care must be taken when operating at low values of $V_{REF}$ because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. The following factors must be considered when operating at low $V_{REF}$ values.

1. Offset
2. Noise
3. Conversion speed (CLK frequency)

### Offset with Reduced $V_{REF}$

The offset of the LTC1197/LTC1197L has a larger effect on the output code when the ADC is operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of LTC1197 Offset Error vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of $V_{OS}$. For example, a $V_{OS}$ of 1mV which is 0.2LSB with a 5V reference becomes 1LSB with a 1V reference and 5LSBs with a 0.2V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the "–" input of the LTC1197/LTC1197L.

### Noise with Reduced $V_{REF}$

The total input referred noise of the LTC1197/LTC1197L can be reduced to approximately 200µV peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced.

For operation with a 5V reference, the 200µV noise is only 0.04LSB peak-to-peak. In this case, the LTC1197/LTC1197L noise will contribute virtually no uncertainty to the output code. However, for reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1V reference, this same 200µV noise is 0.2LSB peak-to-peak. This will reduce the range of input voltages over which a stable output code can be achieved. If the reference is further reduced to 200mV, the 200µV of noise becomes equal to 1LSB and a stable code may be difficult to achieve. In this case averaging readings may be necessary.

This noise data was taken in a very clean setup. Any setup-induced noise (noise or ripple on $V_{CC}$, $V_{REF}$ or $V_{IN}$) will add to the internal noise. The lower the reference voltage to be used, the more critical it becomes to have a clean, noise-free setup.

### Conversion Speed with Reduced $V_{REF}$

With reduced reference voltages the LSB step size is reduced and the LTC1197/LTC1197L internal comparator overdrive is reduced. Therefore, it may be necessary to reduce the maximum CLK frequency when low values of $V_{REF}$ are used.

### Input Divider

It is OK to use an input divider on the reference input of the LTC1197/LTC1197L as long as the reference input can be made to settle within the bit time at which the clock is running. When using a larger value resistor divider on the reference input the "–" input should be matched with an equivalent resistance.

### Bypassing Reference Input with Divider

Bypassing the reference input with a divider is also possible. However, care must be taken to make sure that the DC voltage on the reference input will not drop too much below the intended reference voltage.

## APPLICATIONS INFORMATION

### Signal-to-Noise Ratio

The signal-to-noise ratio (SNR) is the ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other frequency components at the A/D output. This includes distortion as well as noise products and for this reason it is sometimes referred to as signal-to-noise + distortion [S/(N + D)]. The output is band limited to frequencies from DC to one half the sampling frequency. Figure 9 shows spectral content from DC to 250kHz which is 1/2 the 500kHz sampling rate.

### Effective Number of Bits

The effective number of bits (ENOBs) is a measurement of the resolution of an ADC and is directly related to the S/(N + D) by the equation:

$$ENOB = [S/(N + D) - 1.76]/6.02$$

where S/(N + D) is expressed in dB. At the maximum sampling rate of 500kHz the LTC1197 maintains 9.5 ENOBs or better to 200kHz. Above 200kHz the ENOBs gradually decline, as shown in Figure 10, due to increasing second harmonic distortion. The noise floor remains approximately 100dB.

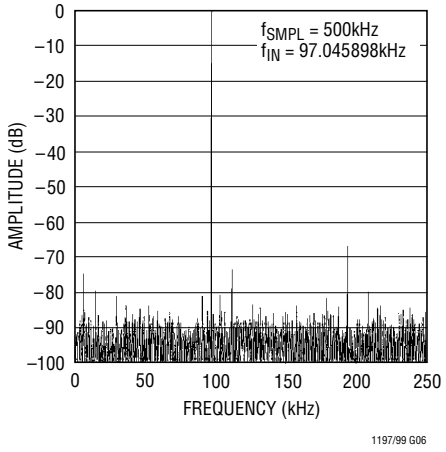


**Figure 9. This Clean FFT of a 97kHz Input Shows Remarkable Performance for an ADC Sampling at the 500kHz Rate**

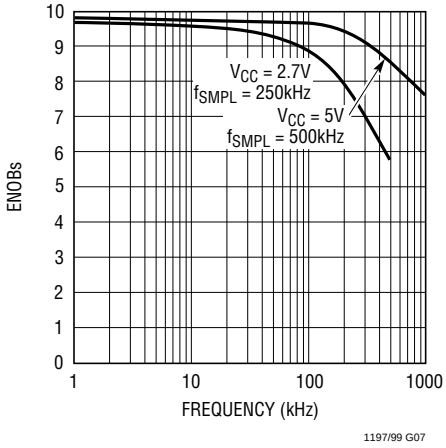


**Figure 10. Dynamic Accuracy is Maintained Up to an Input Frequency of 200kHz for the LTC1197 and 50kHz for the LTC1197L**

# TYPICAL APPLICATIONS

## MICROPROCESSOR INTERFACES

The LTC1197/LTC1197L/LTC1199/LTC1199L can interface directly (without external hardware to most popular microprocessor (MPU) synchronous serial formats (see Table 1). If an MPU without a dedicated serial port is used, then three or four of the MPU's parallel port lines can be programmed to form the serial link. Included here is one serial interface example and one example showing a parallel port programmed to form the serial interface.

### Motorola SPI (MC68HC05C4, MC68HC11)

The MC68HC05C4 has been chosen as an example of an MPU with a dedicated serial port. This MPU transfers data MSB-first and in 8-bit increments. With two 8-bit transfers, the A/D result is read into the MPU. The first 8-bit transfer sends the $D_{IN}$ word to the LTC1199 and clocks the two ADC MSBs (B9 and B8) into the MPU. The second 8-bit transfer clocks the next 8 bits, B7 through B0, of the ADC into the MPU.

ANDing the first MPU received byte with 03Hex clears the six MSBs. Notice how the position of the start bit in the $D_{IN}$ word is used to position the A/D result so that it is right-justified in two memory locations.

**Table 1. Microprocessor with Hardware Serial Interfaces Compatible with the LTC1197/LTC1197L/LTC1199/LTC1199L**

| PART NUMBER | TYPE OF INTERFACE |
|---|---|
| **Motorola** | |
| MC6805S2,S3 | SPI |
| MC68HC11 | SPI |
| MC68HC05 | SPI |
| **RCA** | |
| CDP68HC05 | SPI |
| **Hitachi** | |
| HD6301 | SCI Synchronous |
| HD6303 | SCI Synchronous |
| HD6305 | SCI Synchronous |
| HD63701 | SCI Synchronous |
| HD63705 | SCI Synchronous |
| HD64180 | CSI/O |
| **National Semiconductor** | |
| COP400 Family | MICROWIRE™ |
| COP800 Family | MICROWIRE/PLUS™ |
| NSC8050U | MICROWIRE/PLUS |
| HPC16000 Family | MICROWIRE/PLUS |
| **Texas Instruments** | |
| TMS7000 Family | Serial Port |
| TMS320 Family | Serial Port |
| **Microchip Technology** | |
| PIC16C60 Family | SPI, SCI Synchronous |
| PIC16C70 Family | SPI, SCI Synchronous |

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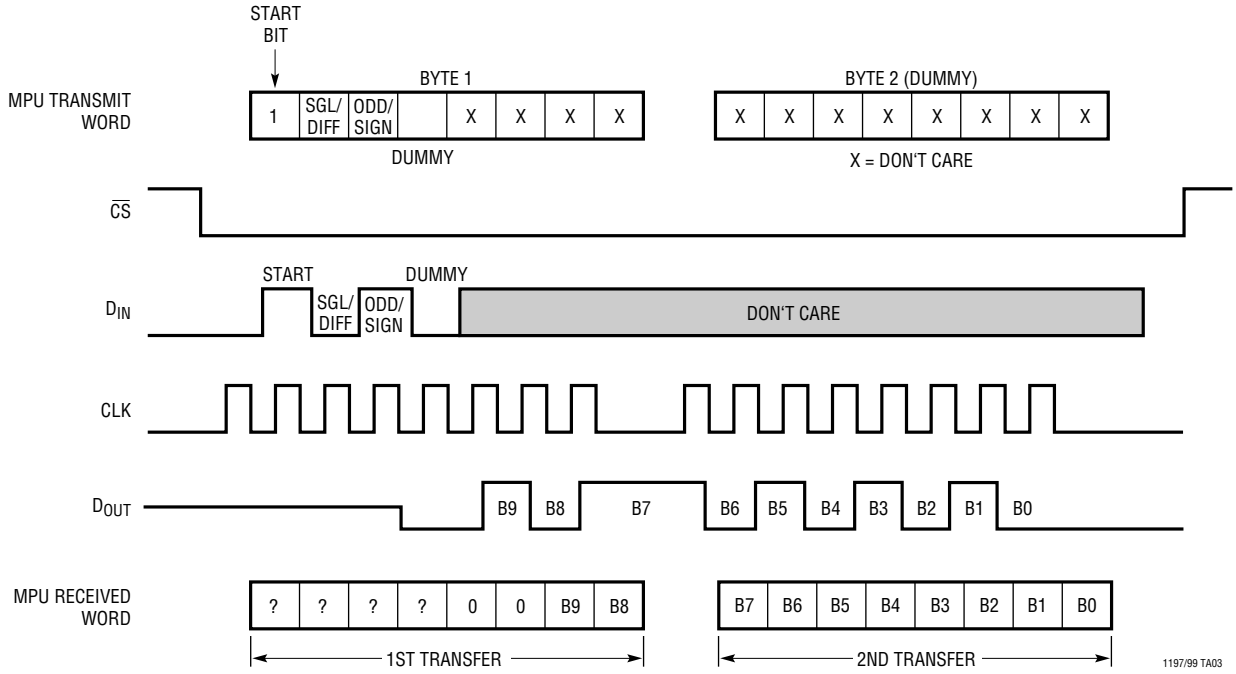
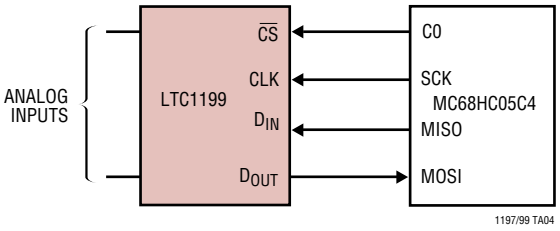
# TYPICAL APPLICATIONS

### Data Exchange Between LTC1199 and MC68HC05C4

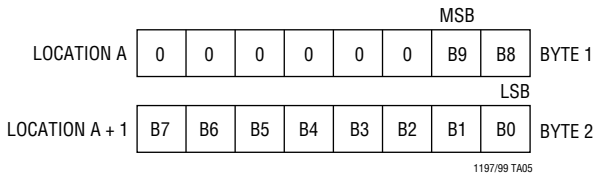



### Hardware and Software Interface to Motorola MC68HC05C4




| LABEL | MNEMONIC | COMMENTS |
|---|---|---|
| START | BCLRn | Bit 0 Port C goes low ($\overline{CS}$ goes low) |
| | LDA | Load LTC1199 $D_{IN}$ word into ACC |
| | STA | Load LTC1199 $D_{IN}$ word into SPI from ACC<br>Transfer begins |
| | TST | Test status of SPIF |
| | BPL | Loop to previous instruction if not done<br>with transfer |
| | LDA | Load contents of SPI data register<br>into ACC ($D_{OUT}$ MSBs) |
| | STA | Start next SPI cycle |
| | AND | Clear 6 MSBs of the first $D_{OUT}$ word |
| | STA | Store in memory location A (MSBs) |
| | TST | Test status of SPIF |
| | BPL | Loop to previous instruction if not done<br>with transfer |
| | BSETn | Set B0 of Port C ($\overline{CS}$ goes high) |
| | LDA | Load contents of SPI data register into<br>ACC. ($D_{OUT}$ LSBs) |
| | STA | Store in memory location A + 1 (LSBs) |

### $D_{OUT}$ from LTC1199 Stored in MC68HC05C4

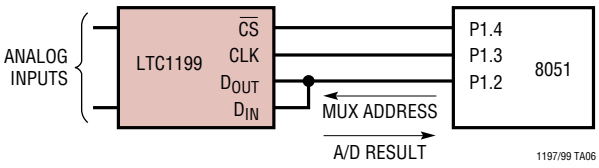


# TYPICAL APPLICATIONS

### Interfacing to the Parallel Port of the Intel 8051 Family

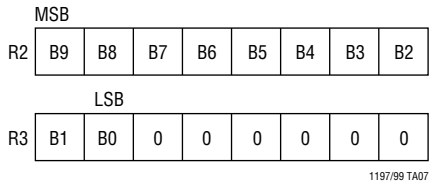
The Intel 8051 has been chosen to demonstrate the interface between the LTC1199 and parallel port microprocessors. Normally the $\overline{CS}$, CLK and $D_{IN}$ signals would be generated on three port lines and the $D_{OUT}$ signal read on a fourth port line. This works very well. However, we will demonstrate here an interface with the $D_{IN}$ and $D_{OUT}$ of the LTC1199 tied together as described in the SERIAL INTERFACE section. This saves one wire.

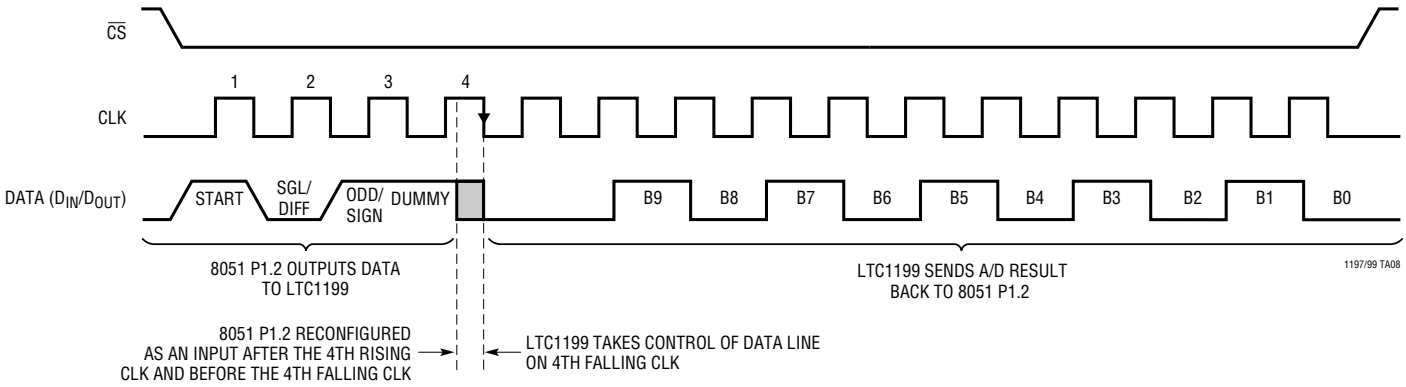
The 8051 first sends the start bit and MUX address to the LTC1199 over the data line connected to P1.2. Then P1.2 is reconfigured as an input (by writing to it a one) and the 8051 reads back the 8-bit A/D result over the same data line.




| LABEL | MNEMONIC | OPERAND | COMMENTS |
|---|---|---|---|
| | MOV | A, #FFH | $D_{IN}$ word for LTC1199 |
| | SETB | P1.4 | Make sure $\overline{CS}$ is high |
| | CLR | P1.4 | $\overline{CS}$ goes low |
| | MOV | R4, #04 | Load counter |
| LOOP 1 | RLC | A | Rotate $D_{IN}$ bit into Carry |
| | CLR | P1.3 | CLK goes low |
| | MOV | P1.2, C | Output $D_{IN}$ bit into Carry |
| | SETB | P1.3 | CLK goes high |
| | DJNZ | R4, LOOP 1 | Next bit |
| | MOV | P1, #04 | Bit 2 becomes an input |
| | CLR | P1.3 | CLK goes low |
| | MOV | R4, #0AH | Load counter |
| LOOP | MOV | C, P1.2 | Read data bit into Carry |
| | RLC | A | Rotate data bit into ACC |
| | SETB | P1.3 | CLK goes high |
| | CLR | P1.3 | CLK goes low |
| | DJNZ | R4, LOOP | Next bit |
| | MOV | R2, A | Store MSBs in R2 |
| | MOV | C, P1.2 | Read data bit into Carry |
| | SETB | P1.3 | CLK goes high |
| | CLR | P1.3 | CLK goes low |
| | CLR | A | Clear ACC |
| | RLC | A | Rotate data bit from Carry to ACC |
| | MOV | C, P1.2 | Read data bit into Carry |
| | RRC | A | Rotate right into ACC |
| | RRC | A | Rotate right into ACC |
| | MOV | R3, A | Store LSBs in R3 |
| | SETB | P1.4 | $\overline{CS}$ goes high |

**$D_{OUT}$ from LTC1199 Stored in 8051 RAM**



## TYPICAL APPLICATIONS

### A "Quick Look" Circuit for the LTC1197

Users can get a quick look at the function and timing of the LTC1197 by using the following simple circuit (Figure 11). $V_{REF}$ is tied to $V_{CC}$. $V_{IN}$ is applied to the + IN input and the – IN input is tied to the ground. $\overline{CS}$ is driven at 1/16 the clock rate by the 74HC161 and $D_{OUT}$ outputs the data. The output data from the $D_{OUT}$ pin can be viewed on an oscilloscope that is set up to trigger on the falling edge of $\overline{CS}$ (Figure 12). Note that after the LSB is clocked out, the LTC1197 clocks out zeros until $\overline{CS}$ goes high. Also note that with the resistor divider on $D_{OUT}$ the output goes midway between $V_{CC}$ and ground when in the high impedance mode.

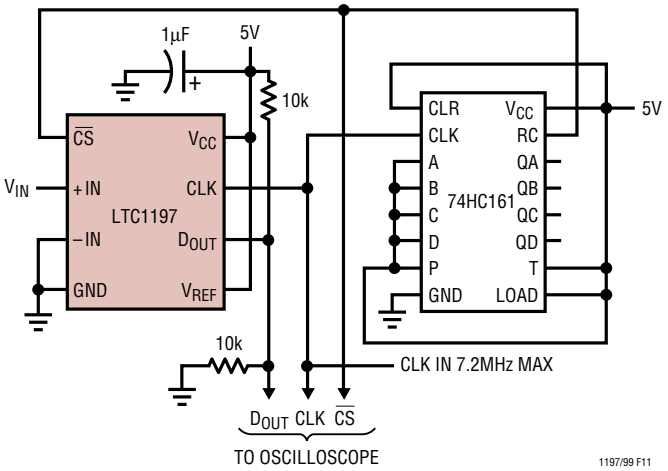



**Figure 11. "Quick Look" Circuit for the LTC1197**

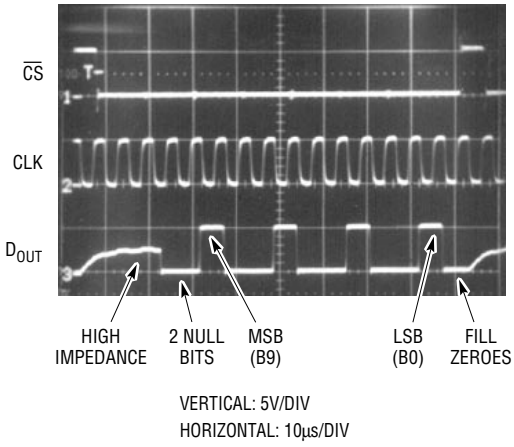



**Figure 12. Scope Photo of the LTC1197 "Quick Look" Circuit Waveforms Showing A/D Output 1001001001 ($249_{HEX}$)**

# TYPICAL APPLICATIONS

### Resistive Touchscreen Interface

Figure 13 shows the LTC1199 in a 4-wire resistive touchscreen application. Transistor pairs Q1-Q3, Q2-Q4 apply 5V and ground to the X axis and Y axis, respectively. The LTC1199, with its 2-channel multiplexer, digitizes the voltage generated by each axis and transmits the conversion results to the system's processor through a serial interface. RC combinations R1C1, R2C2 and R3C3 form lowpass filters that attenuate noise from possible sources such as the processor clock, switching power supplies and bus signals. The 74HC14 inverter is used to detect screen contact both during a conversion sequence and to trigger its start. Using the single channel LTC1197, 5-wire resistive touchscreens are as easily accommodated.

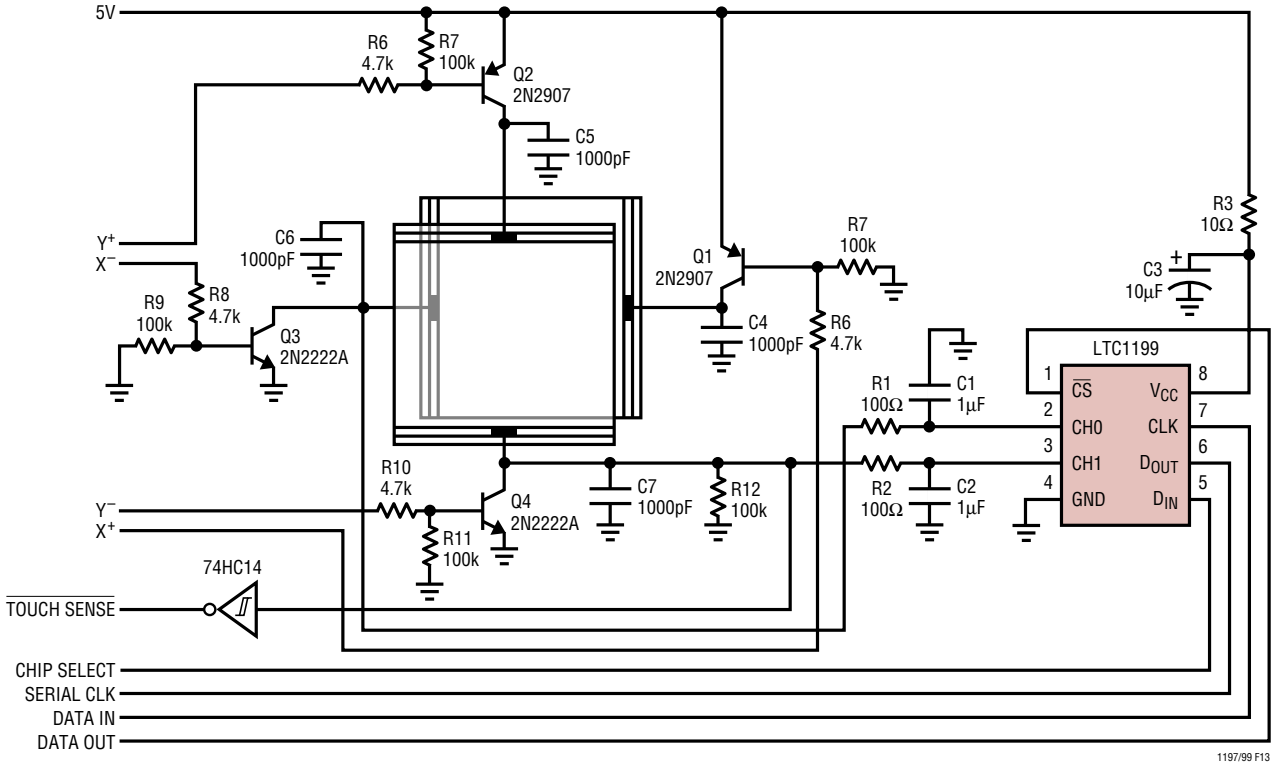



**Figure 13. The LTC1199 Digitizes Resistive Touchscreen X and Y Axis Voltages. The ADC's Auto Shutdown Feature Helps Maximize Battery Life in Portable Touchscreen Equipment**

## TYPICAL APPLICATIONS

### Battery Current Monitor

The LTC1197L/LTC1199L are ideal for 3V systems. Figure 14 shows a 2.7V to 4V battery current monitor that draws only 45μA at 3V from the battery it monitors, sampling at a 1Hz rate. To minimize supply current, the microprocessor uses the LTC1152 SHDN pin to turn on the op amp prior to making a measurement and then turn it off after the measurement has been made. The battery current is sensed with the 0.005Ω resistor and amplified by the LTC1152. The LTC1197L digitizes the amplifier output and sends it to the microprocessor in serial format. After each sample the LTC1197L automatically powers down. The LT1004 provides the full-scale reference for the ADC. The circuit's 45μA supply current is dominated by the reference and the op amp. The circuit can be located near the battery and data transmitted serially to the microprocessor.

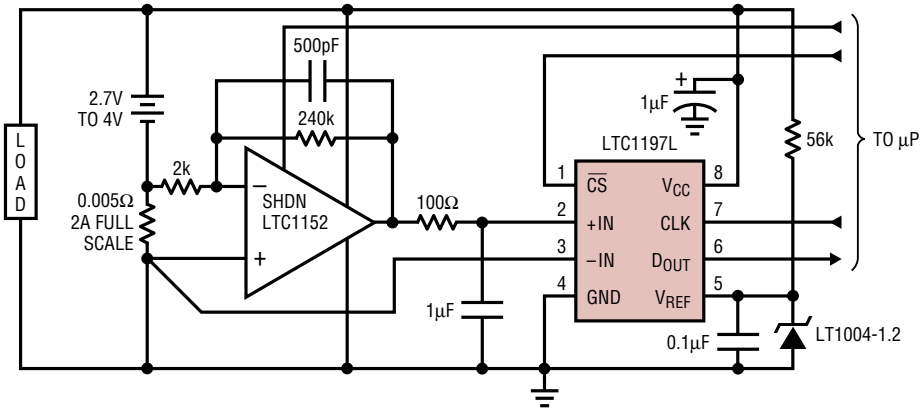
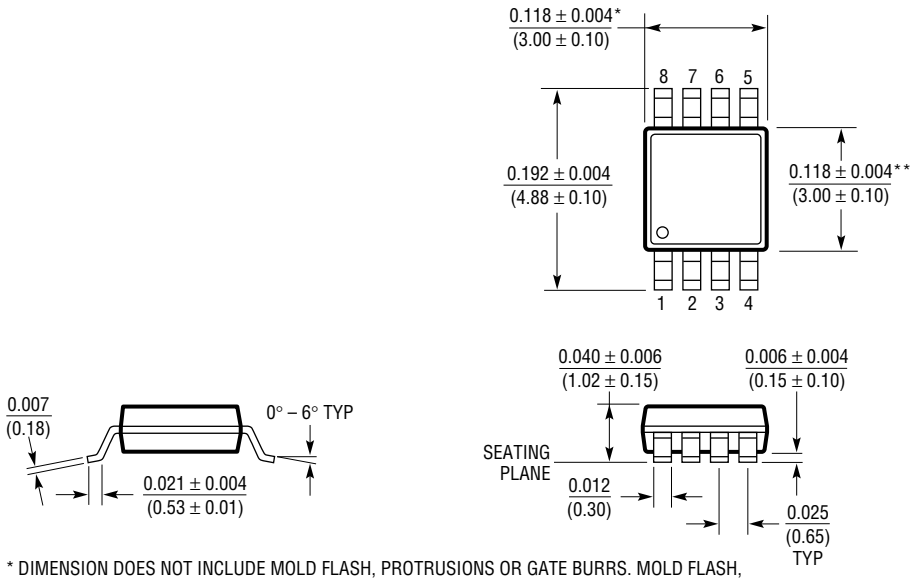



**Figure 14. This 0A to 2A Battery Current Monitor Draws Only 45μA from a 3V Battery**

## PACKAGE DESCRIPTION

**Dimensions in inches (millimeters), unless otherwise noted.**

### MS8 Package
### 8-Lead Plastic MSOP
(LTC DWG # 05-08-1660)

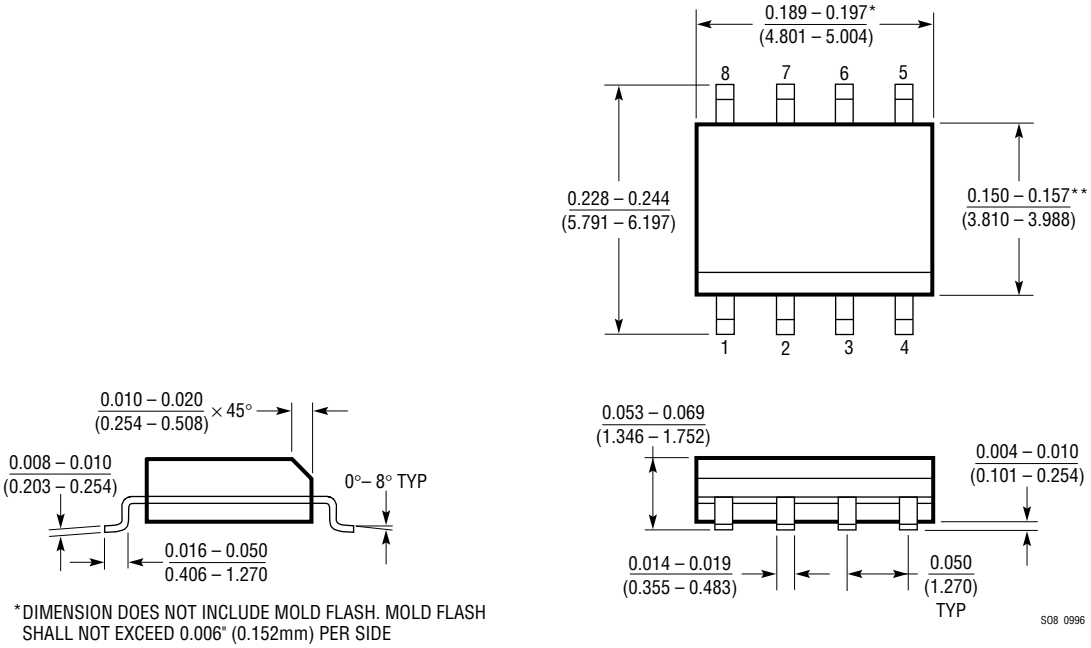



* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

MSOP08 0596

### S8 Package
### 8-Lead Plastic Small Outline (Narrow 0.150)
(LTC DWG # 05-08-1610)




*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

SO8 0996

## RELATED PARTS

| PART NUMBER | SAMPLE RATE | POWER DISSIPATION | DESCRIPTION |
|---|---|---|---|
| **8-Bit, Pin Compatible Serial Output ADCs** | | | |
| LTC1096/LTC1096L | 33kHz/15kHz | 0.5mW* | 1-Channel, Unipolar Operation with Reference Input, 5V/3V |
| LTC1098/LTC1098L | 33kHz/15kHz | 0.6mW* | 2-Channel, Unipolar Operation, 5V/3V |
| LTC1196 | 1MHz/383kHz | 20mW | 1-Channel, Unipolar Operation with Reference Input, 5V/3V |
| LTC1198 | 750kHz/287kHz | 20mW* | 2-Channel, Unipolar Operation, 5V/3V |
| **10-Bit Serial I/O ADCs** | | | |
| LTC1090 | 25kHz | 5mW | 8-Channel, Bipolar or Unipolar Operation, 5V |
| LTC1091 | 30kHz | 7.5mW | 2-Channel, Unipolar Operation, 5V |
| LTC1092 | 35kHz | 5mW | 2-Channel, Unipolar Operation with Reference Input, 5V |
| LTC1093 | 25kHz | 5mW | 6-Channel, Bipolar or Unipolar Operation, 5V |
| LTC1094 | 25kHz | 5mW | 8-Channel, Bipolar or Unipolar Operation, 5V |
| LTC1283 | 15kHz | 0.5mW | 8-Channel, Bipolar or Unipolar Operation, 3V |
| **12-Bit Serial I/O ADCs** | | | |
| LTC1285/LTC1288 | 7.5kHz/6.6kHz | 0.4mW/0.6mW* | 1-Channel with Reference (LTC1285), 2-Channel (LTC1288), 3V |
| LTC1286/LTC1298 | 12.5kHz/11.1kHz | 1.3mW/1.7mW* | 1-Channel with Reference (LTC1286), 2-Channel (LTC1298), 5V |
| LTC1287 | 30kHz | 3mW | 1-Channel, Unipolar Operation, 3V |
| LTC1289 | 33kHz | 3mW | 8-Channel, Bipolar or Unipolar Operation, 3V |
| LTC1290 | 50kHz | 30mW | 8-Channel, Bipolar or Unipolar Operation, 5V |
| LTC1291 | 54kHz | 30mW | 2-Channel, Unipolar Operation, 5V |
| LTC1292 | 60kHz | 30mW | 1-Channel, Unipolar Operation, 5V |
| LTC1293 | 46kHz | 30mW | 6-Channel, Bipolar or Unipolar Operation, 5V |
| LTC1294 | 46kHz | 30mW | 8-Channel, Bipolar or Unipolar Operation, 5V |
| LTC1296 | 46kHz | 30mW | 8-Channel, Bipolar or Unipolar Operation, 5V |
| LTC1297 | 50kHz | 30mW | 1-Channel, Unipolar Operation, 5V |
| LTC1400 | 400kHz | 75mW** | 1-Channel, Bipolar or Unipolar Operation, Internal Reference, 5V |
| LTC1594/LTC1594L | 20kHz/12.5kHz | 1.6mW/0.5mW* | 4-Channel, Unipolar Operation, 5V/3V |
| LTC1598/LTC1598L | 20kHz/12.5kHz | 1.6mW/0.5mW* | 8-Channel, Unipolar Operation, 5V/3V |
| **PART NUMBER** | **DESCRIPTION** | | **COMMENTS** |
| **Low Power References** | | | |
| LT1004 | Micropower Voltage Reference | | 0.3% Max, 20ppm/°C Typ, 10µA Max |
| LT1019 | Precision Bandgap Reference | | 0.05% Max, 5ppm/°C Max |
| LT1236 | Precision Low Noise Reference | | 0.05% Max, 5ppm/°C Max, SO Package |
| LT1460-2.5 | Micropower Precision Series Reference | | 0.075% Max, 10ppm/°C Max, 130µA Max, SO Package |
| LT1634 | Micropower Precision Reference | | 0.05% Max, 25ppm/°C Max, 7µA Max, MSOP Package |

*These devices have auto shutdown which reduces power dissipation linearly as sample rate is reduced from $f_{SMPL(MAX)}$.
**Has nap and sleep shutdown modes.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