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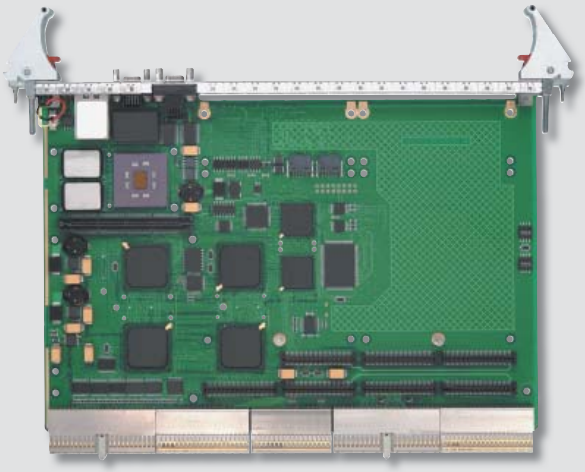
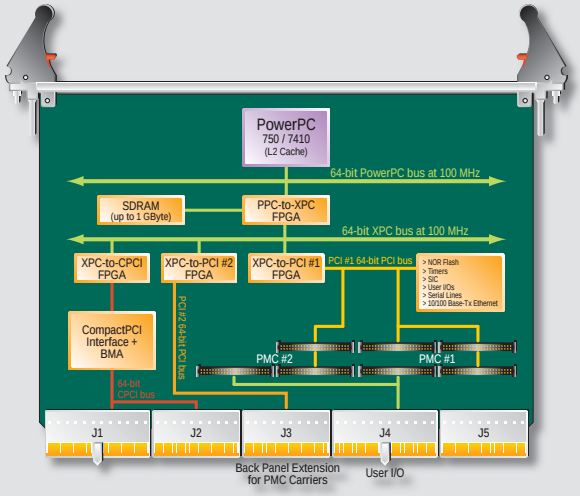
CPCI PROCESSOR BOARDS

RIOC 4065

PowerPC-Based 6U CompactPCI Twin PCI Bus Real-Time Processor Board





HIGHLIGHTS

BRUTE FORCE POWER

- PowerPC 750 at 400 MHz with 1 MByte external L2 cache
- PowerPC 750 at 500 MHz with 1 MByte external L2 cache
- PowerPC 7410 at 500 MHz with 2 MBytes external L2 cache

GLOBAL MEMORY AT CACHE SPEED

- Up to 1 GByte SDRAM at 800 MBytes/s peak

TWIN 64-BIT PCI BUS ARCHITECTURE

- Two onboard dual PMC slots
- Transparent multiprocessing

HIGH-PERFORMANCE COMPACTPCI INTERFACE

- CES-designed PowerPC-to-CompactPCI bridge
- Automatic selection of CompactPCI slot or peripheral slot
- Hot-Swap compliant (PICMG® 2.1, revision 1.0)

TOTALLY UNDER CONTROL

- CES-designed direct PowerPC-to-PCI bridges
- Optimized bus architecture for maximum bus bandwidth
- Multiple arbiters for memory bandwidth allocation
- User-controlled interrupt strategies
- Remotely controllable with CES-designed reprogram and reconfiguration toolkit
- JTAG 1149-1 support

TOTALLY SCALABLE

- PCI 64-bit based on CompactPCI backplane J3 connector
- Up to six PMCs (CES computing cores) controlled by the same RIOC 4065

NATIVELY MULTIPROCESSOR ORIENTED

- High-speed synchronization and message passing
- Global shared memory
- Independent sixteen-channel DMA on CompactPCI

STATE-OF-THE-ART SOFTWARE

- BSPs for LynxOS®, VxWorks®, Integrity®, TimeSys® and Linux® with CES-enhanced specifications
- Network protocols on PCI and CompactPCI (TCP/IP and high-speed channel mode - CES BP-Net)

ADDITIONAL FEATURES

- 16 MBytes of Flash EPROM
- Full duplex 10/100 Base-Tx Ethernet
- Two serial interface ports (RS-232)

GENERAL DESCRIPTION

The RIOC 4065 confirms CES' choice of the winning combination for real-time applications: the PowerPC CPU and the PCI backbone bus.

The RIOC 4065 has been designed to provide a function-level compatibility with the RIOC 4064. It offers two onboard PMC slots as well as a PMC extension system. Compared to the RIOC 4064, it provides a massive speed improvement (by a factor of four), due to an extremely fast global memory and a bandwidth control logic, which allocates the throughput between the CPU, CompactPCI and the two 64-bit PCI buses. It also features FPGA-based CES-designed PowerPC-to-PCI and PowerPC-to-CompactPCI interfaces to reduce the risk of long-term maintenance.

This machine uses the latest CPU, CompactPCI and PCI technological features, including up to 2 MBytes L2 cache, direct CompactPCI-to-memory interface and two independent PCI buses with one directly available on the J3 connector.

It also follows all of the recommendations of the telecom requirement: Hot-Swap, High Availability, JTAG test bus and incorporates a comprehensive set of software maintenance tools.

The RIOC 4065 combines a sustained 100 MBytes/s bandwidth on CompactPCI with 400 MBytes/s global memory bandwidth shared between the different buses. All of these features are totally equipped with an advanced API, which make the RIOC the ideal platform for large computing intensive applications such as aircraft simulation, test and validation, high-speed data-acquisition systems, as well as large ATM switch controllers and base stations.

The integration risk for strategic applications has been significantly reduced by the use of FPGA-based PowerPC-to-PCI and PowerPC-to-CompactPCI bridges, where all of the missing functions in existing commercial bridges have been added and fine-tuning of the application has been made possible.

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COMPACTPCI INTERFACE

The RIOC processor boards benefit from an enhanced CompactPCI interface featuring a direct path between the PowerPC bus and CompactPCI. This architecture improves the cycle latency for CompactPCI-to-local system memory transactions. Special emphasis has been placed on optimizing the interaction between the two buses.

The RIOC processor boards can be used either as system slot controllers or as peripheral slot boards. The CompactPCI master and slave windows are configured by pages (master: 64 pages of 16 MBytes, slave A32: 512 pages of 1 MByte, slave A64: 4 GBytes direct-addressing), which can be allocated dynamically. This MMU mechanism in the CES PowerPC-to-CompactPCI bridge provides a true safe multiprocessor operation on CompactPCI with up to four local processors.

The RIOC processor boards are equipped with a fully hardware-driven chained DMA block transfer engine, which offers sixteen DMA channels with accesses through dedicated FIFOs.

Inter-Processor Communication

The CompactPCI interface is equipped with the same communication FIFOs as the two native PCI buses.

The CES CompactPCI bridge provides indivisible cycles on CompactPCI for rapid and efficient communication and synchronization in a hard real-time multiprocessor environment, which requires microsecond-level communication.

COMPACTPCI SPECIFICATIONS

- 64-bit interface
- Automatic selection of system and peripheral slot functionalities
- Sixteen independent DMA channels with dedicated signaling FIFOs
- Direct transfer CompactPCI-to-global memory without PCI stage
- CompactPCI master mode: 1 GByte master addressing space (64 user-programmable windows of 16 MBytes)
- CompactPCI slave mode: 64-bit: 4 GBytes CompactPCI slave direct-addressing space
- CES BP-Net connectivity for network protocols and high-speed channel modes

SOFTWARE

The RIOC processor boards come with PPCMon, a powerful low-level extended PowerPC monitor.

CES has ported the most popular real-time operating systems on the RIOC processor boards (LynxOS®, VxWorks®, Integrity®, TimeSys® and Linux®). Special care has been taken to exploit all of the hardware features of the board to increase the performance of the operating system features. Several functions have been added to the standard operating system BSPs to provide the user with a comfortable development environment. Amongst them, CES BP-Net, which is installed by default as the standard multiprocessing package. It provides a high-performance inter-processor communication / synchronization and is available over CompactPCI and PCI through a common API. Network services such as TCP/IP are also available with CES BP-Net.

CES' philosophy is to offer a BSP, which is independent from the operating system. This means it will offer the user a complete set of functions accessing nearly all of the clusters or VHDL blocks on the board, which is the same for all supported operating systems. Portability of the application is therefore guaranteed for the user. CES can also assist in the portability study, as well as its realization.

VERSIONS AVAILABLE

RIOC 4065D	PowerPC 750 at 400 MHz, 1 MByte L2 cache
RIOC 4065A	PowerPC 750 at 500 MHz, 1 MByte L2 cache
RIOC 4065C	PowerPC 7410 at 500 MHz, 2 MBytes L2 cache

For more detailed information about any of our products, please do not hesitate to contact us.

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