
# IP-DIGITAL48

# &

# IP-DUALPIT2

## User Manual



Part Number: 89010470 Rev. 1.1

20050413

# IP-DIGITAL48 & IP-DUALPIT2

## High-Density Digital I/O

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# 1 Product Description

IP-DIGITAL48 and IP-DUALPIT2 are two IndustryPack® compatible modules constructed from the same printed circuit board. Each has its own IDROM and factory configuration. However, by changing solder connections, you may convert from one product to the other, or to one of many intermediate configurations.

The IP-DIGITAL48 and the IP-DUALPIT2 are drop-in replacements for the IP-Digital-48 and the IP-Dual-PIT.

The IP-DIGITAL48 and IP-DUALPIT2 emulate two Motorola MC68230 Programmable Interface/Timer (PI/T) ICs (without DMA). Together with the IDROM and additional logic they are integrated in a Xilinx Spartan II FPGA. The FPGA is configured at power up from a serial configuration PROM which is mounted in a socket.

The IP-DUALPIT2 is configured to take advantage of the more sophisticated features of the PI/Ts. Timer, I/O, interrupts, and hardware mediated double-buffered data transfer are supported. 32 general purpose digital I/O lines are available in several programmable modes.

The IP-DIGITAL48 is configured to maximize the number of digital I/O lines. Multiple modes are available via programming.

Users may reconfigure either IndustryPack to implement desired features, while maximizing the number of available I/O lines.

Each MC68230 provides up to three 8-bit I/O ports, one 24-bit timer and five separate interrupt vectors. Ports may be software configured for bit I/O, unidirectional 8-bit and 16-bit I/O, or bi-directional 8-bit and 16-bit I/O. Port modes include single and double buffering, with strobe and handshake options. Due to pin limitations, not all options are available simultaneously.

The IP-DIGITAL48 and IP-DUALPIT2, like all IndustryPacks, use a 50-pin flat ribbon cable connected to the carrier board for I/O. The IP-DUALPIT2 configuration uses 32 lines for bit I/O, 8-bit or 16-bit (unidirectional, bi-directional, single or double buffered) plus eight lines as programmable handshake lines or timer I/O with alternate ground wires.

IP-DIGITAL48 is configured for 48 general purpose lines of bit I/O. These lines may also be used for 8-bit and 16-bit I/O with handshake lines. Timer I/O is also available. In this configuration 48 of the 50 cable lines are I/O, with two ground lines. In this configuration, user provided cabling with additional grounds may be required for high speed operation. Interrupts are unavailable if all 48 lines are used for I/O.

IP-DIGITAL48 and IP-DUALPIT2 connect user I/O lines to the Spartan2 inputs and outputs via 47 ohm serial resistors. They are TTL compatible (output voltage 3.3V, 5V tolerant). Source and sink current is 2mA and leakage current is 10 $\mu$A.

Each of the two MC68230s has a 24-bit programmable timer. Timer clock source is a 250 KHz internal clock or a user provided external clock. Using the internal clock, a resolution of 4 $\mu$s with a maximum time of 64 seconds is available. The timer may be used as a counter, watchdog, or square wave generator. It may generate single or periodic interrupts. An external gate signal as well as an external timer output is available. In general, it is easier to use the timers starting from an IP-DIGITAL48 configuration than from an IP-DUALPIT2 configuration.

All communication between the IndustryPack and the carrier board is performed byte-wide.

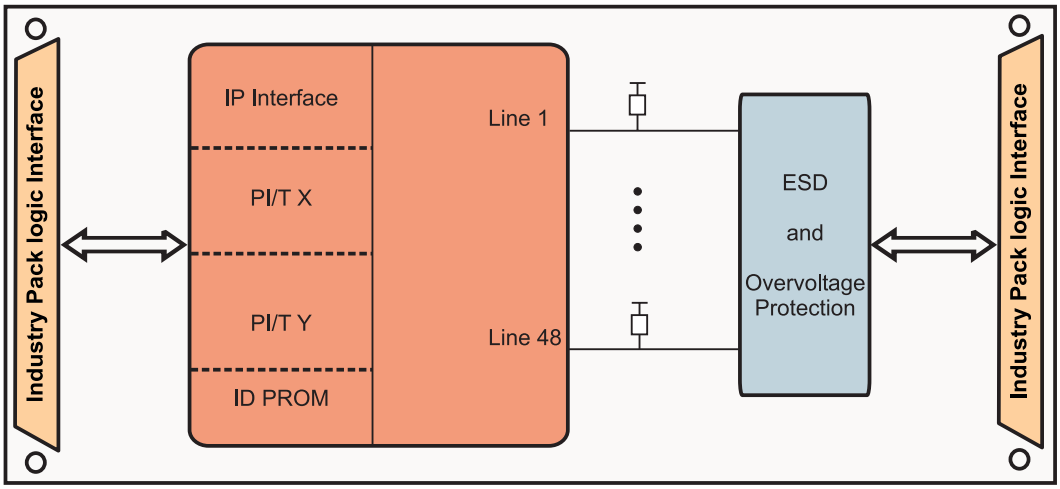


Figure 1-1 : Block Diagram

## 1.1 I/O Circuit

The I/O lines are realized with an Input / Output register built in the XILINX FPGA and a few external passive devices.

**Please note that the length of flat cables connected to the module should be kept very short to prevent large cross talk.**

In the following figure only one I/O line is shown.

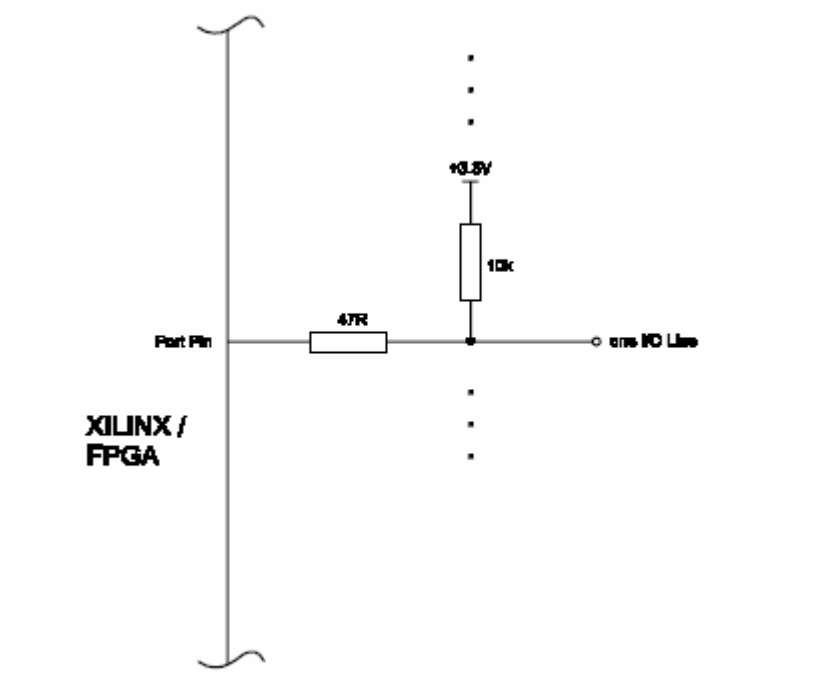


Figure 1-2 : I/O Circuitry

# 2 Technical Specification

| | | |
|---|---|---|
| **IP Interface** | | |
| **Interface** | Single Size IndustryPack® Logic Interface compliant to ANSI/VITA 4-1995 | |
| **ID ROM Data** | Format I | |
| **I/O Space** | Used | |
| **Memory Space** | Not used | |
| **Interrupts** | Int1 / Int2 used | |
| **DMA** | Not supported | |
| **Clock Rate** | 8MHz | |
| **Module Type** | Type I | |
| **Wait States** | ID reads: 0 wait states<br>I/O reads and writes: 1 wait state<br>Interrupt cycles: 1 wait state | |
| **I/O Interface** | | |
| **Interface Connector** | 50-conductor flat cable | |
| **Termination** | 10kohms resistor as pull up to 3.3V for each I/O line of port A and B, H2, H4, PIRQ#, TIRQ# | |
| **Input Voltage Range** | -0.5V to +5.5V | |
| **Output 'High' Voltage** | +3.3V | |
| **Output 'Low' Current** | -2mA on port A and B, H2, H4 and port C (line 0-2,4,6,7)<br>-8mA on port C (line 3 and 5) | |
| **Output 'High' Current** | +2mA on port A and B, H2, H4 and port C (line 0-2,4,6,7)<br>+8mA on port C (line 3 and 5) | |
| **Physical Data** | | |
| **Power Requirements** | 100mA typical @ +5V DC, all lines are inputs | |
| **Temperature Range** | Operating<br>Storage | -40°C to +85°C<br>-65°C to +150°C |
| **MTBF** | 854000h | |
| **Humidity** | 5% – 95 % non-condensing | |

Figure 2-1 : Technical Specification

# 3 ID ROM Contents

| Address | Function | Contents |
|---|---|---|
| 0x01 | ASCII 'I' | 0x49 |
| 0x03 | ASCII 'P' | 0x50 |
| 0x05 | ASCII 'A' | 0x41 |
| 0x07 | ASCII 'C' | 0x43 |
| 0x09 | Manufacturer ID | 0xF0 |
| 0x0B | Model Number IP-DUALPIT2<br>Model Number IP-DIGITAL48 | 0x23<br>0x24 |
| 0x0D | Revision | 0xA2 |
| 0x0F | Reserved | 0x00 |
| 0x11 | Driver-ID Low - Byte | 0x00 |
| 0x13 | Driver-ID High - Byte | 0x00 |
| 0x15 | Number of bytes used | 0x0C |
| 0x17 | CRC IP-DUALPIT2<br>CRC IP-DIGITAL48 | 0x4D<br>0x09 |

Figure 3-1 : ID ROM Contents

The content of the ID ROM can be configured by an additional zero ohm resistor, labeled as R50, between "IP-DIGITAL48" and "IP-DUALPIT2" (see chapter "Jumper Configuration").

# 4 IP Addressing

## 4.1 I/O Addressing

The complete register set of the IP is accessible in the I/O space of the module.

IP-DIGITAL48 and IP-DUALPIT2 are implemented by emulating two Motorola MC68230 chips. These two chips are referenced as X and Y in this manual.

Each 68230 has 23 directly addressable internal registers. IP address lines A1 through A5 are used to select the register. Address line A6 selects either the X or Y 68230. All host accesses to the IP are byte-wide, using the low (D7..D0) byte of the 16-bit data bus. Thus all accesses use an odd address, which is standard for 68000 family peripheral chips. The next figure shows the base address of the X and Y 68230.

| Address | 68230 |
|---|---|
| base + 0x00 | X 68230 |
| base + 0x40 | Y 68230 |

**Note**: All accesses are byte wide, using odd address.

Figure 4-1 : Address Map

Complete register addresses consist of the sum of the carrier board's base address, any offset due to the module location on the carrier board, the X or Y offset, and the register address. Register addresses are shown in the following figure. More information on programming the 68230 is given in the MC68230 Parallel Interface / Timer Data Sheet from Motorola.

| Address | 68230 | Register (byte access) |
|---|---|---|
| 0x01 | X | Port General Control Register |
| 0x03 | X | Port Service Request Register |
| 0x05 | X | Port A Data Direction Register |
| 0x07 | X | Port B Data Direction Register |
| 0x09 | X | Port C Data Direction Register |
| 0x0B | X | Port Interrupt Vector Register |
| 0x0D | X | Port A Control Register |
| 0x0F | X | Port B Control Register |
| 0x11 | X | Port A Data Register |
| 0x13 | X | Port B Data Register |
| 0x15 | X | Port A Alternate Register |
| 0x17 | X | Port B Alternate Register |
| 0x19 | X | Port C Data Register |
| 0x1B | X | Port Status Register |
| 0x21 | X | Timer Control Register |
| 0x23 | X | Timer Interrupt Vector Register |
| 0x27 | X | Counter Preload Register (High) |
| 0x29 | X | Counter Preload Register (Med) |
| 0x2B | X | Counter Preload Register (Low) |

| Address | 68230 | Register (byte access) |
|---|---|---|
| 0x2F | X | Count Register (High) |
| 0x31 | X | Count Register (Med) |
| 0x33 | X | Count Register (Low) |
| 0x35 | X | Timer Status Register |
| | | |
| 0x41 | Y | Port General Control Register |
| 0x43 | Y | Port Service Request Register |
| 0x45 | Y | Port A Data Direction Register |
| 0x47 | Y | Port B Data Direction Register |
| 0x49 | Y | Port C Data Direction Register |
| 0x4B | Y | Port Interrupt Vector Register |
| 0x4D | Y | Port A Control Register |
| 0x4F | Y | Port B Control Register |
| 0x51 | Y | Port A Data Register |
| 0x53 | Y | Port B Data Register |
| 0x55 | Y | Port A Alternate Register |
| 0x57 | Y | Port B Alternate Register |
| 0x59 | Y | Port C Data Register |
| 0x5B | Y | Port Status Register |
| 0x61 | Y | Timer Control Register |
| 0x63 | Y | Timer Interrupt Vector Register |
| 0x67 | Y | Counter Preload Register (High) |
| 0x69 | Y | Counter Preload Register (Med) |
| 0x6B | Y | Counter Preload Register (Low) |
| 0x6F | Y | Count Register (High) |
| 0x71 | Y | Count Register (Med) |
| 0x73 | Y | Count Register (Low) |
| 0x75 | Y | Timer Status Register |

Figure 4-2 : Register Map

# 5 Installation

## 5.1 Jumper Configuration

Four shunts and 16 solder connections are used to set certain non-programmable configuration options. These options are discussed in this section.

Shunts are labeled E1 through E4 on the board and zero ohm resistors are labeled E5 through E12 and E13 through E20.

For removing zero ohm resistors, work on a grounded, static free work surface.

### 5.1.1 Interrupts

Each IndustryPack can generate up to two interrupt requests: IRQ0 and IRQ1. The carrier board maps these IP interrupt requests into the available interrupt levels on the host bus. See your carrier board user manual for more information.

The X 68230 uses the IRQ0 line. The Y 68230 uses the IRQ1 line. Two shunts are used to assist in interrupt configuration. The interrupt vector and most interrupt options are programmed in the 68230s.

In each 68230, the data transfer section (the "interface" portion) is distinct from the timer section. Shunt E1 determines which of these two sections has priority if both are requesting service. Note that the two sections typically have distinct vectors, but share an interrupt level. See figure below.

| | | |
|---|---|---|
| Timer highest priority | E1 IN | **Default** |
| Interface highest priority | E1 OUT | |

Figure 5-1 : Interrupt Priority

Interrupts may be disabled entirely by removing shunt E2. See figure below.

| | | |
|---|---|---|
| Interrupts Disabled | E2 OUT | |
| Interrupts Enabled | E2 IN | **Default** |

Figure 5-2 : Interrupt Enable/Disable Shunt

### 5.1.2 Strobe

The IndustryPack logic specification defines a pin on the interface called Strobe (pin 46). The strobe line is used to input or output special clocks. Some carrier boards provide for shunt or programmable strobe functions.

The IP-DIGITAL48 and IP-DUALPIT2 may use the strobe as clock input or output. The timer in the X 68230 is used for strobe functions. See figure below for configuration options. TIN is Timer IN. TOUT is Timer OUT. See jumper options, later in this section for E19 and E20 usage.

| Shunts | Function | Default |
|---|---|---|
| E3-1 to E3-2 | X–PC3/TOUT to E19 | Default |
| E3-2 to E3-3 | Strobe to X–TOUT | |
| E4-1 to E4-2 | X–PC2/TIN to E20 | Default |
| E4-2 to E4-3 | Strobe to X–TIN | |

Figure 5-3 : Strobe Usage

### 5.1.3 Jumper Options

The shunts E5 to E20 of the IP-DIGITAL48 / IP-DUALPIT2 are zero ohm resistors which can be assembled in two positions. The pads of the zero ohm resistors allow making a direct solder connection between the pads at one of the two positions, after removing the zero ohm resistors. Note that the IP-DUALPIT2 connects position 1 for all solder bridges and the IP-DIGITAL48 connects position 2.

The content of the ID ROM can be configured by an additional zero ohm resistor, labeled as R50, between "IP-DIGITAL48" and "IP-DUALPIT2".

| Jumper Position | I/O Connection | 68230 | Default |
|---|---|---|---|
| | | | |
| E5 – 1 | Pin 49 to Y–H4 | Y | IP-DUALPIT2 |
| E5 – 2 | Pin 49 to Y-PC7 | Y | IP-DIGITAL48 |
| | | | |
| E6 – 1 | Pin 47 to Y–H3 | Y | IP-DUALPIT2 |
| E6 – 2 | Pin 47 to Y–PC6 | Y | IP-DIGITAL48 |
| | | | |
| E7 – 1 | Pin 45 to Y–H2 | Y | IP-DUALPIT2 |
| E7 – 2 | Pin 45 to Y-PC5 | Y | IP-DIGITAL48 |
| | | | |
| E8 – 1 | Pin 43 to Y–H1 | Y | IP-DUALPIT2 |
| E8 – 2 | Pin 43 to Y–PC4 | Y | IP-DIGITAL48 |
| | | | |
| E9 – 1 | Pin 48 to GND | Y | IP-DUALPIT2 |
| E9 – 2 | Pin 48 to Y–PC3/TOUT | Y | IP-DIGITAL48 |
| | | | |
| E10 – 1 | Pin 46 to GND | Y | IP-DUALPIT2 |
| E10 – 2 | Pin 46 to Y–PC2/TIN | Y | IP-DIGITAL48 |
| | | | |
| E11 – 1 | Pin 44 to GND | Y | IP-DUALPIT2 |
| E11 – 2 | Pin 44 to Y-PC1 | Y | IP-DIGITAL48 |
| | | | |
| E12 – 1 | Pin 42 to GND | Y | IP-DUALPIT2 |
| E12 – 2 | Pin 42 to Y–PC0 | Y | IP-DIGITAL48 |

Figure 5-4 : Jumper positions for PI/T Y

**Caution: Never make simultaneous connections on position 1 and 2 of one jumper. Serious damage of the module is possible.**

| Jumper Position | I/O Connection | 68230 | Default |
|---|---|---|---|
| | | | |
| E13-1 | Pin 24 to X–H4 | X | IP-DUALPIT2 |
| E13-2 | Pin 24 to X-PC7 | X | IP-DIGITAL48 |
| | | | |
| E14-1 | Pin 22 to X–H3 | X | IP-DUALPIT2 |
| E14-2 | Pin 22 to X–PC6 | X | IP-DIGITAL48 |
| | | | |
| E15-1 | Pin 20 to X–H2 | X | IP-DUALPIT2 |
| E15-2 | Pin 20 to X-PC5 | X | IP-DIGITAL48 |
| | | | |
| E16-1 | Pin 18 to X–H1 | X | IP-DUALPIT2 |
| E16-2 | Pin 18 to X–PC4 | X | IP-DIGITAL48 |
| | | | |
| E17-1 | Pin 19 to GND | X | IP-DUALPIT2 |
| E17-2 | Pin 19 to X–PC1 | X | IP-DIGITAL48 |
| | | | |
| E18-1 | Pin 17 to GND | X | IP-DUALPIT2 |
| E18-2 | Pin 17 to X–PC0 | X | IP-DIGITAL48 |
| | | | |
| E19-1 | Pin 23 to GND | X | IP-DUALPIT2 |
| E19-2 | Pin 23 to E3 | X | IP-DIGITAL48 |
| | | | |
| E20-1 | Pin 21 to GND | X | IP-DUALPIT2 |
| E20-2 | Pin 21 to E4 | X | IP-DIGITAL48 |

Figure 5-5 : Jumper positions for PI/T X

Caution: Never make simultaneous connections on position 1 and 2 of one jumper. Serious damage of the module is possible.

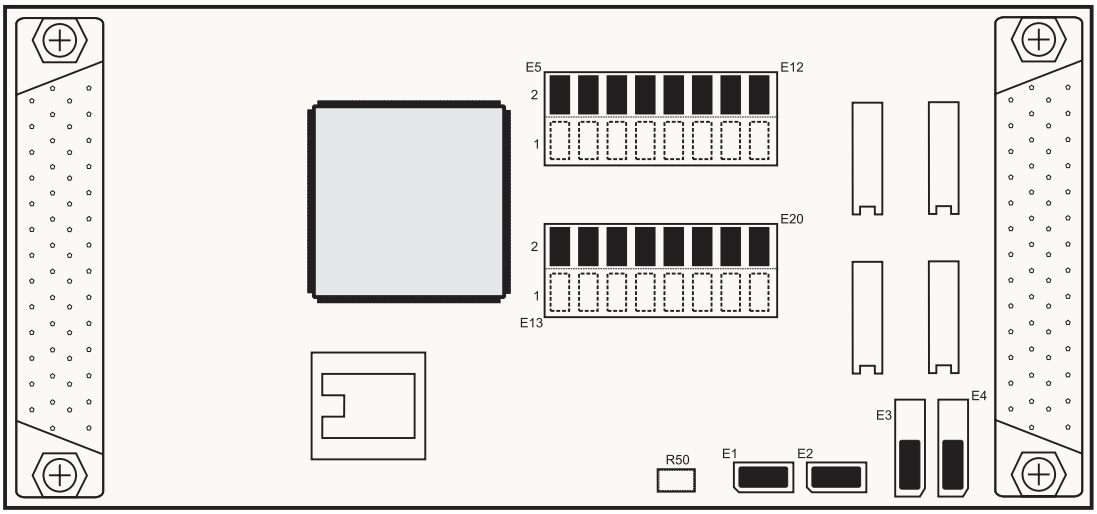


Figure 5-6 : Jumper positions for IP-DIGITAL48

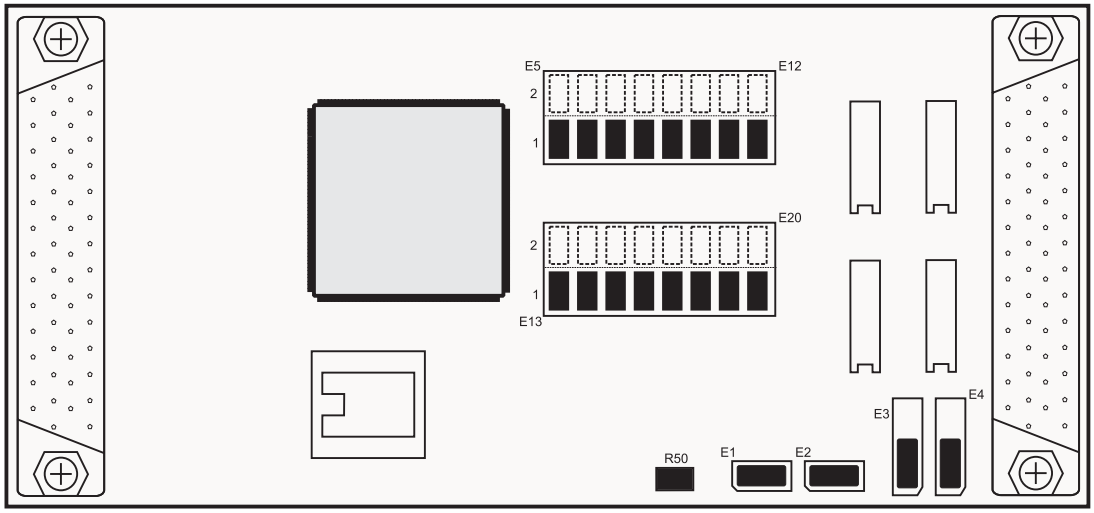


Figure 5-7 : Jumper positions for IP-DUALPIT2

# 6 Pin Assignment – I/O Connector

This section gives the pin assignments for the 50 user I/O lines.

The pin numbers shown in the next figure correspond to numbers on the 50-pin IndustryPack I/O connector, to the wires of a 50-conductor flat cable plugged into a standard IP carrier board, and to the screw terminal numbers on the IP terminal block.

Note that the X and Y 68230s are wired nearly symmetrically. That is, the X PI/T uses the first 25 lines of the I/O cable, and the Y PI/T uses the last 25 lines. Within each group of 25 lines the pin usage is almost the same (factory default). The X PI/T has some shunt options involving its timer. See the jumper options section for more details.

Note that special customer configurations may change this default wiring symmetry.

| Pin Number | X or Y 68230 | Signal Name IP-DUALPIT2 | Signal Name IP-DIGITAL48 |
|---|---|---|---|
| 1 | X | PA0 | PA0 |
| 2 | X | PA1 | PA1 |
| 3 | X | PA2 | PA2 |
| 4 | X | PA3 | PA3 |
| 5 | X | PA4 | PA4 |
| 6 | X | PA5 | PA5 |
| 7 | X | PA6 | PA6 |
| 8 | X | PA7 | PA7 |
| 9 | X | PB0 | PB0 |
| 10 | X | PB1 | PB1 |
| 11 | X | PB2 | PB2 |
| 12 | X | PB3 | PB3 |
| 13 | X | PB4 | PB4 |
| 14 | X | PB5 | PB5 |
| 15 | X | PB6 | PB6 |
| 16 | X | PB7 | PB7 |
| 17 | X | GND | PC0 |
| 18 | X | H1 | PC4 |
| 19 | X | GND | PC1 |
| 20 | X | H2 | PC5 |
| 21 | X | GND | PC2/TIN |
| 22 | X | H3 | PC6 |
| 23 | X | GND | PC3/TOUT |
| 24 | X | H4 | PC7 |
| 25 | | GND | GND |
| 26 | Y | PA0 | PA0 |
| 27 | Y | PA1 | PA1 |
| 28 | Y | PA2 | PA2 |
| 29 | Y | PA3 | PA3 |
| 30 | Y | PA4 | PA4 |
| 31 | Y | PA5 | PA5 |
| 32 | Y | PA6 | PA6 |
| 33 | Y | PA7 | PA7 |
| 34 | Y | PB0 | PB0 |
| 35 | Y | PB1 | PB1 |
| 36 | Y | PB2 | PB2 |
| 37 | Y | PB3 | PB3 |
| 38 | Y | PB4 | PB4 |
| 39 | Y | PB5 | PB5 |
| 40 | Y | PB6 | PB6 |
| 41 | Y | PB7 | PB7 |
| 42 | Y | GND | PC0 |
| 43 | Y | H1 | PC4 |
| 44 | Y | GND | PC1 |
| 45 | Y | H2 | PC5 |
| 46 | Y | GND | PC2/TIN |
| 47 | Y | H3 | PC6 |
| 48 | Y | GND | PC3/TOUT |
| 49 | Y | H4 | PC7 |
| 50 | | GND | GND |

Figure 6-1 : Pin Assignment I/O Connector