CompactPCI® CPN5365 Single Board Computer and CPTM-01 Transition Module

Installation and Use Guide

CPN5365A/IH3

September 2004 Edition

Safety Summary

The following general safety precautions must be observed during all phases of operation, service, and repair of this equipment. Failure to comply with these precautions or with specific warnings elsewhere in this manual could result in personal injury or damage to the equipment.

The safety precautions listed below represent warnings of certain dangers of which Motorola is aware. You, as the user of the product, should follow these warnings and all other safety precautions necessary for the safe operation of the equipment in your operating environment.

Ground the Instrument.

To minimize shock hazard, the equipment chassis and enclosure must be connected to an electrical ground. If the equipment is supplied with a three-conductor AC power cable, the power cable must be plugged into an approved three-contact electrical outlet, with the grounding wire (green/yellow) reliably connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards and local electrical regulatory codes.

Do Not Operate in an Explosive Atmosphere.

Do not operate the equipment in any explosive atmosphere such as in the presence of flammable gases or fumes. Operation of any electrical equipment in such an environment could result in an explosion and cause injury or damage.

Keep Away From Live Circuits Inside the Equipment.

Operating personnel must not remove equipment covers. Only Factory Authorized Service Personnel or other qualified service personnel may remove equipment covers for internal subassembly or component replacement or any internal adjustment. Service personnel should not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, such personnel should always disconnect power and discharge circuits before touching components.

Use Caution When Exposing or Handling a CRT.

Breakage of a Cathode-Ray Tube (CRT) causes a high-velocity scattering of glass fragments (implosion). To prevent CRT implosion, do not handle the CRT and avoid rough handling or jarring of the equipment. Handling of a CRT should be done only by qualified service personnel using approved safety mask and gloves.

Do Not Substitute Parts or Modify Equipment.

Do not install substitute parts or perform any unauthorized modification of the equipment. Contact your local Motorola representative for service and repair to ensure that all safety features are maintained.

Observe Warnings in Manual.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed. You should also employ all other safety precautions which you deem necessary for the operation of the equipment in your operating environment.

Warning

To prevent serious injury or death from dangerous voltages, use extreme caution when handling, testing, and adjusting this equipment and its components.

Flammability

All Motorola PWBs (printed wiring boards) are manufactured with a flammability rating of 94V-0 by UL-recognized manufacturers.

EMI Caution

Caution

This equipment generates, uses and can radiate electromagnetic energy. It may cause or be susceptible to electromagnetic interference (EMI) if not installed and used with adequate EMI protection.Lithium Battery Caution

This product contains a lithium battery to power the clock and calendar circuitry.

Caution

Danger of explosion if battery is replaced incorrectly. Replace battery only with the same or equivalent type recommended by the equipment manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Attention

Il y a danger d'explosion s'il y a remplacement incorrect de la batterie. Remplacer uniquement avec une batterie du même type ou d'un type équivalent recommandé par le constructeur. Mettre au rebut les batteries usagées conformément aux instructions du fabricant.

Vorsicht

Explosionsgefahr bei unsachgemäßem Austausch der Batterie. Ersatz nur durch denselben oder einen vom Hersteller empfohlenen Typ. Entsorgung gebrauchter Batterien nach Angaben des Herstellers.

CE Notice (European Community)

This is a Class A product. In a domestic environment, this product may cause radio interference, in which case the user may be required to take adequate measures.

Motorola Computer Group products with the CE marking comply with the EMC Directive (89/336/EEC). Compliance with this directive implies conformity to the following European Norms:

> EN55022 “Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment”; this product tested to Equipment Class A
>
> EN55024 “Information technology equipment—Immunity characteristics—Limits and methods of measurement”

Board products are tested in a representative system to show compliance with the above mentioned requirements. A proper installation in a CE-marked system will maintain the required EMC performance.

In accordance with European Community directives, a “Declaration of Conformity” has been made and is available on request. Please contact your sales representative.

Notice

While reasonable efforts have been made to assure the accuracy of this document, Motorola, Inc. assumes no liability resulting from any omissions in this document, or from the use of the information obtained therein. Motorola reserves the right to revise this document and to make changes from time to time in the content hereof without obligation of Motorola to notify any person of such revision or changes.

Electronic versions of this material may be read online, downloaded for personal use, or referenced in another document as a URL to the Motorola Computer Group website. The text itself may not be published commercially in print or electronic form, edited, translated, or otherwise altered without the permission of Motorola, Inc.

It is possible that this publication may contain reference to or information about Motorola products (machines and programs), programming, or services that are not available in your country. Such references or information must not be construed to mean that Motorola intends to announce such Motorola products, programming, or services in your country.

Limited and Restricted Rights Legend

If the documentation contained herein is supplied, directly or indirectly, to the U.S. Government, the following notice shall apply unless otherwise agreed to in writing by Motorola, Inc.

Use, duplication, or disclosure by the Government is subject to restrictions as set forth in subparagraph (b)(3) of the Rights in Technical Data clause at DFARS 252.227-7013 (Nov. 1995) and of the Rights in Noncommercial Computer Software and Documentation clause at DFARS 252.227-7014 (Jun. 1995).

Motorola, Inc.
Embedded Communications Computing Group
2900 South Diablo Way
Tempe, Arizona 85282

Contents

CHAPTER 2 Installing the CPTM-01

CHAPTER 3 Starting Up the CPN5365

CHAPTER 4 Functional Description

CHAPTER 5 Connector Pin Assignments

APPENDIX A Specifications

APPENDIX B Thermal Analysis

APPENDIX C Related Documentation

List of Figures

List of Tables

About This Manual

This *CompactPCI® CPN5365 Single Board Computer Installation and Use Guide* describes the installation, components, and configurations of the CPN5365 Single Board Computer and CPTM-01 Rear Transition Module. Use this guide for general and technical information about the CPN5365 Single Board Computer.

Model Numbers	Description
CPN5365-700-01	700 MHz Pentium III, 512MB ECC, 2 PMCs, I/O on J4
CPN5365-700-02	700 MHz Pentium III, 512MB ECC, 1 PMC, 1 HD site, I/O on J4
CPN5365-700-03	700 MHz Pentium III, 512MB ECC, 2 PMCs, no J4
CPN5365-700-04	700 MHz Pentium III, 512MB ECC, 1 PMC, 1 HD site, no J4
CPTM-01	CompactPCI Rear Transition Module with 1 or 2 PIM sites, keyboard/mouse, USB, CompactFlash, EIDE, floppy, serial, parallel Ethernet, video

Summary of Changes

This table summarizes revisions to this manual.

Date	Change
September 2004	Updated model numbers to reflect new configurations.
May 2003	Revised the *Remote Setup* on page 4-9 to reflect correct default BIOS settings. Revised Table 5-3 and Table 2-2.

Overview of Contents

This section contains a short description of the content of each chapter and appendix in this manual.

Chapter 1, *Hardware Preparation and Installation*, describes the features, configuration, basic preparation and installation of the memory mezzanine, PMCs, and the CPN5365.

Chapter 2, *Installing the CPTM-01*, describes the features, functions, and installation of the rear transition module. Pin assignments for the RTM are at the end of this chapter.

Chapter 3, *Starting Up the CPN5365*, provides information about the power-up procedure, switches, and indicators on the single board computer.

Chapter 4, *Functional Description*, provides brief descriptions about the processor, PCI bus, host and nonhost slot mounting, WDT, resets, clock functions and a general description of the CPN5365 on a block diagram level. This chapter also includes information about the PhoenixBIOS.

Chapter 5, *Connector Pin Assignments*, contains the pin assignments for the CPN5365 base board.

Appendix A, *Specifications*, provides physical and mechanical board specifications.

Appendix C, *Thermal Analysis*, provides information about thermally significant components on the single board computer.

Appendix C, *Related Documentation*, lists related Motorola Computer Group documents, manufacturer's documents, and specifications and provides the URLs for this information.

Who Should Use This Guide

The information in this guide is written for system installers, original equipment manufacturers (OEM) and technicians. The procedures assume familiarity with the safety practices and regulatory compliance required

for using and modifying electronic equipment. Personnel who install CompactPCI systems should be trained and experienced with the installation of computers and computer equipment.

Comments and Suggestions

Motorola welcomes and appreciates your comments on its documentation. We want to know what you think about our manuals and how we can make them better. Mail comments to:

Embedded Communications Computing Group
Reader Comments DW164
2900 S. Diablo Way
Tempe, Arizona 85282

You can also submit comments to the following e-mail address:
reader-comments@mcg.mot.com

In all your correspondence, please list your name, position, and company. Be sure to include the title and part number of the manual and tell how you used it. Then tell us your feelings about its strengths and weaknesses and any recommendations for improvements.

Conventions Used in This Manual

The following typographical conventions are used in this document:

bold

is used for user input that you type just as it appears; it is also used for commands, options and arguments to commands, and names of programs, directories and files.

italic

is used for names of variables to which you assign values. Italic is also used for comments in screen displays and examples, and to introduce new terms.

`courier`

is used for system output (for example, screen displays, reports), examples, and system prompts.

<**Enter**>, <**Return**> or <**CR**>

<**CR**> represents the carriage return or Enter key.

CTRL

represents the Control key. Execute control characters by pressing the Ctrl key and the letter simultaneously, for example, **Ctrl-d**.

Hardware Preparation and Installation

1

This chapter gives you information about:

- Unpacking the CPN5365
- ESD precautions
- Startup procedures
- Features and functions of the CPN5365 Single Board Computer
- Board configuration, basic preparation and installation of the memory mezzanine, PMCs, and CPN5365 into a chassis
- Replacing lithium batteries

This document treats the CPN5365 Single Board Computer, hereafter also referred to as the CPN5365, as a component of a system, and assumes that you install it in a CompactPCI backplane that is PCI Industrial Computer Manufacturers Group (PICMG) compliant.

Unpacking Instructions

Note If the shipping carton is damaged upon receipt, request that the carrier's agent be present during the unpacking and inspection of the equipment.

Unpack the equipment from the shipping carton. Refer to the packing list and verify that all items are present. Save the packing material for storing and reshipping of equipment.

Caution Avoid touching areas of integrated circuitry. Static discharge can damage circuits.

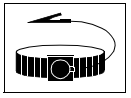
After removing the CPN5365 from its packaging:

- Check for obvious physical damage
- Verify that the coin cell battery is in its holder and inserted correctly

Make sure that you disconnect the chassis from the main power supply before you continue.

Antistatic Precautions

Use ESD



Wrist Strap

Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or upgrading a system. Electronic components, such as disk drives, computer boards, and memory modules, can be extremely sensitive to electrostatic discharge (ESD). After removing the component from its protective wrapper or from the system, place the component flat on a grounded, static-free surface (and, in the case of a board, component side up). Do not slide the component over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available at electronics stores) that is attached to an active electrical ground. Note that a system chassis may not be grounded if it is unplugged.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

Caution

Avoid touching areas of integrated circuitry. Static discharge can damage these circuits.

Equipment Required

A CPN5365 system requires this equipment:

- CompactPCI system enclosure
- System console terminal
- Operating system
- Disk drives
- Transition module (CPTM-01) and connecting cables

Overview of Startup Procedures

The following table shows the things you need to do before you can use this board. It also tells you where to find the information you need to perform each step.

For information about	Go to
Unpacking the hardware	*Unpacking Instructions* on page 1-1
Mounting memory mezzanine cards	*Mounting Memory Mezzanine Modules* on page 1-10
Mounting PCI mezzanine cards (PMC)	*Mounting PCI Mezzanine Cards* on page 1-11
Hardware Configuration	*Hardware Configuration* on page 1-13
Hard drive mounting	*Mounting the Slim Line EIDE Hard Drive* on page 1-12
Installing the CPN5365 and CPTM-01 TM	*Before You Install or Remove a Board* on page 1-14 and *Installing the CPTM-01 Transition Module* on page 2-3
Powering-up the system	*Applying Power to the System* on page 3-1

Introduction

The CPN5365 is a hot swap, single-slot, CompactPCI® compliant computer. It can serve as a standard CompactPCI peripheral CPU in a nonhost slot. It is powered by a Mobile Pentium® III processor and 440GX chip set and includes up to 1GB of on-board system memory. The highly integrated processor gives you a 16MB on-board solid-state disk, USB, PCI EIDE, accelerated graphics, dual Fast Ethernet controllers, and standard I/O, plus two PMC sites for additional expansion and other functions on J4. The optional CPTM-01 TM gives you backplane I/O for PMC sites and on-board devices.

Some models of the CPN5365 can be inserted in an H.110 system and will not interfere with the H.110 interface. These models are the same as other versions except that the J4 connector is removed.

The CPN5365 meets the needs of embedded application developers. Typical applications include broadband data or intelligent network switching, CTI server, industrial control and automation, military and aerospace, and medical, scientific, or imaging products.

Features

The CPN5365 Single Board Computer gives you these features:

- ❏ Low power Pentium III processor for embedded applications
- ❏ Up to 1GB on-board memory
- ❏ On-board AGP video with 4MB integrated video memory
- ❏ Dual Fast Ethernet controllers for monitoring and telecom applications
- ❏ Hot Swap compatibility allowing insertion or removal of the CPN5365 while power is applied
- ❏ On-board I/O via the front panel of the CPN5365 or via the CPTM-01 transition module
- ❏ Models available for H.110 interface

Input/Output Interfaces

Refer to the next table for brief descriptions of the input/output interfaces on the CPN5365 and CPTM-01 transition module.

Note When the identical function is available through the CPN5365 front panel and the rear transition module, you can use either the front or the rear, **not both.**

Table 1-1. Input/Output Interfaces on the CPN5365 and the CPTM-01

Function	CPN5365		CPTM-01 Transition Module	
	Front Panel	On-board	Rear Panel	On-board
Ethernet 1	RJ45	-	RJ45	-
Ethernet 2	-	-	RJ45	-
COM1 (Serial Port 1)	RJ45	-	-	10-pin shrouded
COM2 (Serial Port 2)	-	-	9-pin D-sub	-
PMC Panel	PMC 1 Device	-	PIM slot for PMC 1 Device	-
PMC Panel	PMC 2 Device	-	-	-
Keyboard/Mouse	-	-	6-pin mini-DIN	
Floppy	-	-	-	34-pin connector
Parallel	-	-	-	26-pin connector
USB 0 and USB 1	-	-	-	8-pin connector
Video	-	9-pin unshrouded	15-pin D-sub	-
Primary IDE	-	44-pin connector	-	
Secondary IDE	-	-	-	40-pin connector
CompactFlash	-	-	-	50-pin socket

Front Panel Connectors, Switches, and Indicators

The CPN5365's front panel has connectors and switches for:

- Two PCI Mezzanine Card Panels (PMC1 and PMC2)
- Ethernet 1 (RJ45)
- COM1 serial port (RJ45)
- Board reset (switch)

LED indicator lights on the front panel display of the CPN5365 include:

- Hot Swap status (Blue LED)
- Power (Green LED)

Refer to Figure 1-1 on page 1-7 for the location of the front panel connectors, switches, and indicators. Refer to Table 1-2 on page 1-9 for a list of the front panel connectors.

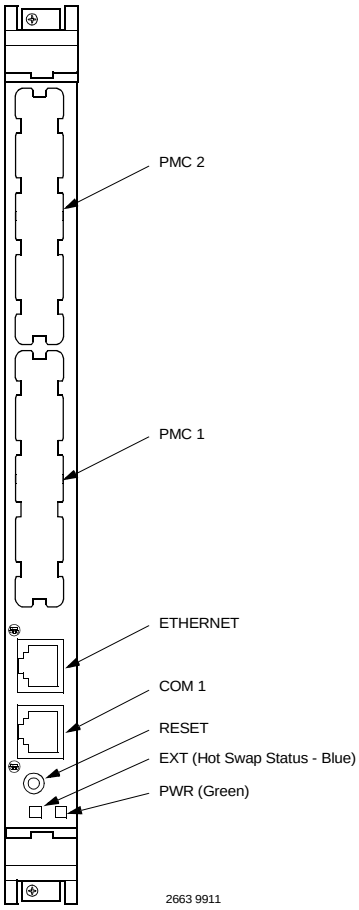


Figure 1-1. Front Panel Connectors, Reset Switch, and LEDs

CPN5365 On-Board Components

The CPN5365 carries components on both sides. Table 1-2 on page 1-9 lists the connectors available to support devices. There are no on-board jumpers.

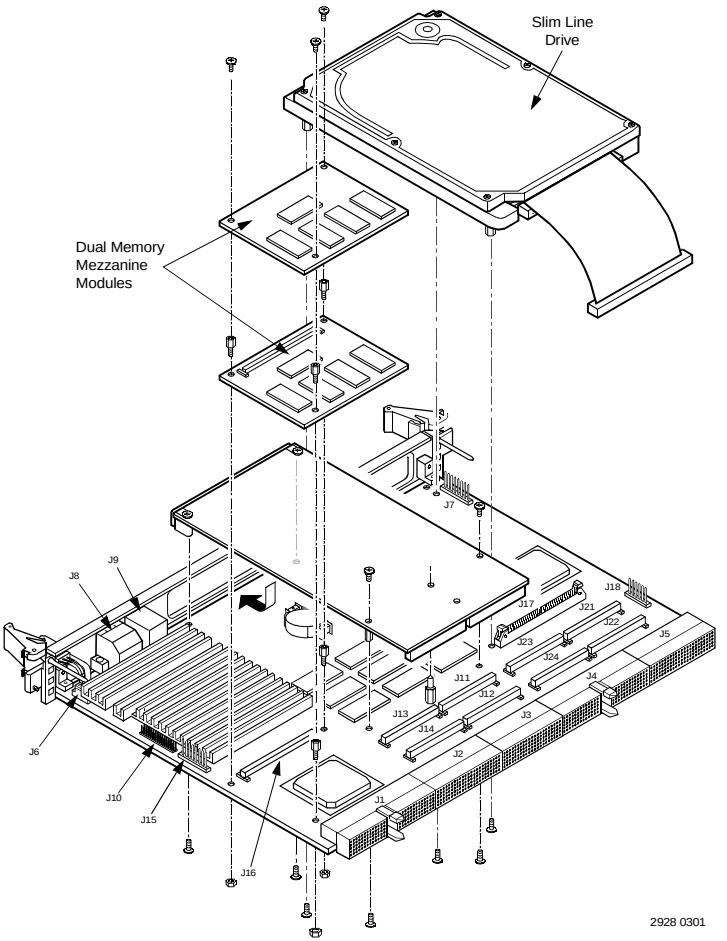


Figure 1-2. Location of On-Board Components

Table 1-2. List of Front Panel Connectors and On-Board Components

Connector	Description
J1	CompactPCI Bus Connector
J2	CompactPCI Bus Connector
J3	Rear I/O CompactPCI Connector
J4	Rear I/O CompactPCI Connector
J5	Rear I/O CompactPCI Connector
J6	(reserved for Motorola use only)
J7	Video connector
J8	COM1 (serial port - RJ45 connector)
J9	Ethernet connector (RJ45)
J10	Debug port
J11	PMC1 bus signal connector
J12	PMC1 bus signal connector
J13	PMC1 64 bit PCI extension
J14	PMC1 I/O connector
J15	(reserved for Motorola use only)
J16	Memory expansion connector
J17	Primary IDE connector
J18	(reserved for Motorola use only)
J21	PMC2 bus signal connector
J22	PMC2 bus signal connector
J23	PMC2 64 bit PCI extension
J24	PMC2 I/O connector

Also refer to Chapter 5, *Connector Pin Assignments*, for more connector information.

Installing Memory Modules, PMCs, and Drives

Refer to *Antistatic Precautions* on page 1-2 before beginning installation.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

Caution

Avoid touching areas of integrated circuitry. Static discharge can damage these circuits.

Mounting Memory Mezzanine Modules

You can mount one or two 256MB memory mezzanine modules on the CPN5365. Refer to *Antistatic Precautions* on page 1-2 before beginning installation. Refer to Figure 1-2 for placement.

1. Attach three standoffs to the CPN5365 base board and secure with three nuts on the secondary side of the board.
2. Place one memory mezzanine module on top of the three standoffs and press gently on the center of the J16 connector, working outward until the connectors are firmly seated.
3. Secure with three screws.

   If mounting a second memory mezzanine module use a second set of three standoffs instead of three screws.
4. Place the second memory mezzanine module on top of the three standoffs and press onto the connector on the first memory mezzanine module, making sure the connectors are firmly seated together.
5. Secure with three screws.

Mounting PCI Mezzanine Cards

You can mount one or two +5V and/or Universal PCI Mezzanine Cards (PMCs) on the CPN5365. Each PMC site is keyed for +5V PCI bus interface.

Caution Inserting or removing PMCs with power applied may result in damage to module components.

Note You cannot install PMC cards that are only compatible with +3.3V PCI.

The upper PMC module I/O (PMC 2) connects to J3 and the lower PMC module I/O (PMC 1) connects to J5. Signal routing for PMC I/O must be about one inch to permit use of different types of high speed devices. If you mount the on-card hard drive you cannot use the upper PMC site (PMC 2).

1. Attach an ESD strap to your wrist. Attach the other end of the ESD strap to the chassis as a ground. Keep the ESD secured throughout this procedure.
2. Shut down the operating system.
3. Turn AC or DC power off and remove the AC cord or DC power lines from the system.
4. Remove chassis or system cover(s) as necessary.
5. Carefully remove the CPN5365 from its card slot and lay it flat, with connectors J1 through J5 facing you.
6. Remove the PMC filler from the front panel.

Caution Do not damage or bend connector pins.

7. Slide the edge connector of the PMC module into the front panel opening from behind and place the PMC module on top of the base board. Align the four connectors on the underside of the PMC module with the corresponding connectors on the CPN5365:

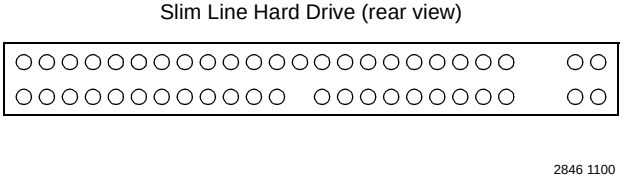
– J11, J12, J13, J14 for PMC1
– J21, J22, J23, J24 for PMC2

Press all connectors until they are firmly seated.

8. Insert the four screws through the holes on the bottom side of the CPN5365 and tighten the screws.
9. Reinstall the CPN5365 in its proper slot. Be sure the module is well seated in the backplane connectors.
10. Reconnect the system to its AC or DC power source and turn the power on.

Mounting the Slim Line EIDE Hard Drive

You can mount a Slim Line EIDE hard drive in the space for PMC 2. Refer to Figure 1-2. No configuration is required. The drive is configured as master with no jumpers installed.



1. Connect the Slim Line EIDE drive cable to the J17 connector on the CPN5365.
2. Position the drive on the CPN5365.
3. Connect the drive cable to the drive.
4. Secure the drive to the CPN5365 using four screws.

Connecting Devices to Board Connectors

The CPN5365 and CPTM-01 rear transition module give you board connectors for attaching peripheral devices. Before installing the baseboard or rear transition module, you may want to connect your peripheral cables to the connectors.

Note When the identical function is available through the CPN5365 front panel or the CPTM-01 rear panel, you can use either the front or the rear, **not both**.

Warning

Always remove power from the system before connecting peripherals to the CPN5365 or CPTM-01. To reduce the risk of personal injury, disconnect the power cord from the power source. Only qualified, experienced electronics personnel should access the interior of a chassis.

Caution

The components of the CPN5365 and CPTM-01 are sensitive to static discharge. While out of the unit, place the modules on a static-dissipative surface or into a static-shielding bag.

Hardware Configuration

To produce the necessary hardware configuration and to make sure the CPN5365 operates properly, you may need to make certain modifications by settings bits in control registers after installing the module in a system. Configuration options for the CPN5365 are:

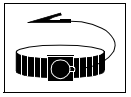
- There are no on-card jumpers or switches
- You cannot configure the CPU speed settings

Before You Install or Remove a Board

Boards may be damaged if improperly installed or handled. Please read and follow the guidelines in this section to protect your equipment.

Observe ESD Precautions

Use ESD



Wrist Strap

Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or upgrading a system. Electronic components, such as disk drives, computer boards, and memory modules, can be extremely sensitive to electrostatic discharge (ESD). After removing the component from its protective wrapper or from the system, place the component flat on a grounded, static-free surface (and, in the case of a board, component side up). Do not slide the component over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available at electronics stores) that is attached to an active electrical ground. Note that a system chassis may not be grounded if it is unplugged.

Watch for Bent Pins or Other Damage

Caution

Bent pins or loose components can cause damage to the board, the backplane, or other system components. Carefully inspect your board and the backplane for both pin and component integrity before installation

MCG and our suppliers take significant steps to ensure there are no bent pins on the backplane or connector damage to the boards prior to leaving our factory. Bent pins caused by improper installation or by boards with damaged connectors could void the MCG warranty for the backplane or boards.

If a system contains one or more crushed pins, power off the system and contact your local sales representative to schedule delivery of a replacement chassis assembly.

Use Caution When Installing or Removing Boards

When first installing boards in an empty chassis, we recommend that you start at the left of the card cage and work to the right when cards are vertically aligned; in horizontally aligned cages, work from bottom to top.

When inserting or removing a board in a slot adjacent to other boards, use extra caution to avoid damage to the pins and components located on the primary or secondary sides of the boards.

Preserve EMI Compliance

Caution

To preserve compliance with applicable standards and regulations for electromagnetic interference (EMI), during operation all front and rear openings on the chassis or board faceplates must be filled with an appropriate card or covered with a filler panel. If the EMI barrier is open, devices may cause or be susceptible to excessive interference.

Understand Hot Swap

Caution

Inserting or removing non-hot swap cards or transition modules with power applied may result in damage to module components. Make sure that your board manufacturer identifies your module as hot swap ready.

The PICMG 2.1 Hot Swap specification defines varying levels of hot swap. A board that is compliant with the specification can be inserted and removed safely with system power on without damage to on-board circuitry. *If a module is not hot swap compliant, you should remove power to the slot or system before inserting or removing the module.*

To facilitate hot swap, PICMG 2.1 specifies a blue LED on the faceplate. This LED is under software control.

If your system is using software that provides full hot swap capabilities, the software will illuminate the blue hot swap LED on the faceplate when software has stopped and it is safe to remove the board.

If your system does not have hot swap-aware software running, behavior of the blue LED may be indeterminate. In this case, you may need to manually shut down applications or operating systems running on the board prior to board removal, even if the blue LED is lit.

Caution

Powering down or removing a board before the operating system or other software running on the board has been properly shut down may cause corruption of data or file systems.

Refer to the documents listed in Appendix C, *Related Documentation* for more information about hot swap and the PCI Industrial Computer Manufacturers Group (PICMG) Hot Swap Specification.

Recognize Different Injector/Ejector Lever Types

The modules you install may have different ejector handles and latching mechanisms. The following illustration shows the typical board ejector handles used with MCG payload cards: (A) Elma Latching, (B) Rittal Type II, (C) Rittal Type IV. All handles are compliant with the CompactPCI specification and are designed to meet the IEEE1101.10 standards.

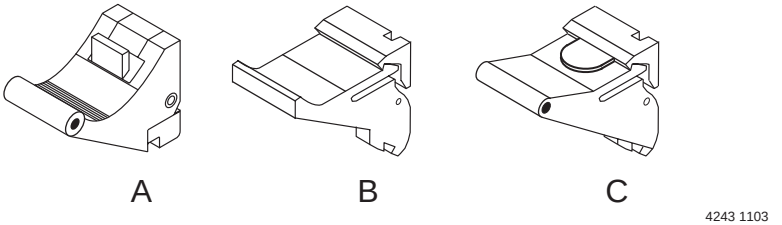


Figure 1-3. Injector/Ejector Lever Types

Each lever type has a latching mechanism to prevent the lever from being opened accidentally. You must press the lever release before you can open the lever. *Never force the lever*. If the lever does not open easily, you may not have pressed firmly enough on the release. If the lever does not close easily, the board may not be properly seated in the chassis.

To open a lever, press the release and move the lever outward away from the faceplate.

To close a lever, move the lever inward toward the faceplate until the latch engages.

Verify Slot Usage

Caution

Prevent possible damage to module components by verifying the proper slot usage for your configuration.

In most cases, connector keying will prevent insertion of a board into an incompatible slot. However, as an extra precaution, you should be familiar with the glyphs and colored card rails used to indicate slot purpose.

The following table lists the colors common to MCG chassis.

Table 1-3. Slot Usage Indicators

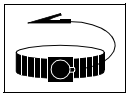
Card Rail Color	Glyph	Usage
Tan	None	**MXP:** Alarm Management Controller slot
		**CPX:** Hot Swap Controller or Bridge slot
Red		**MXP:** Fabric Switch Card slot
		**CPX:** System Controller slot
Black		**MXP:** Payload Card slot
		**CPX:** Non-system Controller or I/O Card slot

Installing a Module

This section describes a recommended procedure for installing a board module in a chassis.

Before you install your module, please read all cautions, warnings, and instructions presented in this section and the guidelines explained in *Before You Install or Remove a Board* on page 1-14.

Use ESD



Wrist Strap

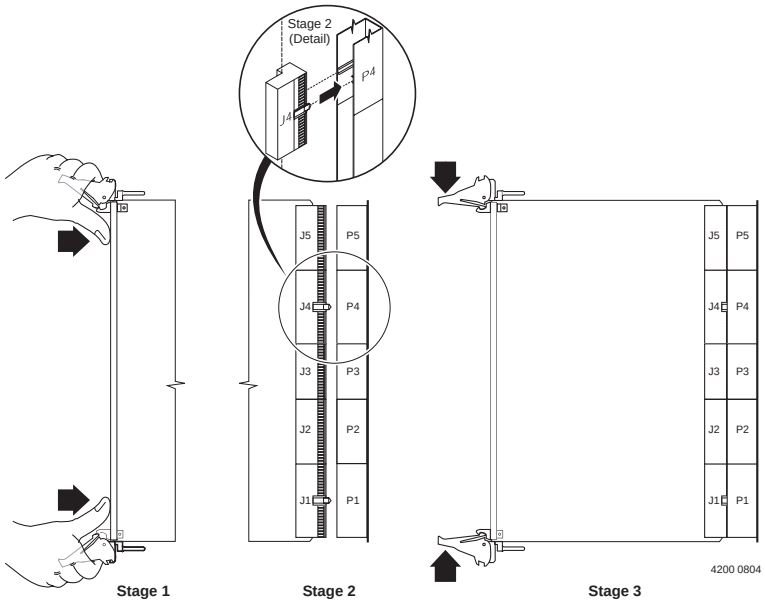
Handling modules and peripherals can result in static damage. Use a grounded wrist strap, static-dissipating work surface, and antistatic containers when handling and storing components.

Caution

Insert the board by holding the injector levers—do not exert unnecessary pressure on the faceplate.

Hot swap compliant modules may be installed while the system is powered on. If a module is not hot swap compliant, you should remove power to the slot or system before installing the module. See *Understand Hot Swap* on page 1-15 for more information.

Refer to the following illustration and perform these steps when installing modules. Note that this illustration is for general reference only and may not accurately depict the connectors and handles on the board you are installing.



1. Open the injector levers on your board (see *Recognize Different Injector/Ejector Lever Types* on page 1-16).
2. Verify the proper slot for the module you are inserting (see *Verify Slot Usage* on page 1-17). Align the edges of the module with the card cage rail guides in the appropriate slot.
3. Using your thumbs, apply equal and steady pressure as necessary to carefully slide the module into the card cage rail guides (Stage 1). Continue to gently push until the prealignment guide pegs engage with the backplane connector (Stage 2) and the injector levers make contact with the chassis rails. *DO NOT FORCE THE BOARD INTO THE BACKPLANE SLOT.*
4. Use the injector levers to seat the module in the slot by closing the levers until they latch into the locked position (Stage 3). If the levers do not completely latch, remove the module from the chassis and visually inspect the slot to ensure there are no bent pins.
5. When the module you are installing is completely latched, secure it by tightening the captive screws at both ends of the faceplate.

Removing a Hot-Swap Module

This section describes a recommended procedure for removing a board module from a chassis.

Before you remove your module, please read all cautions, warnings, and instructions presented in this section and the guidelines explained in *Before You Install or Remove a Board* on page 1-14.

Hot swap compliant modules may be removed while the system is powered on. If a module is not hot swap compliant, you should remove power to the slot or system before removing the module. See *Understand Hot Swap* on page 1-15 for more information.

To remove a board module, follow these steps:

1. Loosen the module's captive screws at both ends of the faceplate.
2. Begin to remove your module by unlatching the ejector lever closest to the blue LED (the lower lever on vertically mounted boards). See *Recognize Different Injector/Ejector Lever Types* on page 1-16. *Do not remove the module immediately.*

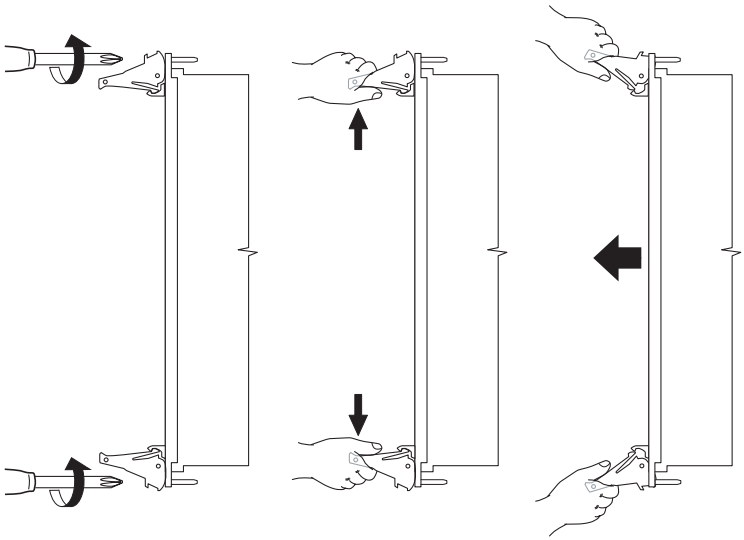
Caution

Powering down or removing a board before the operating system or other software running on the board has been properly shut down may cause corruption of data or file systems.

If your module is hot swap compliant and you are running fully functional hot swap-aware software, unlatching this ejector lever will start the shutdown process on the board. Software will illuminate the blue hot swap LED on the faceplate when it is safe to remove the board.

If your board or system is not running hot swap-aware software, the blue LED may illuminate without regard to software processes still running on the board. Be sure to manually shut down applications or operating systems running on the board prior to board removal. See *Understand Hot Swap* on page 1-15 for more information.

3. Once the applications and operating system running on the board have stopped and it is safe to remove the board, open both ejector levers to partially unseat the module from the backplane connectors.



4. Carefully pull the module from the chassis.

Replacing Lithium Batteries

Follow these safety rules for proper battery operation and to reduce equipment and personal injury hazards when handling lithium batteries. Use the battery for its intended application only.

Note **Do not** recharge, open, puncture or crush, incinerate, expose to high temperatures or dispose of in your general trash collection.

To replace the lithium battery, observe the following guidelines and follow the steps below.

Note When replacing the battery, you must apply power to the board to prevent data loss.

To prevent serious injury or death from dangerous voltages, use extreme caution when handling, testing, and adjusting this equipment and its components.

Warning

Lithium batteries incorporate flammable materials such as lithium and organic solvents. If lithium batteries are short-circuited or exposed to high temperature or pressure, they may burst open and ignite, possibly resulting in injury and/or fire. When dealing with lithium batteries, carefully follow the precautions listed below to prevent accidents.

- ❏ Do not short circuit
- ❏ Do not disassemble, deform or apply excessive pressure
- ❏ Do not heat or incinerate
- ❏ Do not apply solder directly
- ❏ Do not use different models, or new and old batteries together
- ❏ Do not charge
- ❏ Always check proper polarity

To replace the on-board backup battery, follow the steps below.

Caution

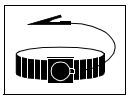
Danger of explosion if battery is replaced incorrectly.

Replace only with the same or equivalent type recommended by the equipment manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Caution

Avoid touching areas of integrated circuitry; static discharge can damage circuits.

Use ESD



Wrist Strap

Attach an ESD strap to your wrist. Attach the other end of the ESD strap to an electrical ground. (Note that the system chassis may not be grounded if it is unplugged.) Secure the ESD strap to your wrist and to ground throughout the procedure.

1. To remove the battery from the module, carefully pull the battery from the socket.
2. Before installing a new battery, make sure that the battery pins are clean.
3. Not the battery polarity and press the new battery into the socket.

Note No soldering is required when the battery is in the socket.

4. Recycle or dispose of the old battery according to local regulations and manufacturer's instructions.

Installing the CPTM-01

2

The optional CPTM-01 TM gives you backplane I/O for PMC sites and on-board devices.

Transition Module On-Board Components and Rear Panel Connectors

The CPTM-01 rear transition module has connectors on the rear panel for:

- Keyboard/mouse (PS/2)
- Video (15 pin high density D-sub)
- COM2 (serial port) (9 pin D-sub)
- Ethernet 1 and Ethernet 2 (RJ45)
- PIM 1

The next table lists all the connectors available to support devices on the CPTM-01 rear transition module.

Table 2-1. Front Panel and On-Board Connectors and Components for the CPTM-01

Connector	Description	Connector	Description
J2	Drive LEDs, Reset	J16	Video
J3	Rear I/O CompactPCI Connector	J18	Ethernet 2
J4	Rear I/O CompactPCI Connector	J19	USB connector
J5	Rear I/O CompactPCI Connector	J20	Parallel connector
J6	Keyboard/Mouse (internal, not installed)	J21	COM1 (serial port 1)

Table 2-1. Front Panel and On-Board Connectors and Components for the CPTM-01 (Continued)

Connector	Description	Connector	Description
J9	Floppy	J25	CompactFlash
J10	PIM connector (PMC I/O)	J26	IDE (secondary)
J13	Ethernet 1	J27	Keyboard/Mouse (external)
J14	PIM connector (PMC I/O)	J28	COM2 (serial port 2)

The following illustration shows the locations of on-board components and rear panel connectors on the CPTM-01.

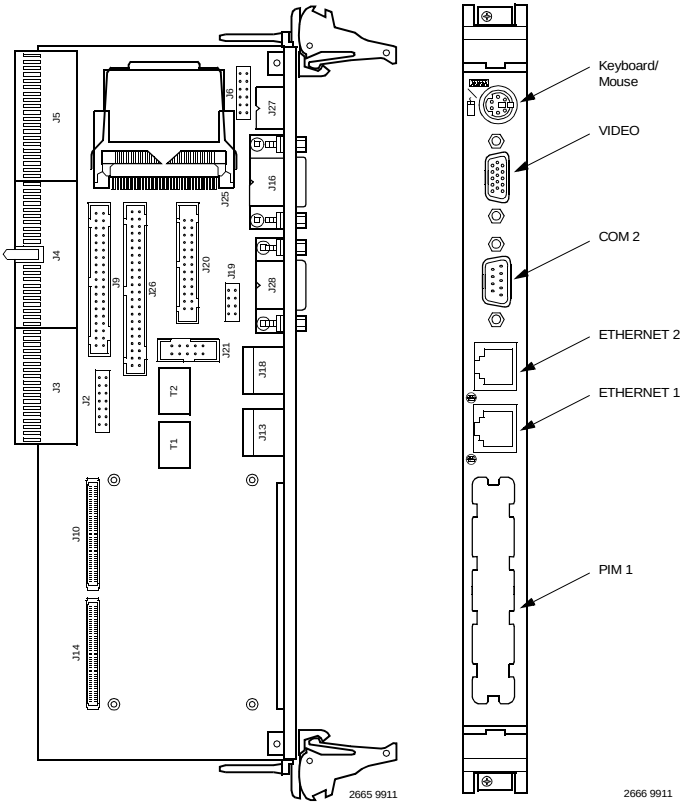
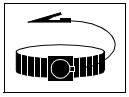


Figure 2-1. CPTM-01 Components and Rear Panel Connectors

Antistatic Precautions

Use ESD



Wrist Strap

Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or upgrading a system. Electronic components, such as disk drives, computer boards, and memory modules, can be extremely sensitive to electrostatic discharge (ESD). After removing the component from its protective wrapper or from the system, place the component flat on a grounded, static-free surface (and, in the case of a board, component side up). Do not slide the component over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available at electronics stores) that is attached to an active electrical ground. Note that a system chassis may not be grounded if it is unplugged.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

Caution

Avoid touching areas of integrated circuitry. Static discharge can damage these circuits.

Installing the CPTM-01 Transition Module

The CPTM-01 transition module may be required to complete the configuration of your particular CPN5365 system. If so, perform the following steps to install this board.

Please read all cautions, warnings and procedures before installing the CPTM-01 into your chassis.

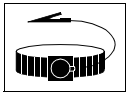
Caution

Note that models of the CPN5365 that include the J4 connector must not be installed in enclosures that have support buses like the H.110 or provide other uses for this J4 connector. Also, the CPTM-01 should only be

installed in an enclosure that does not support buses such as the H.110 or provide other uses for this J4 connector. The CPTM-01 uses the J4 connector for I/O signals from the CPN5365.

Inserting or removing modules in a non-hot swap chassis with the power applied may result in damage to the module components. The CPTM-01 is not a hot swap board, but may be installed in a hot swap chassis with power applied only if the corresponding CPN5365 is removed before the transition module is installed.

Use ESD



Wrist Strap

Motorola strongly recommends that you use an antistatic wrist strap and a conductive foam pad when installing or upgrading a system. Electronic components, such as disk drives, computer boards, and memory modules, can be extremely sensitive to ElectroStatic Discharge (ESD).

After removing the component from the system or its protective wrapper, place the component flat on a grounded, static-free surface (and in the case of a board, component side up). Do not slide the component over any surface.

If an ESD station is not available, you can avoid damage resulting from ESD by wearing an antistatic wrist strap (available at electronics stores) that is attached to an unpainted metal part of the system chassis.

Warning

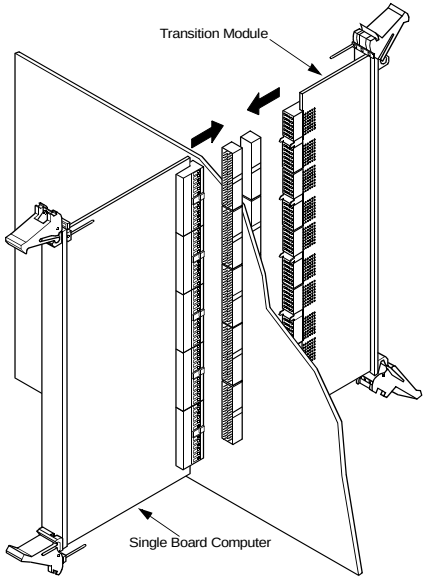
Avoid touching areas of integrated circuitry; static discharge can damage these circuits.

Warning

Dangerous voltages, capable of causing death, are present in this equipment. Use extreme caution when handling, testing, and adjusting.

To install a rear transition module in the chassis, follow these steps:

1. Attach an ESD strap to your wrist. Attach the other end of the strap to the chassis as a ground. The ESD strap must be secured to your wrist and to ground throughout the procedure.
2. Perform an operating system shutdown if you are **not** removing the CPN5365. Turn the AC or DC power off and remove the AC cord or DC power lines from the system. If you are **not** powering off the system, first remove the CPN5365 before installing the RTM.
3. Remove chassis or system cover(s) as necessary for access to the chassis backplane.
4. With the transition module (CPTM-01) in the correct vertical position that matches the pin positioning of the corresponding CPN5365 board, carefully slide the transition module into the appropriate slot and seat tightly into the backplane. Refer to the next figure for the correct connector orientation.



5. Secure in place with the screws provided, making good contact with the transverse mounting rails to minimize RF emissions.
6. Replace the chassis or system cover(s), making sure no cables are pinched.

7. Cable the peripherals to the panel connectors, reconnect the system to the AC or DC power source, and turn the equipment power on.

CPTM-01 Transition Module Connectors

The following tables provide the pin assignments for the connectors on the CPTM-01.

Rear I/O Connectors (J3, J4, and J5)

Table 2-2. CPTM-01 Rear I/O Connector (J3)

Pin	F	E	D	C	B	A
19	GND	-12V (PIM)*	UDATA0-	UDATA0+	UDATA1-	UDATA1+
18	GND	+12V (PIM)*	RI2	DTR2	RI1	DTR1
17	GND	No connect	DCD2	DSR	DCD1	DSR1
16	GND	No connect	TxD2	CTS2	TxD1	CTS1
15	GND	No connect	RxD2	RTS2	RxD1	RTS1
14	GND	VCC	VCC	VCC3	VCC3	VCC3
13	GND	PMC1IO1	PMC1IO2	PMC1IO3	PMC1IO4	PMC1IO5
12	GND	PMC1IO6	PMC1IO7	PMC1IO8	PMC1IO9	PMC1IO10
11	GND	PMC1IO11	PMC1IO12	PMC1IO13	PMC1IO14	PMC1IO15
10	GND	PMC1IO16	PMC1IO17	PMC1IO18	PMC1IO19	PMC1IO20
9	GND	PMC1IO21	PMC1IO22	PMC1IO23	PMC1IO24	PMC1IO25
8	GND	PMC1IO26	PMC1IO27	PMC1IO28	PMC1IO29	PMC1IO30
7	GND	PMC1IO31	PMC1IO32	PMC1IO33	PMC1IO34	PMC1IO35
6	GND	PMC1IO36	PMC1IO37	PMC1IO38	PMC1IO39	PMC1IO40
5	GND	PMC1IO41	PMC1IO42	PMC1IO43	PMC1IO44	PMC1IO45
4	GND	PMC1IO46	PMC1IO47	PMC1IO48	PMC1IO49	PMC1IO50
3	GND	PMC1IO51	PMC1IO52	PMC1IO53	PMC1IO54	PMC1IO55
2	GND	PMC1IO56	PMC1IO57	PMC1IO58	PMC1IO59	PMC1IO60
1	GND	PMC1IO61	PMC1IO62	PMC1IO63	PMC1IO64	VCC3
*Power to pins E18 and E19 are *not* supplied by the CPN5365 SBC.						

Table 2-3. Signal Descriptions for CPTM-01 Rear I/O

Signal	Signal Mnemonic	Signal Description
Universal Serial Bus (Channel 0 and Channel 1)	USDATAn+	(+) signal of differential data pair for USB channel
	USDATAn-	(-) signal of differential data pair for USB channel
Serial COM Ports (1 and 2)	CTSn	Clear to send
	DCDn	Data carrier detected
	DSRn	Data set ready
	DTRn	Data terminal ready
	RIn	Ring indicator
	RTSn	Request to send
	RXDn	Serial receive data
	TXDn	Serial transmit data
General	GND	ground plane
	VCC	+5 Volt power
	VCC3	+3.3 Volt power
	+12V	+12 Volt power
	-12V	- 12 Volt power
PMC1 I/O	PMC1IO [1 to 64]	PMC channel 1 I/O signals 1 through 64

Table 2-4. CPTM-01 Rear I/O Connector (J4)

Pin	F	E	D	C	B	A
25	GND					
24	GND					
23	GND					
22	GND					
21	GND					
20	GND					
19	GND	GRN	RED			
18	GND	BLU	GND			

Table 2-4. CPTM-01 Rear I/O Connector (J4)

Pin	F	E	D	C	B	A
17	GND	HSYNC	DDCCLK			
16	GND	VSYNC	DDCDAT			
15	GND					
KEY						
11	GND					
10	GND					
9	GND					
8	GND					
7	GND	PD2	AFD-	STB-		
6	GND	PD6	PD0	ERR-	PD1	INIT-
5	GND	SLCT	SLIN-	PD3	PD4	PD5
4	GND	DRVDENS0	PD7	ACK-	BUSY	PE
3	GND	DSKCHG-	HDSEL-	RDATA-	WPROT-	TR0-
2	GND	WGATE-	WDATA-	STEP-	DIR-	MTR1-
1	GND	DS0	DS1-	MTR0-	INDEX-	DRVDENS1

Table 2-5. Signal Descriptions for the CPTM-01 Backplane Connector (J4)

Signal	Signal Mnemonic	Signal Description
Floppy Disk Drive	DSKCHG-	Indicates drive door is open
	DIR-	Controls direction of the head during step operations
	DRVDENS[1:0]	Disk density select communication
	DS[1:0]-	Drive selects
	HDSEL-	Selects top or bottom side head
	INDEX-	Indicates the beginning of a track
	MTR[1:0]-	Motor enables
	RDATA-	Data read
	STEP-	Step, pulses move head in or out
	TR0	Indicates that head is positioned above track 00
	WDATA-	Write data to drive
	WGATE-	Enables head write circuitry of drive
	WPROT-	Indicates a disk is write-protected
Parallel LPT Port	ACK-	Pulsed by peripheral to acknowledge data sent
	BUSY	Indicates that the printer cannot accept more data
	ERR-	Peripheral detected an error
	PD[7:0]	Parallel data lines, bits 7- 0
	PE	Paper end, indicates printer out of paper
	AFD-	Auto feed, causes printer to line feed
	INIT-	Initializes the printer
	SLIN-	Select in, selects the printer
	STB-	Data strobe, indicates data is valid
	SLCT	Select, peripheral indicates it is selected

Table 2-5. Signal Descriptions for the CPTM-01 Backplane Connector (J4)

Signal	Signal Mnemonic	Signal Description
Video	RED	Red signal
	GRN	Green signal
	BLU	Blue signal
	HSYNC	Horizontal synchronization
	VSYNC	Vertical synchronization
	DDCCLK	Display Data Channel clock signal for DDC2 support
	DDCDAT	Display Data Channel data signal for DDC2 support

Table 2-6. CPTM-01 Rear I/O Connector (J5)

Pin	F	E	D	C	B	A
22	GND	SDRESET-	SINTRQ	KBDDAT	RD1+	TD1+
21	GND	SCS1-	SDMACK-	KBDCLK	RD1-	TD1-
20	GND	SCS3-	SIORDY	RESET_IN	AUXVCC2	GND
19	GND	SDMARQ	SDIOW-	MDAT	RD2+	TD2+
18	GND	SDA2	SDIOR-	MCLK	RD2-	TD2-
17	GND	SDA1	SDA0	SDD15	AUXVCC1	GND
16	GND	SDD14	SDD13	SDD12	SDD11	SDD10
15	GND	SDD9	SDD8	SDD7	SDD6	SDD5
14	GND	SDD4	SDD3	SDD2	SDD1	SDD0
13	GND					
12	GND					
11	GND					
10	GND					
9	GND					
8	GND					
7	GND					
6	GND					
5	GND					

Table 2-6. CPTM-01 Rear I/O Connector (J5)

Pin	F	E	D	C	B	A
4	GND					
3	GND					
2	GND					
1	GND					GND

Table 2-7. Signal Descriptions for the CPTM-01 Backplane Connector (J5

Signal	Signal Mnemonic	Signal Description
Miscellaneous	AUXVCCn	Auxiliary VCC power, fused at 0.75A maximum
	GND	Digital signal ground plane
EIDE (ATA-2), Secondary Channel	SDMARQ	Drive DMA request
	SDMACK-	Drive DMA acknowledge
	SDIOR-	Drive I/O read
	SDIOW-	Drive I/O write
	SIORDY	Indicates drive is ready for I/O cycle(s)
	SDD[15:0]	Drive data lines, bits 15- 0
	SDRESET-	Reset signal to drive
	SCS1-	Chip select drive 0, also command register block select
	SCS3-	Chip select drive 1, also command register block select
	SDA[2:0]	Drive register and data port address lines
	SINTRQ	Drive interrupt request
Ethernet	RDn+, RDn-	Differential receive lines
	TDn+, TDn-	Differential transmit lines
Keyboard/Mouse Device	MCLK	Clock for PS/2 mouse
	MDAT	Serial data line for PS/2 mouse
	KBDCLK	Clock for PC/AT or PS/2 keyboard
	KBDDAT	Serial data line for PC/AT or PS/2 keyboard

PMC I/O Connectors

Table 2-8. PMC 1 and 2 I/O Connectors (J14, J10)

J14 and J10			
Pin Number	**Signal**	**Signal**	**Pin Number**
1	PMCxIO1	PMCxIO2	2
3	PMCxIO3	PMCxIO4	4
5	PMCxIO5	PMCxIO6	6
7	PMCxIO7	PMCxIO8	8
9	PMCxIO9	PMCxIO10	10
11	PMCxIO11	PMCxIO12	12
13	PMCxIO13	PMCxIO14	14
15	PMCxIO15	PMCxIO16	16
17	PMCxIO17	PMCxIO18	18
19	PMCxIO19	PMCxIO20	20
21	PMCxIO21	PMCxIO22	22
23	PMCxIO23	PMCxIO24	24
25	PMCxIO25	PMCxIO26	26
27	PMCxIO27	PMCxIO28	28
29	PMCxIO29	PMCxIO30	30
31	PMCxIO31	PMCxIO32	32
33	PMCxIO33	PMCxIO34	34
35	PMCxIO35	PMCxIO36	36
37	PMCxIO37	PMCxIO38	38
39	PMCxIO39	PMCxIO40	40
41	PMCxIO	PMCxIO	42
43	PMCxIO	PMCxIO	44
45	PMCxIO	PMCxIO	46
47	PMCxIO	PMCxIO	48
49	PMCxIO	PMCxIO	50
51	PMCxIO	PMCxIO	52

Table 2-8. PMC 1 and 2 I/O Connectors (J14, J10) (Continued)

J14 and J10			
Pin Number	**Signal**	**Signal**	**Pin Number**
53	PMCxIO	PMCxIO	54
55	PMCxIO	PMCxIO	56
57	PMCxIO	PMCxIO	58
59	PMCxIO	PMCxIO	60
61	PMCxIO	PMCxIO	62
63	PMCxIO	PMCxIO	64

Ethernet Connectors

Table 2-9. CPTM-01 Ethernet Connectors (J18) and (J13)

Pin	Signal Mnemonic	Signal Description
1	TX+	Differential transmit lines
2	TX-	Differential transmit lines
3	RX+	Differential receive lines
4	-	-1
5	-	-
6	RX-	Differential receive lines
7	-	-
8	-	-

Serial Port Connectors

Table 2-10. CPTM-01 Serial Port Connector (J28)

Pin	Single Mnemonic	Signal Description
1	DCD-	Data set has detected the data carrier
2	RX	Receives serial data input from communication link
3	TX	Sends serial output to communication link
4	DTR-	Indicates that a data set is ready to establish a communication link
5	GND	Ground
6	DSR-	Indicates that a data set is ready to establish a communication link
7	RTS-	Indicates to data set that UART is ready to exchange data
8	CTS-	Indicates that a data set is ready to exchange data
9	RI-	Indicates that a modem has received a telephone ringing signal

Table 2-11. CPTM-01 Serial Port Connector COM1 (J21)

Pin	Signal Mnemonic	Signal Description
1	DCD-	Data set has detected the data carrier
2	DSR-	Data set is ready to establish a communications link
3	RX	Receives serial data input from communication link
4	RTS-	UART is ready to exchange data
5	TX	Sends serial data to communication link
6	CTS-	Data set is ready to exchange data
7	DTR-	Data set is ready to establish a communication link
8	RI-	Modem has received a telephone ringing signal
9	GND	Ground
10	CGND	Chassis ground

Video Connector

Table 2-12. CPTM-01 Video Connector (J16)

Pin	Signal Mnemonic	Signal Description
1	RED	Red signal
2	GREEN	Green signal
3	BLUE	Blue signal
4	NC	no connection
5	DACVSS	Video return
6	DACVSS	Video return
7	DACVSS	Video return
8	DACVSS	Video return
9	NC	no connection
10	DACVSS	Video return
11	NC	no connection
12	DDCDAT	Display Data Channel data signal for DDC2 support
13	HSYNC	Horizontal synchronization
14	VSYNC	Vertical synchronization
15	DDCCLK	Display Data Channel clock signal for DDC2 support

Keyboard/Mouse P/S2 Connector

Table 2-13. CPTM-01 Keyboard/Mouse Connector (J27)

Pin	Signal Mnemonic	Signal Description
1	KBDDAT	Data line for keyboard
2	AUXDAT	Data line for mouse
3	GND	Ground
4	KBDVCC	Keyboard Power
5	KBDCLK	Clock for keyboard
6	AUXCLK	Clock for mouse
7	CGND	Common Ground

Universal Serial Bus Connectors

Table 2-14. CPTM-01 USB Connector (J19)

Pin	Signal Mnemonic	Signal Description
1	VCC	Current limited USB power
2	VCC	Current limited USB power
3	DATA1-	USB serial communication differential pair
4	DATA0-	USB serial communication differential pair
5	DATA1+	USB serial communication differential pair
6	DATA0+	USB serial communication differential pair
7	GND	USB port common
8	GND	USB port common

Parallel Connector

Table 2-15. CPTM-01 Parallel Connector (J20)

Pin	Signal Mnemonic	Signal Description
1	STROBE-	Indicates data at parallel port is valid
2	AFD-	Causes printer to add a line feed
3	D0	Parallel data lines
4	ERR-	Set low when an error is detected
5	D1	Parallel data lines
6	INIT-	Initializes the printer
7	D2	Parallel data lines
8	SLIN-	Selects the printer
9	D3	Parallel data lines
10	GND	Ground
11	D4	Parallel data lines
12	GND	Ground
13	D5	Parallel data lines
14	Ground	GND

Table 2-15. CPTM-01 Parallel Connector (J20)

Pin	**Signal Mnemonic**	**Signal Description**
15	D6	Parallel data lines
16	GND	Ground
17	D7	Parallel data lines
18	GND	Ground
19	ACK-	Input is pulsed by the peripheral to acknowledge data retrieval
21	BUSY	Printer cannot accept any more data
23	PE	Printer is out of paper
25	SELECT	Set high when selected

EIDE Connector

Table 2-16. CPTM-01 Secondary IDE Connector (J26)

Pin	Signal Mnemonic	Signal Description	Pin	Signal Mnemonic	Signal Description
1	RESET-	Reset signal to drive	2	GND	Ground
3	DD7	Drive data line	4	DD8	Drive data line
5	DD6	Drive data line	6	DD9	Drive data line
7	DD5	Drive data line	8	DD10	Drive data line
9	DD4	Drive data line	10	DD11	Drive data line
11	DD3	Drive data line	12	DD12	Drive data line
13	DD2	Drive data line	14	DD13	Drive data line
15	DD1	Drive data line	16	DD14	Drive data line
17	DD0	Drive data line	18	DD15	Drive data line
19	GND	Drive data line	20	-	-
21	DMARQ	Drive DMA request	22	GND	Ground
23	IOW-	Drive I/O write	24	GND	Ground
25	IOR-	Drive I/O read	26	GND	Ground
27	IORDY	Drive is ready for I/O cycle(s)	28	CSEL-	Cable select
29	DMACK-	Drive DMA acknowledge	30	GND	Ground
31	INTRQ	Drive interrupt request	32	IOCS16-	Indicates a 16 bit register is decoded
33	DA1	Drive register and data port address line	34	PDIAG-	Output from drive 1 and monitored by drive 0
35	DA0	Drive register and data port address line	36	DA2	Drive register and data port address line
37	CS1-	Chip select drive 0, also command register block select	38	CS3-	Chip select drive 1, also command register block select
39	DASP-	Drive active/slave present	40	GND	Ground

CompactFlash Connector

Table 2-17. CPTM-01 CompactFlash Connector (J25)

Pin	Signal Mnemonic	Signal Description	Pin	Signal Mnemonic	Signal Description
1	GND	Ground	26	-	-
2	DD3	Drive data line	27	DD11	Drive data line
3	DD4	Drive data line	28	DD12	Drive data line
4	DD5	Drive data line	29	DD13	Drive data line
5	DD6	Drive data line	30	DD14	Drive data line
6	DD7	Drive data line	31	DD15	Drive data line
7	CS1-	Chip select drive 0, also command register block select	32	CS3-	Chip select drive 1, also command register block select
8	GND	Ground	33	-	-
9	GND	Ground	34	IOR-	Drive I/O read
10	GND	Ground	35	IOW-	Drive I/O write
11	GND	Ground	36	VCC	+5 Volts
12	GND	Ground	37	INTRQ	Drive interrupt request
13	VCC	+5 Volts	38	VCC	+5 Volts
14	GND	Ground	39	CSE:L-DD3	Cable select
15	GND	Ground	40	-	-
16	GND	Ground	41	RESET-	Reset signal to drive
17	GND	Ground	42	IORDY	Drive is ready for I/O cycle(s)
18	DA2	Drive register and data port address lines	43	-	-
19	DA1	Drive register and data port address lines	44	VCC	+5 Volts
20	DA0	Drive register and data port address lines	45	DASP-	Drive active/slave present
21	DD0	Drive data line	46	PDIAG-	Output from drive 1 and monitored by drive 0

Table 2-17. CPTM-01 CompactFlash Connector (J25) (Continued)

Pin	Signal Mnemonic	Signal Description	Pin	Signal Mnemonic	Signal Description
22	DD1	Drive data line	47	DD8	Drive data line
23	DD2	Drive data line	48	DD9	Drive data line
24	-	-	49	DD10	Drive data line
25	-	-	50	GND	Ground

Floppy Connector

Table 2-18. CPTM-01 Floppy Connector (J9)

Pin	Signal Mnemonic	Signal Description
1	GND	Drive Common
2	DRVDENS0	Disk density select communication
3	-	-
4	-	-
5	GND	Drive Common
6	DRVDENS1	Disk density select communication
7	GND	Drive Common
8	INDEX-	Indicates the beginning of a track
9	GND	Drive Common
10	MTR0-	Motor enable outputs
11	GND	Drive Common
12	DS1-	Drive select 1
13	GND	Drive Common
14	DS0-	Drive select 0
15	GND	Drive Common
16	MTR1-	Motor enable outputs
17	GND	Drive Common
18	DIR-	Controls the direction of the FDD head during seek operations
19	GND	Drive Common
20	STEP-	Supplies step pulses to move head during seek operations
21	GND	Drive Common
22	WDATA-	Writes serial data to disk drive
23	GND	Drive Common
24	WGATE-	Enables head of disk drive to write to disk
25	GND	Drive Common
26	TR0-	Indicates that head of FDD is at track 0
27	GND	Drive Common

Table 2-18. CPTM-01 Floppy Connector (J9) (Continued)

Pin	Signal Mnemonic	Signal Description
28	WPROT-	Indicates a disk is write protected
29	GND	Drive Common
30	RDATA-	Raw read data from disk drive
31	GND	Drive Common
32	HDSEL-	Determines side of the floppy disk being accessed
33	GND	Drive Common
34	DSKCHG-	Notifies the disk drive controller that the drive door is open

Indicator LED/Miscellaneous Connector

Table 2-19. CPTM-01 Drive LEDs/Reset Connector (J2)

Pin	Signal Mnemonic	Signal Description
1	VCC	+5 Volt power
2	-	-
3	VCC	+5 Volt power
4	-	-
5	VCC	+5 Volt power
6	EIDE_LEDa	Secondary channel EIDE activity LED
7	VCC	+5 Volt power
8	EIDE_LEDb	Primary channel EIDE activity LED
9	VCC	+5 Volt power
10	-	-
11	GND	Ground
12	PBRESET	Pushbutton reset
13	GND	Ground
14	CSEL-	Tie this pin to ground to make the CompactFlash master

Starting Up the CPN5365 3

This chapter gives you information about the power-up procedure and the CPN5365 switches and indicators.

Applying Power to the System

After you verify that all necessary hardware preparation is complete and all connections are made correctly, you can apply power to the system.

When you are ready to apply power to the CPN5365:

- Verify that the chassis power supply voltage setting matches the voltage present in the country of use (if the power supply in your system is not auto-sensing)
- On powering up, the CPN5365 displays the PhoenixBIOS banner and then runs a memory test

Switches and Indicators

You can access a pushbutton reset switch through the CPN5365 Single Board Computer front panel and program this switch for hard or soft reset.

There are two indicators on the CPN5365 front panel:

- Blue **EXT** LED indicating hot swap status
- Green **PWR** LED indicating power on

Each Ethernet controller has two sets of indicator LEDs mounted on the back side of the board used to debug connection problems (DS3, DS4, DS5, and DS6). A green LED indicates a linked connection and an amber LED indicates packet transmit. Refer to the next figure for the location of these LEDs.

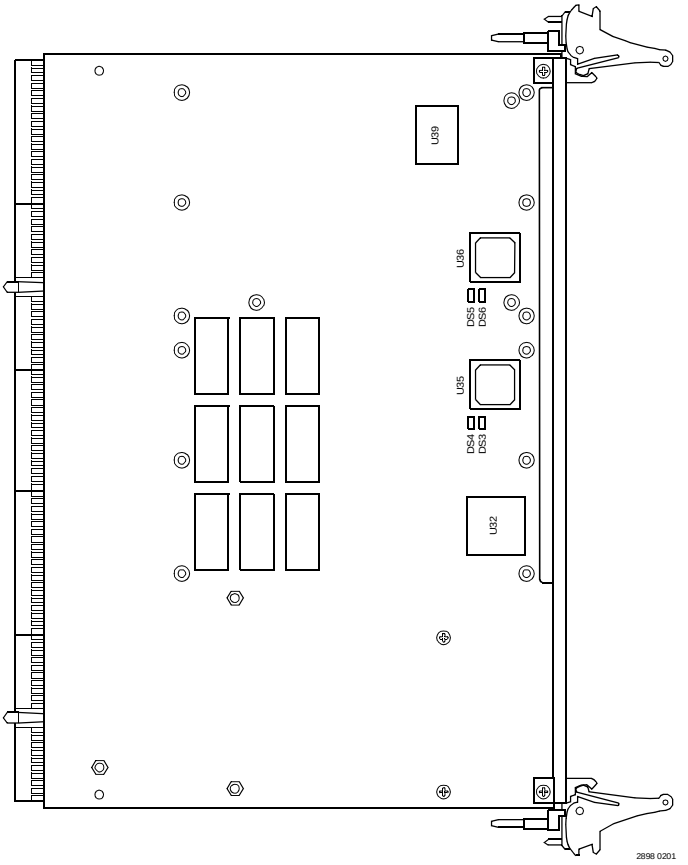


Figure 3-1. Location of the Debug LEDs, CPN5365 Secondary Side

Functional Description

4

This chapter provides a functional description of all major components and devices on the CPN5365.

The following block diagram illustrates the major components and their circuitry on the CPN5365 Single Board Computer.

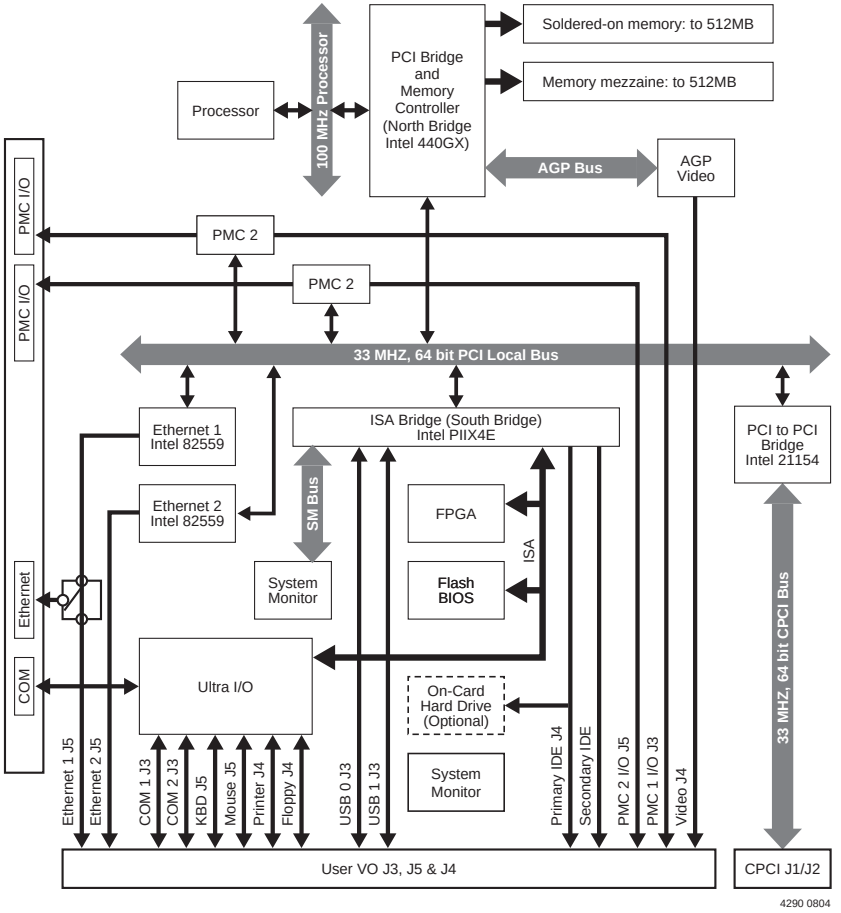


Figure 4-1. Block Diagram of CPN5365

Pentium III Processor

The CPN5365 supports a low power Intel Mobile Pentium III processor that is based on 0.18 micron process. The processor executes Intel MMX technology instruction for enhanced media and communication performance. It includes an integrated on-die L1 4-way associative L1 cache with 16KB instruction and 16KB write-back data cache, and an on-die 256KB, ECC protected cache data array, 8-way set associative L2 cache that operates at full core speed. For further information, refer to Appendix C, *Related Documentation* for the Intel Mobile Pentium III processor data sheet.

Peripheral Component Interconnect (PCI) Local Bus Interface

The PCI local bus is a high-performance, 32-bit bus with multiplexed address and data lines. Use it as an interconnect mechanism between highly-integrated peripheral controller components, peripheral add-in boards and processor/memory systems.

The CPN5365 supports a 32-bit local PCI bus interface. On-board devices connect directly to the local PCI bus.

CompactPCI Bus Interface

The CPN5365 supports a single 64-bit CompactPCI bus interface. You can insert the physical connector into a 64-bit High Availability CompactPCI backplane and make connection to off-card CompactPCI peripherals through the Intel 21555 PCI-PCI bridge.

Unlike a transparent PCI-to-PCI bridge, the Intel 21555 is designed to bridge two processor domains. The system CompactPCI bus is connected to the primary bus side of the bridge, which is also referred to as the host domain or the host processor side. The secondary bus interfaces to the local PCI bus, referred to as the local domain or local processor side. The bridge chip supports independent primary and secondary address spaces

and address translation between the two processor domains. It accepts a Type 0 configuration header with configuration space accessible from both primary and secondary busses. Refer to the *CPIP5365 CompactPCI Single Board Computer Programmer's Reference Guide* for additional information and programming details.

Intel 21555 Non Transparent PCI-to-PCI Bridge

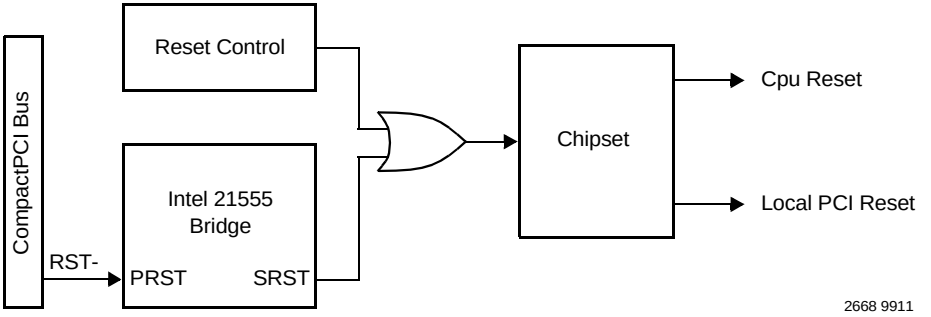
This nontransparent PCI-to-PCI bridge provides the technology for high performance embedded and intelligent I/O applications. The Intel 21555 is designed specifically for applications where a processor is used behind a PCI-to-PCI bridge. It offers independent address spaces and asynchronous clocks to deliver application flexibility and allows the local processor to have complete PCI configuration control of subsystem devices, without host interference. The CPN5365 allows several options for configuring the Intel 21555 using the BIOS. For more information, refer to the *CPN5365 Single Board Computer Programmer's Reference Guide* listed in Appendix C, *Related Documentation*.

CPN5365 in a Nonhost Slot

The CPN5365 is intended for mounting in a nonhost slot as a peripheral CPU. The module configures itself for peripheral mode when it plugs into a peripheral slot. The CompactPCI interface device is a nontransparent bridge (Intel 21555). The local CPU enumerates the local devices and sets up the bridge for configuration by the host CPU. The peripheral CPU can also configure itself onto the Compact PCI bus using a scheme allowing it to map itself to a particular area using the geographical addressing CPCI lines.You can read these lines through the FPGA. Refer to the FPGA register description in the *CPN5365 Single Board Computer Programmer's Reference Guide* for information about reading these bits.

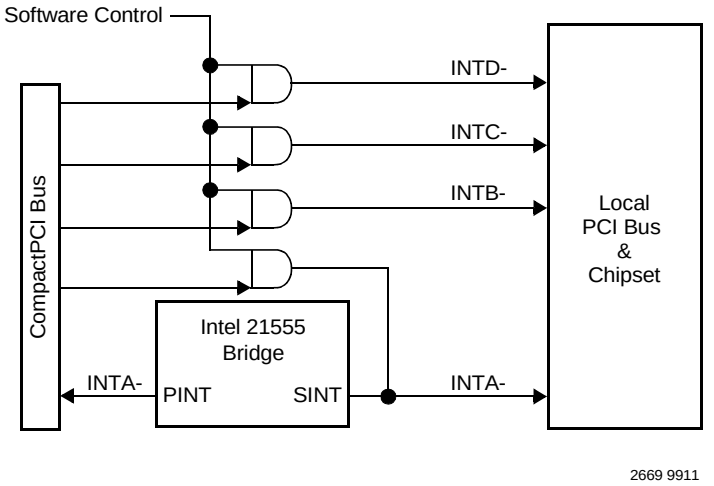
Peripheral Reset Function

In peripheral mode the PCI reset signal comes from the CompactPCI bus through the bridge to reset all on-card functions. You can reset the card independently without affecting other cards in the system.



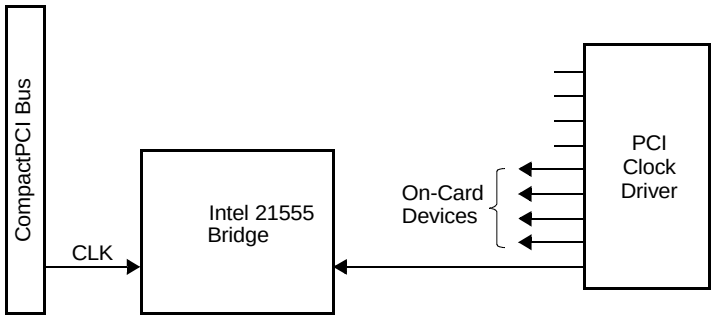
Peripheral PCI Interrupt Function

In peripheral mode the PCI interrupts route as shown below. The Intel 21555 bridge's primary interface can generate a system interrupt via the INTA- line on the CompactPCI bus. Local and host CPUs can generate an interrupt to the other CPU via the Intel 21555's primary and secondary doorbell interrupts.



Peripheral PCI Clock Function

In peripheral mode the Intel 21555's primary interface connects to the CompactPCI CLK (clock) signal. The secondary interface connects to an on-card PCI clock. In this configuration the bridge operates in asynchronous clocking mode.



Peripheral Hot Swap Function

The CPN5365 complies with the CompactPCI Hot Swap Specification in peripheral mode. You must, however, use a compliant backplane with proper pin staging.

Field Programmable Gate Array Registers

Use the system's Field Programmable Gate Array (FPGA) for add-on features and control, and to connect to the internal ISA bus. The FPGA consists of a group of I/O registers for control of features such as a Watchdog Timer, I/O switching control, NVRAM control and decoding, and system management functions. For registers and programming information, refer to the *CPN5365 Single Board Computer Programmer's Reference Guide*.

Watchdog Timer

The Field Programmable Gate Array (FPGA) includes a watchdog timer. The watchdog timer has these modes of operation:

- Disabled
- Sets the timeout flag in the Watchdog Strobe/Status port in ISA I/O memory map
- Sets the timeout flag in the Watchdog Strobe/Status port in ISA I/O memory map + Assert a selectable interrupt (ISA IRQ)
- Sets the timeout flag in the Watchdog Strobe/Status port in ISA I/O memory map + Assert NMI followed by a system Reset or Soft Reset

You can program the watchdog timer using registers in the ISA I/O memory map. Refer to the *CPIP5365 Single Board Computer Programmer's Reference Guide* for more information about the watchdog timer and the watchdog timer register.

Jump to User Code in Alternate Flash Bank

The flash device for the BIOS is a 4MB part consisting of eight 512K banks. The BIOS occupies bank 0 only.

From the boot screen in the BIOS setup, you can select an alternate 512K flash bank to load and execute instead of booting from standard devices in the boot menu. If you select one of the alternate banks (banks 1 - 7), the BIOS looks for the five character signature "_MOT_" in the last five bytes of the selected 512K bank. If found, the BIOS disables interrupts, timers, and the watchdog. Then it reads the top 64K of the selected bank into segment 0F000h and jumps to 0F000:FFF0h. If the signature is not found, the BIOS proceeds normally and attempts to boot from standard floppy and hard drive devices.

Note When the bank switch and jump occurs, it happens very late in POST after all hardware is initialized.

Desktop Management Interface

The Desktop Management Interface (DMI) gives you a standard method for storing information about the computing system. It also provides mechanisms to make this information available to applications programs. You can use the DMI to determine:

- Types of system components
- System capabilities
- Operational status
- Installation date

The CPN5365 BIOS is compatible with the System Management BIOS Reference Specification, Version 2.3.1. You can get this specification on the Distributed Management Task Force, Inc. (DTMF) website. Refer to Appendix C, *Related Documentation* for information about how to access

this document. The BIOS specification defines a way of reading this information through the BIOS using Plug and Play BIOS functions 50h - 5fh.

The specification defines various structures used to store system information as data bytes and/or as ASCII strings. For example, the Type 0 structure stores BIOS information and the Type 1 structure stores system information. The Type 11 structure provides additional information about the system using reserved, custom/OEM strings defined by the manufacturer.

PhoenixBIOS Description

The CPN5365 uses the PhoenixBIOS to provide initial hardware configuration for local devices and local operating system boot.

The CPN5365 BIOS is similar to the CPIP5365 BIOS. Refer to Appendix C, *Related Documentation*, for a listing of related documentation that describes the PhoenixBIOS, PCI-to PCI bridge configuration, and programming information. Refer to *Jump to User Code in Alternate Flash Bank* on page 4-7 for additional information about the CPN5365 BIOS.

Soft Reset

You can generate a soft reset from your keyboard, the watchdog timer, or the front panel push button in Soft Reset Mode. The BIOS preserves as much of the system memory state as possible.

A CPN5365 circuit monitors system power and provides the PWROK signal to the PIIX4E. The PIIX4E distributes the reset to the rest of the board by generating the CPU, PCI, and IDE resets. You can also reset the board using the front panel reset switch and the FPGA watchdog timer. You can program the Watchdog Timer and the front panel push button switch to generate a soft reset. Refer to *Field Programmable Gate Array Registers* on page 4-6 for programming information.

Headless Operation

The BIOS can operate with no keyboard or display. You do, however, need a keyboard and display to change setup options unless you use the remote setup feature.

Remote Setup

You can change setup options remotely through the BIOS Setup - Advanced Menu using a COM port. The default settings for a terminal are 19.2k baud, 1 stop bit, no parity and CTS/RTS flow control.

If the “Active After POST” setting in the BIOS is set to OFF, the serial COM port is released once the system booting has started. This enables other applications to use it. OFF is the default BIOS setting.

If, however, the “Active After POST” setting in the BIOS is set to ON, the serial COM port continues to mirror the console port.

Network Boot

We include the Intel PXE (Pre-boot Execution Environment) 82559 BIOS extension module to provide operating system boot via one of the 82559 ports. This module is built into the BIOS. You can enable the PXE for either port through the BIOS Setup-Advanced-PCI Configuration Menu.

The CPN5365 BIOS stores specific information about the individual board in the Type 11 structure, in this null-terminated ASCII string format:

```
[VPD]
PRODUCT=CPN5365
BOARD_ASSEMBLY=01-W3658f01B
BOARD_SN=1234567
BOARD_BUILD_DATE=01/15/2001
BIOS_VERSION=1.0RM01
BIOS_ASSEMBLY=98-W4079D06A
[FAT]
ENET1_MAC=0001 AF00 5F41
ENET2_MAC=0001 AF00 5F42
```

[VPD] is the first of the Vital Product Data (VPD) strings, and [FAT} is the first of the Factory Assurance Test strings. Each ASCII string starts with a description of the information following the = sign.

The BOARD_SN=nnnnnnn string gives the board serial number. The ENETn_MAC=nnnn nnnn nnnn strings give the MAC addresses of the two Ethernet ports. Characters in bold type are different for different boards, to show the different board serial number and MAC addresses, different BIOS versions and different build dates. Other strings used in the Motorola manufacturing process.

You can also use other tools that make it easier to develop applications that can access DMI data. Software Development Kits (SDKs) and C libraries can make DMI data available through higher-level function calls that can be incorporated into an application program.

Temperature and Voltage Monitoring on the Board and Processor

Two on-board devices (a Maxim MAX1617 temperature sensor and a National LM81 system monitor) provide board and processor, temperature and voltage monitoring. You can read data from and write data to these devices over the System Management Bus (SMBus) through registers in the PIIX4E South Bridge. For register programming information refer to the PIIX4E data sheet listed in Appendix C, *Related Documentation*.

The MAX1617 temperature sensor maps to SMBus address 1001110b. It monitors the Pentium III CPU die temperature and the board temperature at the bottom of the board adjacent to the CPU. The LM81 system monitor maps to SMBus address 0101101b. It monitors the power supplies on the board (+5V, +3.3V, ±12V), the processor I/O voltage (+1.5V), the CPU core voltage, and the board temperature at the top of the board.

Note You cannot use the LM81 system monitor fan tachometer inputs and chassis intrusion functions. There are no connections on the CPN5365 to any of these inputs/outputs.

On both devices, an internal analog to digital converter (ADC) continually measures voltages and/or voltage drops across diodes, and stores the resulting data in internal registers. You can read this data via the SMBus. You can also program the MAX1617 and LM81 through the SMBus accessible registers to set high and low limits for each measured parameter, and to generate an alarm output when these limits are exceeded. Alarm outputs route to the Field Programmable Gate Array, where you can read them from a status register or they can generate an interrupt. For programming information about the MAX1617 temperature sensor and LM81 system monitor, refer to *Field Programmable Gate Array Registers* on page 4-6, and Appendix C, *Related Documentation*.

Connector Pin Assignments

5

This chapter gives you connector pin assignments for CPN5365 Single Board Computer. Pin assignments for the CPTM-01 are located in Chapter 2, *Installing the CPTM-01*.

CPN5365 Single Board Computer Connectors

CompactPCI Bus Connectors (J1 and J2)

The CPN5365 Single Board Computer provides a 64-bit CompactPCI interface on connectors J1 and J2. J1 is a 110 pin connector (2mm hard metric type n) with keying for +3.3Vor +5V. J2 is a 110 pin connector (2mm hard metric type n.) Refer to the next two tables for J1 and J2 pin designations.

Table 5-1. CPN5365 Backplane Connector (J1)

Pin	F	E	D	C	B	A
25	GND	VCC	VCC3	ENUM#	REQ64#	VCC
24	GND	ACK64#	AD[0]	VIO	VCC	AD[1]
23	GND	AD[2]	VCC	AD[3]	AD[4]	VCC3
22	GND	AD[5]	AD[6]	VCC3	GND	AD[7]
21	GND	C/BE[0]#	M66EN	AD[8]	AD[9]	VCC3
20	GND	AD[10]	AD[11]	VIO	GND	AD[12]
19	GND	AD[13]	GND	AD[14]	AD[15]	VCC3
18	GND	C/BE[1]#	PAR	VCC3	GND	SERR#
17	GND	PERR#	GND	SBO#	SDONE	VCC3
16	GND	LOCK#	STOP#	VIO	GND	DEVSEL#
15	GND	TRDY#	BD_SEL#	IRDY#	FRAME#	VCC3
KEY						
11	GND	C/BE[2#]	GND	AD[16]	AD[17]	AD[18]

Table 5-1. CPN5365 Backplane Connector (J1)

Pin	F	E	D	C	B	A
10	GND	AD[19]	AD[20]	VCC3	GND	AD[21]
9	GND	AD[22]	GND	AD[23]	IDSEL	C/BE[3]#
8	GND	AD[24]	AD[25]	VIO	GND	AD[26]
7	GND	AD[27]	GND	AD[28]	AD[29]	AD[30]
6	GND	AD[31]	CLK	VCC3	GND	REQ#
5	GND	GNT#	GND	RST#	BRSVP1B5	BRSVP1A5
4	GND	INTS	INTP	VIO	HLTY	BRSVP1A4
3	GND	INTD#	VCC	INTC#	INTB#	INTA#
2	GND	TD1	TD0	TMS	VCC	TCK
1	GND	VCC	+12V	TRST#	-12V	VCC

Table 5-2. CPN5365 Backplane Connector (J2)

Pin	F	E	D	C	B	A
22	GND	GA0	GA1	GA2	GA3	GA4
21	GND	RSV	RSV	RSV	GND	CLK6
20	GND	RSV	GND	RSV	GND	CLK5
19	GND	RSV	RSV	RSV	GND	GND
18	GND	BRSVP2E18	GND	BRSVP2C18	BRSVP2B18	BRSVP2A18
17	GND	GNT6#	REQ6#	PRST#	GND	BRSVP2A17
16	GND	BRSVP2E16	GND	DEG#	BRSVP2B16	BRSVP2A16
15	GND	GNT5#	REQ5#	FAL#	GND	BRSVP2A15
14	GND	AD[32]	GND	AD[33]	AD[34]	AD[35]
13	GND	AD[36]	AD[37]	VIO	GND	AD[38]
12	GND	AD[39]	GND	AD[40]	AD[41]	AD[42]
11	GND	AD[43]	AD[44]	VIO	GND	AD[45]
10	GND	AD[46]	GND	AD[47]	AD[48]	AD[49]
9	GND	AD[50]	AD[51]	VIO	GND	AD[52]
8	GND	AD[53]	GND	AD[54]	AD[55]	AD[56]

Table 5-2. CPN5365 Backplane Connector (J2)

Pin	F	E	D	C	B	A
7	GND	AD[57]	AD[58]	VIO	GND	AD[59]
6	GND	AD[60]	GND	AD[61]	AD[62]	AD[63]
5	GND	PAR64	C/BE[4]#	VIO	GND	C/BE[5]#
4	GND	C/BE[6]#	GND	C/BE[7]#	BRSVP2B4	VIO
3	GND	GNT4#	REQ4#	GNT3#	GND	CLK4
2	GND	REQ3#	GNT2#	SYSEN#	CLK3	CLK2
1	GND	REQ2#	GNT1#	REQ1#	GND	CLK1

CompactPCI Rear I/O Connectors (J3, J4, and J5)

Table 5-3. CPN5365 Rear I/O Connector (J3)

Pin	F	E	D	C	B	A
19	GND	No connect	USB0-	USB0+	USB1-	USB1+
18	GND	No connect	COM2_RI	COM2_DTR	COM1_RI	COM1_DTR
17	GND	No connect	COM2_DCD	COM2_DSR	COM1_DCD	COM1_DSR
16	GND	No connect	COM2_TxD	COM2_CTS	COM1_TxD	COM1_CTS
15	GND	No connect	COM2_RxD	COM2_RTS	COM1_RxD	COM1_RTS
14	GND	+5V	+5V	+3.3V	+3.3V	+3.3V
13	GND	PMC2IO1	PMC2IO2	PMC2IO3	PMC2IO4	PMC2IO5
12	GND	PMC2IO6	PMC2IO7	PMC2IO8	PMC2IO9	PMC2IO10
11	GND	PMC2IO11	PMC2IO12	PMC2IO13	PMC2IO14	PMC2IO15
10	GND	PMC2IO16	PMC2IO17	PMC2IO18	PMC2IO19	PMC2IO20
9	GND	PMC2IO21	PMC2IO22	PMC2IO23	PMC2IO24	PMC2IO25
8	GND	PMC2IO26	PMC2IO27	PMC2IO28	PMC2IO29	PMC2IO30
7	GND	PMC2IO31	PMC2IO32	PMC2IO33	PMC2IO34	PMC2IO35
6	GND	PMC2IO36	PMC2IO37	PMC2IO38	PMC2IO39	PMC2IO40
5	GND	PMC2IO41	PMC2IO42	PMC2IO43	PMC2IO44	PMC2IO45
4	GND	PMC2IO46	PMC2IO47	PMC2IO48	PMC2IO49	PMC2IO50
3	GND	PMC2IO51	PMC2IO52	PMC2IO53	PMC2IO54	PMC2IO55
2	GND	PMC2IO56	PMC2IO57	PMC2IO58	PMC2IO59	PMC2IO60
1	GND	PMC2IO61	PMC2IO62	PMC2IO63	PMC2IO64	VIO

Table 5-4. Signal Descriptions for Backplane Connector (J3)

Signal	Signal Mnemonic	Signal Description
Universal Serial Bus (Channel 0 and Channel 1)	USB0+	(+) signal of differential data pair for USB channel 0
	USB0-	(-) signal of differential data pair for USB channel 0
	USB1+	(+) signal of differential data pair for USB channel 1
	USB1-	(-) signal of differential data pair for USB channel 1

Table 5-4. Signal Descriptions for Backplane Connector (J3)

Signal	Signal Mnemonic	Signal Description
Serial COM Ports (1 and 2)	COMx_CTS-	Clear to send
	COMx_DCD-	Data carrier detected
	COMx_DSR-	Data set ready
	COMx_DTR-	Data terminal ready
	COMx_RTS-	Request to send
	COMx_RXD	Serial receive data
	COMx_TXD	Serial transmit data
	COMx_RI	Ring Indicator
General	GND	Ground plane
	+/-3.3V, +/-5V	Power
PMC2 I/O	PMC2IO [1 to 64]	PMC channel 2 I/O signals 1 through 64
PMC VIO	VIO	PMC VIO power (+3.3V)

Connector J4 contains floppy, printer port and miscellaneous functions. J4 is an optional connector. Refer to the next two tables.

Table 5-5. CPN5365 Rear I/O Connector (J4)

Pin	F	E	D	C	B	A
25	GND		PRSTDRV-	PINTRQ	PCS1-	GND
24	GND	PDACK-	PCS3-	PIORDY	PDREQ	PIOW-
23	GND	PA2	PIOR-	PA1	PA0	PD15
22	GND	PD14	PD13	PD12	PD11	PD10
21	GND	PD9	PD8	PD7	PD6	PD5
20	GND	PD4	PD3	PD2	PD1	PD0
19	GND	GRN	RED		PDIAG	PDASP-
18	GND	BLU	GND			
17	GND	HSYNC	DDCCLK			
16	GND	VSYNC	DDCDAT			
15	GND					
KEY						
11	GND					
10	GND					
9	GND					
8	GND					
7	GND	PD2	AFD-	STB-		
6	GND	PD6	PD0	ERR-	PD1	INIT-
5	GND	SLCT	SLIN-	PD3	PD4	PD5
4	GND	DRVDENS0	PD7	ACK-	BUSY	PE
3	GND	DSKCHG-	HDSEL-	RDATA-	WPROT-	TR0-
2	GND	WGATE-	WDATA-	STEP-	DIR-	MTR1-
1	GND	DS0-	DS1-	MTR0-	INDEX-	DRVDENS1

Table 5-6. Signal Descriptions for the Backplane Connector (J4)

Signal	Signal Mnemonic	Signal Description
Floppy Disk Drive	DSKCHG-	Indicates drive door is open
	DIR-	Controls direction of the head during step operation
	DS[1:0]-	Drive selects
	HDSEL-	Selects top or bottom side head
	INDEX-	Indicates the beginning of a track
	MTR[1:0]	Motor enables
	RDATA-	Data read
	STEP-	Step, pulses move head in or out
	TR0-	Indicates that head is positioned above track 00
	WDATA-	Write data to drive
	WGATE-	Enables head write circuitry of drive
	WPROT-	Indicates a disk is write-protected
	DRVDENS[1:0]	Disk density select communication
	PDIAG-	Output from drive 1 and monitored by drive 0
	DASP-	Drive active/slave present
	ACK-	Pulsed by peripheral to acknowledge data sent
	BUSY	Indicates that printer cannot accept more data
	ERR-	Peripheral detected an error
	PD[7:0]	Parallel data lines, bits 7--0
	PE	Paper end, indicates the printer is out of paper
	AFD-	Auto feed, causes printer to line feed
	INIT-	Initializes the printer
	SLIN-	Select in, selects the printer
	STB-	Data strobe, indicates data is valid
	SLCT	Select, peripheral indicates it is selected

Table 5-6. Signal Descriptions for the Backplane Connector (J4)

Signal	Signal Mnemonic	Signal Description
EIDE (ATA-2), Primary Channel	PDREQ-	Drive DMA request
	PDACK-	Drive DMA acknowledge
	PIOR-	Drive I/O read
	PIOW-	Drive I/O write
	PIORDY-	Indicates drive is ready for I/O cycle(s)
	PD[15:0]	Drive data lines, bits 15 -- 0
	DRSTDRV	Reset signal to drive
	PCS1	Chip select drive 0, also command register block select
	PCS3	Chip select drive 1, also command register block select
	PA[2:0]	Drive register and data port address lines
	PINTRQ	Drive interrupt request
	PDASP	Drive active
	PDIAG	Drive inter-communication
Video Signals	RED	Red signal
	GRN	Green signal
	BLU	Blue Signal
	HSYNC	Horizontal synchronization
	VSYNC	Vertical synchronization
	DDCCLK	Display Data Channel clock signal for DDC2 support
	DDCDAT	Display Data Channel data signal for DDC2 support

Table 5-7. CPN5365 Rear I/O Connector (J5)

Pin	F	E	D	C	B	A
22	GND	SRSTDRV-	SINTRQ	KBDDAT	ERX0+	ETX0+
21	GND	SCS1-	SDACK-	KBDCLK	ERX0-	ETX0-
20	GND	SCS3-	SIORDY	RESET_IN	AUXVCC	GND
19	GND	SDREQ	SIOW-	MDAT	ERX1+	ETX1+

Table 5-7. CPN5365 Rear I/O Connector (J5)

Pin	F	E	D	C	B	A
18	GND	SA2	SIOR-	MCLK	ERX1-	ETX1-
17	GND	SA1	SA0	SD15	AUXVCC	GND
16	GND	SD14	SD13	SD12	SD11	SD10
15	GND	SD9	SD8	SD7	SD6	SD5
14	GND	SD4	SD3	SD2	SD1	SD0
13	GND	PMC1IO1	PMC1IO2	PMC1IO3	PMC1IO4	PMC1IO5
12	GND	PMC1IO6	PMC1IO7	PMC1IO8	PMC1IO9	PMC1IO10
11	GND	PMC1IO11	PMC1IO12	PMC1IO13	PMC1IO14	PMC1IO15
10	GND	PMC1IO16	PMC1IO17	PMC1IO18	PMC1IO19	PMC1IO20
9	GND	PMC1IO21	PMC1IO22	PMC1IO23	PMC1IO24	PMC1IO25
8	GND	PMC1IO26	PMC1IO27	PMC1IO28	PMC1IO29	PMC1IO30
7	GND	PMC1IO31	PMC1IO32	PMC1IO33	PMC1IO34	PMC1IO35
6	GND	PMC1IO36	PMC1IO37	PMC1IO38	PMC1IO39	PMC1IO40
5	GND	PMC1IO41	PMC1IO42	PMC1IO43	PMC1IO44	PMC1IO45
4	GND	PMC1IO46	PMC1IO47	PMC1IO48	PMC1IO49	PMC1IO50
3	GND	PMC1IO51	PMC1IO52	PMC1IO53	PMC1IO54	PMC1IO55
2	GND	PMC1IO56	PMC1IO57	PMC1IO58	PMC1IO59	PMC1IO60
1	GND	PMC1IO61	PMC1IO62	PMC1IO63	PMC1IO64	TMPRSNT

Table 5-8. Signal Descriptions for the Backplane Connector (J5)

Signal	Signal Mnemonic	Signal Description
Ethernet	ERX1+, ERX1-	Differential receive lines, Ethernet 1
	ETX1+, ETX1-	Differential transmit lines, Ethernet 1
	ERX2+, ERX2-	Differential receive lines, Ethernet 2
	ERX2+, ETX2-	Differential transmit lines, Ethernet 2

Table 5-8. Signal Descriptions for the Backplane Connector (J5)

Signal	Signal Mnemonic	Signal Description
Keyboard/Mouse Device, TTL Levels	MCLK	Clock for PS/2 mouse
	MDAT	Serial data line for PS/2 mouse
	KBDCLK	Clock for PC/AT or PS/2 keyboard
	KBDDAT	Serial data line for PC/AT or PS/2 keyboard
Miscellaneous Signals	TMPRSNT	Indicates transition module is installed
	AUXVCC	Auxiliary VCC power
PMC1 I/O	PMC1IO [1 to 64]	PMC channel 1 I/O signals 1 through 64
EIDE (ATA-2), Secondary Channel, TTL levels	SDREQ-	Drive DMA request
	SDACK-	Drive DMA acknowledge
	SIOR-	Drive I/O read
	SIOW-	Drive I/O write
	SIORDY-	Indicates drive is ready for I/O cycle(s)
	SD[15:0]	Drive data lines, bits 15 -- 0
	SRSTDRV	Reset signal to drive
	SCS1	Chip select drive 0, also command register block select
	SCS3	Chip select drive 1, also command register block select
	SA[2:0]	Drive register and data port address lines
	SINTRQ	Drive interrupt request

PCI Mezzanine Card Connectors

The PCI Mezzanine Card (PMC) bus connects to the internal 32-bit wide, PCI bus (bus 0). Refer to the next two tables for PMC connector pinouts.

Table 5-9. PMC 1 and 2 Connectors (J11, J21)

J11 and J21			
Pin Number	**Signal**	**Signal**	**Pin Number**
1	TCK	-12V	2
3	Ground	INTA-	4
5	INTB-	INTC-	6
7	BUSMODE1-	+5V	8
9	INTD-	PCI-RSVD	10
11	Ground	PCI_RSVD	12
13	CLK	Ground	14
15	Ground	GNT-	16
17	REQ-	+5V	18
19	V (I/O)	AD{31}	20
21	AD[28}	AD[27]	22
23	AD[25]	Ground	24
25	Ground	C/BE[3]	26
27	AD[22]	AD[21]	28
29	AD[19]	+5V	30
31	V (I/O)	AD[17]	32
33	FRAME-	Ground	34
35	Ground	IRDY-	36
37	DEVSEL-	+5V	38
39	Ground	Lock-	40
41	SDONE-	SBO-	42
43	PAR	Ground	44
45	V (I/O)	AD[15]	46
47	AD[12]	AD[11]	48

Table 5-9. PMC 1 and 2 Connectors (J11, J21) (Continued)

J11 and J21			
Pin Number	**Signal**	**Signal**	**Pin Number**
49	AD[09]	+5V	50
51	Ground	C/BE[0}	52
53	AD[06]	AD[05]	54
55	AD[04]	Ground	56
57	V (I/O)	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5V	62
63	Ground	REQ64-	64

Table 5-10. PMC 1 and 2 Connectors (J12, J22)

J12 and J22			
Pin Number	**Signal**	**Signal**	**Pin Number**
1	+12V	TRST-	2
3	TMS	TDO	4
5	TDI	Ground	6
7	Ground	PCI-RSVD	8
9	PCI-RSVD	PCI-RSVD	10
11	BUSMODE2-	+3.3V	12
13	RST-	BUSMODE3-	14
15	+3.3V	BUSMODE4-	16
17	PCI-RSVD	Ground	18
19	AD[30]	AD[29]	20
21	Ground	AD[26]	22
23	AD[24]	+3.3V	24
25	IDSEL	AD[23]	26
27	+3.3V	AD[20]	28
29	AD[18]	Ground	30

Table 5-10. PMC 1 and 2 Connectors (J12, J22) (Continued)

J12 and J22			
Pin Number	**Signal**	**Signal**	**Pin Number**
31	AD[16]	C/BE[2]	32
33	Ground	PMC-RSVD	34
35	TRDY-	+3.3V	36
37	Ground	STOP-	38
39	PERR-	Ground	40
41	+3.3V	SERR-	42
43	C/BE[1]	Ground	44
45	AD[14]	AD[13]	46
47	Ground	AD[10]	48
49	AD[08]	+3.3V	50
51	AD[07]	PMC-RSVD	52
53	+3.3V	PMC-RSVD	54
55	PMC-RSVD	Ground	56
57	PMC-RSVD	PMC-RSVD	58
59	Ground	PMC-RSVD	60
61	ACK-64	+3.3V	62
63	Ground	PMC-RSVD	64

64 Bit Extension on the PMC Connectors

Table 5-11. PMC 1 and 2 Connectors (J13, J23)

J13 and J23			
Pin Number	**Signal**	**Signal**	**Pin Number**
1	-	GND	2
3	GND	C/BE7#	4
5	C/BE6#	C/BE5#	6
7	C/BE4#	GND	8
9	V(I/O)	PAR64	10
11	AD63	AD62	12
13	AD61	GND	14
15	GND	AD60	16
17	AD59	AD58	18
19	AD57	GND	20
21	V(I/O)	AD56	22
23	AD55	AD54	24
25	AD53	GND	26
27	GND	AD52	28
29	AD51	AD50	30
31	AD49	GND	32
33	GND	AD48	34
35	AD47	AD46	36
37	AD45	GND	38
39	V(I/O)	AD44	40
41	AD43	AD42	42
43	AD41	GND	44
45	GND	AD40	46
47	AD39	AD38	48
49	AD37	GND	50
51	GND	AD36	52

Table 5-11. PMC 1 and 2 Connectors (J13, J23) (Continued)

J13 and J23			
Pin Number	**Signal**	**Signal**	**Pin Number**
53	AD35	AD34	54
55	AD33	GND	56
57	V(I/O)	AD32	58
59	-	-	60
61	-	GND	62
63	GND	-	64

PCI Mezzanine Card 1 and 2 I/O

Table 5-12. PMC 1 and 2 I/O Connectors (J14, J24)

J14 and J24			
Pin Number	**Signal**	**Signal**	**Pin Number**
1	PMCxIO1	PMCxIO2	2
3	PMCxIO3	PMCxIO4	4
5	PMCxIO5	PMCxIO6	6
7	PMCxIO7	PMCxIO8	8
9	PMCxIO9	PMCxIO10	10
11	PMCxIO11	PMCxIO12	12
13	PMCxIO13	PMCxIO14	14
15	PMCxIO15	PMCxIO16	16
17	PMCxIO17	PMCxIO18	18
19	PMCxIO19	PMCxIO20	20
21	PMCxIO21	PMCxIO22	22
23	PMCxIO23	PMCxIO24	24
25	PMCxIO25	PMCxIO26	26
27	PMCxIO27	PMCxIO28	28
29	PMCxIO29	PMCxIO30	30
31	PMCxIO31	PMCxIO32	32

Table 5-12. PMC 1 and 2 I/O Connectors (J14, J24) (Continued)

J14 and J24			
Pin Number	**Signal**	**Signal**	**Pin Number**
33	PMCxIO33	PMCxIO34	34
35	PMCxIO35	PMCxIO36	36
37	PMCxIO37	PMCxIO38	38
39	PMCxIO39	PMCxIO40	40
41	PMCxIO	PMCxIO	42
43	PMCxIO	PMCxIO	44
45	PMCxIO	PMCxIO	46
47	PMCxIO	PMCxIO	48
49	PMCxIO	PMCxIO	50
51	PMCxIO	PMCxIO	52
53	PMCxIO	PMCxIO	54
55	PMCxIO	PMCxIO	56
57	PMCxIO	PMCxIO	58
59	PMCxIO	PMCxIO	60
61	PMCxIO	PMCxIO	62
63	PMCxIO	PMCxIO	64

Memory Mezzanine Connector (J16)

Table 5-13. Memory Mezzanine Connector (J16)

J16			
Pin Number	**Signal**	**Signal**	**Pin Number**
1	GND	GND	2
3	DQ00	DQ01	4
5	DQ02	DQ03	6
7	DQ04	DQ05	8
9	DQ06	DQ07	10
11	+3.3V	+3.3V	12
13	DQ08	DQ09	14
15	DQ10	DQ11	16
17	DQ12	DQ13	18
19	DQ14	DQ15	20
21	GND	GND	22
23	DQ16	DQ17	24
25	DQ18	DQ19	26
27	DQ20	DQ21	28
29	DQ22	DQ23	30
31	+3.3V	+3.3V	32
33	DQ24	DQ25	34
35	DQ26	DQ27	36
37	DQ28	DQ29	38
39	DQ30	DQ31	40
41	GND	GND	42
43	DQ32	DQ33	44
45	DQ34	DQ35	46
47	DQ36	DQ37	48
49	DQ38	DQ39	50
51	+3.3V	+3.3V	52

Table 5-13. Memory Mezzanine Connector (J16) (Continued)

J16			
Pin Number	**Signal**	**Signal**	**Pin Number**
53	DQ40	DQ41	54
55	DQ42	DQ43	56
57	DQ44	DQ45	58
59	DQ46	DQ47	60
61	GND	GND	62
63	DQ48	DQ49	64
65	DQ50	DQ51	66
67	DQ52	DQ53	68
69	+3.3V	+3.3V	70
71	DQ54	DQ55	72
73	DQ56	DQ57	74
75	DQ58	DQ59	76
77	DQ60	DQ61	78
79	GND	GND	80
81	DQ62	DQ63	82
83	CKD00	CKD01	84
85	CKD02	CKD03	86
87	CKD04	CKD05	88
89	+3.3V	+3.3V	90
91	CKD06	CKD07	92
93	BA1	BA0	94
95	A12	A11	96
97	A10	A09	98
99	GND	GND	100
101	A08	A07	102
103	A06	A05	104
105	A04	A03	106
107	A02	A01	108

Table 5-13. Memory Mezzanine Connector (J16) (Continued)

J16			
Pin Number	**Signal**	**Signal**	**Pin Number**
109	+3.3V	+3.3V	110
111	A00	CS_C0_L	112
113	CS_E0_L	GND	114
115	CS_C1_L	CS_E1_L	116
117	WE_L	RAS_L	118
119	GND	GND	120
121	CAS_L	+3.3V/DQMA2	122
123	+3.3V/DQMA3	DQMB0	124
125	DQMB1	SCL	126
127	SDA	A1_SPD/DQMA4	128
129	A0_SPD/DQMB5	ME1_L/DQMA6	130
131	ME2_L/DQMA7	GND	132
133	GND	SDCLK1	134
135	SDCLK3	+3.3V	136
137	SDCLK4	SDCLK2	138
139	GND	GND	140

Ethernet Connectors

Refer to the following table for Ethernet connector pin assignments for the CPN5365 baseboard Ethernet (J9) connector.)

Table 5-14. Ethernet Connector Pin Assignments for CPN5365 (J9)

Pin Number	Signal Mnemonic	Signal Description
1	TX+	Differential transmit lines
2	TX-	Differential transmit lines
3	RX+	Differential receive lines
4	-	-
5	-	-
6	RX-	Differential receive lines
7	-	-
8	-	-

Serial Port Connectors

Refer to the following table for pin assignments COM 1 Serial Port 1 for the CPN5365 (J8).

Table 5-15. CPN5365 Serial Port Connector Pin Assignments RJ45 (J8)

Pin	Single Mnemonic	Signal Description
1	DCD-	Data set has detected the data carrier
2	RTS-	Indicates to data set that UART is ready to exchange data
3	GND	Ground
4	TXD	Sends serial output to communications link
5	RXD	Receives serial data input from communications link
6	GND	Ground
7	CTS-	Indicates that data set is ready to exchange data
8	DTR-	Indicates that a data set is ready to establish a communications like

On-board Video Connector (J7)

Table 5-16. On-board Video Connector (J7)

Pin	Signal Mnemonic	Signal Description
1	RED	Red signal
2	GREEN	Green signal
3	BLUE	Blue signal
4	DACVSS	Video return (analog)
5	DACVSS	Video return (digital)
6	HSYNC	Horizontal synchronization
7	VSYNC	Vertical synchronization
8	DDCDAT	Display Data Channel data signal for DDC2 support
9	DDCCLK	Display Data Channel clock signal for DDC2 support

Debug Connector (J10)

Table 5-17. Debug Connector (J10)

J10			
Pin Number	**Signal**	**Signal**	**Pin Number**
1	RESET-	GND	2
3	PB_RESET-	GND	4
5	TCLK	GND	6
7	TMS	TDI	8
9	VTT	TDO	10
11	N/C	TRST-	12
13	GND	CPU_IOV	14
15	GND	PREQ-	16
17	GND	PRDY-	18
19	GND	N/C	20
21	GND	N/C	22

Table 5-17. Debug Connector (J10) (Continued)

J10			
Pin Number	**Signal**	**Signal**	**Pin Number**
23	GND	N/C	24
25	GND	N/C	26
27	GND	N/C	28
29	HOST CLK	N/C	30

Specifications A

This appendix provides the specifications for the physical, electrical, and power requirements for the CPN5365. Information pertaining tot he lithium battery is included.

Table A-1. Physical Characteristics of the CPN5365 Single Board Computer

Parameter	Description
Form Factor	CompactPCI Standard 6U (233mm x 160mm x 20mm) Conforms to PICMG 2.0, CompactPCI (rev. 2.1) and PCI SIG 2.1 specifications
Dimensions	4 HP (.8 inches) wide

Refer to the next table for environmental specifications for the CPN5365 Single Board Computer in a Motorola supplied enclosure.

Table A-2. Environmental Specifications [1]

Parameter	Condition	Specification
Temperature	Operating	0°C to 55°C (32°F to 130°F) [2]
	Nonoperating	-40°C to 65°C (°-40F to 150°F)
Humidity	Operating	5% to 90% @ 40°C, (104°F) noncondensing
	Nonoperating	5% to 95% @40°C, (104°F) noncondensing
Cooling	Operating	35 CFM over the Single Board Computer
MTBF (MIL-HDBK-217F)	Operating	300,000 hours at 30°C (86°F) 100,000 hours at 50°C (122°F)

[1] Environmental Specifications do not include the on-board hard drive option.

[2] Derate the maximum operating temperature by 1° F (1.8° C) per 3280 feet (1000m) above sea level.

Table A-3. Power Input Requirements for the CPN5365 and CPTM-01

Input power [1]	Clock speed
+5V @ 3.0A (15W)	500 MHz with 512 or 1024MB SDRAM
+3.3V @ 2.5A (8.25W)	
+12V @ 100mA (1.2W)	
-12V @ 0A (0W)	
Total power = 24.5W	
+5V @ 3.0A (17.5W)	700 MHz with 512 or 1024MB SDRAM
+3.3V @ 2.5A (8.25W)	
+12V @ 100mA (1.2W)	
-12V @ 0A (0W)	
Total power = 27W	

[1] These values include the CPN5365 SBC with a 500 or 700 MHz EMC2 processor and no PMC devices installed.

Table A-4. Lithium Battery Specifications

Rating	Shelf Life
180mA/hour	2 years

Thermal Analysis B

Ambient temperature, air flow, board electrical operation, and software operation affect board component temperatures. To evaluate the thermal performance of a circuit board assembly, you should test the board under actual operating conditions. These operating conditions vary depending on system design.

Motorola Computer Group performs thermal analysis in a representative system to verify operation within specified ranges. Refer to Specifications, Table A-2. You should evaluate the thermal performance of the board in your application.

This appendix gives systems integrators the information necessary to conduct thermal evaluations of the board in their specific system configuration. It identifies thermally significant components and lists the corresponding maximum allowable component operating temperatures. It also provides example procedures for component-level temperature measurements.

Thermally Significant Components

Table B-1 summarizes components that show significant temperature rises. You should monitor these components to assess thermal performance. Table B-1 also supplies the component reference designator and the maximum allowable operating temperature.

You can find components on the board by their reference designators. Refer to Figure B-1 and Figure B-2.

The preferred temperature measurement location for a component may be:

- Junction - refers to the temperature measured by an on-chip thermal device
- Case - refers to the temperature at the top, center surface of the component
- Air - refers to the ambient temperature near the component

Table B-1. Thermally Significant Components

Reference Designator	Generic Description	Maximum Allowable Component Temperature (degrees C) [1]	Measurement Location
U1	Pentium III CPU	100	Junction
U15	440GX North Bridge	105	Case
U23	21554 PCI Bridge	70	Air
U32	69030 VGA	70	Air
U35, U36	82559 Ethernet	85	Case

[1] maximum temperature for reliable operation specified by the component manufacturer.

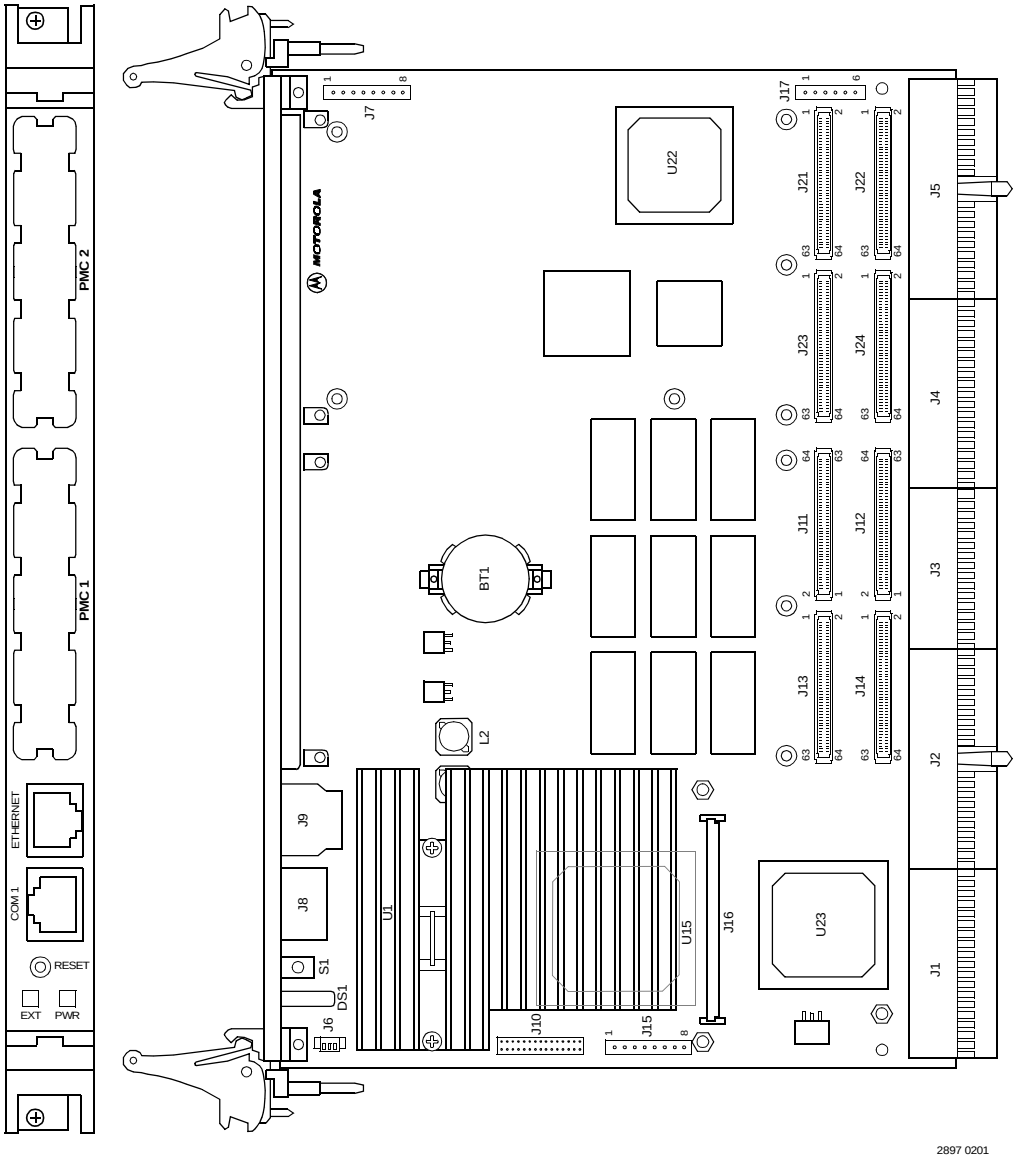


Figure B-1. Location of Thermally Significant Components on the Primary Side

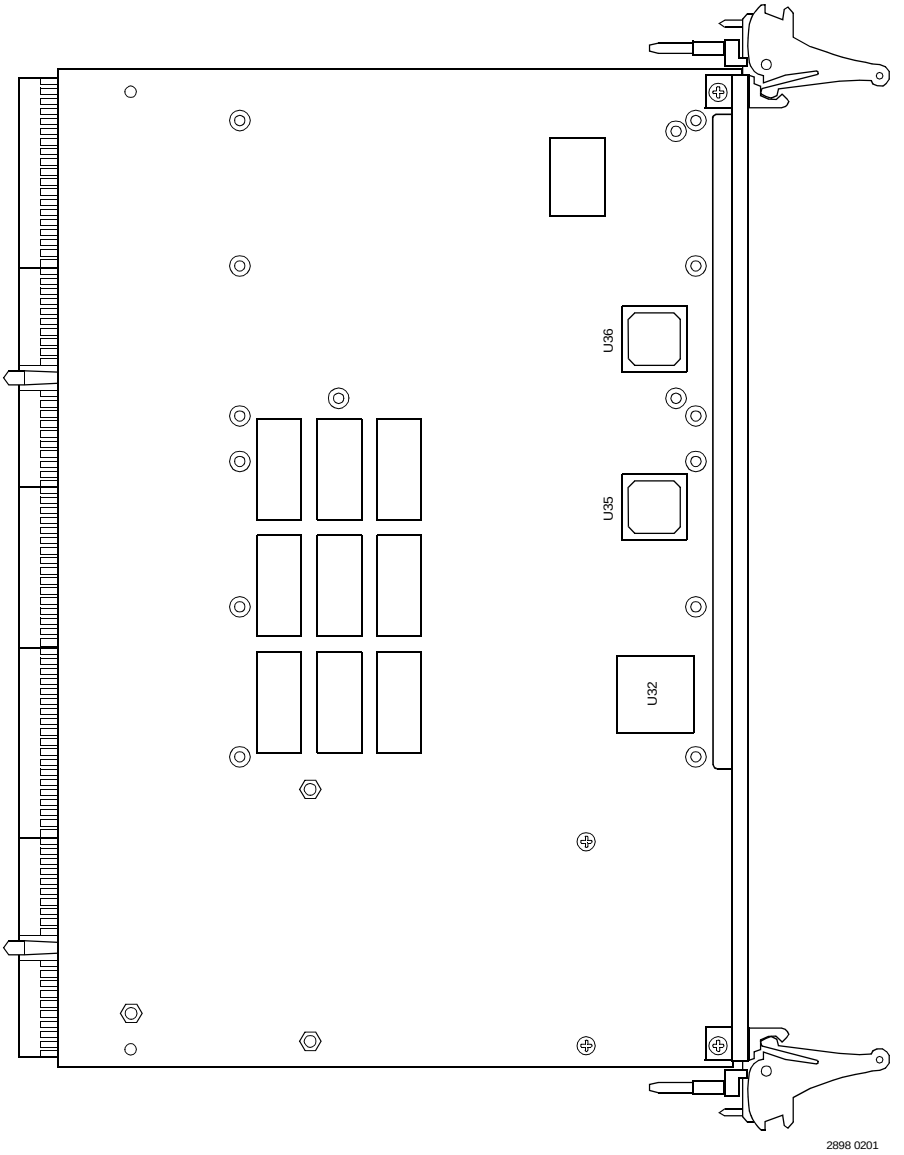


Figure B-2. Location of Thermally Significant Components on the Secondary Side

Component Temperature Measurement

This section outlines general temperature measurement methods. For the specific types of measurements required for thermal evaluation of this board, see Table B-1.

Preparation

We recommend 40-gage thermocouples for all thermal measurements. Larger gage thermocouples can wick heat away from the components and disturb air flowing past the board.

Allow the board to reach thermal equilibrium before taking measurements. Most circuit boards reach thermal equilibrium within 30 minutes. After the warm up period, monitor a small number of components over time to assure that equilibrium is reached.

Measuring Junction Temperature

Some components have an on-chip thermal measuring device such as a thermal diode. For instructions on measuring temperatures using the on-board device, refer to the CompactPCI CPN5365 component manufacturer's documentation listed in Appendix C, Related Documentation.

Measuring Case Temperature

Measure the case temperature at the center of the top of the component. Make sure there is good thermal contact between the thermocouple junction and the component. We recommend you use a thermally conductive adhesive such as Loctite 384.

If components are covered by mechanical parts such as heatsinks, you need to machine these parts to route the thermocouple wire. Make sure that the thermocouple junction contacts *only* the electrical component. Also make sure that heatsinks lay flat on electrical components. Figure B-3 shows one method of machining a heatsink base to provide a thermocouple routing path.

Note Machining a heatsink base reduces the contact area between the heatsink and the electrical component. You can partially compensate for this effect by filling the machined areas with thermal grease. The grease should not contact the thermocouple junction.

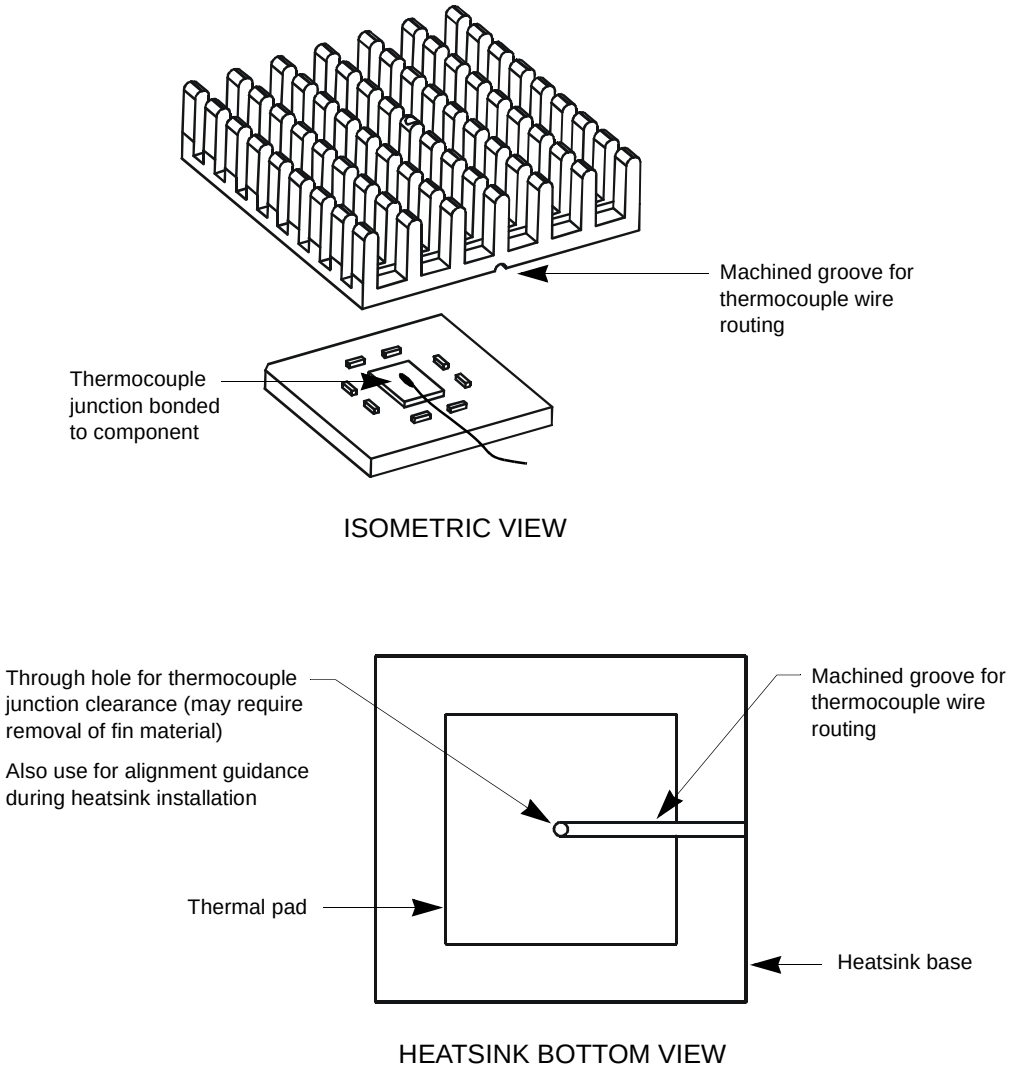


Figure B-3. Mounting a Thermocouple Under a Heatsink

B

Measuring Local Air Temperature

Measure local component ambient temperature by placing the thermocouple downstream of the component. This method is conservative since it includes heating of the air by the component. Figure B-4 shows one method of mounting the thermocouple.

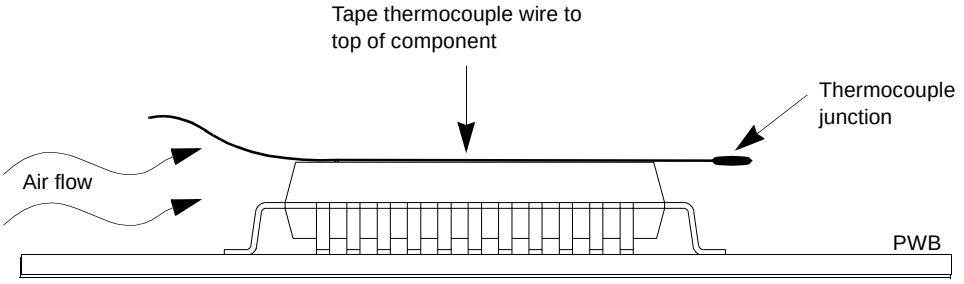


Figure B-4. Measuring Local Air Temperature

Related Documentation C

Motorola Computer Group Documents

The Motorola publications listed below are referenced in this manual, or apply to systems that use this product. You can obtain electronic copies of Embedded Communications Computing Group publications by:

- Contacting your local Motorola sales office, or
- Visiting the Embedded Communications Computing Groups's World Wide Web literature site, http://www.motorola.com/computer/literature

Table C-1. Motorola Computer Group Documents

Document Title	Motorola Publication Number
CPN5365 Single Board Computer Programmer's Reference Guide	CPN5365A/PG

To get the most up-to-date product information in PDF or HTML format, visit http://www.motorola.com/computer/literature.

Manufacturers' Documents

For additional information, refer to the following table for manufacturers' data sheets and user's manuals. For your convenience, a source for the listed document is also provided.

It is important to note that in many cases, the information shown is preliminary and the revision levels of the documents are subject to change without notice.

Table C-2. Manufacturers' Documents

Document Title and Source	Publication Number
Distributed Management Task Force, Inc. Go to **DMTF** to search for documentation	
System Management BIOS Reference Specification, v2.3.1	dsp0119.pdf
Intel Corporation Go to Literature Center for Search Engine	
Mobile Pentium III Processor in BGA2 and Micro-PGA2 Packages—Data Sheet; Intel Corporation	245302.pdf
Intel 82554GC 10/100Base-T Ethernet PCI Bus Controller Intel 82559EI Gigabit Ethernet PCI Bus Controller with Integrated PHY — External Design Specification; Intel Corporation Intel CompactPCI Non-Transparent Bridge - 21555 Using a Serial ROM with the 21555 Non-Transparent PCI-to-PCI Bridge	82544.pdf 82559.pdf 21555.pdf 82559.pdf
Intel PIIX4E South Bridge 82371	290562.pdf
Intel 440GX AGPset: 82443BX Host Bridge/Controller — Data Sheet	290638.pdf
Intel StrataFlash Memory 28F320J5	290606.pdf
Intel 82559ER Fast Ethernet PCI Bus Controller with Integrated PHY — External Design Specification; Intel Corporation	73825902.pdf
Intel AGP Video 69030	69030.pdf
Maxim Corp.	

Table C-2. Manufacturers' Documents (Continued)

Document Title and Source	Publication Number
MAX1617 Remote/Local Temperature Sensor with SMBus Serial Interface; Maxim Corporation; http://pdfserv.maxim-ic.com/arpdf/1855.pdf	1855.pdf
National Semiconductor	
LM81 Microprocessor System Hardware Monitor National Semiconductor Corporation; http://www.national.com/	LM81.html
PC97307VUL (Super I/OTM Enhanced Sidewinder Lite) Floppy Disk Controller, Keyboard Controller, Real-Time Clock, Dual UARTs, IEEE 1284 Parallel Port, and IDE Interface http://www.national.com/pf/PC/PC97307.html	PC97307.html
Phoenix Technologies	
PhoenixBIOS 4.0 Release 6 User's Manual Phoenix Technologies http://www.phoenix.com/pcuser	userman.pdf
Standard Microsystems Corporation (SMSC) Search for documentation at http://www.smsc.com/	
Enhanced Super I/O controller Data Sheet	fdc37c67x.html
SMC Ultra I/O 37C672	fdc37c672.pdf

Related Specifications

For additional information, refer to the following table for related specifications. For your convenience, a source for the listed document is also provided. It is important to note that in many cases, the information is preliminary and the revision levels of the documents are subject to change without notice

Table C-3. Related Specifications

Document Title and Source	Publication Number
IEEE http://standards.ieee.org/catalog/	
IEEE Standard for Compact Embedded PC Modules	IEEE P996.1
IEEE - Common Mezzanine Card Specification (CMC) Institute of Electrical and Electronics Engineers, Inc.	P1386 Draft 2.0
IEEE - PCI Mezzanine Card Specification (PMC) Institute of Electrical and Electronics Engineers, Inc.	P1386.1 Draft 2.0
Bidirectional Parallel Port Interface Specification Institute of Electrical and Electronics Engineers, Inc.	IEEE Standard 1284
Intel Corp.	
Accelerated Graphics Port Interface Specification, Revision 1.0 Intel Corporation http://www.intel.com/technology/agp/agp_index.htm	agp10.pdf
Universal Host Controller Interface (UHCI) Design Guide Intel Corporation; http://www.intel.com/design/litcentr/	297650-002
Universal Serial Bus (USB) Intel Corporation; http://www.intel.com/design/litcentr/	297773-001
Wired for Management, PXE (Preboot Execution Environment) http://www.intel.com/design/litcentr/	
PCI Industrial Manufacturers Group (PICMG) http://www.picmg.com/	

Table C-3. Related Specifications (Continued)

Document Title and Source	Publication Number
Compact PCI Specification	PICMG 2.0 Rev. 2.1 Dated 9/2/97
PCI-PCI Bridge Specification for Single Board Computers	PICMG 1.1 Rev. 1.02
CompactPCI Hot Swap Specification PCI Industrial Computers Manufacturers Group (PICMG)	PIMCG 2.1 R1.0
PCI Special Interest Group (PCI SIG) http://www.pcisig.com/	
Peripheral Component Interconnect (PCI) Local Bus Specification, Revision 2.0, 2.1, 2.2 PCI Special Interest Group;	PCI Local Bus Specification
Miscellaneous	
Open HCI; Open Host Controller Interface Spec for USB Compaq Corporation, Microsoft Corporation, National Semiconductor http://www3.compaq.com/support http://www.national.com/ http://www.microsoft.com/	Open HCI Release 1.0 12/15/95
IrDA SIR Data Specification Infrared Data Association http:/www.irda.org/standards/specifications.asp	IrDA SIR data Specification
“El Torito” Bootable CD-ROM Specification, Version 1.0 Phoenix Technologies, Inc. http://www.phoenix.com/	specs-cdrom.pdf

Index

T

U

W