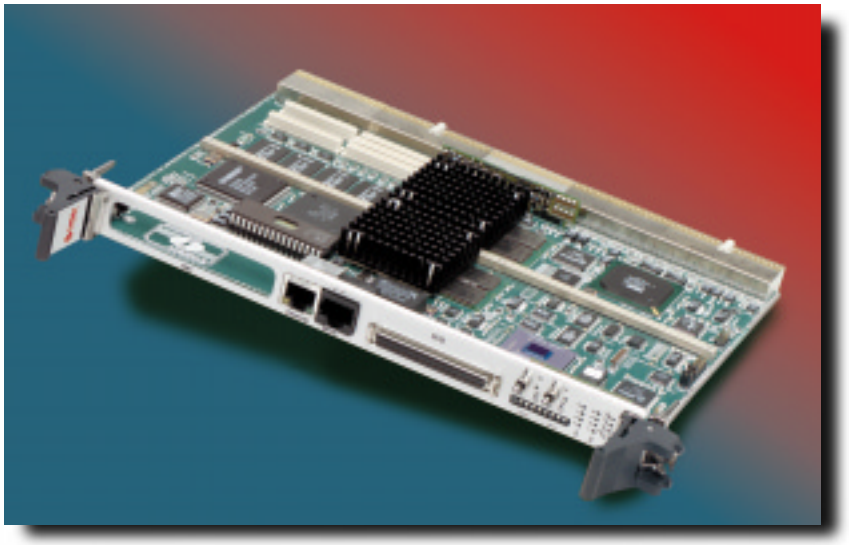
KGM5

Dual PowerPC 750 CompactPCI SBC

Dual PowerPC 750 CPUs and fast L2 cache give you extremely high performance in a CompactPCI SBC!



- *300-466+ MHz 750 CPUs*
- *Dual or single CPUs*
- *One megabyte of backside L2 cache per CPU*
- *Up to 512 MB of high-speed SDRAM*
- *Up to 17 MB on-board Flash*
- *Two serial ports*
- *One 8/16-bit Ultra Wide SCSI port*
- *One Ethernet connection (10Base-T, 100Base-TX)*
- *64-bit PCI bus*
- *Supports two USB ports, up to 12 Mb/sec*
- *VxWorks, Lynx, pSOS, Linux*

Dual PowerPC 750 CPUs

With dual processors, the KGM5 allows you to achieve performance approaching that of two single CPU boards. Yet it costs much less than two boards and takes up just one slot. As the pioneer in dual processor technology, Synergy has optimized the KGM5 to allow the most efficient sharing of resources between two processors. Processor speeds range from 300 MHz to 466 MHz. Synergy will offer higher speeds as processor technology advances.

High-speed L2 cache

The 750 processor features the latest L2 cache technology: backside cache. Backside cache connects directly to the processor over its own private high-speed bus rather than the PowerPC memory bus. While the PowerPC memory bus runs at 425 MB/s maximum, the backside cache bus can run anywhere from 853 MB/s to 1920 MB/s (with even faster speeds available soon). Cache speeds depend on the CPU-to-cache speed ratio and the speed of the CPU.

The KGM5 provides you with one full megabyte of L2 cache for each processor. The cache's capacity and speed of access allow a substantial reduction in the number of accesses to main memory over the slower PowerPC memory bus, boosting overall performance significantly.

Functions in both system and peripheral slots

The KGM5 comes ready to function in either a system or peripheral slot automatically. Simply plug the KGM5 into the desired slot and it will assume the proper functions.

High speed SDRAM

The KGM5's state-of-the-art SDRAM outperforms traditional EDO DRAM by up to 55%. SDRAM is synchronized with the PowerPC clock, eliminating wait states. The KGM5's circuitry optimizes access to the SDRAM for peak performance.

SYNERGY microsystems

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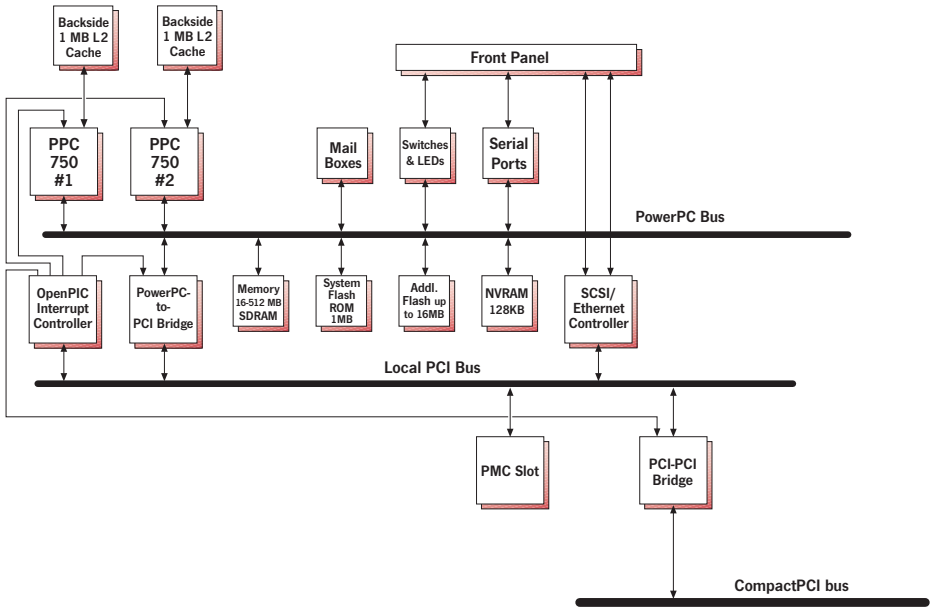
Block Diagram, KGM5 SBC



Specifications: KGM5

Processor:

Dual or single PowerPC 750, 300-466+ MHz

Memory:

Main memory: 16, 32, 64, 128, 256 or 512 MB SDRAM supporting parity

L2 Cache: 1 MB backside L2 cache per CPU @ 2:1 CPU-to-cache speed ratio, optional 1.5:1 or 1:1 ratio (ask for current availability)

Boot Flash: 1 MB loadable via a 32-pin JEDEC socket

Optional user Flash: 2, 4, 8 or 16 MB of 8-bit Flash

NVRAM (& clock calendar): 128 KB

PCI interface:

CompactPCI: 64-bit 33 MHz, up to 264 MB/s, 3 V or 5 V signalling

PCI bus: 64-bit 33 MHz, up to 264 MB/s

PMC interface: 64-bit 33 MHz, up to 264 MB/s

On-board I/O:

Ethernet: autosensing 10Base-T/100Base-TX

Serial: Two RS-232 serial ports, up to 115.2 KB/sec

SCSI: optional Ultra Wide, 8/16-bit, up to 40 MB/s

USB: Host controller (Open HCI 1.0 compliant), two ports routed to J5, up to 12 Mb/sec

Physical dimensions

6U: 6.4" x 9.19" x 0.8" (minus front panel)

Weight:

15.1 oz (428 g)

Power requirement (approx.):

+5 V at 2.2–3.7 A (depends on configuration)

+3.3 V at 1.2 A

Environmental & reliability:

0^{o} to 55^{o} C, 0 to 85% humidity (non-condensing), 200 LFM minimum air flow (other temperature ranges also available)

Storage temperature: -40° to 85° C

Humidity: 0–85% RH non-condensing

Altitude (est.): 10,000 ft./msl

MTBF: 136,243 hours (15.55 years)

Other Features:

- Functions in the system or peripheral slot, switching functions automatically
- Ten status LEDs, eight user-programmable LEDs, an 8-bit readable switch, and two CPU reset/interrupt switches
- OpenPIC™ compliant — any interrupt source can be routed to either CPU at any priority, with priorities set in software
- SMP (symmetric multiprocessing) support
- Four 32-bit counters can be read at any time as well as generate interrupts
- Two 8-bit CPU mailboxes
- Real time clock/calendar, four-digit year (Y2K compliant)
- Two JTAG connectors support the HP JTAG Development System
- Bellcore/Nynex compliance
- Requires only one slot for dual or single CPU

Options:

- VxWorks, LynxOS, pSOS or Linux BSP
- Dual CPUs
- Ultra Wide SCSI interface
- Conformal coating
- Other options include CPU speed, main memory size, Flash size, and L2 cache speed ratio

Your local sales representative:

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