SBS GreenSpring Modular I/O

# IP-Octal Opto

## Eight Channel Optically Isolated Universal Interface Serial Communications IndustryPack®

## User's Manual

Preliminary Revision iii
Corresponding Hardware: Revision C

**IP-Octal Opto**

**Eight Channel Optically Isolated Universal Interface Serial Communications IndustryPack®**

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Manual Revision iii.

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# Product Description

IP-Octal Opto is part of the IndustryPack™ family of modular I/O components. It is a double wide IndustryPack built around the Signetics CMOS SCC2698B Octal Universal Asynchronous Receiver/Transmitter. This component provides eight channels of full-duplex asynchronous serial communications, baud rate generators, state change detection logic, and four 16-bit counter/timers. IP-Octal Opto provides a versatile way of implementing optically isolated serial communication lines to any of five communication standards: RS-232, RS-422, RS-423, 20 mA current loop, or full isolation. In addition, non-standard communication levels can frequently be accommodated. Data rates to 48.4 Kbaud asynchronous are supported.

A block diagram of the IP-Octal Opto is shown below in Figure 1. The IP-Octal Opto provides eight channels of transmit and receive data without modem control signals. Each channel has it own UART and optical buffer. All the optical buffers on the board share a common external ground reference and must be configured to operate at the same voltage levels. All eight receive lines and all eight transmit lines are optically buffered. In addition, all lines have conventional RS-232 connections that are not optically buffered. These connections are provided as a convenience for setup and testing. They may also be used on a permanent basis in place of the optically buffered lines on a per line basis. This permits the mixing of optically isolated and non-isolated channels.

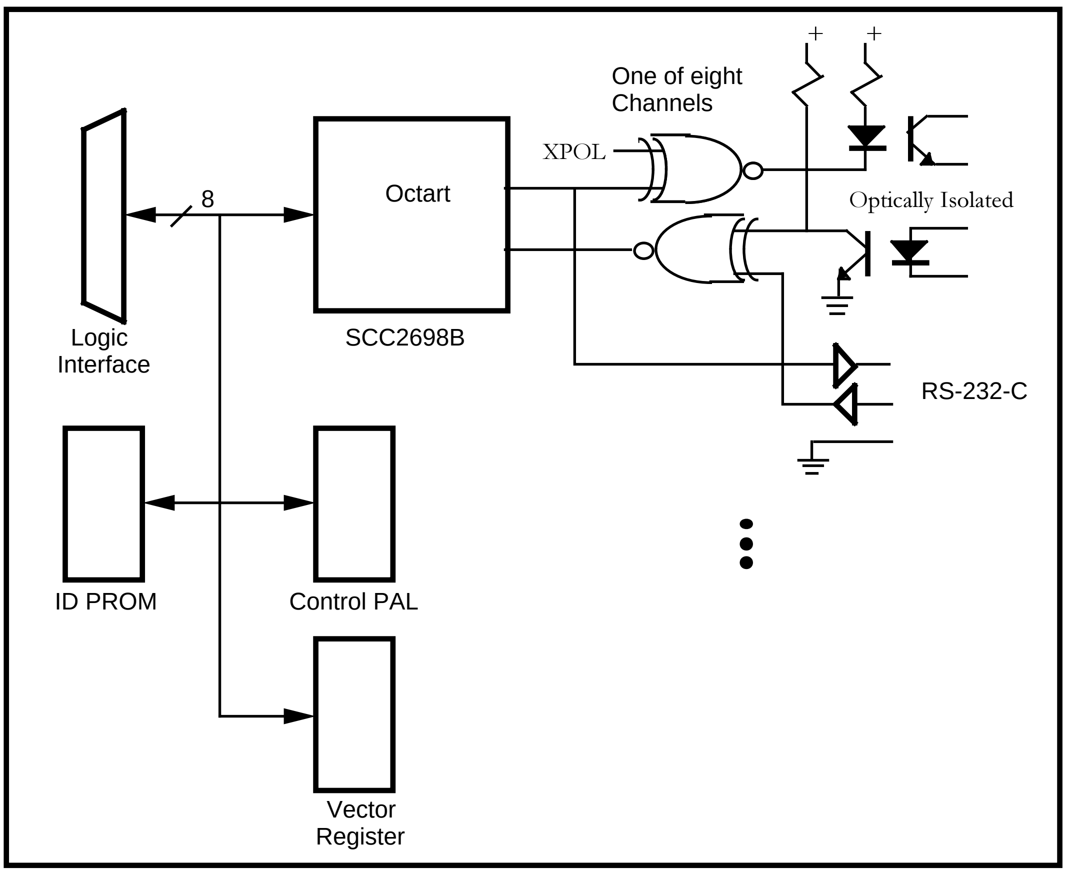


**Figure 1 Block Diagram of IP-Octal Opto Serial**

The maximum recommended voltage differential between any two external lines or between any external line and the host system ground is 60 volts. This recommended voltage limitation is due to the close component spacing and the limits of factory testing as well as operator safety. Typical breakdown voltage is much higher.

An external power supply must be used to achieve full isolation of the host electronics from the external lines. Most conventional power supplies are transformer isolated from the power line and are suitable for this purpose. The user may also provide jumper wires on the appropriate IP-Octal Opto I/O pins to connect the host supply as the necessary external supply. This may be done on a temporary basis for setup and testing or a permanent basis. Even if the host power supplies are used permanently, the optical isolation provides a significant noise and over-voltage improvement over conventional single-ended serial communication implementations.

Different interface levels require different external voltage supplies. Figure 2 below shows which power supplies are required by each interface. External ±12 volt supplies are standard, and support RS-232, RS-423, fully isolated, and current loop interfaces. A +5 supply is also needed for RS-422 interfacing. Only a single +12 volt supply is needed for the fully isolated option.

Full isolation is not a standard communication option. This mode is supported by the IP-Octal Opto. Full isolation has two advantages over standard communication levels: (i) only a single external power supply is needed, (ii) the communication lines are fully optically isolated from the electronics at *both* ends of the line. Taking advantage of this option requires an IP-Octal Opto or similar circuitry at each end of the communication line. This option is recommended for maximum isolation against induced or connected noise, or when the user has no control over the security of the communication line.

| **Comm Standard** | **Power Supplies** | **Nominal Swing** | **Nominal Load** |
|---|---|---|---|
| RS-232 | ±12 V | ±5 to ±12 V single-ended | 3 KΩ typical |
| RS-423 | ±12 V | ±6 V single-ended | 450 Ω to 3 KΩ |
| RS-422 | +5 V | +1 to +3 differential | 100 to 150 Ω typical |
| 20 mA | ±12 V | 20 mA ON or OFF | varies |
| Full isolation* | +12 V | 0 to 12 volts single-ended | 1 KΩ typical |

* Full isolation is not an industry standard, but is an option supported by IP-Octal Opto. See text for details.

**Figure 2 Summary of Communication Standards**

The optical transmit and receive line buffers on the IP-Octal Opto use Siemens ILQ2 quad optocoupler components. Like all optocouplers these are basically current-mode devices. An optocoupler consists of one LED and one photo-transistor in a single package. When current flows through the LED its light causes the photo-transistor to also conduct current. The circuitry on the IP-Octal Opto is designed so that the nominal ON current is 10 mA and the nominal OFF current is zero or negative. Since most standard communication lines are voltage based, resistor values for resistor packs on the IndustryPack are chosen to convert the nominal voltage swing to a 10 mA current.

The 20 mA current loop is an old standard originally used for Teletypes. It is different from the other standards in that the idle state ("Mark") has the current ON, and the signaling state ("Space") has the current OFF. This is the reverse ON/OFF polarity of other common communication protocols. The IP-Octal Opto has exclusive NOR gates on the input and output line that may be used to implement this logic state reversal in support of 20 mA current loop interfaces. Also, resistor values are chosen to increase the nominal currents through the optocouplers from 10 mA to 20 mA.

Vectored interrupts are fully supported. A common 8-bit vector register is provided. Channels a, b, c, and d interrupt on IRQ0. Channels e, f, g, and h interrupt on IRQ1. The IP-Octal Opto has no support for DMA transfers.

All connections to the IP-Octal Opto are made through a standard 50-conductor ribbon cable. A six foot 50-conductor ribbon cable and a 50 screw terminal block are included in the IP-Octal Opto Engineering Kit. Reprints of the Data Sheets for the SCC2698B, Schematic and PAL equations are also part of the IP-Octal Opto Engineering Kit. This Kit is recommended for first time users of the IP-Octal Opto.

# VMEbus Addressing

IP-Octal Opto is accessed using 8-bit bytes at odd locations only. It is usually accessed in the I/O space. Shown below in Figures 3 and 4 are the register maps of the IP-Octal Opto. All addresses are offsets from the I/O base address of the IP as set on the IP carrier board.

The SCC2698B Octal UART has four major internal sections, called functional blocks A through D. Each functional block has two serial channels, one timer, and one I/O port.

| Hex | Dec | Binary | Read | Write |
|---|---|---|---|---|
| | | **Functional Block A** | | |
| 1 | 1 | 0000001 | MR1a, MR2a | MR1a, MR2a |
| 3 | 3 | 0000011 | SRa | CSRa |
| 5 | 5 | 0000101 | RESERVED | CRa |
| 7 | 7 | 0000111 | RHRa | THRa |
| 9 | 9 | 0001001 | IPCRA | ACRA |
| B | 11 | 0001011 | ISRA | IMRA |
| D | 13 | 0001101 | CTUA | CTURA |
| F | 15 | 0001111 | CRLB | CTLRB |
| 11 | 17 | 0010001 | MR1b, MR2b | MR1b, MR2b |
| 13 | 19 | 0010011 | SRb | CSRb |
| 15 | 21 | 0010101 | RESERVED | CRb |
| 17 | 23 | 0010111 | RHRb | RHRb |
| 19 | 25 | 0011001 | RESERVED | RESERVED |
| 1B | 27 | 0011011 | INPUT PORT A | OPCRA |
| 1D | 29 | 0011101 | START C/T A | RESERVED |
| 1F | 31 | 0011111 | STOP C/T A | RESERVED |
| | | **Functional Block B** | | |
| 21 | 33 | 0100001 | MR1c, MR2c | MR1c, MR2c |
| 23 | 35 | 0100011 | SRc | CSRc |
| 25 | 37 | 0100101 | RESERVED | CRc |
| 27 | 39 | 0100111 | RHRc | THRc |
| 29 | 41 | 0101001 | IPCRB | ACRB |
| 2B | 43 | 0101011 | ISRB | IMRB |
| 2D | 45 | 0101101 | CTUB | CTURB |
| 2F | 47 | 0101111 | CRLB | CTLRB |
| 31 | 49 | 0110001 | MR1d, MR2d | MR1d, MR2d |
| 33 | 51 | 0110011 | SRd | CSRd |
| 35 | 53 | 0110101 | RESERVED | CRd |
| 37 | 55 | 0110111 | RHRd | THRd |
| 39 | 57 | 0111001 | RESERVED | RESERVED |
| 3B | 59 | 0111011 | INPUT PORT B | OPCRB |
| 3D | 61 | 0111101 | START C/T B | RESERVED |
| 3F | 63 | 0111111 | STOP C/T B | RESERVED |

**Figure 3 Register Map of SCC2698, Blocks A and B**

| Hex | Dec | Binary | Read | Write |
|---|---|---|---|---|
| | | **Functional Block C** | | |
| 41 | 65 | 1000001 | MR1e, MR2e | MR1e, MR2e |
| 43 | 67 | 1000011 | SRe | CSRe |
| 45 | 69 | 1000101 | RESERVED | CRe |
| 47 | 71 | 1000111 | RHRe | THRe |
| 49 | 73 | 1001001 | IPCRC | ACRC |
| 4B | 75 | 1001011 | ISRC | IMRC |
| 4D | 77 | 1001101 | CTUC | CTURC |
| 4F | 79 | 1001111 | CRLC | CTLRC |
| 51 | 81 | 1010001 | MR1f, MR2f | MR1f, MR2f |
| 53 | 83 | 1010011 | SRf | CSRf |
| 55 | 85 | 1010101 | RESERVED | CRf |
| 57 | 87 | 1010111 | RHRf | THRf |
| 59 | 89 | 1011001 | RESERVED | RESERVED |
| 5B | 91 | 1011011 | INPUT PORT C | OPCRC |
| 5D | 93 | 1011101 | START C/T C | RESERVED |
| 5F | 95 | 1011111 | STOP C/T C | RESERVED |
| | | **Functional Block D** | | |
| 61 | 97 | 1100001 | MR1g, MR2g | MR1g, MR2g |
| 63 | 99 | 1100011 | SRg | CSRg |
| 65 | 101 | 1100101 | RESERVED | CRg |
| 67 | 103 | 1100111 | RHRg | THRg |
| 69 | 105 | 1101001 | IPCRD | ACRD |
| 6B | 107 | 1101011 | ISRD | IMRD |
| 6D | 109 | 1101101 | CTUD | CTURD |
| 6F | 111 | 1101111 | CRLD | CTLRD |
| 71 | 113 | 1110001 | MR1h, MR2h | MR1h, MR2h |
| 73 | 115 | 1110011 | SRh | CSRh |
| 75 | 117 | 1110101 | RESERVED | CRh |
| 77 | 119 | 1110111 | RHRh | RHRh |
| 79 | 121 | 1111001 | RESERVED | RESERVED |
| 7B | 123 | 1111011 | INPUT PORT D | OPCRD |
| 7D | 125 | 1111101 | START C/T D | RESERVED |
| 7F | 127 | 1111111 | STOP C/T D | RESERVED |

**Figure 4 Register Map of SCC2698, Blocks C and D**

Interrupt mapping is a function of the carrier board. Refer to your IP carrier board User Manual for more information.

For NuBus and ISA bus applications refer to the following sections: NuBus Addressing and ISA Bus Addressing.

# NuBus Addressing

Since the Nubus uses only 32-bit wide accesses, 8-bit wide peripherals such as the IP-Octal Opto appear in the host address space every fourth byte.

To calculate the RM1260 Springboard register addresses from the VMEbus address (given in the previous section in Figures 3 and 4), multiply by two and subtract one. To convert VME addresses to RM1270 SupportBoard addresses multiply by two and add one.

Interrupt mapping is a function of the carrier board. Refer to your IP carrier board User Manual for more information.

# ISA (PC-AT) Bus Addressing

ISA (PC-AT) bus addressing requires computing the address from the byte addresses given in Figures 3 and 4 above under VMEbus Addressing. The formula is:

ISA bus byte address = VMEbus byte address – 1

The effect of this formula is to change all 68K odd byte addresses into Intel architecture even byte addresses. All byte data is still transferred on data lines D0..D7.

Interrupt mapping is a function of the selected carrier board. See your IP carrier board User Manual for more information.

# I/O Pin Assignments

This section gives the I/O pin assignments for IP-Octal Opto connections.

| Pin Number | Function |
|---|---|
| 1 | External Common (GND) |
| 2 | Channel 6  RS-232 RxD |
| 3 | Channel 7  RS-232 TxD |
| 4 | External Common (GND) |
| 5 | Channel 7  RS-232 RxD |
| 6 | Channel 8  RS-232 TxD |
| 7 | External Common (GND) |
| 8 | Channel 8  RS-232 RxD |
| 9 | GND |
| 10 | External Pull Up 1 |
| 11 | GND |
| 12 | External Pull Up 2 |
| 13 | GND |
| 14 | External Pull Up 3 |
| 15 | External Common (GND) |
| 16 | +5V Input |
| 17 | +5V Input |
| 18 | +12V Input |
| 19 | +12V Input |
| 20 | +12V Output |
| 21 | +12V Output |
| 22 | –12V Input |
| 23 | –12V Input |
| 24 | –12V Output |
| 25 | –12V Output |
| 26 | –6V Bias Output |
| 27 | External Common (GND) |
| 28 | +5V Bias Output |
| 29 | External Common (GND) |
| 30 | –12V Bias Output |
| 31 | External Common (GND) |
| 32 | +12V Bias Output |
| 33 | RS-422 Bias Output |
| 34 | RS-422 Bias Output |
| 35 | External Common (GND) |
| 36 | GND |
| 37 | +5V Output |
| 38 | +5V Output |
| 39 | +5V Output |
| 40 | +5V Output |
| 41 | +5V Input |
| 42 | +5V Input |
| 43 | +12V Input |
| 44 | +12V Input |
| 45 | +12V Output |
| 46 | +12V Output |
| 47 | –12V Input |
| 48 | –12V Input |
| 49 | –12V Output |
| 50 | –12V Output |

**Figure 5 P2 I/O Pin Assignment (Pack A)**

| Pin Number | Function |
|---|---|
| 1 | Channel 1 Optically Isolated TxD– |
| 2 | Channel 1 Optically Isolated TxD+ |
| 3 | Channel 1 Optically Isolated RxD– |
| 4 | Channel 1 Optically Isolated RxD+ |
| 5 | Channel 2 Optically Isolated TxD– |
| 6 | Channel 2 Optically Isolated TxD+ |
| 7 | Channel 2 Optically Isolated RxD– |
| 8 | Channel 2 Optically Isolated RxD+ |
| 9 | Channel 3 Optically Isolated TxD– |
| 10 | Channel 3 Optically Isolated TxD+ |
| 11 | Channel 3 Optically Isolated RxD– |
| 12 | Channel 3 Optically Isolated RxD+ |
| 13 | Channel 4 Optically Isolated TxD– |
| 14 | Channel 4 Optically Isolated TxD+ |
| 15 | Channel 4 Optically Isolated RxD– |
| 16 | Channel 4 Optically Isolated RxD+ |
| 17 | Channel 5 Optically Isolated TxD– |
| 18 | Channel 5 Optically Isolated TxD+ |
| 19 | Channel 5 Optically Isolated RxD– |
| 20 | Channel 5 Optically Isolated RxD+ |
| 21 | Channel 6 Optically Isolated TxD– |
| 22 | Channel 6 Optically Isolated TxD+ |
| 23 | Channel 6 Optically Isolated RxD– |
| 24 | Channel 6 Optically Isolated RxD+ |
| 25 | Channel 7 Optically Isolated TxD– |
| 26 | Channel 7 Optically Isolated TxD+ |
| 27 | Channel 7 Optically Isolated RxD– |
| 28 | Channel 7 Optically Isolated RxD+ |
| 29 | Channel 8 Optically Isolated TxD– |
| 30 | Channel 8 Optically Isolated TxD+ |
| 31 | Channel 8 Optically Isolated RxD– |
| 32 | Channel 8 Optically Isolated RxD+ |
| 33 | Not Connected |
| 34 | Not Connected |
| 35 | External Common (GND) |
| 36 | Channel 1 RS-232 TxD |
| 37 | Channel 2 RS-232 TxD |
| 38 | Channel 1 RS-232 RxD |
| 39 | Channel 2 RS-232 RxD |
| 40 | External Common (GND) |
| 41 | External Common (GND) |
| 42 | Channel 3 RS-232 TxD |
| 43 | Channel 4 RS-232 TxD |
| 44 | Channel 3 RS-232 RxD |
| 45 | Channel 4 RS-232 RxD |
| 46 | External Common (GND) |
| 47 | External Common (GND) |
| 48 | Channel 5 RS-232 TxD |
| 49 | Channel 6 RS-232 TxD |
| 50 | Channel 5 RS-232 RxD |

**Figure 6 P4 I/O Pin Assignment (Pack B)**

# IndustryPack Logic Interface Pin Assignment

Figures 7 and 8 below gives the pin assignments for the IndustryPack Logic Interface on the IP-Octal Opto. Pins marked n/c below are defined by the specification, but not used on the IP-Octal Opto.

| | | | |
|---|---|---|---|
| GND | GND | 1 | 26 |
| CLK | +5V | 2 | 27 |
| Reset* | R/W* | 3 | 28 |
| D0 | IDSel* | 4 | 29 |
| D1 n/c | 5 | 30 | |
| D2 | MEMSel* | 6 | 31 |
| D3 n/c | 7 | 32 | |
| D4 | INTSel* | 8 | 33 |
| D5 DMAck0* | 9 | 34 | |
| D6 | IOSel* | 10 | 35 |
| D7 DMAck1* | 11 | 36 | |
| n/c | A1 | 12 | 37 |
| n/c | n/c | 13 | 38 |
| n/c | A2 | 14 | 39 |
| n/c | n/c | 15 | 40 |
| n/c | A3 | 16 | 41 |
| n/c | IntReq0* | 17 | 42 |
| n/c | A4 | 18 | 43 |
| n/c | IntReq1* | 19 | 44 |
| n/c | A5 | 20 | 45 |
| n/c | n/c | 21 | 46 |
| –12V | A6 | 22 | 47 |
| +12V | Ack* | 23 | 48 |
| +5V | n/c | 24 | 49 |
| GND | GND | 25 | 50 |

**Note 1:** The no-connect (n/c) signals above are defined by the IndustryPack Logic Interface Specification, but not used by this IP. See the Specification for more information.

**Note 2:** The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IndustryPack.

**Figure 7 P1 Logic Interface Pin Assignment (Pack A)**

| | | | |
|---|---|---|---|
| GND | GND | 1 | 26 |
| n/c | +5V | 2 | 27 |
| n/c | n/c | 3 | 28 |
| n/c | n/c | 4 | 29 |
| n/c | n/c | 5 | 30 |
| n/c | n/c | 6 | 31 |
| n/c | n/c | 7 | 32 |
| n/c | n/c | 8 | 33 |
| n/c | n/c | 9 | 34 |
| n/c | n/c | 10 | 35 |
| n/c | n/c | 11 | 36 |
| n/c | n/c | 12 | 37 |
| n/c | n/c | 13 | 38 |
| n/c | n/c | 14 | 39 |
| n/c | n/c | 15 | 40 |
| n/c | n/c | 16 | 41 |
| n/c | n/c | 17 | 42 |
| n/c | n/c | 18 | 43 |
| n/c | n/c | 19 | 44 |
| n/c | n/c | 20 | 45 |
| n/c | n/c | 21 | 46 |
| –12V | n/c | 22 | 47 |
| +12V | n/c | 23 | 48 |
| +5V | n/c | 24 | 49 |
| GND | GND | 25 | 50 |

**Note 1:** The no-connect (n/c) signals above are defined by the IndustryPack Logic Interface Specification, but not used by this IP. See the Specification for more information.

**Note 2:** The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IndustryPack.

**Figure 8 P3 Logic Interface Pin Assignment (Pack B)**

# Programming

The IP-Octal Opto is designed around the SCC2698B and all of the SCC2698B functions are available. The SCC2698B is divided into four Functional Blocks identified as A through D. Each functional block contains two serial channels. The channels are identified by lower case letters a through h. The SCC2698B contains 64 internal registers, 16 for each functional block. Each of these registers is accessible using a read or write to the I/O space of the IP-Octal Opto. The SCC2698B manual is included with the Technical Documentation of the IP-Octal Opto Engineering Kit to provide the user with detailed information about these registers.

The IndustryPack provides an external interrupt vector register. The address of the vector register, which may also be read normally, is in the upper half of the ID PROM space and in the Memory Space of the IndustryPack. The address offsets are shown in Figure 9.

| **Carrier** | **Bus** | **Address** |
|---|---|---|
| VIPC310 | VMEbus | IP base + $C1 |
| VIPC610 | VMEbus | IP base + $C1 |
| MVME162 | VMEbus | IP Memory base + $1 |
| RM1260 | NuBus | IP ID base + $81 |
| RM1270 | NuBus | IP ID base + $83 |
| ATC4 | ISA Bus | IP ID base + $C0 |

**Figure 9 Location of the Vector Register**

The eight bit vector is loaded by the host software prior to enabling interrupts. The interrupt service routine polls the SCC2698B to determine the detailed cause of the interrupt. Function Blocks A and B interrupt on IRQ0. Function Blocks C and D interrupt on IRQ1. See the User Manual for your IP Carrier for interrupt mapping to your bus. Note that although two distinct interrupt levels are provided, there is a single vector for the IndustryPack.

# ID PROM

Every IP contains an ID PROM, whose size is at least 32 x 8 bits. The ID PROM aids in auto configuration of software and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision be present, it may check for it directly.

Standard data in the ID PROM on the IP-Octal Opto is shown in Figure 10 below. The ID PROM used is an 82S123.

For more information on IP ID PROMs refer to the IndustryPack Logic Interface Specification, available from GreenSpring Computers.

The location of the ID PROM in the host's address space is dependent on which carrier is used. Normally, for VMEbus and ISA (PC-AT) bus carriers, the ID PROM space is directly above the IP's I/O space at IP-base + $80. Macintosh drivers use the ID PROM automatically. RM1260 address may be derived from Figure 10 below by multiplying the addresses given by two, then subtracting one. RM1270 addresses may be derived by multiplying the addresses given by two, then adding one. ISA bus addressing may be derived by subtracting one from the addresses listed below in Figure 10.

| | | |
|---|---|---|
| 3F<br><br>19 | (available for user) | |
| 17 | CRC | (AD) |
| 15 | No of bytes used | (0C) |
| 13 | Driver ID, high byte | (00) |
| 11 | Driver ID, low byte | (00) |
| 0F | reserved | (00) |
| 0D | Revision | (0C) |
| 0B | Model No IP-Octal Opto | (2F) |
| 09 | Manufacturer ID GreenSpring | (F0) |
| 07 | ASCII "C" | (43) |
| 05 | ASCII "A" | (41) |
| 03 | ASCII "P" | (50) |
| 01 | ASCII "I" | (49) |

**Figure 10 ID PROM Data (hex)**

# User Options

User options consist of configuring the optical interface of the IP-Octal Opto for the electrical requirements of various communications protocols. This section describes three configurations of the IP-Octal Opto for external serial data communication channels.

The IP-Octal Opto continues two sets of on board circuitry for each of its eight channels. It includes a conventional non-isolated RS-232 interface that may be used for monitoring or test purposes. It also includes an optically isolated send and receive interface. In general, it is not possible to connect both receive interfaces for any channel at the same time, (since the data from the two interfaces is exclusive NOR'd together).

Before connecting the isolated interface, it is recommended that the system integrator first connect to the non-isolated RS-232 interface and leave the isolated interface connections open. Testing in this way assures that addressing, interrupts, and other host and software issues are out of the way prior to testing the isolated interfaces.

Two basic methods of connecting the isolated interface are described in this section: isolated RS-232 and isolated RS-422. Note that in both cases an isolated external power supply is required. Note also that the RS-232 and RS-422 interfaces do not themselves fully conform to the RS specifications, but are completely reliable if connected to conforming equipment.

The IP-Octal Opto may also be wired to support Teletype® style current loops and doubly isolated current loops.

***Caution:*** *The optical isolation on the IP-Octal Opto is primarily for the purpose of noise reduction. It is not provided to meet safety regulations of any kind. The isolation voltage is specified as ±60 volts.*

## RS-232 Interface Wiring

Wiring for prototype purposes or for low volume production may be conveniently and reliably accomplished using the terminal block supplied in the Engineering Kit for the IP-Octal Opto.

Make the following changes to the default IP-Octal Opto to implement RS-232 compatibility on the isolated inputs and outputs:

1. Check that shunt E4 connects E4.1–E4.2. This controls the output polarity.
2. RP3 should be installed, and have a value of 2KΩ. (See component information in Figure 25 below.)
3. Set shunt E5 to connect E5.2–E5.3.
4. Check that RP7 and RP8 have a value of 1KΩ (the standard default value).
5. Non-isolated RS-232 input lines should be left open.
6. Isolated +12 and –12 volt power must be connected. Use the signal names +12IN and –12IN. +5 volt power is not used. See Figures 21 and 22 below, Figures 5 above or the schematic for pin numbers. The +12OUT and –12OUT may be looped-back for this power if no isolation is desired (when testing, for example). Use ExtCom as the external common signal for both power supplies and connect ExtCom to GND if looped-back local power supplies are used.
7. Connect the RS-232 output signal from the IP-Octal Opto (TXn– for each channel n) to the external equipment's serial input (RxD). See Figure 11 below.
8. Connect the TXn+ signal for each channel n of the IP to the external +12 power. See Figure 11 below.
9. Connect the RS-232 common (pin 7 on a standard DB-25 connector) to the ExtCom external power supply common line.
10. Connect the RS-232 output from the transmit (TxD) of the external equipment to the IP's serial input, RXn+ of each channel n. See Figure 12 below.
11. Connect the RXn– of each channel n to the ExtCom power supply external common line. See Figure 12 below.

The external power supplies do not need to be particularly well regulated, although 60 Hz or 120 Hz ripple is preferred to switching power supply noise. The range of 9 to 15 volts will generally work reliably, although 12 volts is the preferred nominal value. Be sure to connect the common line from the power supplies to ExtCom and ***not*** to the logic ground to maintain the isolation of the optical interface. The power lines into the IP are fused, polarity protected, over-voltage protected and filtered. If everything is connected properly but there is no observable output from the IP be sure to check the fuses. (Turn off all power and use a DMM to measure resistance directly across the fuse.)

The IP output circuit is shown on page 2 of the schematics. The transmit output of the SCC2698 is not inverted by U5 but it can be inverted by adjusting jumper block E4. The output of U5 drives the LED in the optocoupler. The LED is normally off if the Octart is not transmitting. Thus the optocoupler output transistor is normally not conducting and RP3 provides a passive pull-down on the output to –6 volts. When the Octart sends a Space bit, the optocoupler turns on and the output line is pulled up to a nominal +12 volts. The output line must not be shorted, or the output transistor in the optocoupler may be blown. The output voltage swing (no load) is about –6 volts to +12 volts.

The output polarity may be reversed by changing shunt E4 to the E4.2–E4.3 position.

If it is desired to protect the outputs against a short circuit, make the following changes to the numbered instructions above:

8. Leave the TXn+ signal for each channel n of the IP open.

The output voltage swing (no load) is about –6 volts to +6 volts.

The input circuit has a 1KΩ resistor in series with the LED of the optocoupler. It is designed to run at 5 to 10 mA nominal ON current, which corresponds to an input voltage of about +6 to +12 volts for positive voltage (Space), and any negative voltage for Mark. Polarity may be reversed by reversing the RXn+ and RXn– connections or by connecting the non-isolated RS-232 input (RXn_232) to +12IN.

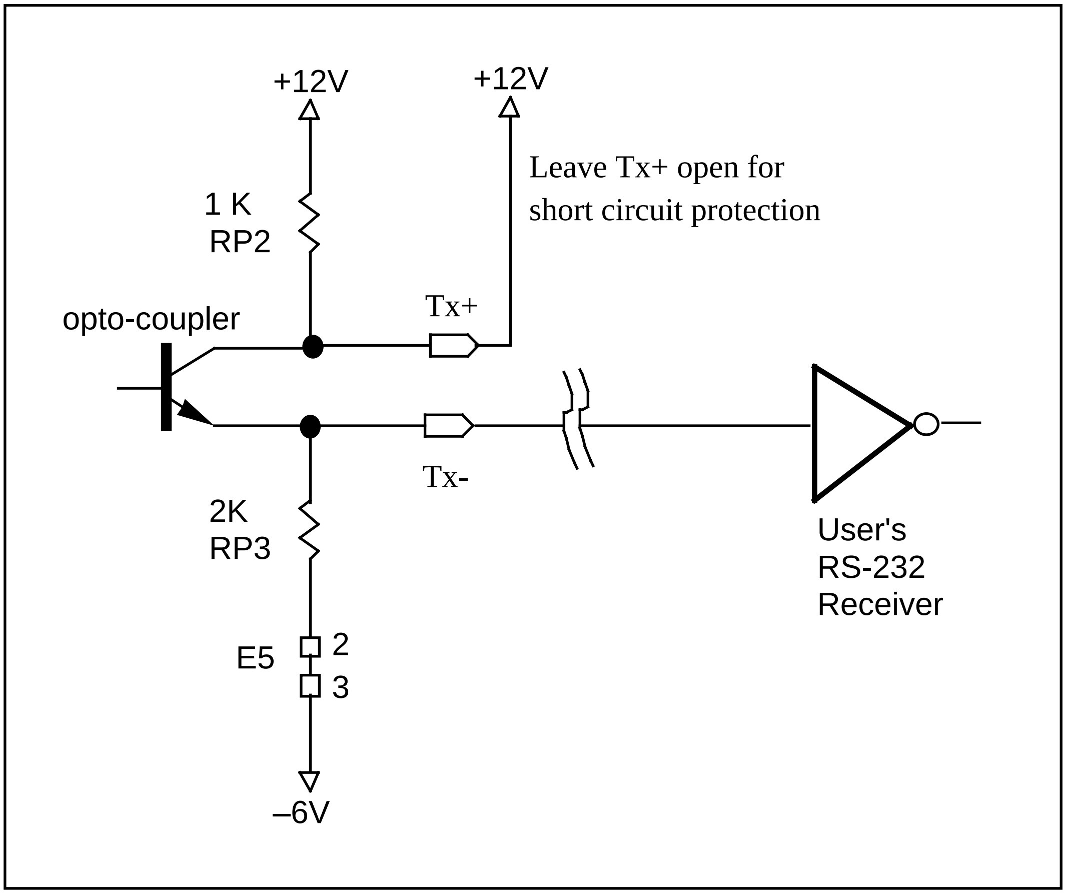


**Figure 11 IP-Octal Opto Output To RS-232**

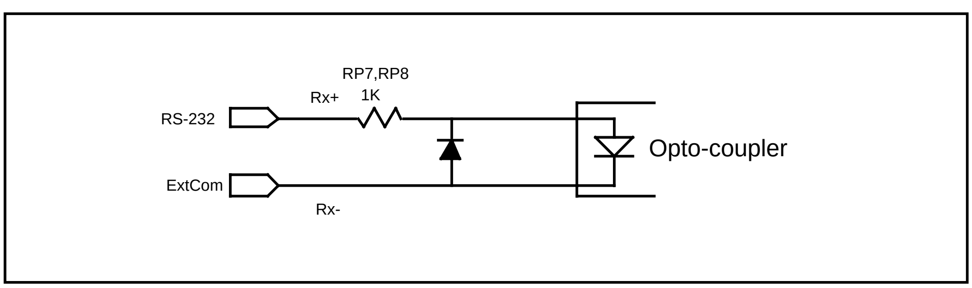


**Figure 12 IP-Octal Opto Input From RS-232**

## RS-422 Interface Wiring

Wiring for prototype purposes or for low volume production may be conveniently and reliably accomplished using the terminal block supplied in the Engineering Kit for the IP-Octal Opto.

RS-422 is a differential voltage signaling standard. This wiring arrangement may also be used to interface with point-to-point (non-multidrop) RS-485, since they share the same voltage specifications. With minor modifications, this wiring arrangement may also be used with RS-423.

Make the following changes to the default IP-Octal Opto to implement RS-422 compatibility on the isolated inputs and outputs:

1. Move shunt E4 to connect E4.1–E4.2. This changes the output polarity.
2. Verify RP2 is installed and has a value of 1 KΩ (the standard default value).
3. RP3 should be installed, and have a value of 1.2KΩ. (See component information in Figure 25 below.)
4. Set shunt E5 to connect E5.2–E5.3.
5. Change RP7 and RP8 to a value of 100 Ω.
6. Non-isolated RS-232 input lines should be left open.
7. Isolated +12, –12 and +5 volt power must be connected. Use the signal names +12IN, –12IN and +5IN. See Figures 21 and 22 below, Figures 5 above or the schematic for pin numbers. The +12OUT, –12OUT and +5 OUT may be looped-back for this power if no isolation is desired (when testing, for example). Use ExtCom as the external common signal for all power supplies (and connect ExtCom to GND if looped-back local power supplies are used).
8. Connect the RS-422+ serial input signal from the external equipment (Rx+ or RD(B)) to the 422Bias signal form the IP-Octal Opto. Use any or all of pins P2.33, 34. This provides a fixed bias voltage of about 0.75 volts DC. See Figure 13 below.
9. Connect the external RS-422– output signal (TXn–) for each channel from the IP-Octal Opto to the external equipment's serial input– (Rx– or RD(A)). The external RS-422 receiver should be terminated at 100Ω or 120Ω. See Figure 13 below.
10. Connect the external equipment's ground to the external power supply common. This signal also connects to the external power supply common line ExtCom on the IP.
11. Connect the RS-422 input+ from the external equipment's transmitter (Tx+ or SD(B)) to the IP's serial input (RXn–) of each channel. See Figure 14.
12. Connect the RS-422 input– from the external equipment's transmitter (Tx– or SD(A)) to RXn+ of each channel. See Figure 14.

Reversing the phase relationship described in s