RIOC 4063 / 4064

PowerPC based RISC I/O Board

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CREATIVE ELECTRONIC SYSTEMS S.A.

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1. INTRODUCTION

1.1 General Description

The RIOC 406x family has been designed to provide general purpose low cost CompactPCI™ platforms for high-speed interfaces based on the PCI I/O bus. His design characteristics has been aimed at the maximum throughput, without compromise on all the buses used.

- 50 Mbytes/s on CompactPCI™
- Power-PC family for CPU power
- 128 Mbytes/s on the PCI interfaces

RIOC 406x Specifications

CPU Subsystem		
Host CPU Type	PPC 604e PID9v @ 200 MHz PPC 603e PID7v @ 200 MHz	PCC MAC5 604R@ 300 MHz / 400 MHz PCC ARTHUR @ 300 MHz
	PCI industry standard backbone bus	
Bridge Controller		
Bridge Type	IBM 27-82660 - (Lanaï / Kauai)	
Memory Resources		
Global Memory	16 or 64 Mbytes on-board DRAM - 60 ns EDO Extension for 16 - 64 Mbytes DRAM directly installable in situ System Memory directly connected to the 64-bit wide memory controller	
L2 Cache	1 Mbyte fast SSRAM Direct mapped, look-aside, and write-through	
Private Memory	128 Kbytes SRAM PCI mapped	
Flash EPROM	4 Mbytes / 8 Mbytes	
RTC / NVRAM	1 x M48T18 chip with 8 Kbytes NVRAM	
I/O Resources		
Counter / Timers	1 x Z-CIO 8536 (3 x 16-bit timers, 1 µs resolution)	
Serial Ports RS 232	2 ports (PC87312 NS) up to 38.4 K (Asynchronous bps)	
Ethernet	AMD PCNET 79C970A Controller - RJ45 10baseT front panel connector	
RTC	SGS Thomson M48T59 with watchdog and alarms	
CompactPCI™ Interface		
	32 bits with 132 Mbytes/s bandwidth System & Peripheral slot functionalities 2 DMA channels with dedicated FIFOs supporting chained block transfers I2O compatible message unit CompactPCI™ Geographic Addressing for multi RIOC boards automatic configuration 8 Mailboxes 2 Doorbell Registers	
Miscellaneous		
	Remote Reset Input (AMP MCX mini-coax)	
	Triggering and synchronization signals	
Real hardware multiprocessor support	Multi-port global memory Eight 255 x 32-bit FIFOs with interrupt capability Autonomous DMA logic Complete interrupt structure	
Mezzanine Extension		
PCI Mezzanines	2 x PMC Slot Extension Form Factor (IEEE P1386 Draft 2.0), + 5 V signaling	

Power Requirement (excluding PMC)	
+ 3.3 V	PowerPC 603ev In = 1.5 A (16 Mb DRAM, cache enabled) PowerPC 604ev In = 2.5 A (16 Mb DRAM, cache enabled) PowerPC 604R In = 1 A (64 Mb DRAM, cache enabled)
+ 5 V	PowerPC 603ev In = 4 A PowerPC 604ev In = 5 A PowerPC 604R In = 4,5 A (64 Mb DRAM, cache enabled)
± 12 V	only for PMCs
Environmental Specifications	
Operating Temperature	0° C to 50° C with forced air cooling (450 LFM)
Storage Temperature	- 40° C to 85° C
Relative Humidity	5% to 90% non condensing
Regulatory Compliance	Immunity EN 50082-2 Emission EN 55022-A Safety EN 60950
Physical dimensions Height Depth Front panel height Front panel depth Front panel width	Double-high Single Slot CompactPCI™ board (6U) 233 mm (9.2 in.) 160 mm (6.3 in.) 262 mm (10.3 in.) 188 mm (7.4 in.) 20 mm (0.8 in.)

RIOC 406x General Block Diagram

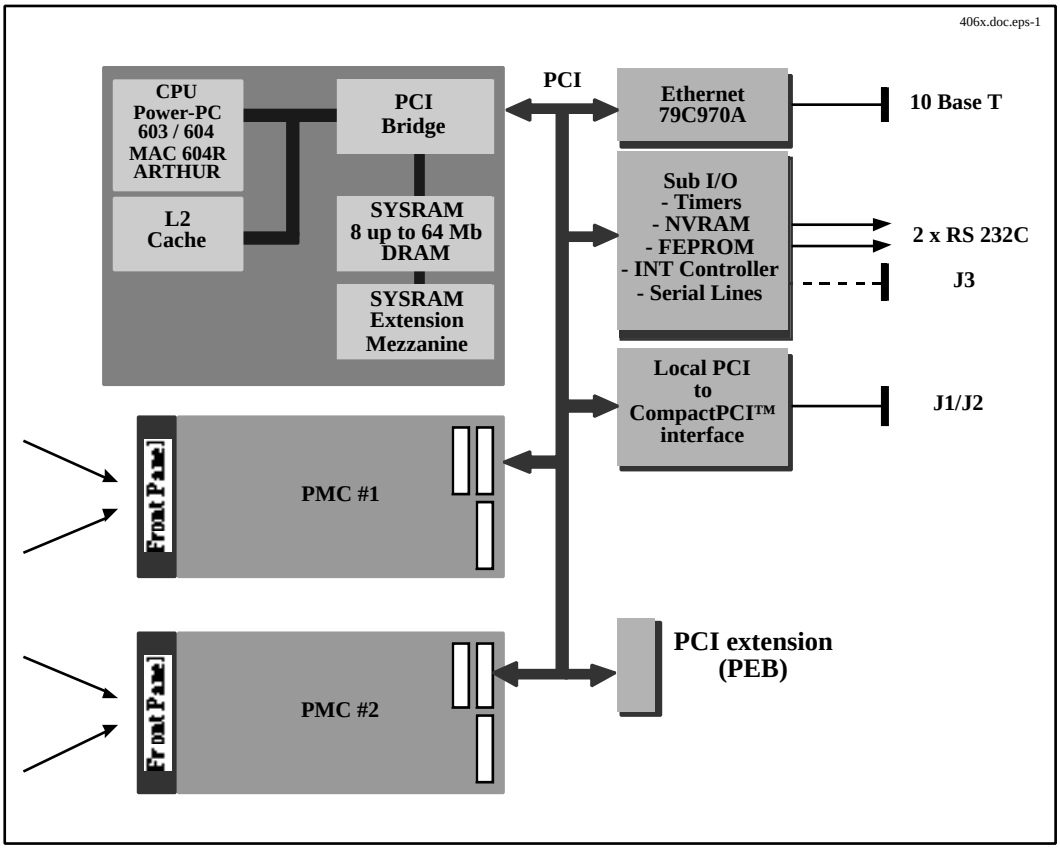

Fig 1.1

1.2 Installing the RIOC 406x

The RIOC 406x is designed to work within the following environmental specifications:

- Operating temperature 0° C to 50° C
- Forced Air cooling (450 LFM)
- Antistatic environment

CES accepts no responsibility for failure should these conditions not be respected

Caution

1. Never use a RIOC board in a non-cooled crate (minimum air flow: 450 LFM over the board). This may burn the processor.
2. RIOC boards support only +5 V signaling. Never use them with other CPCI™ boards which only support +3.3 V signaling. Switch SW3-2 must be OFF.
3. Jumper ST3 (at the bottom-front of the board) must be plugged during handling of the board. This jumper connects the board's mechanical ground (SHIELD) to the board's logical ground (GND).

1.2.1 Unpacking the RIOC 406x

The RIOC 406x is shipped in a box with protection from electrostatic discharges. A CES sticker mentioning the board's name, reference number and serial number should be visible.

The RIOC 406x itself is wrapped in a special plastic bag closed by a sticker. When removing the board from its protection, be careful not to touch the printed circuits with the fingers and use ESD protection.

1.2.2 Setting up Jumpers and Switches

The factory setting of the switches is the following:

SW1	OFF	CES reserved
SW2-1	OFF	Front Panel Reset MCX disabled
SW2-2	OFF	EN_PMCIO
SW2-3	OFF	Do not boot on CES FPROM piggy
SW2-4	OFF	Auto boot enabled
SW3-1	OFF	ROM_SHORT
SW3-2	OFF	CPCI™_KEY
SW3-3	OFF	ENUM
SW3-4	OFF	CPCI™_ENRST

1.2.3 Installing the RIOC 406x in a CompactPCI™ Crate

- Power-off the CompactPCI™ crate.
- Insert carefully the board in the CompactPCI™ crate.
- Screw the board in the CompactPCI™ crate to connect the chassis ground to the unit's front panel.
- Connect all peripherals
- One CPU board must be plugged in the System Slot of the crate.

1.2.4 Connecting Peripherals

Connecting a terminal

Connect a terminal to the serial line tty0 µDB9 connector with a RSC 6731A0 cable.

Set your terminal operating mode to:

- Tx baud rate 9600
- Rx baud rate 9600
- 8 bit no parity
- one stop bit
- local echo off
- newline off
- del = ^H

Connecting to Ethernet 10baseT

Connect the RJ45 cable (ECC 6714A0) from the RIOC 406x to a Hub.

1.2.5 Powering on the System

Power-on first the peripheral devices (terminal, SCSI devices). Power-on the CompactPCI™ crate.

1.3 RIOC 406x Boot Sequence

The first message printed-out by PPCMon is displayed on the screen after ± 4 s.

Refer to the PPCMon manual for a complete description of the on-board monitor.

1.3.1 Auto Boot

When coming out of factory, the board is set with defaults boot parameters to execute the following automatic boot procedure at power-on:

```
PPC Boot Rev 3.20 created Mon Sep 22 15:38:11 1997

  Module Type: 4063AA  rev: A1  serial: 3
  Host CPU: PPC603e   ver: 2.01   speed: 200 Mhz
  PCI Bridge: IBM27-82660 (Lanai/Kauai) rev: 02
  Memory Size: 8+8+0+0+0+0+0+0   = 16 Mbytes  EDO RAM  60 ns   ECC: disabled
  L2 CACHE:  512 kbyte SSRAM
  FPROM: One bank of AMD29F016 installed
  Ethernet Address: 00:8a:a2:a0:b2:00
Entering boot diagnostics

 0    Check System Memory (0x00000000 - 0x00effffc)          0  SKIPPED
 1    Check Interrupt Handler                                0  OK
 2    Check PCI Bridge                                       0  OK
 3    Check Cache and MMU                                    0  OK
 4    Check MK48T08 RTC and NVRAM                            0  OK
 5    Check SIC6351 Interrupt Controller                     0  OK
 6    Check PC87312 Super IO                                 0  OK
 7    Check ZCIO8536 Micro Timers                            0  OK
 8    Check FIFO's (0 - 7)                                   0  OK
 9    Check UPI82C42PC Keyboard and Mouse Controller         0  OK
10    Check DS1620 Digital Thermometer                       0  OK
11    Check PCI devices                                      0  OK
12    Check AM79C970 Ethernet Controller  (PCI slot 0)       0  OK
13    Check PMC #1 Extension  (PCI slot 2)                   0  NO DEVICE
14    Check PMC #2 Extension  (PCI slot 1)                   0  NO DEVICE
15    Check CPCI™ Interface                                 0  OK
```

```
***********************************************
*   PPC_Mon PowerPC monitor - version 3.2     *
*                                             *
***********************************************

PPC_Mon>
```

Note It is always possible to stop the auto boot at any phase by entering a "SPACE" character over the serial line tty0. Typing "x" will stop PPCMon at the end of the power-on diagnostic tests, avoiding the automatic boot of an OS.

1.3.2 Manual Boot

To execute the manual boot procedure, you have to set the RIOC 406x SW2-4 micro switch to ON. After power-on, it will enter PPC_FlashLoad. The purpose of PPC_FlashLoad is to update the contents of the Flash EPROM with new versions of the firmware.

Refer to PPCMon 3317 User Interface Manual for PPC_FlashLoad commands.

```
***********************************************
*   PPC_FlashLoad RIO806x  - version 3.10     *
*                                             *
***********************************************

Two banks of AMD29F016 installed

PPC_FlashLoad>
```

By entering q and CR, you exit PPC_FlashLoad and enter the PPC_Mon command interpreter.

1.3.3 Customizing Auto Boot

The boot parameters can be set to launch automatically an operating system (see the PPCMon commands set and setenv).

1.3.4 In Case of Troubles

If you experience troubles in booting the RIOC 406x:

❶ First power-off the CompactPCI™ crate,

❷ Remove the board from the crate and set the switches as follows:

SW1	OFF	CES reserved
SW2-1	OFF	Front Panel Reset MCX disabled
SW2-2	OFF	EN_PMCIO
SW2-3	OFF	Do not boot on CES FPROM piggy
SW2-4	ON	Manual boot enabled
SW3-1	OFF	ROM_SHORT
SW3-2	OFF	CPCI™_KEY
SW3-3	OFF	ENUM
SW3-4	OFF	CPCI™_ENRST

❸ Install the board in a CompactPCI™ crate

❹ Connect serial line (part RSC 6731A0) from your terminal in the tty0 µDB9 connector

❺ Set your terminal operating mode to

Tx baud rate 9600
Rx baud rate 9600
8 bit no parity
One stop bit
Local echo off
Newline off
DEL = ^H

❻ Power-on the CompactPCI™ crate

The following message should appear on the screen:

```
*********************************************
*   PPC_FlashLoad RIO806x  - version 3.10     *
*          CES SA Copyright 1997              *
*********************************************

Two banks of AMD29F016 installed
PPC_FlashLoad>
```

By entering CR (carriage return) a menu should be displayed.

```
PPC_FlashLoad>
commands are :
Erase flash EPROM :
      erase <start>..<end>
Download from serial line into flash :
      srec
Download from piggy back prom :
      prom <start>..<end> <dest>
PPC_FlashLoad>
```

If nothing appears on the screen, either:

- your terminal is not properly set.
- the RS232 cable is damaged.
- the first sector of the FPROM holding the bootstrap software has been corrupted !!!
- NVRAM parameters have been corrupted.

In the last case, the board must be returned to CES. Corruption of the sector #0 of the FPROM is very unlikely because it is write protected. Make sure all other possibilities have been eliminated before returning the board.

❼ Enter q and CR to continue the boot procedure. The PowerPC starts the board's initialization, runs power-on diagnostics and ends up in the PPC_Moncommand interpreter.

If you get error messages, the firmware should also end up in PPC_Mon If it doesn't, this could indicate a serious hardware problem or a corruption of the FPROM sector 0x20000. In this case, the first thing to try is to reload the PPC_Monfirmware in the FPROM (see PPC_Mon User Interface Manual: Updating the PPC firmware). If this doesn't solve the problem, the board should be returned to CES.

If you end up in PPC_Monwith error messages, this could mean that the EEPROM containing vital parameters for the board behavior or data contained in the sector 0x10000 of the FPROM (code for on-board programmable devices) are corrupted. Integrity of these data is verify by a checksum calculation.

If primary-boot 0 fails, you should reload the PPC firmware in the FPROM (see User Interface Manual: Updating the PPC firmware).

If primary-boot 1 fails, you should update manually the board signature. Because these parameters are vital for the board, they are protected by a password. Call CES' technical support to get the password and update procedure (you must provide CES with the board serial number in order to get the correct values for the board signature parameters).

If primary-boot fails, you have to reload the FPROM sector 0x10000 with the code to be loaded in the FPGA devices (see PPCMon User Interface Manual: Updating the PPC firmware).

Failure of diagnostic 3 - 7 indicates possible hardware problems. Hardware problems can be related to erroneous values in the EEPROM.

1.4 Memory Mapping Summary

1.4.1 PPC Addressing

System Memory			
0x0000'0000	-	0x07FF'FFFF	128 Mbytes System Memory
PCI I/O Cycles Section 1			
0x8000'0000	-	0x807F'FFFF	Bridge Internal Registers (BCRs)
0x8000'0814			L2 Invalidate
0x8000'081C			System Control
0x8000'0821			Memory Controller Misc
0x8000'0840			Memory Parity Error Status
0x8000'0842			L2 Error Status
0x8000'0843			L2 Parity Error Read & Clear
0x8000'0844			Unsupported Transfer Type Error
0x8000'0850			IO Map Type
0x8000'0CF8			PCI/BCR Configuration Address
0x8000'0CFC			PCI/BCR Configuration Data
PCI CONFIG Cycles			
0x8080'0800	-	0x8080'08FF	PCI Slot 0 79C970A Ethernet
0x8080'1000	-	0x8080'10FF	PCI Slot 1 PMC n°2 (upper)
0x8080'2000	-	0x8080'20FF	PCI Slot 2 PMC n°1 (lower)
0x8080'4000	-	0x8080'40FF	PCI Extension Slot (P10)
PCI I/O Cycles Section 2			
0x8100'0000	-	0x813F'FFFF	Flash EPROM (Programming)
0x8140'B000	-	0x8140'B3FF	SIC 6351 IACK Prog
0x8140'B400	-	0x8140'B7FF	SIC 6351 Registers
0x8140'B800	-	0x8140'BBFF	Z-CIO 8536 Registers
0x8140'BD00	-	0x8140'BD0F	Local Registers
0x8140'C000	-	0x8140'CFFC	PC 87312 Registers (Serial Lines Controller)
0x8140'E000	-	0x8140'FFFF	FIFO Ports
0x9000'0000	-	0x9FFF'FFFF	Direct Master access to CompactPCI™ I/O Space
0xA0F5'0000	-	0xA0F5'FFFF	PLX Registers
BCR Transaction			
0xBF80'0000	-	0xBFFF'FFFF	BCR Transaction
0xBF80'1000			PCI IACK Cycle
0xBFFF'EFF0			System Error Address
PCI IACK Cycle			
0xBF80'1000			PCI IACK Cycle
PCI MEMORY Cycles			
0xC000'0000	-	0xCFFF'FFFF	User's available PCI MEMORY Space (256 Mbytes)
0xD000'0000	-	0xDFFF'FFFF	User's available PCI MEMORY Space (256 Mbytes)
0xE000'0000	-	0xEFFF'FFFF	Direct Master access to CompactPCI™ Memory Space

0xF000'0000	-	0xFBFF'FFFF	User's available PCI MEMORY Space (192 Mbytes)
0xFC00'0000	-	0xFEFF'FFFF	Reserved
0xFE00'0000	-	0xFF1F'FFFF	SRAM (128 Kbytes)
0xFE20'0000	-	0xFF20'7FFF	NVRAM & RTC (32 Kbytes)
0xFE20'0000	-	0xFF7F'FFFF	Reserved
0xFE80'0000	-	0xFEFF'FFFF	Flash EPROM
PCI MEMORY I/O Space (489 Mbytes)			
0xA0F6'0000	-	0xBE7F'FFFF	
Remote PCI ROM			
0xFF80'0000	-	0xFFFF'FFFF	Bootstrap ROM, PCI Memory Transaction to Flash EPROMs

1.4.2 PCI Addressing

System I/O PCI_MEMORY Space Mapping

0x1000'0000	-	0x1FFF'FFFF	Direct Master access to CompactPCI™ I/O Space
0x2000'0000	-	0x2FFF'FFFF	Direct Master access to CompactPCI™ Memory Space
0x3E00'0000	-	0x3E01'FFFF	SRAM (128 Kbytes)
0x3E20'0000	-	0x3E3F'FFFF	NVRAM and RTC
0x3E80'0000	-	0x3EFF'FFFF	Flash EPROM

System I/O PCI_IO Space Mapping

0x0100'0000	-	0x013F'FFFF	Flash EPROM (Programming)
0x0140'B000	-	0x0140'B3FC	SIC 6351 IACK Prog
0x0140'B400	-	0x0140'B7FC	SIC 6351 Registers
0x0140'B800	-	0x0140'BBFC	Z-CIO 8536 Registers
0x0140'BD00	-	0x0140'BDFC	Local Registers
0x0140'C000	-	0x0140'CFFC	PC 87312 Registers (Serial Lines Controller)
0x0140'E000	-	0x0140'FFFF	FIFO Ports
0x20F5'0000			PLX Registers
0x8000'0000	-	0x87FF'FFFF	Local System Memory

2. HOST CPU KERNEL

2.1 Host CPU Implementation

The RIOC 406x host CPU kernel (PowerPC 60x) is implemented on the mother board and provides the following functions:

- IBM PowerPC 603e or 604e microprocessor, Mach5 and Arthur 740.
- IBM PowerPC / PCI Bridge 27-82660 (Lanaï - Kauaï chipset)
- Up to 256 Mbytes of System DRAM (with memory extension mezzanine)
- L2 cache support (up to 1 Mbyte)

For complete description of these microprocessors consult the IBM related documentation.

The PCI is always clocked at 33 MHz while the CPU Bus clock is dependent on the PowerPC microprocessor implemented. CPU to PCI clock rates of 1-to-1, the 660 bridge supports 2-to-2 and 3-to-1. The following table gives the different clocks selected:

Bus Clock	PCI Clock	CPU Type / Speed
66 MHz	33 MHz	PowerPC 603x @ 66 MHz up to 400 MHz
66 MHz	33 MHz	PowerPC 604x @ 100 MHz up to 400 MHz

2.1.1 CPU Bus Address Mapping

The IBM 27-82660 PCI Bridge determines the target of a CPU bus Master transaction based on the CPU bus address range as shown in the following table.

CPU Bus Address	*Other Conditions*	*Target Transaction*	*Target Address*
0x0000'0000 - 0x7FFF'FFFF		System Memory	0x0000'0000 to 0x7FFF'FFFF
0x8000'0000 - 0x807F'FFFF	Contiguous	PCI I/O, BCR, or PCI Configuration	0x0000'0000 to 0x007F'FFFF
	Non-Contiguous	(type 1) transaction	0x0000'0000 to 0x0000'FFFF
0x8080'0000 - 0x80FF'FFFF		PCI Configuration (type 0) transaction	0x0080'0000 to 0x00FF'FFFF
0x8100'0000 - 0xCF7F'FFFF		PCI I/O transaction	0x0100'0000 to 0x3F7F'FFFF
0xBF80'0000 - 0xBFFF'FFFF		BCR transaction & PCI interrupt, Ack.	0x3F80'0000 - 0x3FFF'FFFF
0xC000'0000 - 0xFF7F'FFFF		PCI MEMORY transaction	0x0000'0000 to 0x3F7F'FFFF
0xFFE0'0000 - 0xFFFF'FFFF	Remote ROM	PCI MEMORY transaction to I/O Bus Bridge	0x3FE0'0000 to 0x3FFF'FFFF

2.1.2 Error Handling

These error conditions are handled by CES BSPs. The description given in this paragraph is for information only.

The 660 Bridge supports the detection and reporting of several types of errors. The errors are reported to the CPU or the PCI and status information is saved in the 660 register set so that the CPU can do error type determination.

All errors are associated with either a cycle on the CPU bus or a cycle on the PCI bus (there is also one error condition that is not associated with any bus). Errors detected on the memory bus are associated with a cycle on either the CPU bus (when the CPU accesses memory) or the PCI bus (when a PCI master accesses memory). Errors detected on the PCI bus when the 660 Bridge is the PCI master are associated with a CPU bus cycle. Therefore the only errors associated with a PCI bus cycle are errors that are detected while the 660 Bridge is a PCI target.

Errors associated with a CPU bus cycle are reported to the CPU by means of the MCP* or the TEA* signal. Errors associated with a PCI bus cycle are reported to the PCI by means of the PCI_PERR* or the PCI_SERR* signals.

Each error that can be detected has a mask associated with it. If the mask is set, then the detection of that error condition is disabled. There are also masks for the MCP*, TEA*, and PCI_SERR* signals that prevent reporting of any error by means of that signal (these masks do not affect the detection of the error).

The following protocols describe the error handling actions taken by the 660 Bridge. Once an error is detected and the appropriate status, address, and control information is saved, the detection of all subsequent errors is disabled until the error is reset.

CPU Bus Cycle Errors

- CPU bus unsupported transfer type
- CPU bus XATS* asserted
- CPU bus data bus parity error
- CPU bus write to locked flash
- CPU bus memory select error
- Memory parity error (during CPU access to memory)
- PCI data bus parity error (while PCI master)
- PCI bus target abort received (while PCI master)
- PCI bus master abort generated (while PCI master)

If the error is masked, do not detect the error. If the error is detected, perform the following steps.

1. Set status bit indicating error type.
2 Set status bit indicating error during CPU cycle.
3. Save CPU address and control bus values.
4. Report error to the CPU (Reported by means of TEA# if the CPU cycle is still active or by means of MCP# if the CPU cycle has ended.)

Notes - PCI data bus parity errors also cause PCI PERR# to be asserted.

- There is a status bit (PCI Status Register bit <15>) that is set whenever any type of PCI bus parity error is detected. The setting of this status bit is not maskable.

PCI Bus Cycle Errors

- PCI address bus parity error (while PCI target)
- PCI data bus parity error (while PCI target)
- PCI memory select error (while PCI target)

If the error is masked, do not detect the error. If the error is detected, perform the following steps.

1. Set status bit indicating error type.
2. Set status bit indicating error during PCI cycle.
3. Save PCI address and control bus values.
4. Report error to the PCI (If the error is a data bus parity error then report by means of PCI_PERR*. If the error is not a data bus parity error then report by means of PCI_SERR*. Also, if the PCI cycle is still active, then target aborts the cycle.)

Note Data bus parity errors can be enabled to report errors by means of PCI_SERR*. This method is only used if it is determined that PCI_PERR* is not supported by some (or all) of the PCI masters in the system.

Other Error

The only error condition not associated with a CPU or PCI bus cycle is a sampling of NMI active. Report error to the CPU by means of MCP*.

2.2 PowerPC System DRAM

The IBM 27-82660 Bridge controls the RIOC system memory. It can be equipped with up to 4 banks of 72-bit wide DRAM. These memory banks can be of 8, 32 or 64 Mbytes and are mounted on mezzanine board. The memory controller support panache 8 and 32 Mbytes memory banks. The IBM 27-82660 Memory Controller Features:

- Support memory operations for the PowerPC Architecture.

- Data bus path 72 bits wide - 64 data bits and eight bits of optional ECC.
- Full refresh support, including refresh address counter and programmable DRAM refresh timer with low-power mode.

  Burst-mode memory address generation logic: 32 bytes CPU bursts to memory, variable length PCI burst to memory.
- Little-endian and big-endian addressing and byte swapping modes.
- Provides row and column address multiplexing.

The IBM 27-82660 Bridge supports either no parity or one bit per byte parity DRAM, in which one parity bit is associated and accessed with each byte. The bridge is BCR programmable to support either no parity, even parity. The RIOC 406x does not implement ECC.

2.3 PowerPC L2 Cache

The RIOC 406x incorporates a second level cache (L2). The L2 cache controller in the IBM 27-82664 chip set controls external Tag SRAM and the data SSRAMs (Synchronous SRAM) for a second level cache. The L2 cache is reserved only for the system memory space from 0 to 1 Gbyte.

The L2 cache architecture is direct mapped, look-aside, and write-through.

The RIOC 406x owns 1 Mbytes of L2 cache (smaller size can also be supported).

On PowerPC CPU memory reads, the L2 cache only responds to bursts. Single beat reads are ignored. The IBM 27-82664 chip set maintains L2 coherency during PCI to system memory transactions. the L2 supports access time of 3-1-1-1 clocks (66 MHz) for 32 (~ 340MBytes/s)

The embedded L2 cache controller can be controlled through specific bridge registers:

Cache Type	Chip set options 3 Register (BCR 0xD4) bit#3 must be set for Synchronous SRAM
Invalidate	L2 Invalidate Register (0x8000'0814) Write any value causes L2 invalidation
Enable	System control Register (0x8000'081C) bit#6 must be set for L2 cache enable Cache Status register (BCR 0xB1) bit#1 must be set for L2 snooping enable
Freeze	System Control Register (0x8000'081C) bit#7 must be set for normal update bit#7 must be reset for L2 freezing

2.4 PCI to System Memory

PCI MEMORY reads and writes are decoded by the 27-82660 Bridge to determine if they access System memory (PCI MEMORY reads and writes to addresses from $_{PCI}$0x8000'0000 to $_{PCI}$0xFFFF'FFFF on the PCI Bus are mapped by the 27-82660 Bridge as system memory from $_{PPC}$0x0000'0000 to $_{PCI}$0x7FFF'FFFF).

PCI Bus Address	*Target Transaction*	*CPU Bus Address*
0x0000'0000 to 0x7FFF'FFFF	Not decoded	
0x8000'0000 to 0xFFFF'FFFF	System Memory	0x0000'0000 to 0x7FFF'FFFF

2.5 PowerPC Interrupt

The IBM 27-82660 Bridge route the local interrupt from the SIC 6351 (INT & NMI) to the PowerPC CPU. Additional exceptions are directly supplied by the 27-82660 Bridge. Refer to IBM 27-82660 Bridge user's manual for complete information.

2.5.1 SMI Hardware Call

The RIO2 8062 incorporates a logic to issue a PowerPC Interrupt. This logic is controlled through a new local register LOC_CTL4.

PPC Mapped	= PPC0x8140'BD08		
PCI I/O Mapped	= PCI0x0140'BD08		
bit <00>	SMI	(W)	This control bit allows to activate the NMI interrupt 1: Set SMI 0: Clear SMI

2.5.2 Interrupt Priority Level

The RIO2 8062 incorporates a new logic to use the priority level supplied by the SIC 6351. The SIC 6351 interrupt controller is associating each source with a priority level (1 to 7). A new control register allows to setup a level's mask in the PowerPC 60x's interrupt has a higher priority than the mask level specified by mskLEV[2...0] in the LOC_CTL5 register.

Additionally to facilitate the OS's interrupt handling, the mask level can be updated dynamically by the logic during the IACK cycle, with the level of current serviced interrupt. This update is selected with bit<4> in the LOC_CTL5 register

This facility makes the PowerPC's interrupt architecture similar to 68K family and will allows real-time OS to be tuned for interrupt latency performance.

2.6 PCI Central Arbiter

The PCI central arbiter is integrated in a CPLD and handle arbitration process for the 6 PCI agents. A special priority mechanism is implemented allowing CompactPCI™ dead-lock recovery to be handled in an efficient manner.

The following 6 PCI agents are arbitrated:

BREQ/BGNT[0]	PowerPC PCI Bridge 27-82660
BREQ/BGNT[1]	CPCI Slave Interface
BREQ/BGNT[2]	79C970A Ethernet Controller
BREQ/BGNT[3]	PMC Slot 2
BREQ/BGNT[4]	PMC Slot 1
BREQ/BGNT[5]	PCI Extension

The prioritization is a mixed of fixed and round robin priority mechanism. The CPCI Slave Interface has the highest priority in case of CPCI deadlock detection, followed by the Ethernet Controller 79C970A which has the second highest priority.

The other agents, PowerPC, CPCI Slave, PCI Extension and PMCs are handled through a round robin priority algorithm.

When no request are pending, the arbiter grant the PowerPC PCI bridge (PCI Bus parking).

3. SYSTEM I/O

3.1 System I/O Block Diagram

The RIOC I/O are interfaced through a discrete PCI to I/O-Bus bridge allowing the mapping of the following devices:

Flash EPROM	Four 29F016 in 48-pin TSOP packages
SRAM	One 64 K x 16 devices used for: Storage for the Message passing FIFOs General purpose SRAM
PC 87312 Super I/O	RS 232 Serials
MK 48T59	Real-time Clock and 8-Kbyte NVRAM
Z-CIO 8536	Timers and Control / Status bits
LOC_REG	Local CSR registers
SIC 6351	Central interrupt controller

3.2 System I/O Mapping

The System I/O resources are mapped on the PCI MEM Space and PCI I/O Space accommodating access resources from the PPC CPU. The PowerPC associated with the IBM 27-82660 PCI Bridge has PCI addressing limited of 1 Gbyte per Space.

PCI I/O	PCI0x0000'0000 -PCI0x3F7F'FFFF
PCI MEM	PCI0x0000'0000 -PCI0x3FDF'FFFF

3.3 Flash EPROM

The RIOC Flash EPROM is built with four TSOP devices (Type 28F008 or 29F016). These four memory devices are organized in block, which can be erased and reprogrammed separately. The Flash EPROM is organized in two banks, each bank requiring two Flash devices to build a 16-bit wide data bus.

Flash EPROM capacity is ranging from 4 Mbytes to 8 Mbytes.

4 Mbytes	2x29F016 (1 bank)
8 Mbytes	4x29F016 (2 banks)

A status bit located in LOC_CTL #1 specify if the RIOC is equipped with 8-Mbit or 16-Mbit Flash EPROM devices.

The on-board Flash EPROM is storing following firmware:

- PPC Bootstrap & Diagnostic & Monitor/Debugger
- File Storage for the FPGA
- ROMable user's application

3.3.1 Flash EPROM Mapping

Flash EPROM Mapping (16-Mbit = 29F016)

Flash EPROM Bank #1	PPC0xFEC0'0000 -PPC0xFEFF'FFFF	
Flash EPROM Bank #2	PPC0xFE80'0000 -PPC0xFEBF'FFFF	
Flash EPROM Bank #1	PCI0x3EC0'0000 -PCI0x3EFF'FFFF	(PCI MEM)
Flash EPROM Bank #2	PCI0x3E80'0000 -PCI0x3EBF'FFFF	(PCI MEM)

3.3.2 Flash EPROM Programming

The four Flash EPROM devices can be reprogrammed in situ by the CPU.

To write / program / erase the Flash EPROMs, specific PCI I/O spaces shall be used. Access to this address range MUST be done only in 16-bit words. The erase / program firmware MUST handle the AMD algorithm in parallel for the 2 Flash devices building the bank.

Flash EPROM erase / program	PPC0x8100'0000 -PPC0x813F'FFFF
Flash EPROM erase / program	PCI0x0100'0000 -PCI0x013F'FFFF(PCI I/O)

Only one Flash EPROM bank can be erased / programmed at a time. Two control bits in the LOC_CTL1 Register allow the user to select the Flash EPROM bank to be erased / programmed (refer to § 3.13).

Note Software facilities are provided at the PPCMon debugger level to reprogram, erase, boot from the Flash EPROMs directly from the serial line, Ethernet TFTP Boot or SCSI.

3.4 Local SRAM

The local SRAM (128 Kbytes) is built with a single 64 K x 16 device. The System I/O Bridge is converting the PCI 32-bit access into two SRAM accesses. This SRAM is supporting only 32-bit write data transfers.

The SRAM is mainly used for:

- Message passing FIFO data storage
- Message passing FIFO pointer storage

Local SRAM Mapping

The SRAM is mapped at following address:

PPC Mapped	= PPC0xFE00'0000 -PPC0xFE01'FFFF
PCI MEM Mapped	= PCI0x3E00'0000 -PCI0x3E01'FFFF

The SRAM can also be accessed by the PMCs.

Base + 0x0'0000 - 0x0'FFFF	RAM only seen in PCI Memory Space
Base + 0x1'0000 - 0x1'AFFF	RAM seen in PCI I/O and Memory Space
Base + 0x1'B000 - 0x1'DFBF	RAM only seen in PCI Memory Space
Base + 0x1'DFC0 - 0x1'DFFF	FIFO Pointers (32 32-bit locations)
Base + 0x1'E000 - 0x1'FFFF	FIFO Storage (8 Kbytes)

Note The SRAM interface supports PCI burst.

3.5 National PC 87312 Super I/O

The National PC 87312 Super I/O is used to provide on-board RS 232C.

The PC 87312 Super I/O PCLK input is driven by a 24 MHz clock.

The PC 87312 Super I/O can issue three interrupts which are controlled by the "System Interrupt Controller" (refer to § 6.3.5).

3.5.1 PC 87312 Mapping

The PC 87312 Super I/O is mapped at the following address:

PPC Mapped	= PPC0x8140'C000 -PPC0x8140'CFFC
PCI I/O Mapped	= PCI0x0140'C000 -PCI0x0140'CFFC

Three registers constitute the Base Configuration Register set, which controls the set-up of the PC 87312. In general, these registers control the mode of each major function, the I/O addresses of those functions, and whether those functions power down via hardware control or not. These three configuration registers are called the Function Enable Register (FER), the Function Address Register (FAR) and the Power and Test Register (PTR).

These registers can be accessed via hardware or software. During reset, the PC 87312 loads in these configuration registers a set of default values selected by a hardware strapping option. An Index and Data register pair is used to read and write these registers. Each configuration register is pointed by the value loaded in the Index register. The data to be written is transferred via the Data register. Reading a configuration register is done in a similar way (i.e., by pointing to it via the Index register and then reading its contents via the Data register).

The initial hardware configuration sets the I/O address range as follows:

Index Register	➠ base + 0xE60
Data Register	➠ base + 0xE64
UART1 = COM1	➠ base + 0xFE0 - 0xFFC
UART2 = COM2	➠ base + 0xBE0 - 0xBFC

The configuration registers are initialized with the following values:

FER = 0x07: UARTs 1, 2, // Port activated
FAR = 0x10: COM1, COM2, LPT2 configuration
PTR = 0x00: Power down clocks option

Note Refer to National PC 87312 user's manual for programming information.

Registers Mapping

The mapping depends on the DLAB status, bit <07> from its Line Control Register. On reset, this bit is cleared and must be set by writing the LCR.

Addresses given below are offsets from the base address.

DLAB	UART1	UART2	Register
DLAB = 0	0x0FE0	0x0BE0	Receiver Buffer (Read) Transmitter Holding (Write)
	0x0FE4	0x0BE4	Interrupt Enable
	0x0FE8	0x0BE8	Interrupt Identification (Read) FIFO Control (Write)
DLAB = 1	0x0FE0	0x0BE0	Divisor Latch (LSB)
	0x0FE4	0x0BE4	Divisor Latch (MSB)
DLAB independent	0x0FEC	0x0BEC	Line Control
	0x0FF0	0x0BF0	Modem Control
	0x0FF4	0x0BF4	Line Status
	0x0FF8	0x0BF8	Modem Status
	0x0FFC	0x0BFC	Scratch

3.5.2 PC 87312 Serial RS232C Ports

Two full-modem RS 232 serial interfaces are provided on the RIOC Front Panel. They are completely independent. The Front Panel RS 232 are implemented with µDB9 connectors (ITT Cannon MDSM double decker MDSM-18 P E-Z7).

The pins assignment is identical to the standard DB9.

pin n° 1	DCD	Data carrier detect
pin n° 2	SIN	Serial input
pin n° 3	SOUT	Serial output
pin n° 4	DTR	Data terminal ready
pin n° 5	GND	Signal ground
pin n° 6	DSR	Data set ready
pin n° 7	RTS	Request to send
pin n° 8	CTS	Clear to send
pin n° 9	RI	Ring indicator

The RS 232 interfacing is assured by two LT 1337 "Programmable RS 232 Transceiver". This device provides a complete 8-line, jumper-configurable, port RS 232 interface.

Note 2 KV ESD protection is provided on both RS 232 channels.

3.6 MK 48T59 RTC and NVRAM

The MK48T59 TIMEKEEPER RAM is an 8 K x 8 non-volatile static RAM and Real-time clock. The monolithic chip is available in a specially designed package to provide an integrated battery backed-up memory and Real-time clock solution which can be surface mounted. The upper eight memory location are providing the Real-time clock information.

The Real-time clock locations contain years, month, date, day, hour, minute and second in a 24-hour BCD format. Corrections for 28, 29 (leap year), 30 and 31 days are made automatically. The eight clock bytes are not the actual clock counters themselves; they are memory locations consisting of BiPORT read / write memory cells. The MK48T59 includes a clock control circuit which updates the clock bytes with current information once a second.

The MK48T59 features are the following:

- Integrated Ultra low power SRAM, Real-time clock, power-fail control and battery
- Byte wide RAM-like clock access
- BCD coded year, month, day, date, hours, minutes and seconds
- Clock accuracy of ± 1 minute a month at 25° C
- Software controlled clock calibration for high accuracy applications
- 10 years of data retention in the absence of power
- SNAPHAP housing (battery) replaceable
- Battery low warning
- Programmable alarm clock
- Watchdog timer with interrupt or reset capability

For the complete description of the MK48T59, refer to the SGS-THOMSON data sheet.

3.6.1 MK 48T59 PCI Register Mapping

The MK48T59 registers are mapped at the following address:

PPC Mapped	= PPC0xFE20'0000 -PPC0xFE3F'0000	(R/W)
PCI MEM Mapped	= PCI0x3E20'0000 -PCI0x3E3F'0000	(R/W)

The MK48T59 occupies 32 Kbytes:

Base + 0x0000	Non volatile SRAM (first location) NVRAM area (8 Kbytes - 8 bytes, only low byte used)
Base + 0x7FDC	Non volatile SRAM (last location)
Base + 0x7FE0	RTC Control Register
Base + 0x7FE4	RTC seconds
Base + 0x7FE8	RTC minutes
Base + 0x7FEC	RTC hour
Base + 0x7FF0	RTC day
Base + 0x7FF4	RTC date
Base + 0x7FF8	RTC month
Base + 0x7FFC	RTC year

MK 48T59 RTC Control Register

PPC Mapped	= PPC0xFE20'7FE0		(R/W)
PCI MEM Mapped	= PCI0x3E20'7FE0		(R/W)
bits <31...08>	Not implemented	(R/W)	Reserved
bit <07>	W	(R/W)	Write enable control bit
bit <06>	R	(R/W)	Read enable control bit
bit <05>	S	(R/W)	SIGN control bit
bits <04...00>	-	(R/W)	MK48T59 not implemented

MK 48T59 RTC Seconds Register

PPC Mapped	= PPC0xFE20'7FE4		(R/W)
PCI MEM Mapped	= PCI0x3E20'7FE4		(R/W)
bits <31...08>	Not implemented	(R/W)	Reserved.
bit <07>	ST	(R/W)	STOP control bit.
bits <06...00>	SEC	(R/W)	Seconds (BCD format - range: 00 - 59).

MK 48T59 RTC Minutes Register

PPC Mapped	= PPC0xFE20'7FE8		(R/W)
PCI MEM Mapped	= PCI0x3E20'7FE8		(R/W)
bits <31...08>	Not implemented	(R/W)	Reserved.
bit <07>	"0"	(R/W)	MK48T59 reserved.
bits <06...00>	MIN	(R/W)	Minutes (BCD format - range: 00 - 59).

MK 48T59 RTC Hour Register

PPC Mapped	= PPC0xFE20'7FEC		(R/W)
PCI MEM Mapped	= PCI0x3E20'7FEC		(R/W)
bits <31...08>	Not implemented	(R/W)	Reserved.
bit <07..06>	"0"	(R/W)	MK48T59 reserved.
bits <05...00>	HOUR	(R/W)	Hour (BCD format - range: 00 - 23).

MK 48T59 RTC Day Register

PPC Mapped	= PPC0xFE20'7FF0		(R/W)
PCI MEM Mapped	= PCI0x3E20'7FF0		(R/W)
bits <31...08>	Not implemented	(R/W)	Reserved.
bit <07>	"0"	(R/W)	MK48T59 reserved.
bit <06>	FT	(R/W)	Frequency test ("0" for normal operation).
bit <05...03>	"0"	(R/W)	MK48T59 reserved.
bits <02...00>	DAY	(R/W)	Day (BCD format - range: 0 - 7).

MK 48T59 RTC Date Register

PPC Mapped	= PPC0xFE20'7FF4		(R/W)
PCI MEM Mapped	= PCI0x3E20'7FF4		(R/W)
bits <31...08>	Not implemented	(R/W)	Reserved.
bit <07...06>	"0"	(R/W)	MK48T59 reserved.
bits <05...00>	DATE	(R/W)	Date (BCD format - range: 01 - 31).

MK 48T59 RTC Month Register

PPC Mapped	= PPC0xFE20'7FF8		(R/W)
PCI MEM Mapped	= PCI0x3E20'7FF8		(R/W)
bits <31...08	Not implemented	(R/W)	Reserved.
bit <07...05>	"0"	(R/W)	MK48T59 reserved.
bits <04...00>	MONTH	(R/W)	Month (BCD format - range: 01 - 12).

MK 48T59 RTC Year Register

PPC Mapped	= PPC0xFE20'7FFC		(R/W)
PCI MEM Mapped	= PCI0x3E20'7FFC		(R/W)
bits <31...08>	Not implemented	(R/W)	Reserved.
bits <07...00>	YEAR	(R/W)	Year (BCD format - range: 00 - 99).

3.6.2 MK 48T59 RTC Basic Operations

Reading the CLOCK

Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual clock counters, updating the registers can be halted without disturbing the clock itself.

Updating is halted when a "1" is written to the Read bit, the seventh bit in the control register. As long as a "1" remains in that position, updating is halted. After a halt is issued, the registers reflect the count; that is the day, date, and the time that were current at the moment the halt command was issued.

Setting the CLOCK

The eighth bit of the control register is the Write bit. Setting the Write bit to "1", like the Read bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date, and time data in the 24-hour BCD format. Resetting the Write bit to "0" then transfers those values to the actual TIMEKEEPER counters and allows normal operation to resume. The FT bit and those marked to be "0" must be written to "0" for normal TIMEKEEPER operation and SRAM operation.

Stopping and Starting the Oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP bit is the eighth of the seconds register. Setting it to "1" stops the oscillator. When reset to "0", the MK48T59 oscillator starts within 1 second.

3.6.3 MK 48T59 NVRAM Area

The MK48T59 8 Kbytes NVRAM area is wired on the low byte (PCI AD <07...00>) through a 32-bit word aligned addressing.

PPC Mapped	= PPC0xFE20'0000 -PPC0xFE20'7FCC	(R/W)
PCI MEM Mapped	= PCI0x3E20'0000 -PCI0x3E20'7FCC	(R/W)

3.6.4 MK 48T59 Battery Life

The MK 48T59 internal cell has a capacity of 39 mA/h. The device places a nominal RAM and RTC load of less than 445 nA at room temperature.

Note The MK 48T59 battery (SNAPHAT) is replaceable and can be ordered directly to SGS THOMSON, Part number "M4T28BR12-SH1".

3.7 Zilog Z-CIO 8536 Timers

The Z-CIO 8536 is a general purpose peripheral circuit which satisfies most counter / timer I/O and interrupts needs encountered in system design hence helpful in Real-Time situations and interrupt control. The Z-CIO 8536 features are the following:

- Three independent 16-bit counter / timer, each with three output duty cycles (pulsed, one-shot and square-wave) and up to four external access lines (count input, output, gate and trigger). The counter / timers are programmable as re-triggerable or non re-triggerable.
- All registers are Read / Write, accessed in two steps.
- Two independent 8-bit, double buffered, bi-directional I/O port, plus a 4-bit special-purpose I/O port. The I/O ports features programmable polarity, direction (bit mode), 1's catchers and programmable open-drain outputs.
- Flexible pattern-recognition logic.
- Four handshake modes including 3-wire (As IEEE 488).

The Z-CIO is used on the RIOC for:

- Providing three 16-bit counter / timers.
- Port A is used for the CPCI™ control.
- Port B and Port C are used for thermometer control, PMCs BUSMODE and Front Panel interrupt.

The Z-CIO 8536 's PCLK input is driven by a 6 MHz clock. This parameter is important for the counter / timer. The Z-CIO 8536 can issue an interrupt which is controlled by the "System Interrupt Controller" (refer to § 6.3.4).

Note For complete Z-CIO 8536 description refer to Zilog user's manual.

3.7.1 Z-CIO 8536 PCI Register Mapping

The Z-CIO 8536 registers are mapped at the following addresses:

PPC Mapped	= PPC0x8140'B800	(R/W)
PCI I/O Mapped	= PCI0x0140'B800	(R/W)

The Z-CIO 8536 implements 4 registers:

Base + 0x00	Port C Register
Base + 0x04	Port B Register
Base + 0x08	Port A Register
Base + 0x0C	Control Register

Warning Access to the internal Z-CIO 8536's registers requires a two-step sequence. In the first step, a 6-bit address is written to an internal Pointer register. In a second step, the selected register by the pointer is read or written to. These 2 accesses MUST BE INDIVISIBLE and therefore require interrupt protection mechanism

3.7.2 Z-CIO 8536 Port A

Port A

bit <07>	In	UPI_IBF *	CES reserved
bit <06>	In	UPI_OBF	CES reserved
bit <05>	Out	DS1620_RST	Reset signal for digital thermometer
bit <04>	Out	BLO*	Front panel BLO LED control
bit <03>	In	CPCI_GA3	CompactPCI™ geographic address bit 3
bit <02>	In	CPCI_GA2	CompactPCI™ geographic address bit 2
bit <01>	In	CPCI_GA1	CompactPCI™ geographic address bit 1
bit <00>	In	CPCI_GA0	CompactPCI™ geographic address bit 0

3.7.3 Z-CIO 8536 Port B

The Z-CIO 8536 Port B is used to control the on-board thermometer and control the PMCs BUSMODE signaling.

Port B

bit <07>	In	BUSMODE0	PMC#1 (lower) Busmode Status bit 1
bit <06>	In	BUSMODE1	PMC#2 (upper) Busmode Status bit 1
bit <05>	Out	BUSMODE2	PMC Busmode Function bit 2
bit <04>	Out	BUSMODE3	PMC Busmode Function bit 3
bit <03>	Out	BUSMODE4	PMC Busmode Function bit 4
bit <02>	In	DS1620_TCOM	Interrupt request In from digital thermometer
bit <01>	Out	DS1620_CLK	Serial Clock Out for digital thermometer
bit <00>	In / Out	DS1620_DQ	Serial Data In/Out for digital thermometer

3.7.4 Z-CIO 8536 Port C

The Z-CIO 8536 Port C is wired to the Front Panel MCX Reset input. The MCX is driving the 3 inputs controlling the Timer. Internal programming will allow to select the wished function (Trigger - Gate - Count) controlled by the Front Panel input.

Note The logic signal is inverted between the MCX and the Z-CIO inputs.

PORT C

bits <03...01>	In	MCX_RST	Front-panel MCX Reset input
bit <00>	Out	Not used	

3.8 Message passing FIFOs

Eight message passing FIFOs are implemented in the RIOC. Each FIFO is 255 words deep and 32-bit wide. The 8 FIFOs work individually. Each one drives 2 flags: FULL and EMPTY. These 2 flags are monitored by the SIC 6351 which can interrupt the CPU on the following conditions:

FIFO is not EMPTY	Indicates that something is present in the FIFO
FIFO is EMPTY	Indicates that the FIFO is empty
FIFO is FULL	Indicates an overflow of the FIFO (usually an error)

The FIFOs are provided in the RIOC to solve the problems of inter-processor interrupts in a multiprocessor environment such as CompactPCI™. Various use can be made of the FIFOs in multiprocessing or distributed processing, for example:

- Message passing
- Virtual interrupts
- Resource sharing
- Task calling sequence

The eight FIFOs on the RIOC can be used individually, allowing to define priority between the queues (for message passing) or to define one FIFO for message passing and another one for data buffer reservation.

For debugging purposes or for special applications, it is possible to access the FIFO memory buffers directly as standard memory locations (the same for the Write, Read pointers and Word counter). In case of errors (read an empty FIFO or write to a full FIFO), the FIFO control logic will generate a PCI Target Abort. The latter will be treated in the appropriate manner (special error recovery).

Refer to § 6 for FIFOs interrupt implementation.

Note The FIFO's flags and pointer must be initialized after power-up.

FIFOs Resources Mapping

The FIFOs ports are mapped over the PCI I/O at the following addresses:

FIFO #0 Port	PPC 0x8140'E000	PCI 0x0140'E000
FIFO #1 Port	PPC 0x8140'E400	PCI 0x0140'E400
FIFO #2 Port	PPC 0x8140'E800	PCI 0x0140'E800
FIFO #3 Port	PPC 0x8140'EC00	PCI 0x0140'EC00
FIFO #4 Port	PPC 0x8140'F000	PCI 0x0140'F000
FIFO #5 Port	PPC 0x8140'F400	PCI 0x0140'F400
FIFO #6 Port	PPC 0x8140'F800	PCI 0x0140'F800
FIFO #7 Port	PPC 0x8140'FC00	PCI 0x0140'FC00

The FIFOs control register are stored in the SRAM upper area and therefore are mapped over the PCI MEM at the following address:

The offset given in the following table is relative to:

PPC 0xFE01'0000
PCI 0x3E01'0000

FIFO #0 Word Counter	0xDFC0	<D07...D00>
FIFO #0 Write Pointer	0xDFC0	<D23...D15>
FIFO #0 Read Pointer	0xDFC4	<D07...D00>
FIFO #1 Word Counter	0xDFC8	<D07...D00>
FIFO #1 Write Pointer	0xDFC8	<D23...D15>
FIFO #1 Read Pointer	0xDFCC	<D07...D00>
FIFO #2 Word Counter	0xDFD0	<D07...D00>
FIFO #2 Write Pointer	0xDFD0	<D23...D15>
FIFO #2 Read Pointer	0xDFD4	<D07...D00>
FIFO #3 Word Counter	0xDFD8	<D07...D00>
FIFO #3 Write Pointer	0xDFD8	<D23...D15>
FIFO #3 Read Pointer	0xDFDC	<D07...D00>
FIFO #4 Word Counter	0xDFE0	<D07...D00>
FIFO #4 Write Pointer	0xDFE0	<D23...D15>
FIFO #4 Read Pointer	0xDFE4	<D07...D00>
FIFO #5 Word Counter	0xDFE8	<D07...D00>
FIFO #5 Write Pointer	0xDFE8	<D23...D15>
FIFO #5 Read Pointer	0xDFEC	<D07...D00>
FIFO #6 Word Counter	0xDFF0	<D07...D00>
FIFO #6 Write Pointer	0xDFF0	<D23...D15>
FIFO #6 Read Pointer	0xDFF4	<D07...D00>
FIFO #7 Word Counter	0xDFF8	<D07...D00>
FIFO #7 Write Pointer	0xDFF8	<D23...D15>
FIFO #7 Read Pointer	0xDFFC	<D07...D00>
FIFO #0 Storage	0xE000 - 0xE3FF	
FIFO #1 Storage	0xE400 - 0xE7FF	
FIFO #2 Storage	0xE800 - 0xEBFF	
FIFO #3 Storage	0xEC00 - 0xEFFF	
FIFO #4 Storage	0xF000 - 0xF3FF	
FIFO #5 Storage	0xF400 - 0xF7FF	
FIFO #6 Storage	0xF800 - 0xFBFF	
FIFO #7 Storage	0xFC00 - 0xFFFF	

3.9 SIC 6351

The SIC 6351 is an ASIC acting as a complete system interrupt controller. It can control up to 40 interrupt sources and dispatch them over two CPUs through programmable register options. Each interrupt source can be set to work with internal Vector (Vector supplied by the internal SIC 6351's SRAM). Refer to chapter 6.

3.10 DS1620 Digital Thermometer

The DS1620 Digital Thermometer and Thermostat provides a 9-bit temperature readings which indicates the temperature of the device. With three thermal alarms outputs, the DS1620 can also acts as a thermostat. THIGH is driven high if the DS1620 temperature is greater or equal to a user defined temperature TH. TLOW is driven high if the DS1620 temperature is smaller or equal to a user defined temperature TL.

Temperature settings and temperature readings are all communicated to / from the DS1620 over a simple 3-wire interface connected to the Z-CIO 8536 device.

The DS1620 is implemented as follows:

DS1620_RST*	Z-CIO Port A	bit <05>	Reset Input
DS1620_CLK	Z-CIO Port B	bit <01>	Clock Input and standalone Convert Input
DS1620_DQ	Z-CIO Port B	bit <00>	Serial Data Input / Output
DS1620_TCOM	Z-CIO Port B	bit <02>	Interrupt request
DS1620_THIGH	Front Panel LED indicator (OVT)		High Temperature Trigger

The DS1620 is provided on-board to watch over the PowerPC CPU temperature. It allows the generation of alarms when the CPU temperature is exceeding the manufacturer specification. Moreover a Front Panel LED indicates if the temperature is exceeding the high limit. The low and high temperature limits are loaded through the 3-wire interface.

The DS1620 is physically placed on the PCB solder size at the middle of the CPU device giving direct CPU's case temperature

Note Refer to Dallas DS1620 data sheet for complete programming information.

3.11 Local Registers

The sub I/O logic integrates 4 registers implementing control & status bits:

- FPGA loading
- PowerPC Reset control
- Flash EPROM programming

Note These registers are accessible by the PPC processor but the user should take particular care while manipulating them.

3.11.1 LOC_CTL0 Register

PPC Mapped = PPC 0x8140'BD00
PCI I/O Mapped = PCI 0x0140'BD00

bits <31...04>	Not implemented		Reserved.
bit <03>	Reserved	(R)	Always "1"
bit <02>	fpgaLOADED	(R/W)	This control bit allows to assert / deassert the fpgaLOADED control signal. It must be positioned to 1 while the FPGA is loaded
bits <01...00>	Not implemented		Reserved.

3.11.2 LOC_CTL1 Register

PPC Mapped = PPC0x8140'BD04
PCI I/O Mapped = PCI0x0140'BD04

bits <31...04>	Not implemented		Reserved.
bit <03>	Flash_PRG	(R/W)	This control bit enables the Flash EPROM memory programming mode.
bit <02>	FEPROM Size	(R)	This status bit gives information about the size of the Flash EPROM devices installed (0: 8 Mbits, 1: 16 Mbits)
bit <01>	FEPROM1 Sel	(R/W)	Flash EPROM selection for programming.
bit <00>	FEPROM0 Sel	(R/W)	These 2 bits allows to select the Flash EPROM Bank to be programmed: = 00: Disabled = 01: Bank 1 = 10: Bank 2 = 11: Reserved

3.11.4 LOC_CTL2 Register

PPC Mapped = PPC0x8140'BD08
PCI I/O Mapped = PCI0x0140'BD08

bits <31...03>	Not implemented		Reserved.
bit <02>	CPCI_nCONFIG	(W)	Enables the down-line load for the CPCI ALTERA FPGA.
	Reserved	(R)	Always "1".
bit <01>	fpga_DCLK	(W)	Data Clock Down-line load for ALTERA FPGA.
	CPCI_nSTATUS	(R)	Status from the CPCI ALTERA FPGA.
bit <00>	fpga_DATA	(W)	Data Down-line load for the FPGA.
	Reserved	(R)	Always "1".

3.11.4 LOC_CTL3 Register

PPC Mapped = PPC0x8140'BD0C
PCI I/O Mapped = PCI0x0140'BD0C

bits <31...04>	Not implemented		Reserved.
bit <03>	PgmRESET	(W)	This control bit allows to generate a hardware RESET.
bit <02>	dram_4M	(R)	This status bit reflect the DRAM Bank 0 technology: = 0: 16 Mbits DRAM = 1: 64 Mbits DRAM
bit <01>	dram_EDO	(R)	This status bit reflect the DRAM information: = 0: Standard DRAM = 1: EDO DRAM
bit <00>	boot_JUMP	(R)	This status bit reflect state of micro-switch SW2-4. It is used to control the PowerPC boot process = 0: Switch - OFF = 1: Switch - ON

3.11.5 LOC_CTL4 Register

PPC Mapped	= PPC0x8140'BD10		
PCI I/O Mapped	= PCI0x0140'BD10		
bits <31...02>	Not implemented.		Reserved
bit <01>	ATOMIC	(W)	= 1: Set ATOMIC flag = 0: Clear ATOMIC flag Write PPC & TRDY -> Clear ATOMIC Read PPC & Target ABORT -> Clear
bit <00>	SMI	(W)	This control bit allows to activate the NMI interrupt = 1: Set SMI = 0: Clear SMI

3.11.6 LOC_CTL5 Register

This register holds the control bits for the interrupt priority support. This register is updated by the OS general interrupt handler, permits to mask the lower priority interrupt.

PPC Mapped	= PPC0x8140'BD14		
PCI I/O Mapped	= PCI0x0140'BD14		
bits <02...00>	mskLEV	(R/W)	This 3-bit field is defining the mask level.
bit <03>	clrIACK	(R/W)	This bit allows to control the mskLEV update = 0: mskLEV[2:0] not updated = 1: mskLEV[2:0] updated at every IACK cycle with the interrupt level serviced

3.12 Central RESET Logic

The RIOC owns an on-board central RESET logic. This logic is conditioned by:

- Dallas DS1834 Power Monitor (+5 V & 3.3 V)
- Thomson MK48T59 RTC/NVRAM (Battery-backup)
- Front Panel Reset Button
- Front Panel Remote Reset Mini-coax MCX (dip-switch enabled)
- Back Panel Remote Reset (J3 backpanel connector)
- UPI Keyboard and Mouse Controller (Soft Reset)
- RIOC Reset Register (Local Register 3 Soft Reset)
- CompactPCI™ RST signal, when RIOC is Peripheral Slot. (dip-switch disabled)
- CompactPCI™ PRST signal, when RIOC is System Slot (dip-switch enabled)

They generate a signal (ini_RESET*) which resets all the logic and the PowerPC CPU.

Action of the Front Panel MCX mini-coax can be disabled with the switch SW2-1, in this case the MCX input can be used to control one Z-CIO Timer. Remote RESET on the MCX connector requires an active TTL low signal.

CompactPCI™ RST & PRST signals generation can be controlled by SW3-4.

4. ETHERNET INTERFACE

4.1 Ethernet Block Diagram

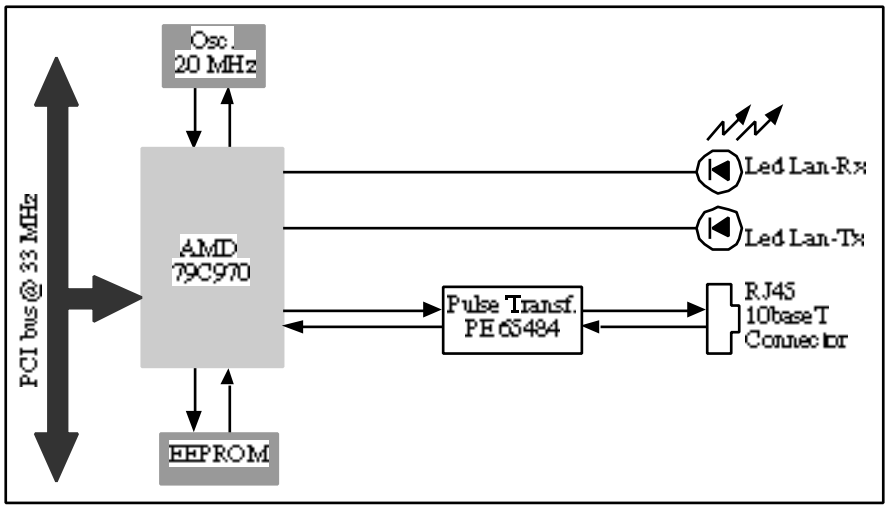

Fig 4.1

The RIOC provides an integrated Ethernet controller with direct connection to 10baseT.

The PC-Net 79C970A is interfaced directly on the local PCI and also to a serial EEPROM storing network parameters.

4.2 PC-Net 79C970A Description

The PC-Net 79C970A Ethernet controller is a highly integrated Ethernet system solution providing the following basic capabilities:

- Single-chip Ethernet controller for PCI local bus.
- Supports ISO 8803-3 (IEEE/ANSI 802.3) and Ethernet standard.
- High-performance Bus Master architecture with integrated DMA buffer management for low CPU and PCI utilization.
- Big Endian and Little-Endian byte alignment.
- Microwire EEPROM interface supports.
- Individual 136-byte transmit and 128-byte receive FIFOs provide frame buffering for increased system latency (~ 100 µs).
- Provides 10baseT transceiver.
- Internal / External loop-back capability.

Note Refer to AMD documentation for complete technical information's and for programming model.

4.3 PCI Slave Mapping

The PC-Net 79C970A Ethernet controller occupies 2 PCI Spaces:

PCI CONFIG Space	256 bytes
PCI I/O Space	64 bytes

4.3.1 PCI Configuration Space

The PC-Net 79C970A Ethernet controller is mapped on the PCI Configuration Space with:

PCI-CONFIG-Space IDSEL(0)

From the PPC, access to the PC-Net 79C970A Configuration Register can be done through:

PPC Mapped	= PPC0x8080'0800	PC-Net 79C970A

4.3.2 PCI I/O Space

After configuration, the PC-Net 79C970A control registers requires a 32-byte address space in the PCI I/O to map its control registers. This mapping is done dynamically at Power-ON by the on-board firmware. The address returned by this dynamic mapping can be read at:

PPC Mapped	= PPC0x8080'0810

4.4 PCI Master

The PC-Net 79C970A Ethernet controller can act as PCI Initiator to fetch / deposit network data. The RIOC PCI arbiter is giving the Ethernet controller the highest priority.

The PC-Net 79C970A can theoretically address all PCI Target devices. Nevertheless only on-board system memory is commonly used.

PCI0x8000'0000 - PCI0x87FF'FFFF	PowerPC System Memory

4.5 LAN Serial EEPROM

The PC-Net 79C970A Ethernet controller attached serial EEPROM is storing:

- ISO 802-3 station physical address and relative PC-Net 79C970A initialization
- CES tracability.

Firmware at the HOST CPU is provided to read and update authorized EEPROM data fields.

79C970 LAN Related Information

The serial EEPROM is storing the Ethernet basic configuration control bits for the PC-Net 79C970A. After an hardware RESET, the PC-Net 79C970A reads out the serial EEPROM for its auto configuration. The EEPROM data structure is built as follows:

0x00 - 0x05	ISO 8802-3 (IEEE/ANSI 802.3)	Station physical address
0x06 - 0x07	0x0000	Reserved
0x08	0x00	Reserved
0x09	Hardware Revision	
0x0A - 0x0B	0x0000	Not used
0x0C - 0x0D	Checksum	
0x0E - 0x0F	0x5757	
0x10 - 0x11	BCR_16 <15...00>	79C970A internal register
0x12 - 0x13	BCR_17 <15...00>	79C970A internal register
0x14 - 0x15	BCR_18 <15...00>	79C970A internal register
0x16 - 0x17	BCR_2 <15...00>	79C970A internal register
0x18 - 0x19	BCR_21 <15...00>	79C970A internal register
0x1A - 0x1E	0x0000	Reserved
0x1F	Checksum	
0x20 - 0x21	0x0000	Reserved

5. COMPACT PCI INTERFACE

5.1 CompactPCI™ Interface Description

The RIOC product is a 6U CompactPCI™ board that can support the CompactPCI™ interfacing as System-Slot as well as Peripheral-Slot. The CompactPCI™ interface implements the bottom J1 and J2 CompactPCI™ connectors and J3 User_I/O connector for back panel implementation. The LocalPCI to CompactPCI™ Bridge is implemented by using a CES proprietary solution around the PLX family chips, an Altera 10K Family FPGA and an Isplsi PLD Logic.

CompactPCI™ Highlights

- Support CompactPCI™ 32-bit @ 33 MHz (PCI Rev. 2.1)
- Support CompactPCI™ System-Slot and Peripheral-Slot
- Support CompactPCI™ Signaling for 5 V (3.3 V available with the Rev. 3 of PLX 9080)
- Support up to 7 CompactPCI™ Peripheral-Slots as CompactPCI™ System-Slot (since PCB n°445.1)
- Support the 4 CompactPCI™ Interrupt Request as CompactPCI™ System-Slot
- Support PCI I/O cycles and all PCI MEMORY cycles Access
- Support PCI Prefetchable-MEMORY cycle Access
- Support Configuration cycle Type_0 and Type_1 (as System Slot)
- Support concurrent Master & Slave direct accesses through dedicated FIFOs
- Provide two DMA channels with concurrent accesses through dedicated FIFOs
- Provide CompactPCI™ address re-mapping through mapping registers for Master and Slave
- Provide Communication Mailboxes and Doorbell registers for multi-processor environment
- Provide I2O Compatible Message Unit
- Support CompactPCI™ ENUM interrupt as System Slot

A library is provided with CES BSPs for VxWorks and Lynx-OS for the complete initialization of the PLX, for CompactPCI™ Master and Slave direct and DMA accesses.

5.2 CompactPCI™ Mapping

The RIOC CompactPCI™ interface supports mapping through register programming for both Master direct and Slave direct accesses. The PLX chip provides registers for the following PCI cycles:

Master Direct

CompactPCI™ Memory Space window (256 Mbytes)
CompactPCI™ I/O Space and Configuration space window (256 Mbytes)

Slave Direct

CompactPCI™ Memory Space window (up to 256 Mbytes)
CompactPCI™ I/O Space window (up to 256 Mbytes)
CompactPCI™ Configuration Type_0

Note: Thanks to the PLX address-remapping registers, the previous windows can be located anywhere into the 4 Gbytes CompactPCI™ address spaces.

The PLX local registers can be accessed at the following addresses:

PLX registers `PPC0xA0F5'0000 -PPC0xA0F5'FFFF`
`PCI0x20F5'0000 -PCI0x20F5'FFFF`

Note: For the All PLX registers description, please refer to the PLX 9080 Data Book (documents available on the Web at: http://www.plxtech.com).

5.2.1 CompactPCI™ Direct Master Cycles

For Master Direct Cycles, the address generated to the CompactPCI™ depends on the initialization of the internal PLX chip registers (Local Address Range Register, Local Base Address Register and PCI Base Address Register), used as descriptor registers to re-map the address into the CompactPCI™ Memory Space and CompactPCI™ I/O Space.

The following values are set by the CES logic (PCI addresses):

Local PCI Memory Base Address = 0x2000'0000
Local PCI I/O & Config Base Address = 0x1000'0000
Local PCI Address Range = 0x1000'0000

Direct Master Accesses Mapping

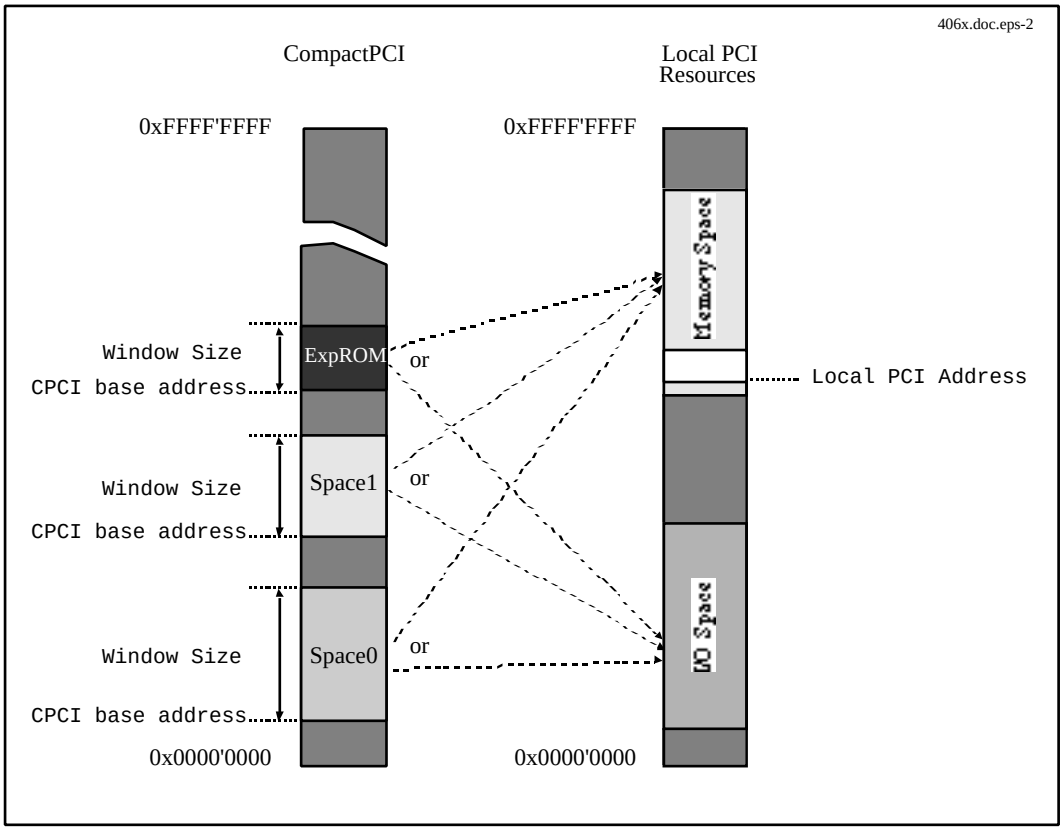

Fig 5.1

5.2.2 CompactPCI™ Mapping

Three windows can be used to access RIOCs resources from the CPCI™ bus. They are referenced as the Space0, Space1 and Expansion ROM. Two additional slave windows, labeled Configuration Register Windows 0 and 1 can be used to access the PCx registers from the CompactPCI™ side.

Each of these windows can be accessed either in Memory space or I/O space and can map local PCI Memory space or I/O space. The different parameters controlling the mapping of the windows are defined by a set of 3 registers (located into the PLX chip) for each window. Thanks to the address re-map, the CompactPCI™ bus Master can map the RIOC Local PCI resources into the 4 Gigabytes CompactPCI™

Memory Space or I/O Space.

The CompactPCI™ slave access allows the external CompactPCI™ agents to access to the RIOC local resources. A dedicated Bi-FIFO (8 Words deep Read and 8 Words deep Write) allows high performance burst accesses.

The base address mapping of the RIOC resources are initialized from the external CompactPCI™ Agent (System-Slot) during the boot of PPCMon or of the OS.

Direct Slave Accesses Mapping

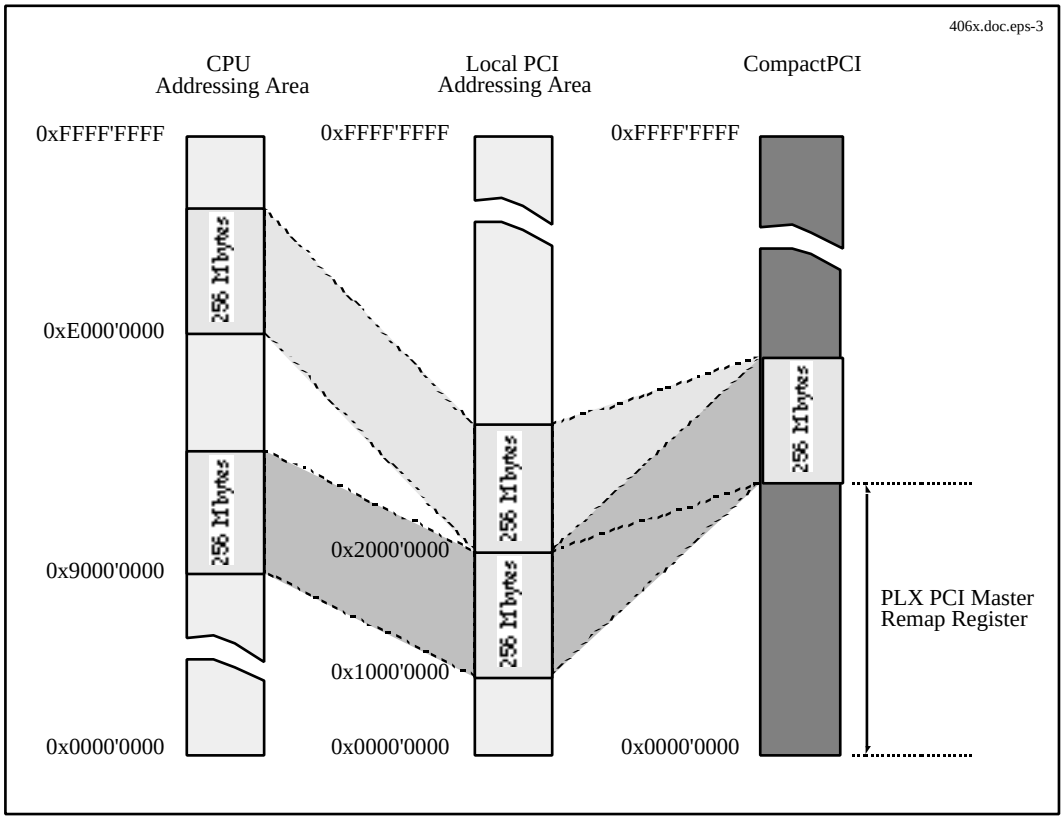

Fig 5.2

5.3 CompactPCI™ Config Cycles

The RIOC interface supports CompactPCI™ Configuration cycles.

As System Slot, the RIOC interface supports CompactPCI™ Configuration cycle Type 0 through the PLX registers programming (Reg. 0xAC). For PLX 9080, the Dev_sel value for the CompactPCI™ slots are the following:

PCI Device	CompactPCI™ Logical slot	Register Value
31	Slot 2	0xA000
30	Slot 3	0x9800
29	Slot 4	0x9000
28	Slot 5	0x8800
27	Slot 6	0x8000
26	Slot 7	0x7800
25	Slot 8	0x7000

As Peripheral Slot, the PLX chip is able to answer to Config Cycle Type 0 since Power ON.

5.4 CompactPCI™ DMA

The PLX chip provides two independent DMA channels, transferring data between the CompactPCI™ and the Local PCI Busses. The programmable DMA Controller supports both chaining and non-chaining transfer modes.

The PLX DMA registers are accessible from both Local PCI and CompactPCI™ bus. The user has to guarantee that DMA will ever access to existing addresses onto the Local PCI, because the PLX chip does not support Local PCI Abort. The hardware will assumes to never lock the system if bad DMA addresses are generated onto the Local PCI.

Note The FPGA allows for bursts of undetermined length. It handles automatically local PCI or CompactPCI™ target disconnect and target retry without software intervention.

5.5 Doorbell Registers

There are two 32 bits Doorbell Interrupt / Status register into the PLX chip. One is assigned to the CompactPCI™ side and the other one to the Local PCI side. The PLX Interrupt request line is connected to the SIC Interrupt controller.

Notes - The RIOC PowerPC can generate interrupt to the CompactPCI™ by writing to PCI doorbell register.

- A CompactPCI™ agent can generate interrupt to the Local PCI by writing to the Local doorbell register.

Doorbell Interrupt

Each bit in the Doorbell registers is individually controlled. Each side can set bits into the associated Doorbell register to generate interrupt on the other side, the interrupt must be cleared by the other side by writing 1 to that bit position.

Notes - Bits in the Local to PCI Doorbell register can only be set by the Local side (by writing 1).

- Bits in the Local to PCI Doorbell register can only be cleared by the PCI side (by writing 1).

5.6 Mailbox Registers

There are eight 32-bit mailbox registers into the PLX chip that can be written and read by both busses. These registers can be used to pass command and status information between the Local Processor and the other CompactPCI™ agents.

Mailbox Interrupt

The PLX Interrupt / Control Register allows enabling Local Interrupt to be generated when an external CompactPCI™ agent writes to any PLX mailbox register. To clear the Local Interrupt, the RIOC Processor has to read the Interrupt / Control register to determine which Mailbox register was accessed and then read to the Mailbox register. Four mailboxes amongst the eight available are able to generate interrupts.

5.7 CompactPCI™ Reset Functions

The RIOC supports the CompactPCI™ PRST and RST signals for System Slot and Peripheral Slot. The incoming PRST Resets request must be enabled by closing the Dip-Switch SW3-4.

5.8 CompactPCI™ Arbiter/Requester

The RIOC interface provides a CompactPCI™ Arbiter / Requester to support both CompactPCI™ System Slot and Peripheral Slot. The arbitration logic is automatically disabled when the RIOC is not in the System Slot of the backplane.

The CES arbiter logic provides a security mechanism when a CompactPCI™ master requests the bus and does not assert the Pci_FRAME signal within 16 Clocks after the end of the previous cycle. The arbiter removes its Grant signal for this master and continues to arbitrate for the next requester or parks the bus if there is no other request.

PLX Internal Arbiter

The PLX chip provides an internal logic to arbitrate between the Direct Master / Slave Access and the 2 DMA channels access that can occur concurrently. The Direct access has higher priority than DMA access.

Dead Lock Condition

A Dead Lock condition occurs when a master on CompactPCI™ tries to access a resource on the Local PCI while a Local PCI master has been granted Local PCI bus for a cycle on the CompactPCI™.

The PLX / FPGA Logic resolves the dead lock conditions.

6. INTERRUPT STRUCTURE

6.1 Interrupt Structure Implementation

The RIOC interrupt structure is based on a CES proprietary ASIC (SIC 6351). All on-board interrupts are routed to the SIC 6351 and dispatched to the PowerPC CPU through the 27-82660 Bridge's device with programmable registers.

6.1.1 PowerPC Interrupt Dispatching

The SIC 6351 allows the association of a relative priority to each interrupt source from 1 to 7. The interrupt controller continuously scans all interrupt sources to find out the pending interrupt of highest priority. Because the PowerPC RISC processor does not incorporate any priority level (as the 68K family), the interrupts are routed to the two IBM 27-82660 Bridge's interrupts signal.

SIC 6351's Interrupt with priority 7 and 6	➠	27-82660 Bridge's NMI*
SIC 6351's Interrupt with priority 5 to 1	➠	27-82660 Bridge's INT*

The SIC 6351 internal prioritization is run by a specific 3-bit field associated with each interrupt source. In case of source pending with the same level, the ACT value assigns the priority. The prioritization is handled during the interrupt acknowledge cycle.

Note Refer also to the IBM 27-82660 Bridge's user manual.

6.1.2 Interrupt Acknowledge

The SIC 6351 internally holds the 42 8-bit vectors associated with the sources. The CPUs are acknowledging their interrupt by reading at a specified PCI address. The SIC 6351 will supply the vector associated with the highest priority currently assigned.

PPC Mapped	= PPC0x8140'B000	(R)
PCI I/O Mapped	= PCI0x0140'B000	(R)

The SIC 6351 is also responding on PCI IACK Cycle with the same behavior as programmed address (PCI0x0140'B000).

6.2 CES SIC 6351 System Interrupt Controller

The SIC 6351 is an ASIC designed by CES to act as a complete interrupt controller. It can control up to 40 interrupt sources and can dispatch them over two CPUs through programmable register options. Each interrupt source can be set to work with an internal Vector (Vector supplied by the internal SIC 6351's SRAM).

Each interrupt source is associated with a Source Input Register (ICRx), containing information such as input polarity, edge or level sensitivity, destination, destination relative priority, masked or enabled.

The SIC 6351 incorporates flags logic for the message passing FIFO, accommodating up to 8 FIFOs. Each of them includes full and empty flags which are able to generate interrupts:

- on empty or not empty conditions
- on full condition (level).
- on full condition (edge).

The internal register access is assured through an 8-bit interface. Only the PCI low byte pciAD <07...00> is wired to the SIC 6351 interface, therefore the SIC 6351 registers are aligned on 32-bit words.

6.2.1 CES SIC 6351 Register Mapping

The SIC 6351 registers occupy 1 Kbyte and are mapped at the following addresses:

PPC Mapped	= PPC0x8140'B400- PPC0x8140'B7FC	(R/W)
PCI I/O Mapped	= PCI0x0140'B400- PCI0x0140'B7FC	(R/W)

The SIC 6351 owns 64 registers:

Base + 0x000	Read Only	Control Status Register	CSR
Base + 0x004 - 0x01C	Read / Write	CES Reserved	
Base + 0x020	Read Only	Source Status Register #0	SSR0
Base + 0x024	Read Only	Source Status Register #1	SSR1
Base + 0x028	Read Only	Source Status Register #2	SSR2
Base + 0x02C	Read Only	Source Status Register #3	SSR3
Base + 0x030	Read Only	Source Status Register #4	SSR4
Base + 0x034	Read / Write	CES Reserved	
Base + 0x038	Write Only	Clear Register #0	CLR0
Base + 0x03C	Write Only	Clear Register #1	CLR1
Base + 0x040 - 0x0FC	Read / Write	CES Reserved	

Base + 0x100	Read / Write	CPCI Interrupt Line A	CPCI_INTA
Base + 0x104	Read / Write	CPCI Interrupt Line B	CPCI_INTB
Base + 0x108	Read / Write	CPCI Interrupt Line C	CPCI_INTC
Base + 0x10C	Read / Write	CPCI Interrupt Line D	CPCI_INTD
Base + 0x110	Read / Write	CES Reserved	
Base + 0x114	Read / Write	CES Reserved	
Base + 0x118	Read / Write	CES Reserved	
Base + 0x11C	Read / Write	CPCI Power Status	CPCI_DEG

Base + 0x120	Read / Write	ICR for FIFO#0 Empty Flag	ICR_FIF0_EF
Base + 0x124	Read / Write	ICR for FIFO#1 Empty Flag	ICR_FIF1_EF
Base + 0x128	Read / Write	ICR for FIFO#2 Empty Flag	ICR_FIF2_EF
Base + 0x12C	Read / Write	ICR for FIFO#3 Empty Flag	ICR_FIF3_EF
Base + 0x130	Read / Write	ICR for FIFO#4 Empty Flag	ICR_FIF4_EF
Base + 0x134	Read / Write	ICR for FIFO#5 Empty Flag	ICR_FIF5_EF
Base + 0x138	Read / Write	ICR for FIFO#6 Empty Flag	ICR_FIF6_EF
Base + 0x13C	Read / Write	ICR for FIFO#7 Empty Flag	ICR_FIF7_EF

Base + 0x140	Read / Write	ICR for FIFO#0 Full Flag	ICR_FIF0_FF
Base + 0x144	Read / Write	ICR for FIFO#1 Full Flag	ICR_FIF1_FF
Base + 0x148	Read / Write	ICR for FIFO#2 Full Flag	ICR_FIF2_FF
Base + 0x14C	Read / Write	ICR for FIFO#3 Full Flag	ICR_FIF3_FF
Base + 0x150	Read / Write	ICR for FIFO#4 Full Flag	ICR_FIF4_FF
Base + 0x154	Read / Write	ICR for FIFO#5 Full Flag	ICR_FIF5_FF
Base + 0x158	Read / Write	ICR for FIFO#6 Full Flag	ICR_FIF6_FF
Base + 0x15C	Read / Write	ICR for FIFO#7 Full Flag	ICR_FIF7_FF

Base + 0x160	Read / Write	CES Reserved	
Base + 0x164	Read / Write	CPCI Power Status	CPCI_FAL
Base + 0x168	Read / Write	CES Reserved	
Base + 0x16C	Read / Write	RTC_IRQ	RTC_IRQ

Base + 0x170	Read / Write	ICR for PMC 1	ICR_PMC1
Base + 0x174	Read / Write	PLX_INTo	PLX_INTo
Base + 0x178	Read / Write	CPCI_MASABO	CPCI_MASABO
Base + 0x17C	Read / Write	ICR for PCIEXT_0	ICR_PCIEXT0
Base + 0x180	Read / Write	CES Reserved	

Base + 0x184	Read / Write	PLX_SERR	PLX_SERR
Base + 0x188	Read / Write	ICR for PCI_SERR	ICR_SERR
Base + 0x18C	Read / Write	ICR for PMC 2	ICR_PMC2
Base + 0x190	Read / Write	ICR for PC-Net 79C970A	ICR_LAN
Base + 0x194	Read / Write	ICR for PCIEXT_1	ICR_PCIEXT1
Base + 0x198	Read / Write	ICR for ZCIO 8536	ICR_ZCIO
Base + 0x19C	Read / Write	ICR for PC87312 Serial #0	ICR_PC_S0
Base + 0x1A0	Read / Write	ICR for PC87312 Serial #1	ICR_PC_S1
Base + 0x1A4 - 0x1FC		CES Reserved	
Base + 0x200 - 0x2FC	Read / Write	Base Address ICOD RAM	CES Reserved
Base + 0x300	Read / Write	Base Address VECTOR RAM	Refer to § 8.2.2

6.2.2 CES SIC 6351 Vector Table Initialization

The SIC 6351 is able to implement vectoring supplied by the peripheral or by the integrated 43 x 8 SRAM. The RIOC supports only vectoring issued by the SIC 6351's vector SRAM.

The SRAM mapping is as follows:

Base + 0x300	Read / Write	Spurious interrupt	ACT = 0x00
Base + 0x304	Read / Write	FIFO#0 Empty interrupt	ACT = 0x01
Base + 0x308	Read / Write	FIFO#1 Empty interrupt	ACT = 0x02
Base + 0x30C	Read / Write	FIFO#2 Empty interrupt	ACT = 0x03
Base + 0x310	Read / Write	FIFO#3 Empty interrupt	ACT = 0x04
Base + 0x314	Read / Write	FIFO#4 Empty interrupt	ACT = 0x05
Base + 0x318	Read / Write	FIFO#5 Empty interrupt	ACT = 0x06
Base + 0x31C	Read / Write	FIFO#6 Empty interrupt	ACT = 0x07
Base + 0x320	Read / Write	FIFO#7 Empty interrupt	ACT = 0x08
Base + 0x324	Read / Write	FIFO#0 Full interrupt	ACT = 0x09
Base + 0x328	Read / Write	FIFO#1 Full interrupt	ACT = 0x0A
Base + 0x32C	Read / Write	FIFO#2 Full interrupt	ACT = 0x0B
Base + 0x330	Read / Write	FIFO#3 Full interrupt	ACT = 0x0C
Base + 0x334	Read / Write	FIFO#4 Full interrupt	ACT = 0x0D
Base + 0x338	Read / Write	FIFO#5 Full interrupt	ACT = 0x0E
Base + 0x33C	Read / Write	FIFO#6 Full interrupt	ACT = 0x0F
Base + 0x340	Read / Write	FIFO#7 Full interrupt	ACT = 0x10
Base + 0x344	Read / Write	PC-Net 79C970A interrupt	ACT = 0x11
Base + 0x348	Read / Write	PMC2* interrupt	ACT = 0x12
Base + 0x350	Read / Write	PC87312 Serial #1 interrupt	ACT = 0x14
Base + 0x354	Read / Write	PC87312 Serial #0 interrupt	ACT = 0x15
Base + 0x358	Read / Write	ZCIO 8536 interrupt	ACT = 0x16
Base + 0x35C	Read / Write	MASABO interrupt	ACT = 0x17
Base + 0x360	Read / Write	PLX_INTo interrupt	ACT = 0x18
Base + 0x36C	Read / Write	INT_A interrupt	ACT = 0x1B
Base + 0x370	Read / Write	INT_B interrupt	ACT = 0x1C
Base + 0x374	Read / Write	INT_C interrupt	ACT = 0x1D
Base + 0x378	Read / Write	INT_D interrupt	ACT = 0x1E
Base + 0x388	Read / Write	PCI SERR* interrupt	ACT = 0x22
Base + 0x38C	Read / Write	PLX SERR* interrupt	ACT = 0x23
Base + 0x398	Read / Write	PMC1* interrupt	ACT = 0x26
Base + 0x3A0	Read / Write	RTC interrupt	ACT = 0x28

The ACT value is used as address for the 42 x 8 vector SRAM and to resolve priority with the same level.

6.2.3 CES SIC 6351 Register Description

This chapter describes the general SIC 6351's internal registers as:

- CSR
- SSR0, SSR1, SSR2, SSR3, SSR4
- CLR0, CLR1

The ICR Registers are individually described in § 6.3 and the Vector table in previous chapter.

SIC 6351 CSR Register

This register holds the ACT_COD of the last interrupt source serviced by a SIC IACK cycle. After a reset, the content is equal to 0x3F. It is updated at each IACK cycle.

PPC Mapped	= PPC0x8140'B400		(R/W)
PCI I/O Mapped	= PCI0x0140'B400		(R/W)
bits <07...06>	"0 0"	(R)	Not implemented, read at 0
bits <05...00>	sicACTCOD <05...00>	(R)	Encoded signature of latest source serviced (see § 6.2.2 to get correspondence with the interrupt source).

After an hardware reset, these register is set to 0x3F.

SIC 6351 SSR0 Register

This register reflects the state of the input cell associated with each interrupt input. The values read in the SSR are not affected by the individual mask / enable bits in the ICR register, but take into account the level / edge options as well as the polarity. A "0" in the status bit reflects a "TRUE" condition.

PPC Mapped	= PPC0x8140'B420		(R/W)
PCI I/O Mapped	= PCI0x0140'B420		(R/W)
bit <07>	FIFO#7 Empty	(R)	FIFO #7 Empty flag
bit <06>	FIFO#6 Empty	(R)	FIFO #6 Empty flag
bit <05>	FIFO#5 Empty	(R)	FIFO #5 Empty flag
bit <04>	FIFO#4 Empty	(R)	FIFO #4 Empty flag
bit <03>	FIFO#3 Empty	(R)	FIFO #3 Empty flag
bit <02>	FIFO#2 Empty	(R)	FIFO #2 Empty flag
bit <01>	FIFO#1 Empty	(R)	FIFO #1 Empty flag
bit <00>	FIFO#0 Empty	(R)	FIFO #0 Empty flag

SIC 6351 SSR1 Register

This register reflects the state of the input cell associated with each interrupt input. The values read in the SSR are not affected by the individual mask / enable bits in the ICR register, but take into account the level / edge options as well as the polarity. A "0" in the status bit reflects a "TRUE" condition.

PPC Mapped	= PPC0x8140'B424		(R/W)
PCI I/O Mapped	= PCI0x0140'B424		(R/W)
bit <07>	FIFO#7 Full	(R)	FIFO #7 Full flag
bit <06>	FIFO#6 Full	(R)	FIFO #6 Full flag
bit <05>	FIFO#5 Full	(R)	FIFO #5 Full flag
bit <04>	FIFO#4 Full	(R)	FIFO #4 Full flag
bit <03>	FIFO#3 Full	(R)	FIFO #3 Full flag
bit <02>	FIFO#2 Full	(R)	FIFO #2 Full flag
bit <01>	FIFO#1 Full	(R)	FIFO #1 Full flag
bit <00>	FIFO#0 Full	(R)	FIFO #0 Full flag

SIC 6351 SSR2 Register

This register reflects the state of the input cell associated with each interrupt input. The values read in the SSR are not affected by the individual mask / enable bits in the ICR register, but take into account the level / edge options as well as the polarity. A "0" in the status bit reflects a "TRUE" condition.

PPC Mapped	= PPC0x8140'B428	(R/W)	
PCI I/O Mapped	= PCI0x0140'B428	(R/W)	
bit <07>	PLX_INTo	(R)	PLX_INTo Interrupt
bit <06>	MASABO	(R)	MASABO Interrupt (FPGA logic error)
bit <05>	CIO_IRQ	(R)	Z-CIO 8536 Interrupt
bit <04>	ICR_PC_S0	(R)	IRQ for Serial #0 Port
bit <03>	ICR_PC_S1	(R)	IRQ for Serial #1 Port
bit <02>	PCIEXT#1	(R)	PCI Extension INT#1
bit <01>	PMC2	(R)	PMC 2 Interrupt
bit <00>	LAN_IRQ	(R)	PC-Net 79C970A Interrupt

SIC 6351 SSR3 Register

This register reflects the state of the input cell associated with each interrupt input. The values read in the SSR are not affected by the individual mask / enable bits in the ICR register, but take into account the level / edge options as well as the polarity. A "0" in the status bit reflects a "TRUE" condition.

PPC Mapped	= PPC0x8140'B42C	(R/W)	
PCI I/O Mapped	= PCI0x0140'B42C	(R/W)	
bit <07..06>	Reserved	(R)	
bit <05>	CPCI_INTD	(R)	CPCI™ Interrupt D
bit <04>	CPCI_INTC	(R)	CPCI™ Interrupt C
bit <03>	CPCI_INTB	(R)	CPCI™ Interrupt B
bit <02>	CPCI_INTA	(R)	CPCI™ Interrupt A
bit <01>	PCIEXT#0	(R)	PCI Extension INT#0
bit <00>	ICR_PC_P0	(R)	Reserved

SIC 6351 SSR4 Register

This register reflects the state of the input cell associated with each interrupt input. The values read in the SSR are not affected by the individual mask / enable bits in the ICR register, but take into account the level / edge options as well as the polarity. A "0" in the status bit reflects a "TRUE" condition.

PPC Mapped	= PPC0x8140'B430	(R/W)	
PCI I/O Mapped	= PCI0x0140'B430	(R/W)	
bit <07>	RTC_IRQ	(R)	RTC Interrupt
bit <06>	CPCI_FAL	(R)	CPCI_FAL Interrupt (power supply fail)
bit <05>	PMC1_INTA	(R)	PMC 1 Interrupt
bit <04>	CPCI_DEG	(R)	CPCI_DEG Interrupt (power supply derate)
bit <03>	CPCI_ENUM	(R)	CPCI_ENUM Interrupt (live insertion IRQ)
bit <02>	PLX_SERR	(R)	PLX_SERR Interrupt (PLX system error)
bit <01>	PCI_SERR	(R)	PCI_SERR
bit <00>	Reserved	(R)	

Note The CompactPCI™ signals FAL, DEG, ENUM are only available for System Slot. ENUM is enabled through the dip switch SW3-3 for the System Slot.

SIC 6351 CLR0 Register

The CLRx register allows to clear the input cells corresponding to interrupts that are or may be set to be edge sensitive under software control. Although the edge sensitive input cell are normally cleared when the corresponding interrupt is serviced by an IACK cycle, a software may be needed for:

- Test purpose
- In Order to execute a software IACK rather than an hardware IACK

Moreover, when changing the polarity of an edge sensitive interrupt, the input cell will be activated and therefore needs to be cleared before the interrupt is enabled.

Each edge sensitive interrupt has a dedicated bit on one of the two CLR registers. To clear the input cell, write the corresponding bit to "1" and then write it to "0".

PPC Mapped	= PPC0x8140'B438	(R/W)	
PCI I/O Mapped	= PCI0x0140'B438	(R/W)	
bit <07>	FIFO#7 Full	(W)	FIFO #7 Full flag Clear command
bit <06>	FIFO#6 Full	(W)	FIFO #6 Full flag Clear command
bit <05>	FIFO#5 Full	(W)	FIFO #5 Full flag Clear command
bit <04>	FIFO#4 Full	(W)	FIFO #4 Full flag Clear command
bit <03>	FIFO#3 Full	(W)	FIFO #3 Full flag Clear command
bit <02>	FIFO#2 Full	(W)	FIFO #2 Full flag Clear command
bit <01>	FIFO#1 Full	(W)	FIFO #1 Full flag Clear command
bit <00>	FIFO#0 Full	(W)	FIFO #0 Full flag Clear command

SIC 6351 CLR1 Register

The CLRx register allows to clear the input cells corresponding to interrupts that are or may be set to be edge sensitive under software control. Although the edge sensitive input cell are normally cleared when the corresponding interrupt is serviced by an IACK cycle, a software may be needed for:

- Test purpose
- In Order to execute a software IACK rather than an hardware IACK

Moreover, when changing the polarity of an edge sensitive interrupt, the input cell will be activated and therefore needs to be cleared before the interrupt is enabled. Each edge sensitive interrupt has a dedicated bit on one of the two CLR registers. To clear the input cell, write the corresponding bit to "1" and then write it to "0".

PPC Mapped	= PPC0x8140'B43C	(R/W)	
PCI I/O Mapped	= PCI0x0140'B43C	(R/W)	
bit <07>	PCI_SERR	(W)	PCI SERR detected
bit <06..03>	Reserved	(W)	
bit <02>	PMC1	(W)	PMC1 Interrupt Clear command
bit <01..00>	Reserved	(W)	

6.3 Interrupt Sources

Each interrupt source is conditioned by an associated ICR register. These registers allow to define options for each sources. Nevertheless, the 42 implemented input cells do not incorporate all options capability.

Generic ICR Register

bit <07>	Enable	(R/W)	Source gate = 0 Interrupt masked. = 1 Interrupt enabled.
bit <06>	Reserved	(R)	Read as "0"
bit <05>	Edge	(R/W)	Edge / Level selection = 0 Level sensitive = 1 Edge sensitive
bit <04>	Polarity	(R/W)	Polarity selection = 0 Active Low = 1 Active High
bit <03>	CPU	(R/W)	CPU destination ("0").
bits <02..00>	Level <02..00>	(R/W)	Destination level. This 3-bit field encodes the relative priority of the considered cell = 000 Disabled = 001 Lower priority = 111 Highest priority

Note The Edge bit can be combined with the Polarity:

Edge	Polarity	
0	0	Level Active Low
0	1	Level Active High
1	0	Negative Edge
1	1	Positive Edge

The ICR's Enable control bit allows to enable / mask the interrupt sources. Enabling a source means that if the input cell is activated, it will generate an interrupt request to the selected CPU with the associated priority specified by Level <02..00>. If the source is masked, it will not generate the interrupt but the status of the cell will be still reflected in the corresponding SSRx Register.

6.3.1 RTC Interrupt

The M48T59 IRQ signal is associated with following SIC6351 registers:

ACT_{rtc}	= 0x28
VEC_{rtc}	= PPC0x8140'B7A0
ICR_{rtc}	= PPC0x8140'B56C

The IRC associated with the RTC's IRQ is defined as follows:

bit <07>	Enable	(R/W)	
bit <06>	Reserved	(R)	
bit <05>	Edge	(R)	Fixed at "1" Edge (negative)
bit <04>	Polarity	(R)	Fixed at "1" Active Low
bit <03>	Reserved	(R)	
bits <02..00>	Level	(R)	Fixed at "7" NMI interrupt

The watchdog logic implemented in the RTC 48T59 is designed to issue a 'system reset' or a NMI interrupt to the CPU if no 'clear' command was not detected during a programmable period of time.

6.3.2 FIFO Interrupts

FIFO Empty / Not Empty Interrupts

The eight FIFO empty interrupts allow the generation of an interrupt on empty or on not-empty conditions.

ACT_{FIF0_EF}	= 0x01		
ACT_{FIF1_EF}	= 0x02		
ACT_{FIF2_EF}	= 0x03		
ACT_{FIF3_EF}	= 0x04		
ACT_{FIF4_EF}	= 0x05		
ACT_{FIF5_EF}	= 0x06		
ACT_{FIF6_EF}	= 0x07		
ACT_{FIF7_EF}	= 0x08		
VEC_{FIF0_EF}	= PPC0x8140'B704	PCI_IO0x0140'B704	(R/W)
VEC_{FIF1_EF}	= PPC0x8140'B708	PCI_IO0x0140'B708	(R/W)
VEC_{FIF2_EF}	= PPC0x8140'B70C	PCI_IO0x0140'B70C	(R/W)
VEC_{FIF3_EF}	= PPC0x8140'B710	PCI_IO0x0140'B710	(R/W)
VEC_{FIF4_EF}	= PPC0x8140'B714	PCI_IO0x0140'B714	(R/W)
VEC_{FIF5_EF}	= PPC0x8140'B718	PCI_IO0x0140'B718	(R/W)
VEC_{FIF6_EF}	= PPC0x8140'B71C	PCI_IO0x0140'B71C	(R/W)
VEC_{FIF7_EF}	= PPC0x8140'B720	PCI_IO0x0140'B720	(R/W)
ICR_{FIF0_EF}	= PPC0x8140'B520	PCI_IO0x0140'B520	(R/W)
ICR_{FIF1_EF}	= PPC0x8140'B524	PCI_IO0x0140'B524	(R/W)
ICR_{FIF2_EF}	= PPC0x8140'B528	PCI_IO0x0140'B528	(R/W)
ICR_{FIF3_EF}	= PPC0x8140'B52C	PCI_IO0x0140'B52C	(R/W)
ICR_{FIF4_EF}	= PPC0x8140'B530	PCI_IO0x0140'B530	(R/W)
ICR_{FIF5_EF}	= PPC0x8140'B534	PCI_IO0x0140'B534	(R/W)
ICR_{FIF6_EF}	= PPC0x8140'B538	PCI_IO0x0140'B538	(R/W)
ICR_{FIF7_EF}	= PPC0x8140'B53C	PCI_IO0x0140'B53C	(R/W)

All eight ICRs have the same bit allocation:

bit <07>	Enable	(R/W)	Source gate	
bit <06>	Reserved	(R)	No action	
bit <05>	Edge	(R)	Edge / Level selection	Fixed at "0" Level sensitive
bit <04>	Polarity	(R)	Polarity selection	
bit <03>	CPU	(R/W)	CPU destination	Fixed at "0"
bits <02...00>	Level <02...00>	(R/W)	Destination level	

FIFO Full Interrupts

The eight FIFO full interrupts allow the generation of an interrupt only on a full condition.

ACT_{FIF0_FF}	= 0x09
ACT_{FIF1_FF}	= 0x0A
ACT_{FIF2_FF}	= 0x0B
ACT_{FIF3_FF}	= 0x0C
ACT_{FIF4_FF}	= 0x0D
ACT_{FIF5_FF}	= 0x0E
ACT_{FIF6_FF}	= 0x0F
ACT_{FIF7_FF}	= 0x10

VEC_{FIF0_FF}	= PPC 0x8140'B724	PCI_IO 0x0140'B724	(R/W)
VEC_{FIF1_FF}	= PPC 0x8140'B728	PCI_IO 0x0140'B728	(R/W)
VEC_{FIF2_FF}	= PPC 0x8140'B72C	PCI_IO 0x0140'B72C	(R/W)
VEC_{FIF3_FF}	= PPC 0x8140'B730	PCI_IO 0x0140'B730	(R/W)
VEC_{FIF4_FF}	= PPC 0x8140'B734	PCI_IO 0x0140'B734	(R/W)
VEC_{FIF5_FF}	= PPC 0x8140'B738	PCI_IO 0x0140'B738	(R/W)
VEC_{FIF6_FF}	= PPC 0x8140'B73C	PCI_IO 0x0140'B73C	(R/W)
VEC_{FIF7_FF}	= PPC 0x8140'B740	PCI_IO 0x0140'B740	(R/W)
ICR_{FIF0_FF}	= PPC 0x8140'B540	PCI_IO 0x0140'B540	(R/W)
ICR_{FIF1_FF}	= PPC 0x8140'B544	PCI_IO 0x0140'B544	(R/W)
ICR_{FIF2_FF}	= PPC 0x8140'B548	PCI_IO 0x0140'B548	(R/W)
ICR_{FIF3_FF}	= PPC 0x8140'B54C	PCI_IO 0x0140'B54C	(R/W)
ICR_{FIF4_FF}	= PPC 0x8140'B550	PCI_IO 0x0140'B550	(R/W)
ICR_{FIF5_FF}	= PPC 0x8140'B554	PCI_IO 0x0140'B554	(R/W)
ICR_{FIF6_FF}	= PPC 0x8140'B558	PCI_IO 0x0140'B558	(R/W)
ICR_{FIF7_FF}	= PPC 0x8140'B55C	PCI_IO 0x0140'B55C	(R/W)

The eight ICRs have the same bit allocation:

bit <07>	Enable	(R/W)	Source gate	
bit <06>	Reserved	(R)	No action	
bit <05>	Edge	(R/W)	Edge / Level selection	
bit <04>	Polarity	(R)	Polarity selection	Fixed at "1" Active High, only FULL condition
bit <03>	CPU	(R/W)	CPU destination	Fixed at "0"
bits <02..00>	Level <02...00>	(R/W)	Destination level	

6.3.3 Ethernet Interrupt

The PC-Net 79C970A interrupt:

ACT_{net}	= 0x11			
VEC_{net}	= PPC 0x8140'B744		PCI_IO 0x0140'B744	(R/W)
ICR_{net}	= PPC 0x8140'B590		PCI_IO 0x0140'B590	(R/W)
bit <07>	Enable	(R/W)	Source gate	
bit <06>	Reserved	(R)	No action	
bit <05>	Edge	(R)	Edge / Level selection	Fixed at "0" Level sensitive
bit <04>	Polarity	(R)	Polarity selection.	Fixed at "0" Active Low
bit <03>	CPU	(R/W)	CPU destination	Fixed at "0"
bits <02..00>	Level <02...00>	(R/W)	Destination level	

Note Refer to AMD 79C970A user's manual for programming guide.

6.3.4 PMC2 Interrupt

ACT_{ext}	= 0x12			
VEC_{ext}	= PPC0x8140'B748		PCI_IO0x0140'B748	(R/W)
ICR_{ext}	= PPC0x8140'B58C		PCI_IO0x0140'B58C	(R/W)
bit <07>	Enable	(R/W)	Source gate	
bit <06>	Reserved	(R)	No action	
bit <05>	Edge	(R)	Edge / Level selection	Must be at "0" Level sensitive
bit <04>	Polarity	(R)	Polarity selection	Must be at "0" Active Low
bit <03>	CPU	(R/W)	CPU destination	Fixed at "0"
bits <02...00>	Level <02...00>	(R/W)	Destination level	

6.3.5 Serial Line Interrupts

The NS PC87312 issues three different interrupt lines.

ACT_{pc_s0}	= 0x15			
ACT_{pc_s1}	= 0x14			
VEC_{pc_s0}	= PPC0x8140'B754		PCI_IO0x0140'B754	(R/W)
VEC_{pc_s1}	= PPC0x8140'B750		PCI_IO0x0140'B750	(R/W)
ICR_{pc_s0}	= PPC0x8140'B59C		PCI_IO0x0140'B59C	(R/W)
ICR_{pc_s1}	= PPC0x8140'B5A0		PCI_IO0x0140'B5A0	(R/W)

The three ICRs have the same bit allocation:

bit <07>	Enable	(R/W)	Source gate	
bit <06>	Reserved	(R)	No action	
bit <05>	Edge	(R)	Edge / Level selection	Fixed at "0" Level sensitive
bit <04>	Polarity	(R)	Polarity selection	Fixed at "0" Active Low
bit <03>	CPU	(R/W)	CPU destination	Fixed at "0"
bits <02...00>	Level <02...00>	(R/W)	Destination level	

Note Refer to National PC 87312 user's manual for programming guide.

6.3.6 Z-CIO 8536 Interrupt

The Z-CIO 8536 interrupt:

ACT_{cio}	= 0x16			
VEC_{cio}	= PPC0x8140'B758		PCI_IO0x0140'B758	(R/W)
ICR_{cio}	= PPC0x8140'B598		PCI_IO0x0140'B598	(R/W)
bit <07>	Enable	(R/W)	Source gate	
bit <06>	Reserved	(R)	No action	
bit <05>	Edge	(R)	Edge / Level selection	Fixed at "0" Level sensitive
bit <04>	Polarity	(R)	Polarity selection	Fixed at "0" Active Low
bit <03>	CPU	(R/W)	CPU destination	Fixed at "0"
bits <02...00>	Level <02...00>	(R/W)	Destination level	

Notes - Refer to Zilog Z-CIO 8536 user's manual for programming guide.

- The Z-CIO 8536 Port A bit <07> and <06> are used to control the keyboard and mouse interrupts from the UPI82C42.

6.3.7 MASABO Interrupt

The MASABO interrupt:

ACT_{masabo}	= 0x17			
VEC_{masabo}	= PPC0x8140'B75C		PCI_IO0x0140'B75C	(R/W)
ICR_{masabo}	= PPC0x8140'B578		PCI_IO0x0140'B578	(R/W)
bit <07>	Enable	(R/W)	Source gate	
bit <06>	Reserved	(R)	No action	
bit <05>	Edge	(R)	Edge / Level selection	Fixed at "0" Level sensitive
bit <04>	Polarity	(R)	Polarity selection	Fixed at "0" Active Low
bit <03>	CPU	(R/W)	CPU destination	Fixed at "0"
bits <02...00>	Level <02...00>	(R/W)	Destination level	

6.3.8 PLX_INTo Interrupt

The PLX_INTo interrupt:

ACT_{into}	= 0x18			
VEC_{into}	= PPC0x8140'B760		PCI_IO0x0140'B760	(R/W)
ICR_{into}	= PPC0x8140'B574		PCI_IO0x0140'B574	(R/W)
bit <07>	Enable	(R/W)	Source gate	
bit <06>	Reserved	(R)	No action	
bit <05>	Edge	(R)	Edge / Level selection	Fixed at "0" Level sensitive
bit <04>	Polarity	(R)	Polarity selection	Fixed at "0" Active Low
bit <03>	CPU	(R/W)	CPU destination	Fixed at "0"
bits <02...00>	Level <02...00>	(R/W)	Destination level	

6.3.9 INT_A Interrupt

The INT_A interrupt:

ACT_{inta}	= 0x1B			
VEC_{inta}	= PPC0x8140'B76C		PCI_IO0x0140'B76C	(R/W)
ICR_{inta}	= PPC0x8140'B500		PCI_IO0x0140'B500	(R/W)
bit <07>	Enable	(R/W)	Source gate	
bit <06>	Reserved	(R)	No action	
bit <05>	Edge	(R)	Edge / Level selection	Fixed at "0" Level sensitive
bit <04>	Polarity	(R)	Polarity selection	Fixed at "0" Active Low
bit <03>	CPU	(R/W)	CPU destination	Fixed at "0"
bits <02...00>	Level <02...00>	(R/W)	Destination level	

6.3.10 INT_B Interrupt

The INT_B interrupt:

ACT_{intb}	= 0x1C			
VEC_{intb}	= PPC 0x8140'B770		PCI_IO 0x0140'B770	(R/W)
ICR_{intb}	= PPC 0x8140'B504		PCI_IO 0x0140'B504	(R/W)
bit <07>	Enable	(R/W)	Source gate	
bit <06>	Reserved	(R)	No action	
bit <05>	Edge	(R)	Edge / Level selection	Fixed at "0" Level sensitive
bit <04>	Polarity	(R)	Polarity selection	Fixed at "0" Active Low
bit <03>	CPU	(R/W)	CPU destination	Fixed at "0"
bits <02...00>	Level <02...00>	(R/W)	Destination level	

6.3.11 INT_C Interrupt

The INT_C interrupt:

ACT_{intc}	= 0x1D			
VEC_{intc}	= PPC 0x8140'B774		PCI_IO 0x0140'B774	(R/W)
ICR_{intc}	= PPC 0x8140'B508		PCI_IO 0x0140'B508	(R/W)
bit <07>	Enable	(R/W)	Source gate	
bit <06>	Reserved	(R)	No action	
bit <05>	Edge	(R)	Edge / Level selection	Fixed at "0" Level sensitive
bit <04>	Polarity	(R)	Polarity selection	Fixed at "0" Active Low
bit <03>	CPU	(R/W)	CPU destination	Fixed at "0"
bits <02...00>	Level <02...00>	(R/W)	Destination level	

6.3.12 INT_D Interrupt

The INT_D interrupt:

ACT_{intd}	= 0x1E			
VEC_{intd}	= PPC 0x8140'B778		PCI_IO 0x0140'B778	(R/W)
ICR_{intd}	= PPC 0x8140'B50C		PCI_IO 0x0140'B50C	(R/W)
bit <07>	Enable	(R/W)	Source gate	
bit <06>	Reserved	(R)	No action	
bit <05>	Edge	(R)	Edge / Level selection	Fixed at "0" Level sensitive
bit <04>	Polarity	(R)	Polarity selection	Fixed at "0" Active Low
bit <03>	CPU	(R/W)	CPU destination	Fixed at "0"
bits <02...00>	Level <02...00>	(R/W)	Destination level	

6.3.13 PCI SERR

ACT_{serr}	= 0x22			
VEC_{serr}	= PPC 0x8140'B788		PCI_IO 0x0140'B788	(R/W)
ICR_{serr}	= PPC 0x8140'B588		PCI_IO 0x0140'B588	(R/W)
bit <07>	Enable	(R/W)	Source gate	
bit <06>	Reserved	(R)	No action	
bit <05>	Edge	(R)	Edge / Level selection	Fixed at "1" Edge sensitive
bit <04>	Polarity	(R)	Polarity selection	Fixed at "0" Active Low
bit <03>	CPU	(R/W)	CPU destination	Fixed at "0"
bits <02...00>	Level <02...00>	(R/W)	Destination level	

6.3.14 PLX_SERR

ACT_{serr}	= 0x23			
VEC_{serr}	= PPC 0x8140'B78C		PCI_IO 0x0140'B78C	(R/W)
ICR_{serr}	= PPC 0x8140'B584		PCI_IO 0x0140'B584	(R/W)
bit <07>	Enable	(R/W)	Source gate	
bit <06>	Reserved	(R)	No action	
bit <05>	Edge	(R)	Edge / Level selection	Must be at "0" Level sensitive
bit <04>	Polarity	(R)	Polarity selection	Must be at "0" Active Low
bit <03>	CPU	(R/W)	CPU destination	Fixed at "0"
bits <02...00>	Level <02...00>	(R/W)	Destination level	

6.3.15 PMC1 Interrupt

ACT_{ext}	= 0x26			
VEC_{ext}	= PPC 0x8140'B798		PCI_IO 0x0140'B798	(R/W)
ICR_{ext}	= PPC 0x8140'B570		PCI_IO 0x0140'B570	(R/W)
bit <07>	Enable	(R/W)	Source gate	
bit <06>	Reserved	(R)	No action	
bit <05>	Edge	(R)	Edge / Level selection	Must be at "0" Level sensitive
bit <04>	Polarity	(R)	Polarity selection	Must be at "0" Active Low
bit <03>	CPU	(R/W)	CPU destination	Fixed at "0"
bits <02...00>	Level <02...00>	(R/W)	Destination level	

6.3.16 CPCI™ Interrupts

The CompactPCI™ interrupts INTA A, B, C and D, are connected to the SIC interrupt controller when the RIOC 406x board is plugged into the CompactPCI™ system-slot (ref. to chapter 5).

7. RIOC PCI EXTENSIONS

7.1 PMC PCI Mezzanine Module

The PMC is a standard PCI Mezzanine Card defined by the IEEE P1386. These mezzanines are mechanically and electrically defined to be used as CompactPCI™ on-board extensions.

The RIOC holds two 32-bit PCI PMC slots which can be equipped with two single PMCs or with a double size PMC.

Refer to: IEEE P1386 Draft 2.0 - Common Mezzanine Card Specification (CMC) -
IEEE P1386 Draft 2.0 - PCI Mezzanine Card Specification (PMC) -

7.1.1 Mechanical

The RIOC PMC implementation follows the IEEE P1386 Draft 2.0 recommendation.

7.1.2 Power-Supply

The RIOC supplies the following Power supply for the two PMCs.

+5 VI/O	Max	4 A
+5 V	Max	6 A
+3.3 V	Max	9 A
+12 V	Max	1 A
-12 V	Max	1 A

The +3.3 V, +5 V, +12 V and -12 V are directly taken from the CompactPCI™ power supply. The two PMCs shall not exceed the CompactPCI™ specification.

The IEEE P1386 Draft 2.0 - Common Mezzanine Card Specification (CMC) allows a maximum single PMC Power dissipation of 7.5 W (6 W bottom, 1.5 W top). The RIOC accepts higher power dissipation for the two PMCs provided that the corresponding adapted forced air cooling is supplied.

7.1.3 PMCs BUSMODE

The 4 BUSMODE signal are routed to each PMC.

The RIOC drives and monitors the BUSMODE signal through the on-board Z-CIO 8536 Port B (refer to § 3.7.3), allowing the firmware to access these information. These lines are put in a known state at Power ON with pull down / pull up resistors.

BUSMODE[4:2]# shall be driven by the Z-CIO 8536 and are connected to the 2 PMCs.
BUSMODE[1]# of each PMC is received by the Z-CIO 8536

7.1.4 PMCs Configuration

The 2 PMCs PCI configuration space are selected as follows:

IDSEL PMC#1 = IDSEL Slot 2 (pciAD13).
IDSEL PMC#2 = IDSEL Slot 1 (pciAD12).

Notes - Refer to § 2.4.

- The two PMCs interrupt INTA# are directly routed to the SIC 6351 (refer to chapter 6).

- Only the INTA# interrupt is routed to the Central interrupt controller SIC 6351. The other 3 PMC interrupts are only connected between the 2 PMCs.

7.1.5 PMC Connectors

The RIOC implements six 64-pin connectors supplying the PCI to the two PMCs

JN11 / JN21

1	TCK	-12V	2
3	GND	PMC_INTA_	4
5	INTB	INTC	6
7	BUSMODE1#	+5V	8
9	INTD	Reserved	10
11	GND	Reserved	12
13	CLK	GND	14
15	GND	PMCGNT_	16
17	PMCREQ_	+5V	18
19	VI/O	AD31	20
21	AD28	AD27	22
23	AD25	GND	24
25	GND	C/BE3_	26
27	AD22	AD21	28
29	AD19	+5V	30
31	Not Used	AD17	32
33	FRAME_	GND	34
35	GND	IRDY_	36
37	DEVSEL_	+5V	38
39	GND	LOCK_	40
41	SDONE	SBO	42
43	PAR	GND	44
45	VI/O	AD15	46
47	AD12	AD11	48
49	AD09	+5V	50
51	GND	C/BE0_	52
53	AD06	AD05	54
55	AD04	GND	56
57	VI/O	AD03	58
59	AD02	AD01	60
61	AD00	+5V	62
63	GND	REQ64 (*)	64

(*) with 10 KΩ pull-up.

JN12 / JN22

1	+12V	TRST_	2
3	TMS	TDO	4
5	TDI	GND	6
7	GND	Reserved	8
9	Reserved	Reserved	10
11	BUSMODE2#	+3.3V	12
13	RST_	BUSMODE3#	14
15	+3.3V	BUSMODE4#	16
17	Reserved	GND	18
19	AD30	AD29	20
21	GND	AD26	22
23	AD24	+3.3V	24
25	IDSEL	AD23	26
27	+3.3V	AD20	28
29	AD18	GND	30
31	AD16	C/BE2_	32
33	GND	Reserved	34
35	TRDY_	+3.3V	36
37	GND	STOP_	38
39	PERR_	GND	40

41	+3.3V	SERR_	42
43	C/BE1_	GND	44
45	AD14	AD13	46
47	GND	AD10	48
49	AD08	+3.3V	50
51	AD07	Reserved	52
53	+3.3V	Reserved	54
55	Reserved	GND	56
57	Reserved	Reserved	58
59	GND	Reserved	60
61	ACK64 (*)	+3.3V	62
63	GND	Reserved	64

(*) with 10 KΩ pull-up.

Note JTAG signals are connected between the 2 PMCs.

7.2 PCI Extension Connector

The RIOC implements a 60-pin connector allowing to extend the local PCI to a second PCI segment. This second slot can be used to implement specific interface or for a PMC carrier. The two PCI Extension's interrupts are routed to the SIC 6351.

The PCI Extension configuration space is selected by:

IDSEL PCI_EXT = IDSEL Slot 3 (pciAD14).

Note The PMC Extension is defined to interface to a PCI / PCI Bridge or to connect the CES debugging tool.

Connector type: AMP Microstrip 121340-2 female

Signal Name	Number	Number	Signal Name
pciCLK	1	2	Not used
GND	3	4	Not used
pciAD0	5	6	pciAD1
pciAD2	7	8	pciAD3
pciAD4	9	10	pciAD5
pciAD6	11	12	pciAD7
pciAD8	13	14	pciAD9
pciAD10	15	16	pciAD11
pciAD12	17	18	pciAD13
pciAD14	19	20	pciAD15
pciAD16	21	22	pciAD17
pciAD18	23	24	pciAD19
pciAD20	25	26	pciAD21
pciAD22	27	28	pciAD23
pciAD24	29	30	pciAD25
pciAD26	31	32	pciAD27
pciAD28	33	34	pciAD29
pciAD30	35	36	pciAD31
Not used	37	38	Not used
pciCBE0	39	40	pciCBE1
pciCBE2	41	42	pciCBE3
pciRST#	43	44	pciDEVSEL#
pciFRAME#	45	46	pciTRDY#
pciIRDY#	47	48	pciSTOP#
pciPAR	49	50	pciSERR#
pciPERR#	51	52	pciLOCK#
pciIDSEL	53	54	
pciBGNT	55	56	pciBREQ
extINT#0	57	58	extINT#1
Not used	59	60	Not used

7.3 J3 User I/O Connector

19	RESET#	NC	NC	NC	NC	GND
18	NC	NC	NC	NC	NC	GND
17	NC	NC	sio_PD0	sio_PD1	sio_PD2	GND
16	sio_PD3	sio_PD4	sio_PD5	sio_PD6	sio_PD7	GND
15	sio_PE	sio_BUSY	sio_SELECT	sio_ERR*	sio_ACK*	GND
14	3.3V	3.3V	3.3V	5V	5V	GND
13	Jn24_5	Jn24_4	Jn24_3	Jn24_2	Jn24_1	GND
12	Jn24_10	Jn24_9	Jn24_8	Jn24_7	Jn24_6	GND
11	Jn24_15	Jn24_14	Jn24_13	Jn24_12	Jn24_11	GND
10	Jn24_20	Jn24_19	Jn24_18	Jn24_17	Jn24_16	GND
9	Jn24_25	Jn24_24	Jn24_23	Jn24_22	Jn24_21	GND
8	Jn24_30	Jn24_29	Jn24_28	Jn24_27	Jn24_26	GND
7	Jn24_35	Jn24_34	Jn24_33	Jn24_32	Jn24_31	GND
6	Jn24_40	Jn24_39	Jn24_38	Jn24_37	Jn24_36	GND
5	Jn24_45	Jn24_44	Jn24_43	Jn24_42	Jn24_41	GND
4	Jn24_50	Jn24_49	Jn24_48	Jn24_47	Jn24_46	GND
3	Jn24_55	Jn24_54	Jn24_53	Jn24_52	Jn24_51	GND
2	Jn24_60	Jn24_59	Jn24_58	Jn24_57	Jn24_56	GND
1	NC	Jn24_64	Jn24_63	Jn24_62	Jn24_61	GND
Pin	A	B	C	D	E	F

8. STATIC OPTIONS

8.1 Front Panel Description

8.1.1 Front Panel Connectors and Switches

The RIOC provides the following Front Panel connectors and switches:

P4	10baseT	RJ45 Modular Jack 8 pins female
P8	RS 232C channel 1	ITT Cannon MDSM-18 P E-Z7 (bottom)
P8	RS 232C channel 2	ITT Cannon MDSM-18 P E-Z7 (top)
SW1	RESET push-button	C & K EP 12
MCX	Remote RESET or FP Timer / Interrupt	MCX Radial R113665 or AMP 829560-2

8.1.2 LED Indicator

The RIOC's LED display gives visual information of the most current status of the unit.

SL1	Lit ON when the RIOC is System Slot
CMA	Lit ON during master direct access on CompactPCI™ (Read or Write)
CSL	Lit ON during slave direct access from CompactPCI™ (Read or Write)
DMA	Lit ON during DMA access from or to CompactPCI™ (both channels). Not stretched.
LRx	Lit ON when the LAN controller receives Data from Ethernet
LTx	Lit ON when the LAN controller transmits Data on Ethernet
OVT	Lit ON if the CPU is exceeding the temperature limit fixed in the DS1620 Digital Thermometer
BLO	Software controlled LED (Z-CIO port A bit <04>)

8.2 Mechanics and PCB layout

Mother Board

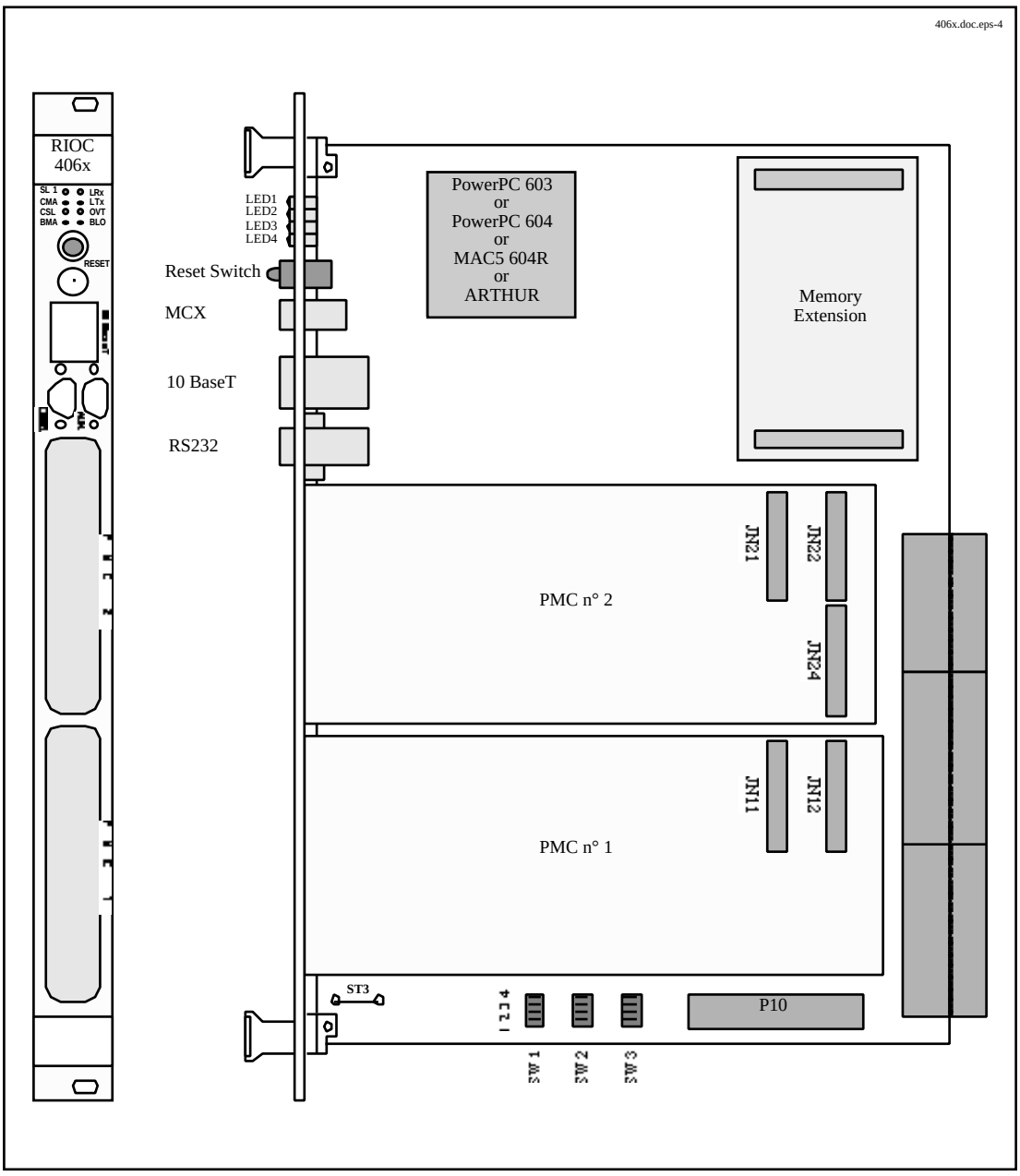

Fig 8.1

8.3 Jumpers and Micro switches

The RIOC incorporates 12 static options distributed over 3 4-position SMT micro switches (labeled SW1, SW2, SW3).

SMT micro switches SW1

SW1-1	Reserved
SW1-2	Reserved
SW1-3	Reserved
SW1-4	Reserved

SMT micro switches SW2

SW2-1	FPMCX_RST	When 'ON', the front panel MCX mini-coax input generates a RIOC RESET
SW2-2	EN_PMCIO	Reserved
SW2-3	Boot_DEBUG	When 'ON', the CPU will boot on the CES proprietary EPROM PMC module. It allows to program the Flash EPROM for the first time
SW2-4	Boot_JUMP	When 'ON', the CPU will stop after the primary boot. The state of this switch is reflected in LOC_CTL#3 register, allowing the CPU to abort its bootstrap process

SMT micro switches SW3

SW3-1	ROM_SHORT	When 'ON', the PLX initializes for the Short ROM
SW3-2	CPCI_KEY	When 'ON', the PLX drives 3.3 V CompactPCI™
SW3-3	ENUM	Should be 'ON' only for CompactPCI™ System Slot (1)
SW3-4	CPCI_ENRST	When 'ON', CompactPCI™ RST or PRST input are enabled

Jumper ST3

Jumper ST3 (at the bottom-front of the board) must be plugged during handling of the board. This jumper connects the board's mechanical ground (SHIELD) to the board's logical ground (GND).

8.4 RIOC Connectors

8.4.1 Serial Port RS232

Connector Type ITT Cannon MDSM double decker MDSM-18 P E-Z7).

The pins assignment is identical to the standard DB9.

pin n° 1	DCD	Data carrier detect
pin n° 2	SIN	Serial input
pin n° 3	SOUT	Serial output
pin n° 4	DTR	Data terminal ready
pin n° 5	GND	Signal ground
pin n° 6	DSR	Data set ready
pin n° 7	RTS	Request to send
pin n° 8	CTS	Clear to send
pin n° 9	RI	Ring indicator

8.4.2 10baseT Connector

The RIOC implements a 10baseT Ethernet connector located on the Front Panel.

Connector Type RJ45 Modular Jack 8-pin female (AMP 215877-1 or COMPONA 327-388-1)

MAU Function	*RJ45 pin*
TD+	1
TD-	2
RD+	3
NC1	4
NC2	5
RD-	6
NC3	7
NC4	8

8.4.3 MCX Connector

The Front Panel MCX can be used as a RESET or as an interrupt or as a Timer Trigger / Gate / Count (50 Ω TTL input, active LOW, minimum pulse length: 1 µs). The switch 2-1 allows to disable the RESET function if the Timer Trigger / Gate / Count is used. The logic signal is inverted between the MCX and the Z-CIO inputs.

Connector Type MCX (Radial R113665 or AMP 829560-2)

8.5 PCB Ground Separation

The RIOC's PCB integrates two separate ground to fulfill EMI/RFI requirement. The isolation between the shield ground and the logical ground requires that the VME Front Panel is connected to 0 V. To assure that the shield ground is not floating.

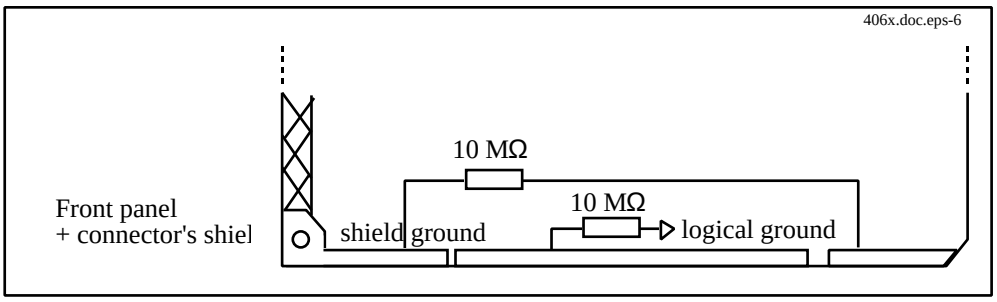

Fig 8.3

The metallic parts of Front Panel connectors are connected to the shield ground, as well as the ESD protection devices coupled with the IO signals.

8.6 Document References

PowerPC 603	User's Manual	IBM MPR603UMU-01
PowerPC 604	User's Manual	IBM MPR604UMU-01
27-82660 PCI Bridge	User's Manual	IBM MPR660UMU-01
PCNEt 79C970A	PCI Ethernet Controller UM	AMD
MK48T59	RTC and NVRAM DS	SGS THOMSON
PC87312	Super I/O DS	NS
Z-CIO 8536	Counter/Timer and I/O	ZILOG
MAX 214	RS232 Transceiver	MAXIM
MAX 662	+12 V Flash Memory Programming	MAXIM
28F008	Flash EPROM	INTEL
29F016	Flash EPROM	AMD
DS1620	Digital Thermometer	DALLAS
PCI	Specification Rev 2.0	PCIG
PMC	Specification P1386 Draft 2.0	IEEE
Monitor	PPCMon Monitor and Debugger	CES