User Manual

IP-Thermistor

16 Channel Thermistor
Temperature Reading
IndustryPack®

Manual Revision:4 7/28/99

Hardware Revision: B

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16 Channel Thermistor
Temperature Reading
IndustryPack®

The electronic equipment described herein generates, uses, and can radiate radio frequency energy. Operation of this equipment in a residential area is likely to cause radio interference, in which case the user, at his own expense, will be required to take whatever measures may be required to correct the interference.

GreenSpring's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of SBS GreenSpring.

This product has been designed to operate with IndustryPack carriers and compatible user-provided equipment. Connection of incompatible hardware is likely to cause serious damage.

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Product Description

IP-Thermistor is a precision, low cost, temperature reading IndustryPack for 16 channels of thermistor based sensors. It is a complete IP, providing a current source, multiplexers, buffers and amplifier, 12-bit analog to digital converter, factory-set offset and gain adjustment circuitry, timing and interrupt logic, and IP bus interface. IP-Thermistor is a single-high IndustryPack.

Thermistors are a popular temperature sensor available from many sources, including: YSI, Ketema, Philips, Rosemount, Koa-Speer, Therm-O-Disc. See the list of suppliers including addresses at the end of this section.

Thermistors are available over a wide range of cost v. accuracy, from a few cents per sensor to ultra-stable sensors. (NASA approved with 0.05°C repeatability from YSI; repeatability to 0.2°C from Ketema.) A wide variety of mounting configurations, probe styles, and wire type are available supporting use in cost sensitive OEM equipment, high-reliability medical instrumentation, or rugged exposed industrial environments. Thermistors are negative temperature coefficient resistors. They have a large temperature coefficient, typically 1,290 ? /°C near room temperature. This permits their use in two-wire or three-wire configurations since wire resistance is negligible. IP-Thermistor supports both 2-wire and 3-wire configurations.

To measure temperature using a thermistor, a small stable current is passed through the sensor. Then the voltage drop is read using a buffered Analog to Digital Converter (ADC). IP-Thermistor uses a switched, highly stable, 1 mA current source. (Other current source values are available on special order). The current source is switched among the sixteen sensors, minimizing self-heating. The current source may be switched off to all sensors via software. A 12-bit ADC with an integral sample/hold is used to convert the voltage to a digital value. A conversion cycle takes a total of 17 µseconds. All timing, control logic, conversion and buffering is provided on the IP. When the conversion is done, the IP will either generate a programmable, vectored interrupt, or a ADC_BUSY bit may be polled by the host. The 12-bit data is sign-extended by the control logic to fill a 16-bit word, and may be read any number of times by the host until the next conversion has completed.

Reading a sensor requires a 14 µsec conversion. Additional 3 µsec is required between consecutive conversions for the internal sample-and-hold to settle. Therefore the continuous conversion rate is one conversion every 17 µsec for a 58.8 Ksample/sec maximum scan rate. All timing and sequencing is handled by the hardware on the IP. An ADC_BUSY bit may be polled or an interrupt may be generated at the end of conversion.

The IP-Thermistor includes a programmable 16-bit pacer clock with one µsec resolution. This clock may be programmed to start a conversion every 17 to 65,535 µsec continually. Alternatively the pacer clock may be used as a general purpose timer. The pacer clock has interrupt capability.

Overvoltage protection of the IP-Thermistor's inputs is provided the multiplexers. These multiplexers can withstand up to ±35V continuous, with or without power applied.

IP-Thermistor includes a calibration 2 Kbit EEPROM. Normally this EEPROM is not required. However it is fully supported and may be used to store per-channel information by the system integrator, This is useful, for example, for holding thermistor type and calibration data that is sensor or system dependent.

Thermistors have a temperature v. resistance curve that is roughly logarithmic. Complete tables, equations and coefficients are generally available from the sensor manufacturer.

Additional software running under OS-9® is available from SBS GreenSpring. Contact the factory for more information.
IP-Thermistor supports sensors wired in two wire and three-wire configurations. The two-wire configuration is standard. The three-wire configuration provides a separate drive and sense line, plus a common ground. The external ground line should be the largest wire size practical, to minimize the voltage drop on this leg. In either two-wire or three-wire configurations one leg of the thermistor is connected on the IP to analog ground. This ground is connected on the IP to the host system ground. All sensors and their wiring must be installed floating to prevent ground currents. The ground connection of one leg of each sensor on the IndustryPack means that the sensors operate close to the host system ground potential. Note that overvoltage protection is reduced when using a three wire sensor and that overvoltage on one channel will affect other channels on the IP.

The maximum excitation voltage under operating conditions is 5.12 volts. The maximum drive voltage open circuit is about 7.5 volts. The ADC voltage range is 0 to 5.12 volts.

The current source and ADC are both driven by an extremely stable voltage reference: 5 ppm/°C typical drift. DC offset voltage is trimmed by the factory on the IndustryPack to an accuracy of ±2 LSB. The current source (and ADC span) is trimmed by the factory on the IndustryPack to an accuracy of 0.1%. The ADC has a worst case linearity error of ±2 LSB, which is ±0.05% of full scale range.

IP-Thermistor provides a programmable 8-bit interrupt vector. The seven most significant bits are programmed by the host. The LSB is set to one for ADC conversion complete interrupts, and set to zero for Pacer Clock interrupts. Complete status bits are provided to determine interrupt source and ADC and pacer clock status.

The registers on the IP-Thermistor consist of:

- two 8-bit Control/Status Registers
- 8-bit Vector Register
- 16-bit Data Register
- 16-bit Pacer Clock Register
- Convert Trigger Address

The Control/Status registers consist of:

- 4 bits for input channel selection
- 1 bit for current source enable
- 2 bits for interrupt enable/clear
- 1 bit for pacer clock mode.
- 1 bit for ADC Conversion BUSY/DONE.
- 1 bit for multiplexer Ready
- 1 bit for Pacer Clock RUN/STOP

Key Features

- Sixteen temperature input channels
- Supports two-wire thermistor temperature sensors
- Heavy duty over-voltage protection
- Switched, low drive current reduces self-heating
- Supports high scan rates to 58.8 Ksample/sec
- Internal analog sample/hold and digital data buffer permit pipelined operation
- High accuracy, low drift, factory calibration
- Basic accuracy to 0.2°C (sensor dependent).
- Complete IP—no external signal conditioning, timers or ADC required

- Built-in pacer clock and interrupt logic supports background scanning
- Low cost, under $25 per channel
- Up to 64 channels per VME slot

List of Thermistor Suppliers

Thermistors are available from the following sources:

YSI Inc Yellow Springs Ohio 45387 (800) 765-4974	High Rel, NASA Approved Very high precision (.05°C) 1% 4400X, under $10 each.
Ketema 2900 Blue Star Street Anaheim, CA 92806 tel: (714) 630-0081 fax: (714) 630-4131	High precision available
Philips Components 2001 W. Blue Heron Blvd PO Box 10330 Riviera Beach FL 33404 tel: (407) 881-3200 fax: (407) 881-3300	
Rosemount 1256 Trapp Road Eagan MN 55121 Tel: (612) 681-8900 Fax: (612) 681-8909	Also makes Pt RTD sensors
Koa Speer Bolivar Drive PO Box 547 Bradford PA 16701 tel: (814) 362-5536 fax: (814) 362-8883	
Therm-O-Disc Subsidiary of Emerson Electric 1320 S. Main Street Mansfield OH 44907-0538 tel: (419) 525-8450 fax: (419) 525-8344	
muRata Erie 2200 Lake Park Drive Smyrna GA 30080 tel: (800) 831-9172 fax: (404) 684-1541	NTH4G series has 1% tolerance, fast time constant—one second [Catalog No. G-01-B, page 70]

List of Resistor Suppliers

The following suppliers make suitable 5.11K, 1/4 watt, 0.1% shunt resistors
(lower precision resistors may be acceptable depending on customer's application):

Philips Components Airport Road PO Box 760 Mineral Wells, TX 76067 tel: (817) 325-7871 fax: (817) 325-8397 toll free literature, (800) 447-3762	Type RNC55E 0.1% recommended Type 5033Y, 0.5% alternate Type 50233Z for higher precision Distributed by Marshall Sales Offices in most states
IRC PO box 1860 Boone, North Carolina 28607 tel: (704) 264-8861 fax: (704) 264-8865	T9-55-5.11K-0.1% recommended

Other suitable resistor manufacturers include Dale, Vishay, and others.

Theory of Operation

IP-Thermistor consists of the following subsystems:

- Input Protection
- Input multiplexers
- Current Source
- Current Source Multiplexer
- Buffer Amplifiers
- Pacer Clock
- Interrupt Logic
- ADC and Sequencer
- EEPROM
- Control Logic and Bus Interface

Input Protection

Each of the 16 input channels has a dedicated location to mount one Schottky diode and a 1K current limiting resistor. The factory default configuration is both diodes and resistors installed.

The current limiting, series resistor is used to protect the input voltage sense circuit. The Schottky diode provides significant protection for the current sourcing circuit. In addition, the four multiplexers on-board the IP-Thermistor can withstand a continuous ±35V overvoltage, with or without power applied to the IP.

Input Multiplexers

The input multiplexers consist of two 8-input multiplexer ICs that are wired to support sixteen input channels.

Selection of the input channel is accomplished by programming four Select bits in one of the control registers

Connecting the Thermistor

For standard two-wire configuration connect one lead of the sensor to Sense, and the other lead to the adjacent ground. The Schottky diode is connected between the Drive and Sense signals internally on the IP, and normally the external Drive line is left open.

The recommended cable type for standard two-wire thermistors is shielded twisted pair. Connect the two lines in the twisted pair as described above, and connect the shield ***at one end only*** to the ground line. The recommended shield connection end is at the IndustryPack. If there are significant noise sources located near the sensor then better noise rejection may occur if the shield is connected to the ground leg at the sensor.

The larger the wire gauge and the shorter the cabling the less error will be introduced by the resistance of the cable. For most applications the wire resistance is ignored. A good quality first order correction may be implemented by assuming the cable resistance is fixed (actually it varies with temperature somewhat) and subtracting it from measured resistance prior to converting the resistance to a temperature. Although charts are available for computing the cable resistance, it is generally simpler and more reliable to measure the cable resistance directly. To do this short the cable leads close to the sensor, then measure the total cable resistance at the IP end of the cable using a good quality low-ohm meter that has been recently zeroed. Be sure that you have good solid connections prior to taking this measurement. The cable resistance may be stored in the EEPROM on the IP, if desired.

For three wire configuration, connect the two wires of one leg of the thermistor to the Drive and Sense lines respectively, and the other leg of the thermistor to the adjacent ground line. Use the heaviest conductor possible (for example the shield on some cables) for the common ground line to minimize the voltage drop on this leg. The ground leg cable resistance may also be measured and removed from the reading if desired.

Current Source

A high precision, low drift current source on the IP-Thermistor provides a constant 1.000 milliamps of current across the thermistor sensor. This current source consists of a precision 5 volt reference, a voltage divider network, a low-drift resistor, and a voltage to current converter circuit that uses an FET driven in a constant current configuration.

The current source—ADC combination is trimmed at the factory to produce an ohm meter that reads 0.800 bits/? exactly. (This corresponds to a current source of 1.000 mA and a voltage span of 5.120 volts.) Thus a 5000 ? resistor will read 0.800 x 5000 = 4000 counts.

Current Source Multiplexer

The current source multiplexer operates in tandem with the input multiplexer. It uses the same four Select lines to route the precision current source to the same thermistor that is selected by the input Multiplexer.

The current source may be disabled by writing a zero to the appropriate bit in the control register.

By connecting the current source to each thermistor only during actual measurement self heating of the Thermistor is minimized. A typical thermistor has about 1 mW/°C power dissipation in still air. For a continuously-on current source, with a sensor resistance of 1000 ? , the power is I*I*R = one milliwatt, for a temperature rise of about one °C. If all 16 Thermistors are scanned continuously the average power is 1/16 as much, for a rise of 0.06°C. A thermistor in liquid, moving gas, or attached to a massive object will generally have a much higher thermal coefficient, and thus have a lower temperature rise.

Buffer Amplifier

A fast precision buffer amplifier follows the input multiplexer. Two levels of high frequency filtering are implemented along with the amplifier to reduce noise. Input voltage range is 0 to 5.12 volts. Dual Schottky diodes are used to prevent the ADC from having excessive voltage applied to it.

Pacer Clock

A programmable 16-bit pacer clock is provided by the IP's control logic. This clock is programmable as either a timer (runs once) or as a clock (runs continuously). It has a resolution of 1.0 µsec. A 16-bit divider provides any time from 0 µsec to 65,536 µsec.
The pacer clock is a loadable up-count counter. Upon power up or reset the counter load value is initialized to zero. This value may be changed by the user. The load value remains intact until reprogrammed by the user. The counter always starts counting from its load value up to the terminal count value of $FFFF. The counter must be enabled by the configuration bit in the Clock Control Register for it to start counting. Any change of load value must take place prior to this. The pacer clock in either mode is capable of generating an interrupt upon reaching its terminal count. The interrupt is enabled by setting the interrupt bit in the Clock Control Register.

In the clock (run continuous) mode, the counter starts counting from the programmed load value and counts up to $FFFF and then reinitializes itself to the load value and repeats the count cycle. The counter also starts an ADC conversion at the beginning of its count. The allowable load value range for the counter is $0000 to $FFEF corresponding to 65,536 to 17 µsec count respectively. The load value $FFEF is the maximum bandwidth of the ADC at 58.8 Ksample/sec. Any value greater than this is less than the cycle time of the ADC resulting in erroneous conversion. The counter must be enabled by the enable bit in the Clock Control Register for it to run. Once this bit is set, the pacer clock runs continuously until this bit is cleared.

By programming the pacer clock to operate in clock mode it is easy to implement a background, interrupt driven, scanning routine.

In the timer (run once) mode the counter starts counting from its load value and counts up to $FFFF and then stops. Unlike in the continuous mode, the counter does not start an ADC conversion. To start an ADC conversion, a write to Convert Trigger Address is required. Therefore the pacer clock is totally independent of the ADC and may be used as a general purpose timer. The counter begins counting immediately after the clock enable bit in the Clock Control Register is set to one. As soon as the counter is enabled, this bit reads as one until the counter reaches $FFFF and then changes to zero. To count again this bit must be set to one.

Interrupt Logic

There are two interrupts available from the IP-Thermistor: ADC conversion complete and pacer clock.

If the ADC conversion interrupt is enabled, interrupt request will be driven immediately by the ADC following completion of its conversion. The interrupt will be cleared automatically by the IP hardware during interrupt acknowledge cycle or by disabling the ADC interrupt . The interrupt vector for conversion complete is always odd; that is, the LSB is one. This interrupt takes priority over the pacer clock interrupt

If the pacer clock interrupt is enabled, interrupt request will be driven immediately following the pacer clock reaching terminal count $FFFF. The interrupt will be cleared automatically by the IP hardware during the interrupt acknowledge cycle or by disabling the pacer clock interrupt bit . Do not toggle the pacer clock interrupt enable bit unless you wish to reload the pacer clock to a different value. The interrupt vector for conversion complete is always even; that is, the LSB is zero. This interrupt has lower priority than the ADC conversion complete interrupt.

ADC and Sequencer

The ADC IC used on the IP-Thermistor is a bit-serial type. It must be precisely clocked. It shifts out 12 data bits in sequence, MSB first, with each clock pulse. It performs the conversion at the same time as the data is shifted so no additional time is required for data shifting in addition to the time needed for the data conversion itself. The sequencer, shift register, and data holding register to run the ADC are provided as part of the IP's control logic.

The IP's control logic guarantees minimum settling time from the time the input multiplexers are set to the desired channel and the time the ADC starts converting. This guarantees that the current source, cabling, and input buffer amplifier have had a chance to settle. This time is 3 µsec. Long cabling may require longer minimum settling time. A bit is provided in the control register called multiplexer ready. This bit is zero after power up or reset and at the end of an ADC conversion cycle. Once an ADC conversion cycle is started, this bit goes high within 4 µseconds to indicate the ADC has sampled and held the selected channel. The user may change the input channel when this bit goes high without corrupting the current ADC conversion in progress. There is a period of 14 µseconds when this bit stays high during any ADC conversion cycle. By changing channel during this period the user can achieve the maximum ADC throughput rate of 58.8 Ksample/sec. If the user does not change channel during this period, the ADC throughput reduces proportionately from the time this bit goes low until the next ADC conversion is started.

The ADC IC is driven from a common power supply and voltage reference buffer set to 5.120 volts. This voltage is derived from the precision voltage reference, then amplified, buffered, and separately filtered for the power pin and the voltage reference pin of the ADC. The voltage reference is factory trimmed for a precision combined current source—ADC span equal to 0.800 bits per ? , ±0.1%. DC offset is separately trimmed to less than ±2 LSB.

The IP provides a dedicated data holding register that is only updated following completion of a conversion. This allows the user to read from the data register the prior data value up to the time a new value is loaded. The data register may be read any number of times and there are no read artifacts.

The IP's control logic drives the high four lines of the data bus to zero so a valid 16-bit integer in the range of 0 to 4095 is always read.

Factory calibration of zero and full-scale span is set with POT2 and POT2 respectively. These adjustments should not have to be changed by the customer. Zero is such that zero ? through an 18" cable (actual resistance about 0.8?) reads zero counts. Full scale is such that a 5.000 K? resistor through 18" cable reads 4000 counts.

Typical noise is 3 counts peak to peak for 100 readings with 18" unshielded cable. Typical RMS noise is about 1/2 count. Noise is random, "white" noise and may be effectively and accurately reduced by simple software averaging, which is recommended.

Recommended cabling is shielded twisted pair, with the shield connected at one end only, at or near the IP, to ground.

EEPROM

The IP-Thermistor provides a 2-K bit EEPROM used to store calibration or other user data.

This EEPROM is not generally programmed by SBS GreenSpring. It may be programmed by the user to hold sensor specific data, channel configuration, or calibration data.

Possible useful information and the suggested data size could include:

- Sensor type (one byte)
- Sensor configuration (one bit)
- cable resistance (two bytes)
- Sensor calibration point one (two bytes)
- Sensor calibration point two (two bytes)
- Last calibration date (three bytes)

For 16 channels this information would take up 117 out of 512 available bytes.

Programming details are given in the Programming Section below. Approximately one host read or write operation to the IndustryPack is required per bit read or written from the EEPROM.

Control Logic

Control logic for IP-Thermistor is implemented in a 100 pin fine-pitch Xilinx® IC. Control logic consists of bus interface, registers, ID PROM, access to the EEPROM, pacer clock, ADC sequencer and interrupt logic.

VMEbus Addressing

The address map of the IP-Thermistor is given below in Figure 1 below. Byte accesses are on data lines D0..D7. Word accesses are on data lines D0..D15.

Register Name	**68K Address**	**Access**	**Notes**
Select Reg	$01	R/W, byte	Input selection
Clock Control Reg	$03	R/W, byte	Pacer clock control
Clock Data Reg	$04	R/W, word	Pacer clock rate divider
Convert Command	$06	W, word	Convert command
ADC Data Reg	$08	R, word	ADC data
Vector Reg	$0B	R/W, byte	Read/write interrupt vector
EEPROM Data	$0D	R/W, byte (1)	R/W one bit of EEPROM Data
EEPROM Select	$0F	W, byte (2)	Select EEPROM

Note (1) One bit only. See text in Programming section for details.
Note (2) See text in Programming section for details.

Figure 1 VMEbus Address Map

See Programming section for register details.

NuBus Addressing

NuBus addressing requires computing the address from the byte addresses given above under VMEbus Addressing. The formula for byte accesses is:

NuBus byte address = (VMEbus byte address * 2) – 1

All byte data is transferred on data lines D0..D7.

All word accesses use the same address as for VME. Data is transferred on data lines D0..D15.

NuBus word address = VMEbus word address

Interrupt mapping is a function of the selected carrier board. See your IP carrier board User Manual for more information.

ISA (PC-AT) Bus Addressing

ISA (PC-AT) bus addressing requires computing the address from the byte addresses given above under VMEbus Addressing. The formula for byte accesses is:

ISA bus byte address = VMEbus byte address – 1

The effect of this formula is to change all 68K odd byte addresses into Intel architecture even byte addresses. All byte data is still on data lines D0..D7.

All word accesses use the same address as for VME. Data is transferred on data lines D0..D15.

ISA word address = VMEbus word address

Interrupt mapping is a function of the selected carrier board. See your IP carrier board User Manual for more information.

Getting Started

This section is intended to assist the user to get to a quick start with IP-Thermistor. The following steps perform a single shot conversion on channel one with an installed resistor as a thermistor and reads the result. The user should consult the Programming Section for bit interpretation of registers given in this exercise. The required equipment are an IP-Thermistor, a 2.5K 0.1% resistor, and a host system with system debugger as software tool.

1) The Engineering Kit contains a 2.5 K? precision resistor, a cable, and a standard 50-pin terminal block.
   a) Install the IP-Thermistor on your carrier board.
   b) Install the 50-pin data cable from your carrier board to the terminal block.
   c) Install the precision 2.5K? resistor on channel one by connecting it between pins 2 and 3 on the terminal block

2) Power-up the system and verify that you can read the IP-Thermistor's ID PROM from your debugger.

3) Using your debugger, write the byte hex value $10 to VME IP I/O offset hex address $01.

4) Under debugger write the word hex value $FFFF to VME IP I/O offset hex address $06.

5) Under the debugger read the conversion result from VME IP I/O offset hex address $08. The result should read word hex value $07CC (1996 decimal) within ±4 LSB accuracy.

Programming

This section gives the bit assignments of the registers for the IP-Thermistor. It also provides basic sequencing information for programming the IP-Thermistor, and power-up defaults.

This section should be used by programmers for all platforms.

Accesses to the registers are both byte-wide and word-wide. The correct data width must be used for proper operation. All registers are mapped within the IP I/O space.

Register Name	Access	Notes
Select Reg	R/W, byte	Input selection
Clock Control Reg	R/W, byte	Pacer clock control
Clock Data Reg	R/W, word	Pacer clock rate divider
Convert Command	W, word	Convert command
ADC Data Reg	R, word	ADC data
Vector Reg	R/W, byte	Read/write interrupt vector
EEPROM Data	R/W, byte (1)	R/W one bit of EEPROM Data
EEPROM Select	W, byte (2)	Select EEPROM

Note (1) One bit only. See text in Programming section for details.
Note (2) See text in Programming section for details.

Figure 2 Register Map

Register Summary

Select Register — This read/write byte-wide register contains eight useful bits. It is used to select one of sixteen input channels and to enable or disable the current source and the conversion complete interrupt. Normally the current source is left enabled. Three status bits provide ADC and interrupt status. This register powers up to zero, with the current source and the interrupt disabled.

Clock Control Reg — This read/write byte-wide register contains three useful bits. It is used to enable the pacer clock and select its mode. This register powers up to zero, with the pacer clock disabled.

Clock Data Reg — This read/write word-wide register is used to set the pacer clock divider. The value programmed into this register determines the number of microseconds that the pacer clock runs before triggering the ADC, and optionally, generating an interrupt.

Convert Command — A write to this word triggers the ADC to start converting. A write to either byte will also trigger the ADC. Conversion complete may be determined by polling the ADC_BUSY bit in the Select Register or by enabling a conversion complete interrupt. ADC conversion takes 17 µsec. Reads at this address have no effect.

ADC Data	Reading a word from this address provides a sign-filled 16-bit integer containing the data from the last ADC conversion. The 12-bits of data are justified in the LSBs. The high four bits always read as zero, giving a possible range of zero to 4000. Data may be read any time until a new conversion complete replaces the previous data. Writes to this address have no effect. Reading zero counts corresponds to zero ? . Reading 4000 counts corresponds to 5.000 K? . Readings are linear.
Vector Register	This byte-wide read/write register holds the interrupt vector. Only the high seven bits are used. The LSB is set to one or zero by the IP to identify an ADC conversion complete interrupt or a pacer clock interrupt respectively. This register powers up to all ones and must be programmed prior to enabling interrupts.
EEPROM Data	Reads and writes to this byte address are used to read and write one bit of data to or from the EEPROM on the IP. See the Programming Section for details.
EEPROM Select	Writes to this byte address are used to enable the EEPROM on the IP. See the Programming Section for details

Select Reg

This 8-bit register is used to select the input channel and to enable the current source and the conversion complete interrupt.

The four bit Input Select field selects which thermistor is being read. These bits also route the precision current source to the same thermistor.

The Select Register powers up and resets to all zero.

Bits [3..0] 4-bit Input Select (read/write)

0000	Channel 1
0001	Channel 2
0010	Channel 3
0011	Channel 4
0100	Channel 5
0101	Channel 6
0110	Channel 7
0111	Channel 8
1000	Channel 9
1001	Channel 10
1010	Channel 11
1011	Channel 12
1100	Channel 13
1101	Channel 14
1110	Channel 15
1111	Channel 16.

Bit [4] Current Source Enable (read/write)

0	Current Source Disabled
1	Current Source Enabled.

Bit [5] ADC Conversion Complete Interrupt Enable (read/write)

0 ADC Conversion complete interrupt disabled
1 ADC Conversion complete interrupt enabled.

Bit [6] Multiplexer Ready (read only)
0 This bit is normally low. It goes high briefly during a conversion. See notes below.
1 This bit is one for a brief time during conversion. See notes below.

This bit may be used by programmers who wish to implement high throughput scanning. The ADC includes an integral sample and hold. After approximately 4 µsec following a conversion start, the sample and hold has completed its settling and entered hold mode. At this point during the conversion, it is possible to change the input without impacting the conversion in progress. Complete settling to a final value of a new input may takes up to 10 µsec due to long cabling to the Thermistor.

Programmers should insure that at least 10 µseconds has elapsed from the time the Input Select field has been changed and a conversion is started. One way to insure this settling time is to change the input to the next channel during the current conversion after this bit, Multiplexer Ready, changes from zero to one.

This bit is provided for convenience to the programmer only. No accesses to the IP are blocked or altered by the hardware depending on the state of this bit.

Please refer to Theory of Operation under ADC and Sequencer for more detailed description of this bit.

Bit [7] ADC_BUSY (read only)
1 The ADC is converting.
0 The ADC is done converting. A new data value may be read from the ADC Data Register.

If the ADC Data Register is read during conversion, generally the last data value will be read. When the conversion is complete the hardware will automatically update the Data Register with the new value. If a read occurs during this update, data read may not be consistent. If the programmer can assure that any reads that occur after the start of conversion will complete within 12 µsec, the old data may be read reliably.

This bit may be read as the sign bit for a byte read. In some cases this can simplify a polling loop, over using a bit test instruction.

As an alternative to polling this bit, a conversion complete interrupt may be used. Note however, that in many systems the software overhead for an interrupt handling is higher than the 17 µsec it takes for a conversion to complete. The pacer clock may be used to implement background scanning that is interrupt based and does not require any polling.

Clock Control Register

This read/write byte-wide register contains three useful bits. It is used to enable the pacer clock and select its mode. This register powers up to zero, with the pacer clock disabled

Bit [0] Pacer Clock Enable (read/write)

0 The pacer clock is disabled
1 The pacer clock is enabled

This bit if enabled will go to zero in timer mode after the pacer clock reaches its terminal count of $FFFF. This bit if set to zero initializes the pacer clock to its programmed load value. Load value is a 16 bit programmable counter latch value.

Bit [1] Pacer Clock Mode (read/write)
1 clock mode: The pacer clock runs continually
0 timer mode: The pacer clock runs as timer

Whenever the pacer clock expires, in clock mode, with or without the pacer clock interrupt enabled, a conversion is started. See Pacer Clock under Theory of Operation.

Bit [2] Pacer Clock interrupt Enable (read/write)
0 Disable the pacer clock as interrupter
1 Enable the pacer clock as interrupter

Bit [3]..[6] Scratch bits (read/write)
User general purpose read/write. No artifacts to the IP-Thermistor operation.

Bits [7] Reserved

ADC Convert Command

Writing any value (write artifact) to this address starts a new conversion.

ADC Data Register

Reading a word from this address provides a sign-filled 16-bit integer containing the data from the last ADC conversion. The 12-bits of data are justified in the LSBs. The high four bits always read as zero, giving a possible range of zero to 4000. Data may be read any time until a new conversion complete replaces the previous data. Writes to this address have no effect.

Reading zero counts corresponds to zero ? . Reading 4000 counts corresponds to 5.000 K? . Readings are linear.

Vector Register

This 8-bit read/write register is used to provide a vector for interrupts. Only the seven most significant bits are user configurable. The two sources of interrupts on the IP-Thermistor are the ADC and the pacer clock. The LSB distinguishes between the ADC conversion complete and the pacer clock expiration. This register should be loaded prior to enabling interrupts.

The Vector Register powers up or resets to $FF.

EEPROM Data Register, EEPROM CS Register

The IP-Thermistor provides a 2-K bit EEPROM used to store calibration data or other user data. Programming of this device requires reference to the Catalyst Semiconductor CAT93CS56 data sheet, or the data sheet for a compatible device.

The EEPROM IC has four relevant pins: Chip Select (CS), Clock (SK), Data In (DI) and Data Out (DO). Note that DI is data from the host into the EEPROM (corresponding roughly to conventional memory Write) and DO is data to the host from the EEPROM (corresponding roughly to conventional memory Read).

CS is normally driven true. Accessing (typically any write cycle) the EEPROM CS Register drives the chip CS low for 250 nsec to reset it. The chip's clock (SK) signal is generated automatically by the control logic in the IP-Thermistor. The data in and data out lines are written and read respectively in D0 of the EEPROM Data Register.

The control logic on the IP-Thermistor provides some low level timing assistance for accessing data in the EEPROM. However the programmer must construct specific sequences of IP-Thermistor read and write cycles in order to access data in the EEPROM. Roughly one read ore write operation from the host is needed for each bit read or written in the EEPROM, plus one write operation from the host for each bit of command and address to the EEPROM.

The EEPROM is configured for 16-bit words. All EEPROM accesses are word access, except for those that affect the entire EEPROM.

The basic access sequence is:

1. Write to the EEPROM CS Register, data value irrelevant. This generates a 250 nsec inter-command clear pulse on the EEPROM CS line.

2. Write to the EEPROM Data Register, setting data line D0 to the desired value. Write the three-bit opcode for the EEPROM operation, starting with a "1". Each write is "self-timed," in that only a single host write per bit is required.

3. Write the nine bit EEPROM address, one bit at a time in D0, using the EEPROM Data Register as above, staring with the A8 MSB.

4A. If writing data, now write the 16 data bits, MSB first. Data is written in D0 of the EEPROM Data Register.

4B. If reading data first execute one read of the EEPROM Data Register. D0 should be "0." This bit is discarded. Now read the 16 data bits, MSB first. Data is read in D0 of the EEPROM Data Register.

5. Write to the EEPROM CS Register, data value irrelevant. This generates a 250 nsec inter-command clear pulse on the EEPROM CS line.

Other operations to the EEPROM such as clear all, read all, write all, are similar, but the detailed sequence differs appropriately. See the chip data sheet for more information.

I/O Pin Wiring

This section gives the pin assignments for IP-Thermistor.

The pin numbers given in Figures 3 and 4 below correspond to numbers on the 50-pin IndustryPack I/O connector, to the wires on a 50-pin flat cable plugged into a standard IP carrier board, and to the screw terminal numbers on the IP-Terminal block.

Pin Number	Channel	Signal Input
1	1	Drive 1
2	1	Sense 1
3	1	GND
4	2	Drive 2
5	2	Sense 2
6	2	GND
7	3	Drive 3
8	3	Sense 3
9	3	GND
10	4	Drive 4
11	4	Sense 4
12	4	GND
13	5	Drive 5
14	5	Sense 5
15	5	GND
16	6	Drive 6
17	6	Sense 6
18	6	GND
19	7	Drive 7
20	7	Sense 7
21	7	GND
22	8	Sense 8
23	8	Sense 8
24	8	GND

Figure 3 I/O Pin Assignment First Half

Note: For standard 2-wire thermistors, wire one leg to Sense and the other leg to the adjacent GND line; leave Drive line as no-connect.

Pin Number	Channel	Signal Input
25	9	Drive 9
26	9	Sense 9
27	9	GND
28	10	Drive 10
29	10	Sense 10
30	10	GND
31	11	Drive 11
32	11	Sense 11
33	11	GND
34	12	Drive 12
35	12	Sense 12
36	12	GND
37	13	Drive 13
38	13	Sense 13
39	13	GND
40	14	Drive 14
41	14	Sense 14
42	14	GND
43	15	Drive 15
44	15	Sense 15
45	15	GND
46	16	Drive 16
47	16	Sense 16
48	16	GND
49	all	(spare)
50	all	GND

Figure 4 I/O Pin Assignment Second Half

Note: For standard 2-wire thermistors, wire one leg to Sense and the other leg to the adjacent GND line; leave Drive line as no-connect.

IndustryPack Logic Interface Pin Assignment

Figure 5 below gives the pin assignments for the IndustryPack Logic Interface on the IP-Thermistor. Pins marked n/c below are defined by the specification, but not used on IP-Thermistor. See also your User Manual for your IP Carrier board for more information.

GND	GND	1		26	
CLK	+5V		2		27
Reset*	R/W*	3		28	
D0	IDSel*		4		29
D1	n/c	5		30	
D2	MEMSel*		6		31
D3	n/c	7		32	
D4	INTSel*		8		33
D5	n/c	9		34	
D6	IOSel*		10		35
D7	n/c	11		36	
D8	A1		12		37
D9	n/c	13		38	
D10	A2		14		39
D11	n/c	15		40	
D12	A3		16		41
D13	IntReq0*	17		42	
D14	A4		18		43
D15	n/c	19		44	
BS0*	A5		20		45
n/c	n/c	21		46	
BS1*	A6		22		47
n/c	Ack*	23		48	
+5V	n/c		24		49
GND	GND	25		50	

Note 1: The no-connect (n/c) signals above are defined by the IndustryPack Logic Interface Specification, but not used by this IP. See the Specification for more information.

Note 2: The layout of the pin numbers in this table corresponds to the physical placement of pins on the IP connector. Thus this table may be used to easily locate the physical pin corresponding to a desired signal. Pin 1 is marked with a square pad on the IndustryPack.

Figure 5 Logic Interface Pin Assignment

ID PROM

Every IP contains an IP PROM, whose size is at least 32 x 8 bits. The ID PROM aids in software auto configuration and configuration management. The user's software, or a supplied driver, may verify that the device it expects is actually installed at the location it expects, and is nominally functional. The ID PROM contains the manufacturing revision level of the IP. If a driver requires that a particular revision be present, it may check for it directly.

Standard data in the ID PROM on the IP-Thermistor is shown in Figure below.
For more information on IP ID PROMs refer to the IndustryPack Logic Interface Specification, available from SBS GreenSpring. The ID PROM is implemented in the IP-Thermistor internally in the Xilinx LCA.

The location of the ID PROM in the host's address space is dependent on which carrier is used. Normally for VMEbus carriers the ID PROM space is directly above the IP's I/O space, or at IP-base + $80. Macintosh drivers use the ID PROM automatically. RM1260 address may be derived from Figure below by multiplying the addresses given by two, then subtracting one. RM1270 addresses may be derived by multiplying the addresses given by two, then adding one.

3F 19	(available for user)	
17	CRC	(2A)
15	No of bytes used	(0C)
13	Driver ID, high byte	(00)
11	Driver ID, low byte	(01)
0F	reserved	(00)
0D	Revision	(B1)
0B	Model No IP-Thermistor	(4B)
09	Manufacturer ID GreenSpring	(F0)
07	ASCII "C"	(43)
05	ASCII "A"	(41)
03	ASCII "P"	(50)
01	ASCII "I"	(49)

Figure 6 ID PROM Data (hex)

Construction and Reliability

IndustryPacks were conceived and engineered for rugged industrial environments. The IP-Thermistor is constructed out of 0.062 inch thick FR4 V0 material. The six copper layers consist of four signal layers, and two internal layers. The internal layers are power and ground planes.

Through hole and surface mounting of components is used. IC sockets are screw-machined pins, gold plated. High insertion and removal forces are required, which assists in keeping components in place. If the application requires unusually high reliability or is in an environment subject to high vibration, the user may solder the four corner pins of each socketed IC into the socket, using a grounded soldering iron.

The IndustryPack connectors are keyed, shrouded and gold plated on both contacts and receptacles. They are rated at 1 Amp per pin, 200 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The IP is secured to the carrier with four metric M2 stainless steel screws. The heads of the screws are countersunk into the IP. The four screws provide significant protection against shock, vibration, and incomplete insertion. For most applications they are not required.

The IndustryPack provides a low temperature coefficient of 0.89 W/°C for uniform heat. This is based on the temperature coefficient of the base FR4 material of .31 W/m-°C, and taking into account the thickness and area of the IP. This coefficient means that if 0.89 Watts is applied uniformly on the component side, that the temperature difference between the component and the solder side is one degree Celsius.

Warranty and Repair

GreenSpring Computer warrants this product to be free from defects in workmanship and materials under normal use and service and in its original, unmodified condition, for a period of one year from the time of purchase. If the product is found to be defective within the terms of this warranty, GreenSpring Computer's sole responsibility shall be to repair, or at GreenSpring Computer's sole option to replace, the defective product. The product must be returned by the original customer, insured, and shipped prepaid to SBS GreenSpring. All replaced products become the sole property of SBS GreenSpring.

GreenSpring Computer's warranty of and liability for defective products is limited to that set forth herein. SBS GreenSpring disclaims and excludes all other product warranties and product liability, expressed or implied, including but not limited to any implied warranties of merchandisability or fitness for a particular purpose or use, liability for negligence in manufacture or shipment of product, liability for injury to persons or property, or for any incidental or consequential damages.

GreenSpring's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of SBS GreenSpring.

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. SBS GreenSpring will not be responsible for damages due to improper packaging of returned items. For service on GreenSpring Products not purchased directly from SBS GreenSpring contact your reseller. Products returned to SBS GreenSpring for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

For Service Contact:

Customer Service Department
SBS/GreenSpring Modular I/O
181 Constitution Drive
Menlo Park, CA 94025
(415) 327-1200
(415) 327-3808 fax
InterNet Address support@greenspring.com

Specifications

This section gives the technical specification for the IP-Thermistor.

Logic Interface	IndustryPack Logic Interface, 0.7.1 compatible
Thermistor Range	0 to 5.11 K? , 0.2 W
Input Overvoltage Protection	±35V Continuous, with or without power to the IP
Current Source	1 mA constant, 5 ppm/°C typical drift, software switch on/off, factory trimmed to accuracy of 0.1%
Number of Channels	Sixteen temperature input channels
Wire Configuration	Two-wire or Three-wire
ADC resolution	12 bits with integral sample and hold
ADC Data Format	16 bits binary, hardware sign extended
ADC Conversion Rate	58.8K samples per second continuous
ADC Settling time	3 µsec to 0.01% (instrumentation amp), typical
ADC Dynamic Linearity	±2 LSB, ±0.05% of full scale range
ADC Factory Trim	DC offset voltage to ±2 LSB accuracy, reference voltage to +5.12 V
Pacer Clock	16-bits, 1 usec resolution, optional interrupt
Interrupts	Vectored, generated by pacer clock or ADC
Memory	2 Kbits serial EEPROM, user calibration data and etc.
Host Interface	Register based mapped within IP I/O space
Onboard Options	User installed optional shunt resistors for thermistors over 5.11K? .
Interface Options:	50 pin flat cable 50 screw terminal block interface User cable
Dimensions:	Standard Single IndustryPack width and length. 1.8 x 3.9 inches
Construction:	6 Layer Printed Circuit, Through Hole and Surface Mount Components. Programmable parts are socketed.
Temperature Coefficient:	.89 W/°C for uniform heat across IP
Test conditions	20°C, typical
Power Requirements	+5 VDC, 110 mA typ +12 VDC, 30 mA typ –12 VDC, 30 mA typ
Environmental	Operating temperature: 0 to 70°C Humidity: 5 - 95% non-condensing Storage temperature: –10 to +85°C