API429-8/16
Hardware Manual

Eight/Sixteen Channel ARINC429 Module

for

PCIbus

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July 2006
V01.02 Rev. A

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DOCUMENT HISTORY

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V01.01	April 2002	B. Schweitzer	Modification of AIM- Address
V01.01 A	February 2004	J. Furgerson	Applied new AIM formatting
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V01.02 A	26.07.2006	M. Mutter	Wrong description of Trigger Input Event. Trigger Input reacts on falling edge.

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1. INTRODUCTION

1.1 General

This document comprises the Hardware User's Manual for the API429-8 and API429-16 PCI-Bus modules. The document covers the hardware installation, the board connections the technical data and a general description of the hardware architecture. For programming information please refer to the according documents listed in the 'Applicable Documents' section.

The API429 modules are members of AIM's new family of advanced PCI-Bus modules for analysing, simulating, monitoring and testing of avionics databus systems.

The API429 provides eight or sixteen fully configurable ARINC429 channels on a short form factor PCI-card, whereby the eight channel board is an assembly variant of the API429 sixteen channel board. Each channel can be individually configured by software as a transmit *or* receive channel with different front plate connector outputs and inputs.

On transmit channels the API429 acts as an autonomously operating bus traffic simulator, supporting multiple modes of transmission sequencing. Full error injection capabilities are available, whereby the error injection is programmable individually for each channel and label. For special transmission operating modes the parity bit can be used alternative as an additional data bit. The output level and the rise and fall time of the bus signals are individually programmable by software for each transmit channel.

For the receive channels the API429 provides an advanced monitor and analyzer function, with unique on-board error detection, triggering and filtering capabilities. Both functions are available concurrently and independent from each other. The hardware architecture provides resources to guarantee that the performance of one function is not effected by the current load of the other function. The rise and fall time of the bus signals are individually programmable for each receive channel. To adapt to different transmit speeds the transmission rate can be varied in discrete steps between appr. 90- and 120Kbits on the high speed bus and between 11.5 and 16.0 on the low speed lines. Speed setting is global for all channels.

The hardware architecture provides enough resources (i.e. processing capability and memory) to guarantee that all specified interface functions on all channels are fully available concurrently. The on-board processing capabilities and the large memory size of the DRAM enables autonomous operation with minimal interaction of the PC host processor.

The advanced architecture uses two processors, a powerful 64bit RISC processor (ASP) assists and supports the application and driver software tasks, and expands the capability of the API429 modules to that of a high level instrument. To fulfil the real-time requirements of avionics type databus systems a high performance 32bit RISC processor (BIP) is implemented on the Bus Interface Unit (BIU).

An IRIG B Time Code Decoder is implemented on the API429 boards to satisfy the requirements of 'multi-channel time tag synchronization' on system level.

1.2 How This Manual is Organized

This API429-8/16 Hardware Manual is comprised of the following sections.

Section 1 - *INTRODUCTION* - contains an overview of this manual.

Section 2 - *INSTALLATION* - describes the steps required to install the API429-8/16 device, and connect the device to other external interfaces including; ARINC-429 interfaces, IRIG-B, and triggers.

Section 3 - *STRUCTURE OF THE* API429-8/16 - describes the physical hardware interfaces on the API429-8/16 using a block diagram and a description of each main component

Section 4 - *TECHNICAL DATA* - describes the technical specification of the API429-8/16.

For programming information please refer to the Reference Manual API429 Application Interface Library.

1.3 Applicable Documents

The following documents shall be considered to be a part of this document to the extent that they are referenced herein. In the event of conflict between the documents referenced and the contents of this document, the contents of this document shall have precedence.

1.3.1 Industry Documents

ARINC MARK 33 Digital Information Transfer System (DITS)
ARINC Specification 429-14
Published: March 10, 1993

PCI LOCAL BUS Specification
Revision 2.1, June 1, 1995.

IDT79RV4640 and IDT79R4650 RISC Processor Hardware User's
Manual Version 1.1, November 1995

Digital Semiconductor SA-110 Microprocessor,
Technical Reference Manual,
Revision B of a preliminary document, June 1996.

Technical Reference Manual GT64011 PCI and System Controller
for R4640 Processors, Preliminary Revision 1.2 , 2.7.97

1.3.2 Product Specific Documents

AIM - Reference Manual API429 Application Interface Library
Detailed description of the programming interface between the PC and the onboard driver software.

AIM - API429 Firmware Specification
Detailed description of the hardware / software interface between the BIU processor firmware and the onboard driver software.
This document is available on request.

AIM - User's Manual 'ASP Boot Monitor Program'
Description of the Debug Monitor commands and functions.
This document is available on request.

AIM - User Manual 'PAA-429 PC Based ARINC429 Analyzer for Windows'
(delivered together with the according Software package.)

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2. INSTALLATION

2.1 Preparation and Precaution for Installation

The API429-8/16 features full PCI ***Plug-and Play*** capability. There are no jumpers or switches on the board which have to be modified by the user.

It is recommended to use a wrist strap for any installations. If there is no wrist wrap available, then touch a metal plate on your system to ground yourself and discharge any static electricity during the installation work.

The following instructions describe how to install the API429 card in your system. Please follow the instructions carefully, to avoid any damage on the device.

2.2 Installation Instructions

The following instructions describe how to install the API429-8/16 module in your system. Please follow the instructions carefully, to avoid any damage on the device.

▶ **To Install the API429-8/16**

1. Switch off your system and all peripheral devices. Unplug the power cord from the wall outlet.
2. Touch a metal plate on your system to ground yourself and discharge any static electricity.
3. Remove the cover from your system.
4. Find a free PCI-expansion slot in your system with suitable size.
5. Remove the metal plate from the slot you have chosen and put the screw aside.
6. Align the API429 cards slot connector with the PCI expansion slot and gently lower the card into the free slot.
7. Secure the card to the expansion slot with the screw you removed from the metal plate.
8. Replace the cover of your system.

   and turn on the power to your system.

2.3 Connecting to Other Devices

The external interfaces of the API429-8/16, including those listed below, connect via a front plate male 80 pin mini DSUB connector. The pin assignments are shown in Table 2.3-I

a. ARINC429 lines

b. Trigger In/Out signals

c. IRIG In/Out interface for multi-channel time tag synchronization.

d. RS-232 Maintenance interface

Note: An optional Breakout cable (appr. two meters) can be ordered with two standard female 37pin DSUB connectors (ARINC429 RX and TX) and one female 15pin DSUB for the miscellaneous signals.

2.3.1 ARINC429 Channel Connection

For each ARINC429 channel a receive and transmit data pair is provided on the connector as shown in Table 2.3-I. Only one set is active depending on the programmed mode of the according channel (either receiver or transmitter).

2.3.2 Trigger, IRIG-B, and RS-232 Connection

Besides the ARINC429 receive and transmit signals the 80 pin mini DSUB connector comprises the trigger input- and output signals, the IRIG-B input and output and the RS-232 signals as listed in Table 2.3-I.

The IRIG-IN and IRIG-OUT signals shall be connected depending on the timetag method used as shown below.

1. Single AIM-Module no external IRIG-B source

   - No connection required

2. Multiple AIM-Modules with no common synchronization requirement

   - No connection required

3. Single or multiple AIM-Module(s) with external IRIG-B source

   - Connect external IRIG-B source to IRIG-IN and GND of all modules

4. Multiple AIM-Modules with no external IRIG-B source internally synchronized.

   - Connect the IRIG-OUT signal and the GND of the module you have chosen as the time master to all IRIG-IN signals (including the time master).

Figure 2.4-1 AVI429-8/16/32 Frontplate DSUB Connector

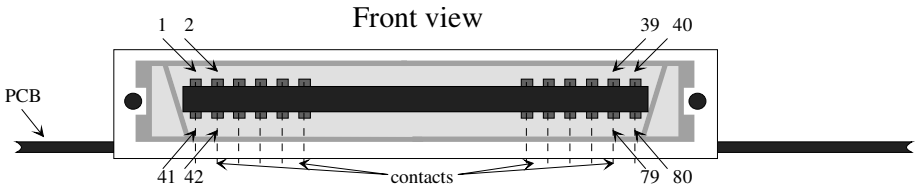


Table 2.3-I Frontpanel Connector Pin Description

Pin	Signal Description	Pin	Signal Description
1	Transmitter Channel 1 (True)	41	Transmitter Channel 1 (Complement)
2	Receiver Channel 1 (True)	42	Receiver Channel 1 (Complement)
3	Transmitter Channel 2 (True)	43	Transmitter Channel 2 (Complement)
4	Receiver Channel 2 (True)	44	Receiver Channel 2 (Complement)
5	Transmitter Channel 3 (True)	45	Transmitter Channel 3 (Complement)
6	Receiver Channel 3 (True)	46	Receiver Channel 3 (Complement)
7	Transmitter Channel 4 (True)	47	Transmitter Channel 4 (Complement)
8	Receiver Channel 4 (True)	48	Receiver Channel 4 (Complement)
9	Transmitter Channel 5 (True)	49	Transmitter Channel 5 (Complement)
10	Receiver Channel 5 (True)	50	Receiver Channel 5 (Complement)
11	Transmitter Channel 6 (True)	51	Transmitter Channel 6 (Complement)
12	Receiver Channel 6 (True)	52	Receiver Channel 6 (Complement)
13	Transmitter Channel 7 (True)	53	Transmitter Channel 7 (Complement)
14	Receiver Channel 7 (True)	54	Receiver Channel 7 (Complement)
15	Transmitter Channel 8 (True)	55	Transmitter Channel 8 (Complement)
16	Receiver Channel 8 (True)	56	Receiver Channel 8 (Complement)
17	Transmitter Channel 9 (True)	57	Transmitter Channel 9 (Complement)
18	Receiver Channel 9 (True)	58	Receiver Channel 9 (Complement)
19	Transmitter Channel 10 (True)	59	Transmitter Channel 10 (Complement)
20	Receiver Channel 10 (True)	60	Receiver Channel 10 (Complement)
21	Transmitter Channel 11 (True)	61	Transmitter Channel 11 (Complement)
22	Receiver Channel 11 (True)	62	Receiver Channel 11 (Complement)
23	Transmitter Channel 12 (True)	63	Transmitter Channel 12 (Complement)
24	Receiver Channel 12 (True)	64	Receiver Channel 12 (Complement)
25	Transmitter Channel 13 (True)	65	Transmitter Channel 13 (Complement)
26	Receiver Channel 13 (True)	66	Receiver Channel 13 (Complement)
27	Transmitter Channel 14 (True)	67	Transmitter Channel 14 (Complement)
28	Receiver Channel 14 (True)	68	Receiver Channel 14 (Complement)
29	Transmitter Channel 15 (True)	69	Transmitter Channel 15 (Complement)
30	Receiver Channel 15 (True)	70	Receiver Channel 15 (Complement)
31	Transmitter Channel 16 (True)	71	Transmitter Channel 16 (Complement)
32	Receiver Channel 16 (True)	72	Receiver Channel 16 (Complement)
33	Trigger Out 0	73	Trigger Out 2
34	Trigger Out 1	74	Trigger Out 3
35	Trigger In 0	75	Trigger In 2
36	Trigger In 1	76	Trigger In 3
37	Ground	77	Ground
38	IRIG In	78	Ground
39	Ground	79	IRIG Out
40	RS-232 RXD	80	RS-232 TXD

2.4 Front Panel LED's

Four subminiature LED's, as listed in Table 2.4-I, indicate the various conditions of the module at the front panel. The LED's are located in a quadruple LED- Array on the physical interface daughterboard. The first LED is used for indication of ARINC429 data streams of one or more channels. If data are transmitted, the green LED will be flashed. The second LED is used for board fail indication. If the board or any of the selftest routines have failed, the red LED will still be illuminated after power-up. After power-up this LED is illuminated for app. 5 seconds. The third and fourth LED is used for error indication in a received data stream on any of the sixteen (eight) channels. If any error occurs, the third red LED will be flashed. The error event is stored and leads to an illumination of the fourth LED. During power-up or reset all LEDs are illuminated for selftest purposes.

Table 2.4-I Front Panel LEDs

LED Name	Color	Description
ACTIVITY	Green	LED flashes If data is transmitted on any channel.
FAIL	Red	LED illuminates if an error during the BIU selftest occurs.
RX-ERR	Red	LED flashes if an error on any channel is detected.
RX-ERR-LATCH	Red	LED illuminates if an error on any channel is detected (stored error).

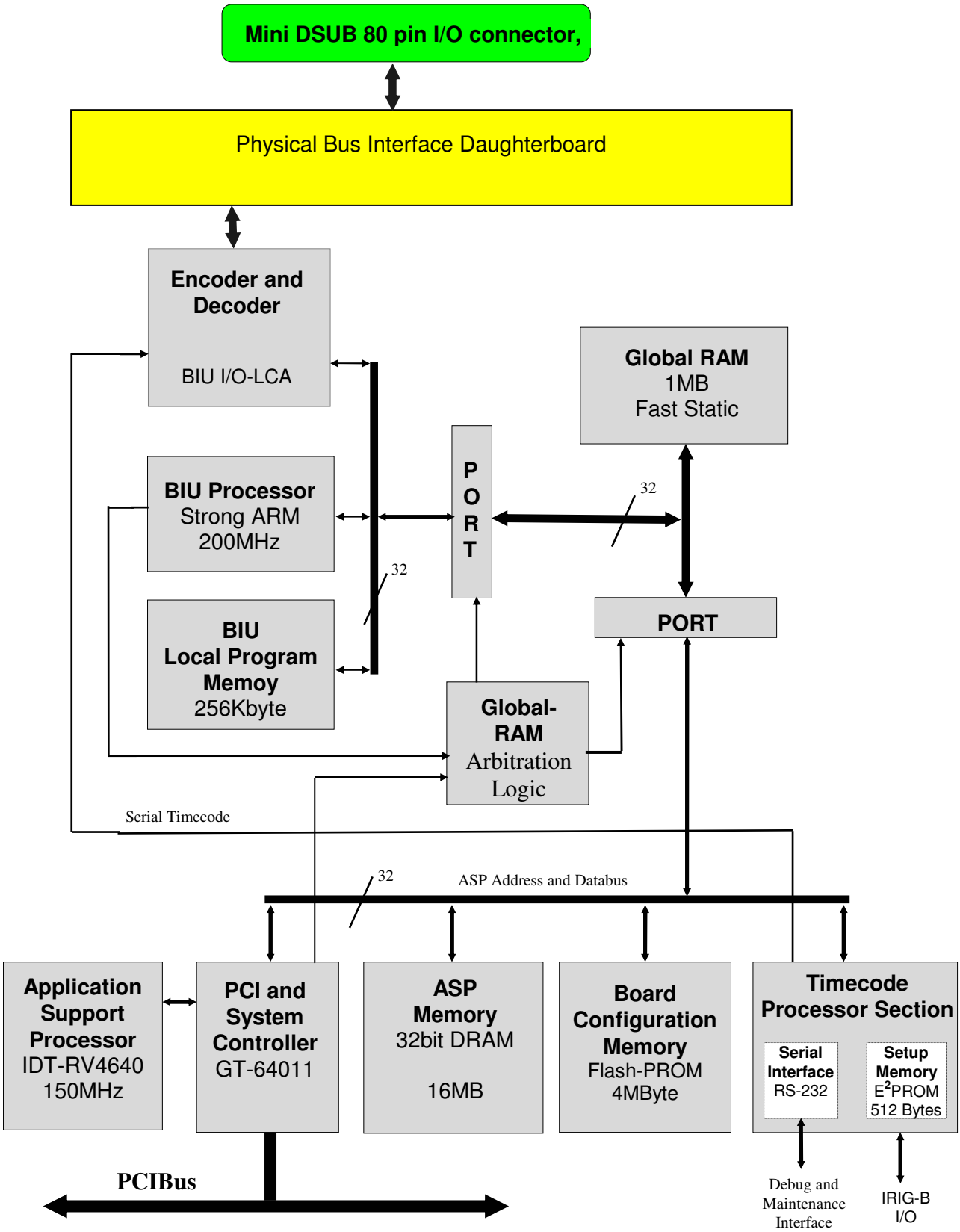
3. STRUCTURE OF THE API429-8/16

The structure of the API429 board is shown in Figure 3-1.

The API429 is comprised of five main sections:

❑ ASP Section	ASP with local Program Memory, PCI System Controller, and Board Configuration Memory
❑ BIU Section	BIP with local Program Memory and I/O-LCA
❑ Global RAM	Tri-port Arbitration Logic, Global RAM
❑ Time Code Section	Time Code Generation, and E^2PROM
❑ Physical Bus Interface (PBI)	Encoder / Decoder and ARINC receiver and transmitter

Figure 3-1 API429-8/16 Block Diagram



3.1 ASP Section

The ASP-Section is divided into six subsections:

- ASP Processor
- PSC (PCI and System Controller)
- ASP Program Memory
- Board Configuration Memory
- Time Code Processor Section with Board Setup Memory (E^2PROM)

  and Debug and Maintenance Serial Interface (RS-232)
- Global RAM Port

3.1.1 Application Support Processor (ASP)

The ASP is a 64bit IDT79RV4640 Processor based on the MIPS RISC architecture with a internal core speed of 150 MHz and a external Memory bus speed of 50Mhz. The Processor incorporates a 32 bit single precision floating point coprocessor on chip. Double precision floating point operations are supported via a software library.

The ASP is the master control processor and performs the following tasks:

- Runs the on board driver software
- Sets up the Global RAM for BIU Processor operation
- Configures the programmable BIU I/O LCAs with the Bit stream data from FLASH
- Provides the program data for the BIU Processors (stored in the FLASH)

3.1.2 PCI and System Controller (PSC)

The GT-64011 provides a single-chip solution for building a system with memory, I/O devices and PCI Bus interface around the IDT-79RV4640 processor.

The GT-64011 has a three bus architecture:

- A 32 bit address and databus interface to the IDT-79RV4640.

- A 22 bit address and a 32 bit databus interface to the memory and I/O devices.
- A 32 bit address and databus interface to the PCI Bus.

3.1.3 Time Code Generation

The Time Code generation is based on a IRIG B Time Code decoder. The Time Code Information is used for time-tagging and multi-channel synchronization.

The time tag on the board is generated in the following format:

Binary Coded Time Tag

Time Element	Number of bits
DAYS of year	9
HOURS of Day	5
MINUTES of Hour	6
SECONDS of Minute	6
MICROSECONDS of Second	20
Summary	46 (6 Bytes, stored in two 32bit words)

This comprehensive time tag information provides the API429 with a flexible, application dependent time tag for the avionics databus traffic.

3.1.4 Debug and Maintenance Interface

For debugging during hardware and Firmware integration as well as for maintenance purposes, a serial RS-232 interface is provided.

3.1.5 Global RAM Port

The Global RAM is shared between both BIU processors (BIP), the ASP and the PCI Bus. The ASP has access to the common Global RAM via a 32 bit wide data and 24 bit wide address port. The arbitration implements a round robin scheme to guarantee maximum latencies for all requests.

3.1.6 PCI Interface

The PSC interfaces directly with the PCI bus. The PSC can be either a master initiating a PCIbus operation, or a target responding to a PCIbus operation. The PSC incorporates 96-bytes of posted write and read prefetch buffers for efficient data transfer between the ASP / DMA to PCIbus, and PCIbus to host memory. The PSC becomes a PCIbus master when the ASP or the internal DMA engine initiates a bus cycle to a PCIbus device. The PSC configuration register set is PCI Plug and Play compatible.

3.2 Bus Interface Unit (BIU)

The Bus Interface Unit (BIU) implemented on the API429 module handles eight or four ARINC429 channels. The BIU provides a StrongArm RISC processor, a fast program and data memory, a large programmable Gate Array for I/O functions, and a fast port to the Global RAM.

3.2.1 Bus Interface Processor (BIP)

The BIP handles the real time critical control of the ARINC429 channel. The BIP has access to the Global RAM and receives its program (firmware) from the ASP during the initialization phase of the API429 module.

The BIP performs the following main tasks:

- Initializes BIU hardware including encoder and decoder.
- Executes a BIU power-up selftest.
- Services the encoders and decoders to handle the demanded bus traffic in real time.
- Stores the received data in the Global RAM as demanded.

The features of the used StrongARM processor include full 32 bit operation at a core speed of 200Mhz with a very low power consumption due to the 2.0V core power supply.

3.2.2 Program and Data Memory

A fast RAM is implemented as the program and data memory for the BIP using a single 64kx32 non pipelined synchronous static burst RAM (SSRAM) device. The RAM uses power saving 3.3V technique and is housed in a space saving high density 100-lead TQF-Package.

3.2.3 ARINC429 Encoder

The encoder converts the parallel data into a serial ARINC429 encoded data stream and appends the parity and the gap bits. The programmable frame times between two labels can be set in the range from 0 up to 255 ARINC429 bits.

The encoder provides the following error injection capabilities:

- Gap Error (-1 bit)
- Bitcount Error (+/- 1 bit)
- Coding Error (fixed at bit position 12)
- Parity Error (if no special transmission mode is chosen)

3.2.4 ARINC429 Decoder

The decoder converts the serial received data stream into a parallel data double word and generates additionally a 16 bit report for each received label. The decoder measures the gap time between two labels for gap error detection and bus load traffic detection.

The decoder provides the following error detection capabilities:

- Gap Error Detection
- Bit count Error Detection
- Coding Error Detection
- Parity Error Detection (if no special transmission mode is chosen)

For selftest purpose an internal selftest bus is used. Via two external signals the selftest mode can be activated. For the selftest mode 1, all units are configured as encoders in automatic mode. For the selftest mode 2, all units are divided in groups of four, each group is switched to its individual internal selftest bus, whereby the first unit is configured as an encoder in automatic mode, the remaining three units are configured as decoders.

3.2.5 External Trigger-Inputs and Outputs

Four trigger inputs and four trigger outputs are provided. The trigger outputs are TTL level signals. The trigger output signals are a high active strobe signal with a pulse width of app. 120 ns. The outputs are protected by a 100 Ω series resistor. A driver for the four trigger outputs with its protection are provided on the PBI. The trigger inputs are also TTL level sensitive signals. The trigger input signal is caught by a high to low transition of min. 100 ns. A driver for the four trigger inputs is provided on the PBI.

3.2.6 Global RAM Interface

The BIP has fast access to the Global RAM of the API429 module. This memory is shared between the BIU processor, the ASP and the PCI master of the PC.

3.3 Global RAM

The Global RAM is shared between the BIU, the local bus of the ASP section and the PCI interface. The databus of the memory is 32bit wide. The arbiter is running with a frequency of 50 MHz. and handles the prioritization of the bus requester in a round robin process. A standard high-speed static RAM is used for the Global RAM. The arbiter and control logic does the arbitration between the different ports.

3.4 Time Code Processor Section

The various functions of the Time Code Processor Section are:

- IRIG-B compatible Time Code Decoder and Encoder function.
- UART with an RS-232 interface for debug and maintenance purposes.
- E^2PROM to save module specific parameters.

This functionality is based on the single chip microcontroller that provides or can emulate most of the functions above. To transfer data between the microcontroller and the ASP an eight bit wide I/O port of the microcontroller is connected to the local bus of the ASP Section.

3.5 Voltage Supplies

All voltages needed on the board other than the standard +5V and +/-12 Volts from the PC-Supply are generated on the board. Several devices on the board require a +3.3V voltage, which is generated from +5V using a DC-DC Converter. The 2.0V needed for the StrongARM processor is generated from +3.3V using a linear regulator.

3.6 Physical Bus Interface Board

The Physical Bus Interface (PBI) is a plug-in board, which is mounted on the API429 main board. There are two ARINC429 PBI's implemented:

- eight channel ARINC429 interface board
- sixteen channel ARINC429 interface board

Both PBI's are identical except for the number of programmable channels. All ARINC429 - encoders and decoders as well as all the interface specific components are located on a the daughterboard. The encoders and decoders are implemented in two (one) 44000 gate equivalent loadable gate arrays. Because of the high current demands from the ARINC429 transmitters on the +/-12 Volt supplies and the fact that the -12V supply is typically very weak on standard Desktop and portable PC's (appr. 350 to 750 mA), the -12V supply for the line transmitters are generated via a DC-DC converter from the +5V. The PBI is equipped with a total of sixteen (eight) ARINC429 line transmitters and sixteen (eight) ARINC429 line receivers.

3.6.1 ARINC429 Line Transmitter Channels

The ARINC429 line transmitter provides the physical interface to the ARINC429 bus system. An off-the-shelf well proven transmitter device with adjustable rise and fall time and variable output voltage is used. The adjustable rise and fall time allows the user to adapt the signal

waveform to the transmission speed. To adapt to different transmit speeds the transmission rate can be varied in discrete steps between appr. 90- and 120Kbit on the high speed bus and between 11.5 and 16.0 on the low speed lines.

3.6.2 ARINC429 Line Receiver Channels

The ARINC429 line receiver provides a high differential input impedance of typically 50 kΩ to the ARINC429 bus signal. The bus signal is converted by that line receiver to TTL level. The additional selftest inputs can be used for system tests. The adjustable input filter allows optimised bus signal reception independent of high or low speed operation. To adapt to different transmit speeds the sampling clock rate can be varied in discrete steps between appr. 90- and 120Kbit on the high speed bus and between 11.5 and 16.0 on the low speed lines.

4. TECHNICAL DATA

PCI Interface: Fully compatible with PCI Standard (Revision 2.1)
5V card, 33Mhz, 32bit operation
Clock speed up to 33MHz with no wait states
Supports burst operation on PCI for efficient data transfer
Supports fast back-to-back transactions
One interrupt output to PCIbus.
Full PCI-Busmaster capability.

ASP Section: One 64bit RISC Processor IDT-79RV4640, with a core speed of 150 MHz and a external bus speed of 50 MHz, Implements 8Kbyte of internal instruction- and 8 KByte of data-cache. Integrates a 64 bit integer and a 32 bit (IEEE single precision) floating point unit
Low power dissipation of max. 2W @ 3.3V.

Memory: Eight Megabyte of 32 bit wide ASP local dynamic memory
Eight Megabyte 32 bit wide ASP-PCI shared dynamic memory
One Megabyte of 32 bit wide fast Global Static RAM shared between ASP, PCI and BIU processor.
256 KByte local SSRAM for BIU processor.

BIU-Section: 32 bit RISC Processor ARM-SA-110-CA with a core speed of 200MHz, an external bus speed of 50MHz,16kbyte of internal instruction and 16Kbyte of data-cache, low power dissipation of max 0.9W @ 2.0V.
Large (20000 gates) programmable Gate Array implements the interface to the ARINC encoder / decoders on the PBI.

Channels: Total of sixteen (eight) channels programmable as Encoder or Decoder.
The transmitter transmission rate and receiver sampling clock rate is controllable in the following discrete steps (setting controls all channels) :

Setting	Low Speed Rate	High Speed Rate
low	11.54KBit	92.3KBit
low+	12.31KBit	92.3KBit
nominal	12.50KBit	100.0kBit
nominal+	13.33KBit	100.0KBit
high	13.64KBit	109.1KBit
high+	14.55KBit	109.1KBit
highest	15.00KBit	120.0KBit
highest+	16.00KBit	120.0KBit

Encoder: Programmable Bitrate High / Low Speed (100 / 12.5 Kbit/sec)
Programmable gap between two labels in the range from 0 up to 255 ARINC-429 bits.
ARINC429-Label Bit-32 programmable as Parity or additional Data Bit

Error injection capabilities:

- Gap Error (-1 bit)
- Bitcount Error (+/- 1 bit)
- Coding Error (fixed at bit position 12)
- Parity Error (if no special transmission mode is chosen)

Decoder: Programmable Bitrate High / Low Speed (12.5Kbit / 100Kbit)
Valid Receive Range Transmission speed select +/- appr. 10%
ARINC429-Label Bit-32 programmable as Parity or additional Data Bit
Measurement of gap between two labels in the range from 0.0 to 58.75 bits with 0.25bit resolution.

Error detection capabilities:

-Gap Error Detection
- Bitcount Error Detection
- Coding Error Detection
- Parity Error Detection (if no special transmission mode is chosen)

Time Tagging:

IRIG B Time Tag

For absolute time tagging a special time code processor implements an IRIG-B decoder. If no external IRIG-B source is available a time code in IRIG B like format is generated and can be used to synchronise multiple boards or modules.

Decoder:

Resolution :	1 µs
Width:	1 Year (46 Bit)
Signal Waveform:	Amplitude modulated sinewave or square wave
Modulation Ratio:	3:1 to 6:1
Input Amplitude:	$0.5V_{p-p}$ to $5V_{p-p}$
Input Impedance:	> 10k Ohm
Coupling:	AC coupled
Time Jitter:	+/- 5 µs (typical, module to module) depending on input signal quality
Lock time:	1 to 5 seconds depending on input signal quality

Encoder:

Format:	AIM Standard (based on IRIG B format)
Absolute Accuracy:	+/-50ppm
Signal Waveform:	Amplitude modulated square wave
Output Amplitude:	$0.5V_{p-p}$ to $3V_{p-p}$ at 2kOhms Load
Carrier Frequency:	1kHz +/-50ppm

Maintenance: Except for the Emergency Boot Monitor Program the BIU Firmware, ASP driver software and hardware configuration data for the programmable logic is downloaded via the PCI Bus or the RS-232 maintenance and debug interface.

Bus Frontend: All interface specific components are located on a Physical Bus Interface (PBI) daughterboard.
Total of sixteen (eight) line receivers and line transmitters are implemented.

Line Transmitter: Programmable bus signal amplitude of 0 .. ± 11 V
(corresponds appr. with the setting of 0 to 150 on the eight bit DA converter)

High / Low Speed : 100 / 12.5 Kbit/sec

Rise and Fall time automatically switched via Analog Switches to meet the requirement for High / Low Speed operation

Line Receiver: Input Impedance A to B : typ. 50 kΩ
Input Impedance A/B to GND : typ. 25 kΩ

Input Filter capacitors are automatically switched via Analog Switches for optimum results on High / Low Speed operation

Connectors: One 80 pin mini DSUB connector, located on the PBI

ARINC429 : Sixteen (eight) receive and transmit line pairs.

Trigger In: TTL-Input, 1.0 K Pullup to 5V and 270pf EMV capacitor.
Falling Edge sensitive, Pulsewidth > 100ns

Trigger Out: TTL- Output with 100 Ohm series resistor, 270pf EMV capacitor,
High Pulse width strobe, 120ns duration.

IRIG-IN: AC-coupled appr. 10Kohm, 270pf EMV capacitor.
0.5 to 5.0 Vpp input voltage

IRIG-OUT: DC-coupled appr. 250 Ohm, 270pf EMV capacitor

Dimensions: PCI standard 'SHORT CARD', 174.6mm x 106.7mm.

Supply Voltage: Standard PC – Supply 5.0V +/- 5%, +/-12 Volt +/- 5%

Power (typical):		**API429-8**	**API429-16**
5V :	Idle:	9.0 Watts	10.5 Watts
	Operating:	11.5 Watts	13.0 Watts (*)
12V:	Idle:	1.2 Watts	2.4 Watts
	Operating:	1.5 Watts	3.0 Watts (*)

(*) The operating conditions are expecting almost unloaded transmit busses. If transmitting into the worst case load (400 OHM || 30000pF) the following additional power will be drawn by the each transmitter from the supplies (approximate values)

Padd [Watt] = Tx-DutyCycle[%] * 0.01 * 0.35[Watt] (on Low Speed. 12.5 Kbit/sec)

Note: Less than 20 mA is drawn from the -12V supply which is typically weak on standard desktop or portable PC's. Since the -12Volt necessary for the line transmitters is generated via an on-board DC-DC converter from the 5V supply.

Weight:	**API429-8**	appr. 250g
	API429-16	appr. 300g

Temperature:	0	to	+45°C. Standard Operating
	-15	to	+60°C Extended Temperature
	-40	to	+85°C Storage.

Humidity: 0 to 95% (non condensing)

5. NOTES

5.1 Acronyms

ARINC	AERONAUTICAL RADIO, INC.
ADC	Analog to Digital Converter.
ALBI	ASP Local Bus Interface
ARM	Advanced RISC Machine
ASP	Application Support Processor
BIP	Bus Interface Processor.
BIU	Bus Interface Unit.
DAC	Digital to Analog Converter.
DRAM	Dynamic Random Access Memory
EDO	Enhanced Data Output
EEPROM	Electrically Erasable and Programmable Read Only Memory
EPROM	Erasable Programmable Read Only Memory
FLASH	Page oriented electrical erasable and programmable memory.
IRIG	Inter Range Instrumentations Group
IRIG B	Inter Range Instrumentations Group Time code Format Type B
I/O	Input / Output
LCA	Logic Cell Array (XILINX - Programmable Gate Array)
MAC	Media Access Controller
PBI	Physical Bus Interface
PMC	PCI Mezzanine Card
PC	Personal Computer
PROM	Programmable Read Only Memory
PCI	Peripheral component interconnect
PSC	PCI and System Controller
RISC	Reduced Instruction Set Computer
RAM	Random Access Memory
SDRAM	Synchronous Dynamic Random Access Memory
SIMM	Single Inline Memory Module
SSRAM	Synchronous Static Random Access Memory
TCP	Time Code Processor
UART	Universal Asynchronous Receiver and Transmitter

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