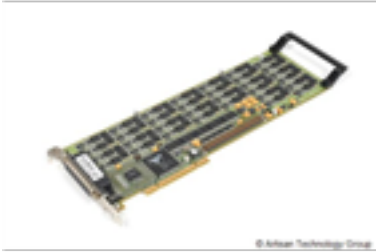
ICS ICS-610A-32A

32-Channel, 108 kHz/ch. Data Acquisition Board



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ICS-610

OPERATING MANUAL

Interactive Circuits and Systems Ltd.

February 2006

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1 INTRODUCTION

The ICS-610 is a PCI analog input board providing up to 32 differential input channels. It is currently being offered as the ICS-610A, a 2nd generation product. Note: The ICS-610 product is still available for legacy customers. All references in this manual to ICS-610 refer to both products unless otherwise specified.

The ICS-610 board offers the following features:

- Up to 32 differential input channels;
- 2-pole anti-aliasing filter consistent with the requirements of Sigma-Delta ADCs;
- Programmable gain;
- Built-in over voltage protection;
- Simultaneous sampling at rates of up to 108 kHz/ch;
- Software-selectable high-pass filter for low frequency rejection;
- External or internal clock and trigger;
- Internal clock programmable in steps of less than 20 Hz at output frequency;
- Greater than 90 dB Signal-to-noise ratio;
- 1 M Sample on-board swing buffer memory;
- Continuous, one-shot and transient (pre-trigger) data capture;
- Programmable-length PCI Bus interrupt;
- 33 MHz master/slave PCI interface
- Universal PCI Signaling Environment
- Optional FPDP and synchronization interface;
- Up to 32 ICS-610 boards can be operated synchronously to ensure simultaneous sampling;
- Comprehensive software device driver supporting Windows NT, Windows 2000, Windows XP and Windows Server 2003

1.1 Product Versions

The ICS-610 is available in a number of versions providing a different number of differential analog input channels to the board. The product version is given on a label on the product, and is represented as follows:

Version: **ICS-610y-x**

x	8, 16, 32	Number of Analog Input Channels
	32A	Max. 20 Vpp Full Scale Input

y	Blank	Original Product
	A	2nd Generation Product

2 GENERAL DESCRIPTION

Figure 1 shows a simplified block diagram of the ICS-610. The board includes up to 32 separate 24-bit Sigma-Delta ADCs to simultaneously digitize all channels at rates up to 108 kHz per channel. All inputs are differential in order to suppress common-mode noise. The ICS-610 includes signal conditioning for each channel.

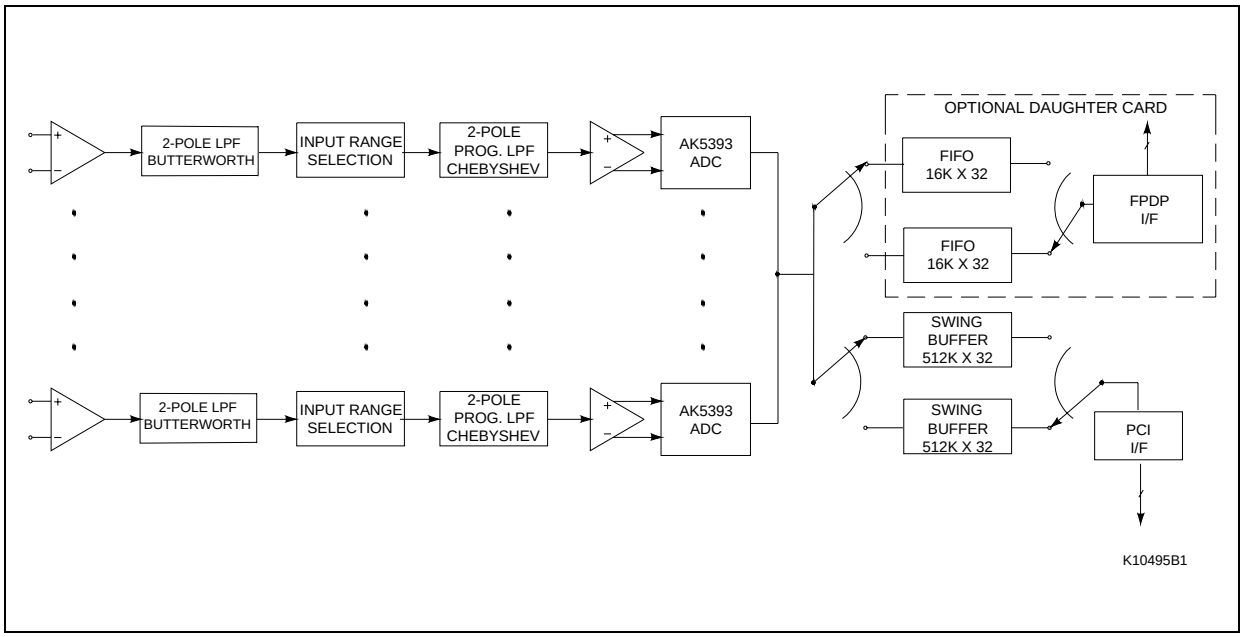


Figure 1 - ICS-610 Block Diagram (only two channels shown)

The differential signals at the front panel analog input connectors are buffered and converted to single ended signals. The signal for each channel then passes through a fixed two-pole, 75 kHz anti-alias filter with a Butterworth characteristic. The filter output is applied to an input range selection stage; the input voltage is selectable from one of four ranges that provide full scale outputs for inputs of 1 Vpp, 2 Vpp, 5 Vpp and 10 Vpp on each wire of the differential input. The ICS-610-32A product version has selectable inputs of 2 Vpp, 4 Vpp, 10 Vpp and 20 Vpp on each wire of the differential input. The signal then goes through a bandwidth selection stage. This programmable low pass filter provides the proper filtering for bandwidths of 0 – 2 kHz, 2 – 6 kHz, 6 – 20 kHz and 20 – 45 kHz.

After the filter stage, the signal is buffered and is then applied to the ADC. The serial output from the ADC is converted to a 24-bit parallel word before either being stored in a swing buffer memory for subsequent read-out over the PCI Bus, or being stored in a dual-banked FIFO on the optional FPDP daughter card interface.

Data is acquired in frames, where a frame contains one sample from each selected channel at a single sampling instant. Any numbers of channels (multiples of 2 only) up to the maximum for the board may be selected for operation, but the channels are always allocated in ascending order starting at channel one.

At the output, 24-bit signed (2's complement) samples are presented in the most significant 24 bits of each 32-bit data word; the least significant 8 bits are forced to zero. If preferred, the 24-bit data may be truncated to 16-bits. In this case, data from consecutive odd and even channels is combined to form a 32-bit word in order to make the most efficient use of bus bandwidth. This is known as the packed data

mode of operation. The PCI Bus interface supports block transfers. A PCI Bus interrupt at swing buffer swap can be generated to facilitate real-time operation.
The sampling clock for the ICS-610 board can be either an external clock or the board's programmable frequency internal clock. The clock frequency must be 128 times the output data rate for each channel when using the ADCs at double speed, and 256 times the output data rate when using ADC at normal speed. The output data rate is equivalent to the sampling rate of conventional ADCs. The input signal is sampled at one half the clock rate, which is 64 or 128 times the input signal bandwidth; this is known as the oversampling rate. This high sampling rate virtually eliminates the need for anti-aliasing. Each Sigma-Delta ADC uses internal digital filtering and decimation to produce an output at the desired sampling rate. The output data rate can be further reduced using a programmable on-board decimation register; however, care must be taken to ensure that the input signal is properly anti-aliased before decimating the ADC output.

The internal sampling clock of the ICS-610 can produce a user-specified sampling rate to within 20 Hz at the output rate. The clock is programmed by writing the appropriate clock frequency program word to the board's ADC clock frequency register. Software is included with the software device driver for the board to simplify computation of this programming word.

Data acquisition can be triggered using either an external signal or by software control. When using the external trigger, the signal is applied to the EXT_TRIG input and must conform to TTL signal levels. Acquisition starts when the signal changes from the low state to the high state.

The ADCs can be operated either in continuous or capture modes. In the continuous mode, data is continuously supplied to the selected interface upon application of a trigger signal until the acquisition is disabled. In capture mode, a fixed number of samples are acquired upon each application of the trigger. There are two ways in which this may be done. When using pre-trigger storage, the ICS-610 stores samples continuously before the trigger and acquires a programmable number of samples following the trigger (to a maximum of 32768 samples/channel in packed mode and 16384 samples/channel in unpacked mode if all 32 channels are active). When pre-trigger storage is not used, conversion starts at each application of the trigger and a programmable number of samples are acquired.

In capture mode without pre-trigger storage, the acquisition length and buffer length may be programmed separately. Thus it is possible to perform multiple capture sequences at each occurrence of the trigger, until the buffer is filled to the programmed length.

The ICS-610 board can generate PCI Bus interrupts at any user-programmed interval (number of samples acquired).

When using the optional FPDP daughter card, up to 32 ICS-610 boards may be configured as a cluster to provide simultaneous sampling with excellent synchronization. When operating in this configuration, one board must be configured as Sampling Master, while the remaining boards are configured as Slaves. This board generates the sampling clock and trigger (external or internal) and feeds them to all other boards in the cluster. The signals required to provide this functionality are routed on the P4 Local Bus connector located on the FPDP daughter card.

The ANSI/VITA 17 Front panel Data Port (FPDP) on the daughter card provides a 32-bit parallel, synchronous interface which is connected using ribbon cable. This may be used in point-to-point and multi-drop configurations to carry sampled data to other devices such as digital signal processors and storage devices. Please see the ICS website (see cover page) for names of FPDP partner companies.

When using multiple board configurations, the Front Panel Data Port (FPDP) can operate in a multiplexed fashion so that a composite data frame is generated on FPDP containing data from all channels in the cluster. The control signals required to generate composite FPDP frames with the correct timing are also included on the P4 Local Bus interface.

2.1 Specifications

ICS-610 Board	
Number of Differential Analog Inputs	8, 16 or 32
Input Impedance	>1 MOhm
Full Scale Input: ICS-610	1, 2, 5, 10 Vpp differential*
ICS-610-32A	2, 4, 10, 20 Vpp differential*
Maximum Safe Input Voltage	±37 V each wire
Fixed Anti-alias Lowpass Filter	2-pole Butterworth characteristic Cutoff frequency 75 kHz
Programmable Anti-alias Lowpass Filter	Signal Bandwidth Cutoff
	0 – 2 kHz 6.5 kHz 2 – 6 kHz 20 kHz 6 – 20 kHz 65 kHz 20 – 45 kHz 150 kHz
Maximum Input Signal Bandwidth	49 kHz
Input Sampling Rate	128 x Output rate for BW < 24 kHz 64 x Output rate for BW > 24 kHz
Output Rate (Effective Sampling Rate)	Max. 108 kHz/ch
	Min. 1 kHz/ch (External Clock)
	Min. 2 kHz/ch (Internal Clock)
Internal Sample Clock	Programmable in steps of 20 Hz (at output freq.)
Signal-to-Noise Ratio	> 90 dB
Total Harmonic Distortion	< -90 dBFS
Crosstalk	< -90 dBFS
On-board Storage	2 MSamples (16-bit truncated data) 1 MSample (24-bit data)
Output Word Length	32 bits packed for 2 channels 24 bits for 1 channel
PCI Bus Interface: ICS-610	32-bit 33 MHz Master/Slave
ICS-610A	Universal 32-bit 33 MHz Master/Slave
Power: ICS-610	3.8 Amps @ +5 V 0.79 Amps @ +12 V 0.66 Amps @ -12 V
ICS-610A	0.15 Amps @ +3.3 V 3.7 Amps @ +5 V 0.79 Amps @ +12 V 0.66 Amps @ -12 V
Operating Temperature	0 to +50 °C
Storage Temperature	-40 to +85 °C
Humidity	≤ 95% Rel. Humidity, non-condensing
Board Size	Full-length PCI
DC-610 Daughter Board (Optional)	
FPDP Interface	ANSI/VITA 17 (32-bit @ 160 MBytes/second)
Output Word Length	32 bits packed for 2 channels 24 bits for 1 Channel

Specifications subject to change without notice

* This voltage is on each wire of the differential pair, with respect to ground. When providing a single-ended input, the input must be twice this value in order to achieve a full scale output. The ICS-610 standard product cannot achieve full scale output when using a single-ended input on the 10 Vpp range. The ICS-610-32A product version cannot achieve full scale output when using a single-ended input on the 20 Vpp range. For details see Section 3.3.

2.2 Cooling

It is essential that the user provides adequate cooling air to the ICS-610 when it is installed in the target system. It is not possible to design high performance, high density A/D and D/A converter products with very low power consumption requirements. Higher power requirements translate to a greater requirement for heat dissipation. Many PCI backplane/enclosure systems are not designed to provide a flow of cooling air to the boards. In some cases, a flow of air is provided through the case, but this may not directly cool the boards. In other situations, no cooling arrangements exist, apart from a fan in the power supply unit and a separate one for the CPU. The ideal cooling arrangement consists of a laminar flow of cooling air over each surface of the board, with the warm air being removed to the external environment. However, this may not be possible to achieve at all times. We recommend that the user consider the following approaches:

1. Use a PCI backplane/enclosure system that has been designed to provide a laminar flow of cooling air to the boards.
2. Use a 'fan card' in a slot adjacent to the component side of the ICS-610.
3. Examples of such products may be found at:
   http://www.antec-inc.com/
   http://www.thecardcooler.com
4. Mount a fan in close proximity to the ICS-610.

2.3 Power

It is not possible to design high performance, high density A/D and D/A converter products with very low power consumption requirements. Many backplane/enclosure products do not measure or limit the power consumption of each PCI slot. However, some products are now taking this approach. We therefore recommend that the user should consider the PCI backplane/enclosure/system to be used with the ICS-610 and avoid products that specifically limit power consumption to 25 Watts.

3 DETAILED DESCRIPTION

3.1 Sigma-Delta Analog Conversion

The operation of a Sigma-Delta ADC differs significantly from traditional ADCs. A 1-bit analog-to-digital conversion is performed at a very high rate. The total quantization noise energy remains constant, but by spreading it over a wider spectrum, the amount in the frequency band of interest is reduced. The noise in the passband is further reduced by filtering (noise shaping). The oversampled signal is then lowpass filtered to remove the out-of-band quantization noise. This is achieved using a decimation comb filter and a FIR low-pass filter/decimator. The resulting output spectrum is equivalent to a traditional ADC.

For more information on Sigma-Delta analog-to-digital conversion techniques, see Reference [6].

3.2 Anti-Alias Filtering

The ICS-610 board uses an AKM AK5393 Sigma-Delta converter. This device is designed to sample the input signal at a rate which is greater than 128 times the signal bandwidth, when an output rate of up to 54 kHz is required. A 64x oversampling mode is also provided for output rates up to 108 kHz.

Since the Nyquist frequency is at least six (6) octaves away from the highest signal frequency, no more than a 3-pole filter is required for anti-aliasing. The input differential amplifiers buffering the analog inputs on the ICS-610 board, however, have a finite bandwidth. Further, in many applications, the input signal strength reduces naturally beyond the passband of interest. There are 2-pole, fixed Butterworth anti-alias filters provided on the ICS-610 filter (see Section 3.17) along with a programmable 2-pole Chebyshev filter.

The Sigma-Delta ADC limits the signal bandwidth to approximately 45.35% of the output data rate by digital filtering. The minimum output rate is 1 kHz (2 kHz when using the on-board programmable sampling clock). However, lower output rates can be achieved by using the on-board decimation feature. In this case, care must be taken to ensure that the input signal is bandlimited to less than half the final output rate in order to avoid aliasing.

3.3 Analog Inputs

The ICS-610 standard board accepts true differential analog input signals with peak amplitudes of 1 Vpp, 2 Vpp, 5 Vpp and 10 Vpp (2 Vpp, 4 Vpp, 10 Vpp and 20 Vpp for the ICS-610-32A version) on each differential leg (for a nominal gain control setting of 0 dB), as shown in Figure 2. The input impedance is 1 MOhm. The converted samples are presented as two's complement (signed) 24-bit values.

For best performance, differential input signals are recommended on both the ICS-610 standard board and ICS-610-32A product versions. If, however, a single-ended input must be used, the negative (-) input terminals can be tied together to a common analog ground, preferably the ground of the source. The input signal is applied to the positive (+) terminal. Users should note that, for ICS-610, it will not be possible to drive the input to full scale on the 10 Vpp range when using a single-ended input. This would nominally require a 20 Vpp input; the output will appear to clip at approximately 14 Vpp.

For the ICS-610-32A version, when using a single-ended input, it would normally require a 40 Vpp signal in order to achieve a full scale output; the output will appear to clip at approximately 20 Vpp.

The ICS-610-32A version linear range of operation does not extend to full scale input on the 20 Vpp range; the linear range limit is approximately 14 Vpp on each wire.

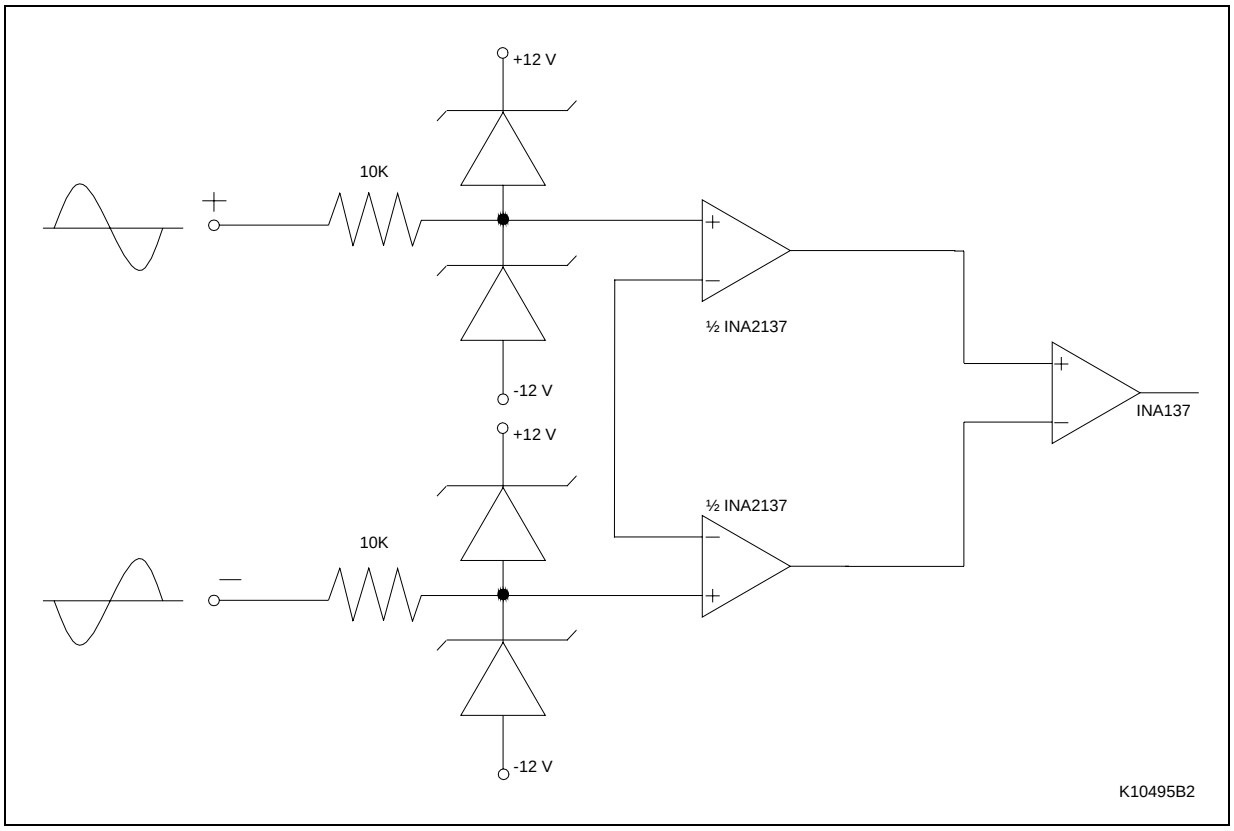


Figure 2 - ICS-610 Analog Input Configuration

3.4 Matched Channels

The ICS-610 offers excellent gain and phase matching across channels. Since the Sigma-Delta converters employ minimal analog technologies, such performance is expected. In the design of the ICS-610 board, extreme care has been taken in the generation of sampling clocks in order to assure precise simultaneous sampling on every card, and across cards in a multiple board system.

3.5 Sampling Clock

The ICS-610 board can be configured (by programming the control register) to use either the internal programmable-frequency sampling clock or an external clock. If used, the external sampling clock signal must be a TTL level signal and must be applied to the EXT_CLK pin on the front panel analog input connector. The frequency of the clock signal must be 128 times the desired output rate when operating in 64x oversampling mode, or 256 times the desired output rate when operating in 128x oversampling mode.

The buffered clock signal (whether internally or externally sourced) is available at the Local Bus connector pins on the optional daughter card in order to supply clock signals to other ICS-610 boards for synchronous operation. The board generating the clock signal must be programmed as the ADC Sampling Master so that the appropriate slave clock signals are routed to the P4 connector. All boards, including the master, see identical propagation delays for the clock signal, regardless of whether it is generated by an ICS-610 board or applied from an external source.

The maximum clock frequency is 13.824 MHz and the minimum clock frequency is 256 kHz (external) and 512 kHz (internal).

3.6 Output Decimation

The output rate can be further reduced using the on-board decimation feature. At the output, samples are automatically discarded, which has the effect of lowering the effective sampling rate. The maximum decimation factor that may be programmed is 256.

The user is cautioned that decimating the output requires anti-alias filtering (similar to using a conventional ADC) in order to bandlimit the input signal to a Nyquist frequency that is equal to half the final output rate. Thus, output decimation is only recommended for reducing the output rate below 1 kHz.

3.7 Clock vs. Channel Output Rate Relationship

The channel output rate is directly related to the frequency of the internal programmable or external clock signal frequency as follows:

Channel Output Rate = Fs / (2 x OSR x DF)

where Fs is the clock frequency, OSR is the oversampling ratio selected in the Control register (64x or 128x), and DF is the decimation factor (see Section 3.6).

Thus, for a maximum 13.824 MHz clock, using 64x oversampling and assuming no output decimation, the channel output rate is:

Channel Output Rate = 13,824,000 / (2 x 64 x 1)
= 108 kHz.

For a maximum 13.824 MHz clock, using 128x oversampling and assuming no output decimation, the channel output rate is:

Channel Output Rate = 13,824,000 / (2 x 128 x 1)
= 54 kHz.

For a minimum 256 kHz clock, when using the internal ADC clock and 128x oversampling (and assuming no output decimation), the channel output rate is:

Channel Output rate = 256,000 / (2 x 128 x 1)
= 1.0 kHz.

3.8 External Trigger

Triggering of acquisition can be either internally controlled from the PCI Bus by writing to the Control register, or externally controlled via the front panel analog input connector EXT_TRIG signal. In either case, the effect is to start enabling and inhibiting writes to the board's swing buffer memory. The operation is data frame-oriented; acquisition can only be started at the beginning of a frame or stopped at the end of a frame. A frame includes all channel data corresponding to a given sample period. Note that the ADCs are never stopped, they are always operating.

3.9 Modes of Operation

Three modes of operation are provided in the ICS-610 design:

- Capture mode without pre storage,
- Capture mode with pre storage,
- Continuous mode, which has no pre storage option.

In the Capture mode without pre storage, data is acquired for a programmable number of samples following the application of each trigger.

Important note: When using Capture mode without pre-trigger storage, the memory buffer length programmed must always be an integral number of acquisition lengths. See Figure 3.

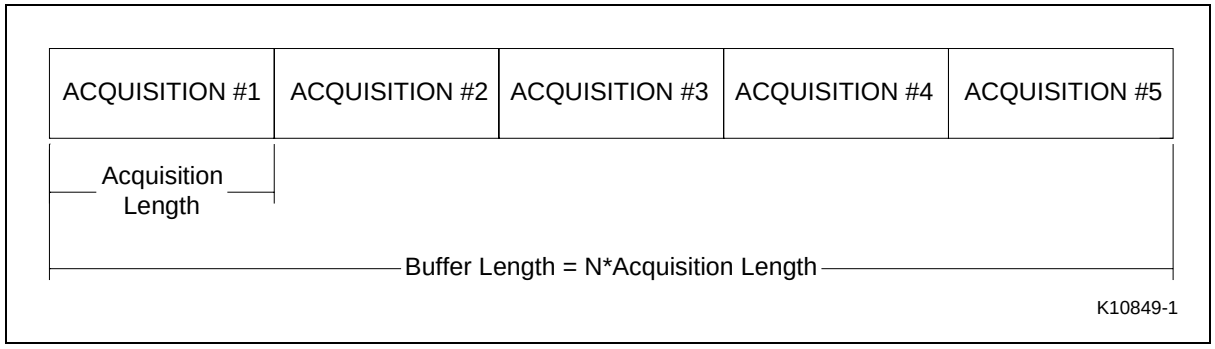


Figure 3 – Buffer Length in Terms of Acquisition Length

In the Capture mode with pre storage, the ICS-610 memory is used as a circular buffer of programmable length. The ICS-610 is armed by the user, and the control logic continuously fills the circular buffer with fresh data samples in anticipation of the trigger signal. When the trigger signal is received, the final acquisition length number of samples is stored in memory, and acquisition is automatically terminated.

To select pre-trigger storage of data in Capture mode, the Arm register must be written to as the last action of configuring the board. This will cause the board to start acquiring data. If the Arm register is not written to, pre-trigger storage will not occur.

Note: When using pre-trigger storage, acquisition length and memory buffer size may be independently set. Data stored in the memory buffer will be divided into two sections: data acquired before the application of the trigger, and data acquired after the application of the trigger. See Figure 4.

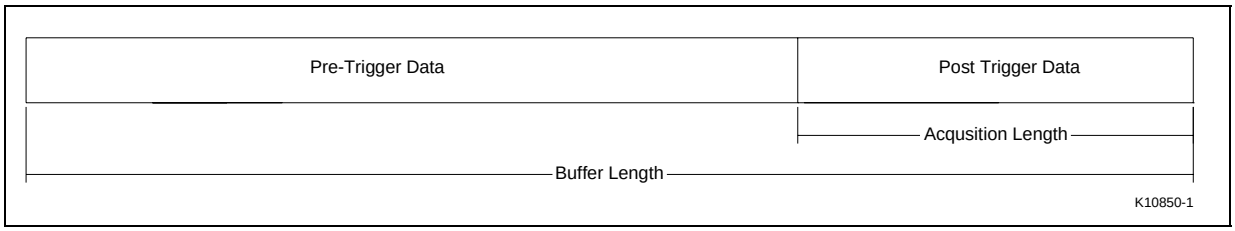


Figure 4 – Trigger Data Storage

In the Continuous mode of operation, acquisition begins upon application of the trigger and continues until the board is disabled.

3.10 Data Packing

Data packing is available on both PCI and FPDP interfaces. 24-bit resolution is provided on the ICS-610, and when unpacked data is selected (CR<04>), it drives data on only the most significant 24 bits of each 32-bit PCI or FPDP word; the least significant 8 bits are read as zeroes. When packed data is selected, the 24-bit samples are truncated to 16 bits and two samples are contained in each 32-bit FPDP or PCI word, with the lower channel number in the upper 16 bits of each word.

3.11 Optional FPDP Interface

The ANSI/VITA 17 Front Panel Data Port (FPDP) is a synchronous parallel data transfer bus which uses ribbon cable. It is ideally suited to the requirements of high speed real-time data transfer. Since only one bus master is allowed, and there is no addressing on the bus, the maximum possible bandwidth is available for data transfer. FPDP provides a simple and inexpensive mechanism for off-loading data from PCI Bus.

The FPDP protocol for data transfer is supported by all ICS current products. An 80- pin ribbon cable connector is provided for the FPDP (see APPENDIX D).

When unpacked data is selected (see Section 3.10), the undriven least significant 8 bits of the 32-bit bus contain zeroes.

The FPDP burst rate (Data Strobe frequency) is software programmable up to 20 MHz. In addition to the Data Strobe signal, positive-logic ECL differential clocks (+PECL Strobe & -PECL Strobe) are also supplied in order to support longer cable lengths, high speed operation, and greater immunity from clock-related problems.

The Front Panel Data Port interface operates using two FIFO memories in a swing buffer configuration. During one frame, data is converted and written to one FIFO memory, while the FPDP interface reads data from the other and transmits it over the FPDP cable. At the end of the frame, the two banks switch. Before any new ADC data is written to the swapped FIFO memory, it is automatically reset to ensure channel synchronization. If the synchronization is somehow lost, this scheme ensures that the synchronization is recovered in the next frame.

By programming the frame length register, the user can set the bank switch to occur after storing a specified number of frames.

3.12 FPDP Timing Limits

When using the FPDP in a multiple board configuration, it must be noted that the maximum FPDP data rate is 20 MHz. The value programmed for the FPDP Data Strobe frequency using the FPDP Clock Frequency register should not exceed this value (see Section 5.15 and APPENDIX A). The user must ensure that whatever FPDP Data Strobe frequency is programmed is sufficient to provide the data throughput required by the selected sampling frequency. The minimum required data strobe rate is the sample output frequency multiplied by the number of channels programmed for the system (i.e. for all ICS-610 boards connected on the same FPDP). This channel count is programmed in the Master Control register.

At the 108 kHz maximum channel output rate, approximately 190 channels can be used (108 kHz x 190 = 19.7 MHz). Note that the on-board decimator reduces the output rate. If the decimator is used, this should be taken into account when calculating the FPDP throughput and required Strobe frequency.

In cases where the user's requirement would exceed the maximum transfer rate of FPDP, it is possible to set up multiple board configurations with multiple FPDP outputs. This is possible because the Sampling Master and FPDP Master functions of the ICS-610 are separate. By configuring a system with a single Sampling Master and multiple FPDP masters, the cluster of ICS-610 boards will all sample synchronously, but will output data on two or more FPDP cables. Details of board configuration are given in Section 4.

3.13 PCI Bus Interface

The ICS-610 implements a 33 MHz, 32-bit, PCI Bus Master/Slave interface compliant with the PCI 2.1 specification, using the V3 Semiconductor V360EPC integrated circuit. At power-on, the operating system will automatically set the PCI base addresses for the board.

Important note: The data on the PCI Bus is in little-endian format, i.e. ascending byte address read from LSB to MSB of the data.

3.14 Interrupts

When enabled, the ICS-610 will generate a PCI interrupt when a swing buffer swap occurs. To enable the interrupt, the ADC Interrupt Enable bit in the Interrupt Mask register must be set.

When an interrupt occurs, the user may transfer data using either conventional or block transfer cycles. The swing buffer input side should be completely emptied in order to prevent a further interrupt before the next swing buffer swap.

3.15 Block Transfers

The ICS-610 can act as either a master or a slave device for block (DMA) transfers on the PCI Bus. When using the V360EPC DMA Controller, chained DMA transfers are not supported. An interrupt can be generated at DMA transfer completion.

When addressing the ADC Data/ Diagnostics area of the PCI Bus memory map, successive reads need not be to sequential addresses. Any access within the valid address range from the base address (see above) will read the next data value from the swing buffer. It is valid to use the same address on every access, if desired.

3.16 Converter Programmable Features

3.16.1 Converter Calibration

The AKM5393 converter requires calibration before use. Calibration occurs automatically following power-up and whenever the ADC sampling clock frequency is changed.

3.16.2 Converter High Pass Filter

The AKM AK5393 converter includes a first order high pass digital filter at the output, which may be used to remove DC offset. The filter 3 dB cut-off frequency is 1.0 Hz when the output rate is 48 kHz, and it scales linearly with frequency. The filter is enabled by setting bit 11 of the control register.

3.17 Signal Conditioning

The signal conditioning feature provides up to 32 channels of programmable input voltage range selection and programmable input signal bandwidth selection. The block diagram in

Figure 1 shows the arrangement of the signal conditioning elements.

The design includes pre-gain anti-alias filters consisting of 2-pole low pass filters with a Butterworth characteristic. The cut-off frequency of these filters is fixed at 75 kHz.

There are four input voltage ranges that can be selected under software control: 1 Vpp, 2 Vpp, 5 Vpp, and 10 Vpp on each differential input wire for the ICS-610 standard product and 2 Vpp, 4 Vpp, 10 Vpp & 20 Vpp for the ICS-610-32A product version on each differential input wire.

The 2-pole post-gain low pass filter has a Chebyshev characteristic and is programmable to select the desired input signal bandwidth. There are four input bandwidth selection ranges as follows. The signal band is considered to extend from DC to one of the following ranges:

Input Signal Bandwidth	Post-Gain Filter Selection
0 – 2 kHz	6.5 kHz
2 – 6 kHz	20 kHz
6 – 20 kHz	65 kHz
20 – 45 kHz	150 kHz

3.18 Multiple Board Configurations

The ICS-610 is designed to allow simultaneous sampling across all channels on a board, and also across all channels on multiple boards. The optional FPDP daughter board must be present for the latter feature to be used, even if FPDP output is not used. To facilitate multiple board clusters, timing and external clock/trigger signals are bussed on the P4 Local Bus cable. In addition, if the Front Panel Data Port (FPDP) is used for data output, multiple ICS-610 boards may be bussed on the same FPDP cable.

Several multiple board cluster configurations are possible:

- All ICS-610 boards on one Local Bus cable, data read over PCI Bus from each board
- All ICS-610 boards on one Local Bus cable and on one FPDP cable
- All ICS-610 boards on one Local Bus cable, and on two or more FPDP cables

The latter case addresses the situation where a single FPDP cable would not have sufficient throughput, or where the FPDP/R- (receiver) board has insufficient throughput and multiple receiving boards must be used.

For the purposes of correctly driving and terminating bussed front panel signals, there are four possible software-controlled configurations for an ICS-610 board. These are:

- Master - the board drives timing signals and terminates received signals
- Mid-Slave - the board does not terminate or drive signals except data lines
- End-Slave - the board terminates timing signals and drives data lines
- Stand-alone Master - the board drives and terminates all signals

These classifications are applicable to both Local Bus and FPDP operation. It is possible for a board to be a Local Bus Mid-Slave but an FPDP Master, FPDP End-Slave or FPDP Stand-alone Master. The Master board must be located at one end of the cable. The End-Slave is located at the opposite end of the cable to the Master. The Mid-Slaves are located in between the Master and End-Slave boards. In a two board system, only Master and End-Slave configurations apply. The Stand-Alone Master refers to a one board system. The required Control register settings are determined by which of these four cases applies to the board in question. Also, switch settings are affected by whether a configuration uses internal or external clock (EXT_CLK) and trigger (EXT_TRIG) signals.

In PCI Bus systems, it is sometimes difficult to be sure which board is the master and which is the slave. In general, board PCI Bus address spaces are allocated by the BIOS in sequence from one end of the bus to the other, but it may not be immediately apparent which the starting end is. To resolve this uncertainty, a test should be done in which all boards are inserted in the system, and only one board is operated (as a stand-alone master). This board should be at one end of the group. An analog signal should be applied to channel 1 of each board in turn. It will then be apparent which board is the selected board, indicating which end of the bus is the starting end for PCI configuration.

When operating multiple boards, and reading data over PCI Bus (not FPDP), the last board to be read following each swing buffer swap interrupt must be the master board, in order to ensure that buffer swap signals required by the slave board/s are correctly generated.

If the ICS-610 board/s is/are connected to one or more Digital Signal Processor (DSP) or Array Processor boards using the FPDP, the DSP board/s should be installed in the chassis as the End-Slave of the FPDP cable (i.e. the ordering should be Master, Mid-slaves, End-Slave, DSP). If FPDP is not being used, the position of the DSP board/s in the chassis with respect to the ICS-610 boards is not important. The Master board (ICS610/0), should be inserted in the lower numbered PCI slot and should be initiated first by the driver. Slave board/s should be inserted in higher numbered PCI slot/s than the Master and should be initialized after the Master board. For example, the Master board is installed in slot 10 and the Slave boards should be inserted in slots 12 and higher.

4 HARDWARE CONFIGURATION

This section provides information necessary for hardware preparation of both single board and multiple board ICS-610 systems. Figure 5 shows the position of the switch block on the ICS-610 motherboard. There are no switches on the daughter board.

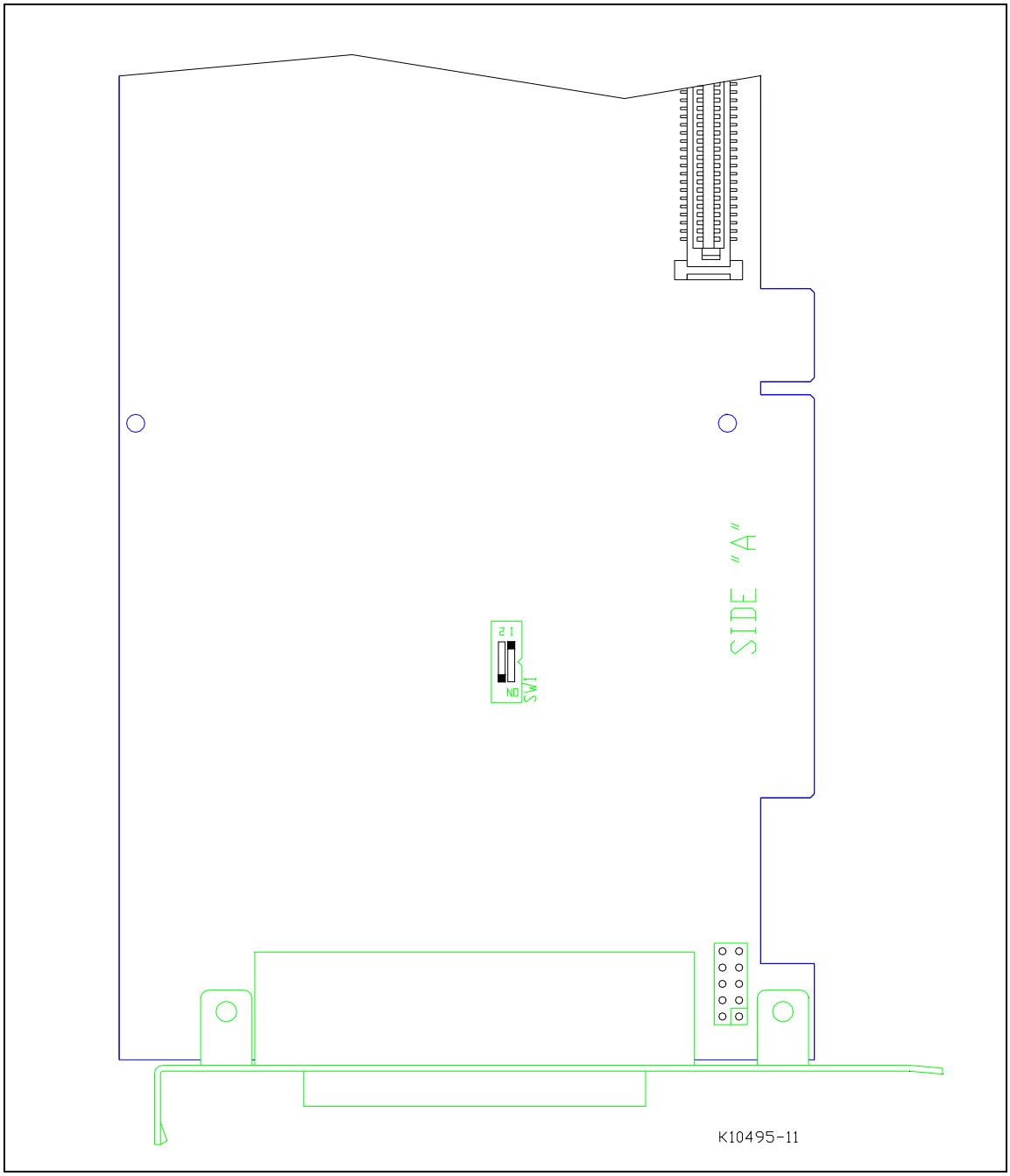


Figure 5 - ICS-610 Switch Locations

4.1 Functions of Board Switches

The ICS-610 has a switch block that must be configured by the user according to the required operating configuration. Figure 5 shows the location of this switch block on the ICS-610 motherboard.

4.2 External Clock and Trigger Terminations

Switch block SW1 is used to connect parallel (pull-up/pull-down) resistive terminations to the External Clock and Trigger signals, as shown in the following table. These are required if the user chooses not to use serial terminating resistors at the signal transmitter/s. The resistive terminations are 220 Ohm pull-up to +5 VDC and 330 Ohm pull-down to ground on each signal.

Functions of the P4 Local Bus can be programmed by software using the Control Register (see Section 5.7). When connecting external clock and/or trigger signals to a multiple board FPDP configuration, the signals must be connected and terminated on the sampling master board. The external clock signal must be applied as a TTL level signal to pin 1 of the Analog Input connector. The external trigger signal must be applied as a TTL level signal to pin 2 of the Analog Input connector. The rising edge of the external trigger will cause sampling to start, if external triggering has been selected.

SWITCH	FUNCTION (When switch in “ON” or Closed Position)
SW1-1	Terminate External Trigger Input
SW1-2	Terminate External Clock Input

4.3 Front Panel Data Port (FPDP) Connections

The FPDP provides a bus style interface between multiple ICS-610 boards and one or more Digital Signal Processor (Array Processor) boards. Up to 32 ICS-610 boards may be linked on a single FPDP connection. Figure 6 shows, as an example, how four ICS-610 boards can be bussed together. The 80-pin ribbon cable busses the four FPDP outputs, while the 26-pin Local Bus ribbon cable busses the synchronization signals. The Control Register FPDP Master bit (CR<07>), FPDP term bit (CR<08>) and ADC Master bit (CR<05>) must be set on the master board. The ADC Term bit (CR<06>) must be set on the End-Slave board. None of these bits must be set on Mid-Slave boards (if present).

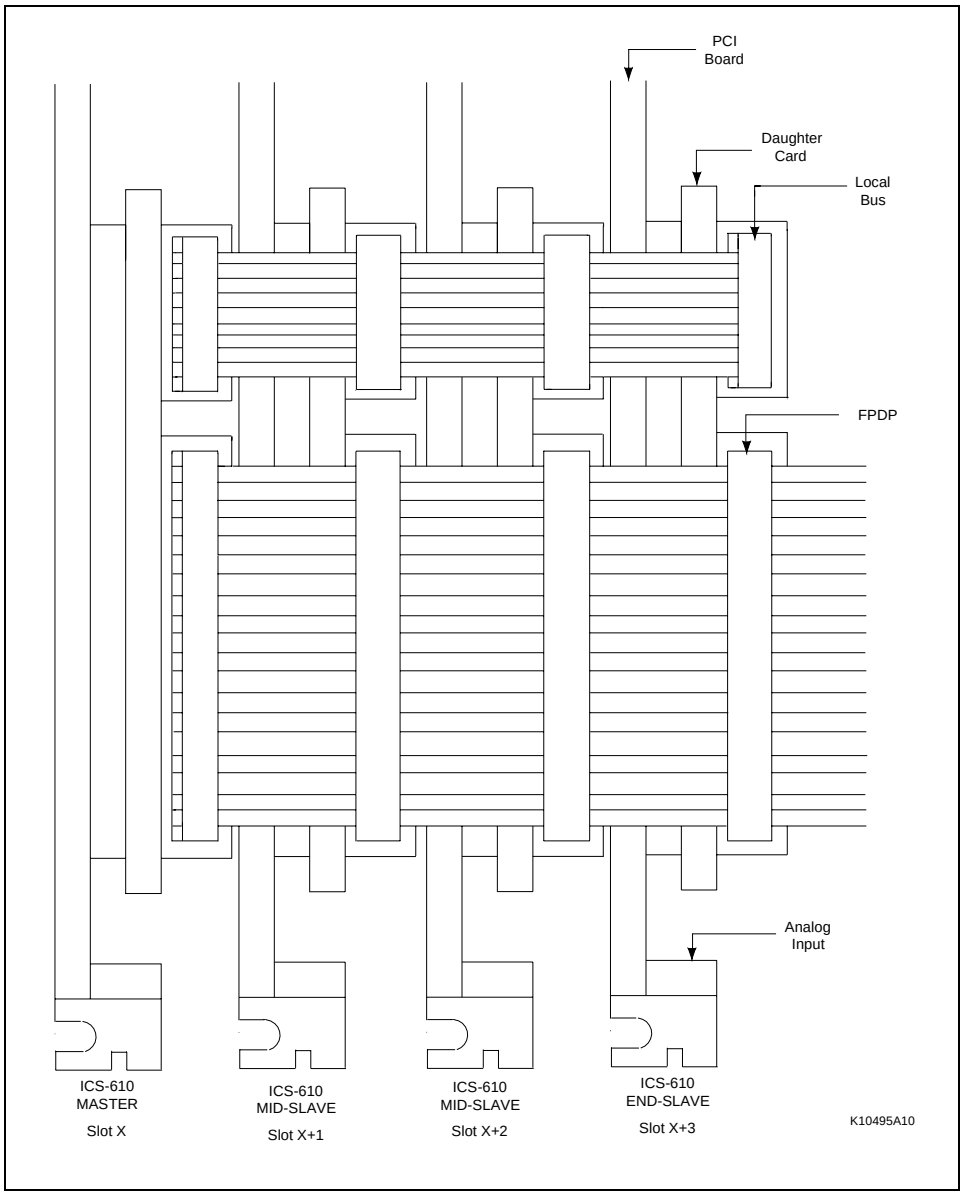


Figure 6 - ICS-610 FPDP and Local Bus Connections

5 PROGRAMMING MODEL

The ICS-610 PCI Bus Memory and I/O Map are shown in Table 5.1 below. The individual bit fields of the registers are shown in Figure 7 and Figure 8. Detailed register descriptions are given in the following sections. All programming and control of the ICS-610 is accomplished through the PCI Bus interface using 32-bit transfers. All control register bits that are not defined have no effect on the operation of the ICS-610. All undefined bits may be read as zero or one.

5.1 General Notes

Individual bits in the 32-bit registers are referred to in braces. e.g. CR<00> corresponds to ICS-610 Control register bit 0, and MCR<09:00> refers to Master Control register bits 9 through 0, inclusive.

Table 5.1 - ICS-610 Memory Map

Register	PCI Bus Address	Type
V360EPC Configuration	PCI_IO_BASE	Read/Write
ICS-610 Register Set	PCI_BASE0 + 0x00000000	
ADC Data/Diagnostics area	PCI_BASE1 + 0x80000000	Read Only/Write Only
DMA Chain Memory	PCI_BASE1 + 0xE0000000	Read/Write

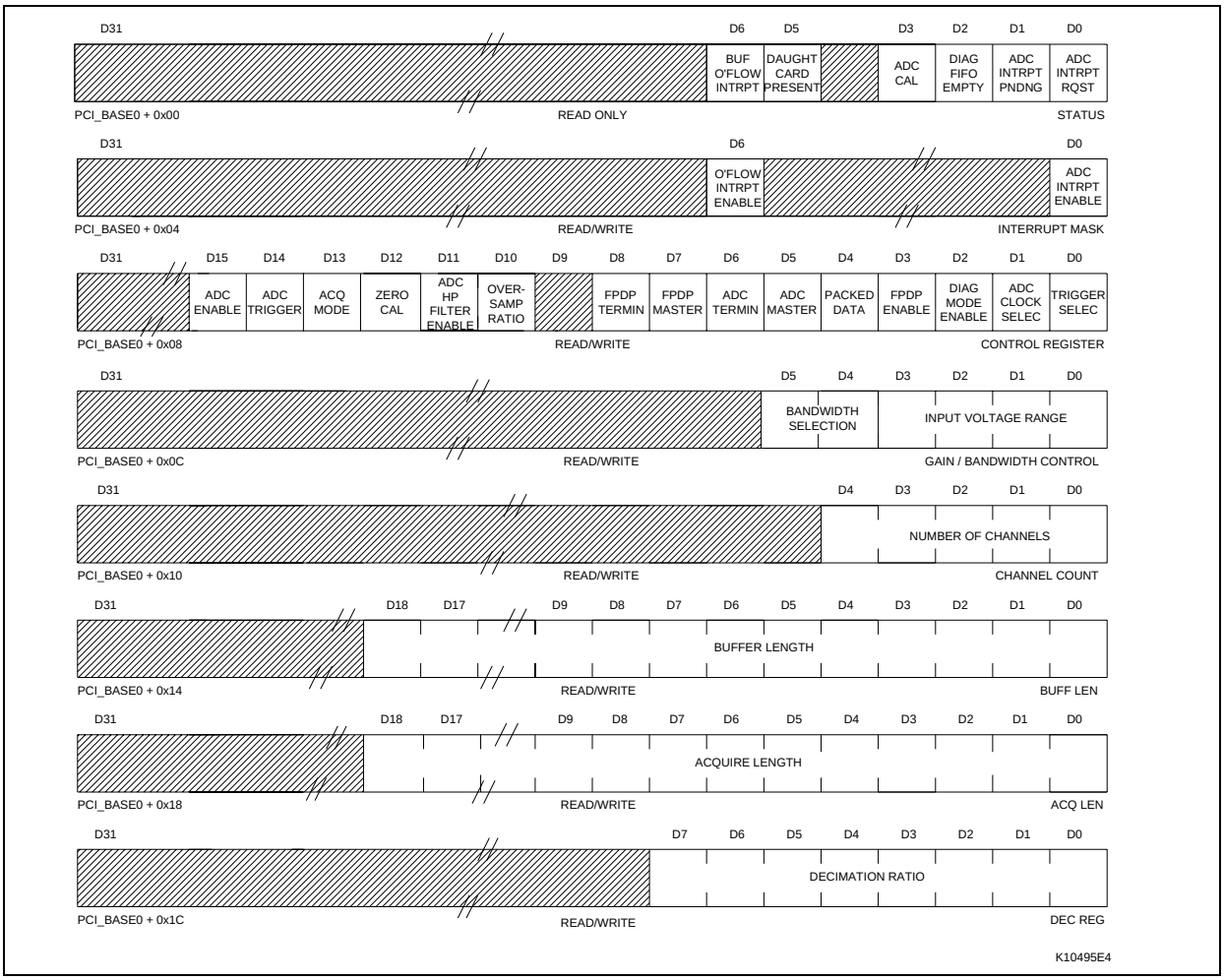


Figure 7 - ICS-610 Register Definitions

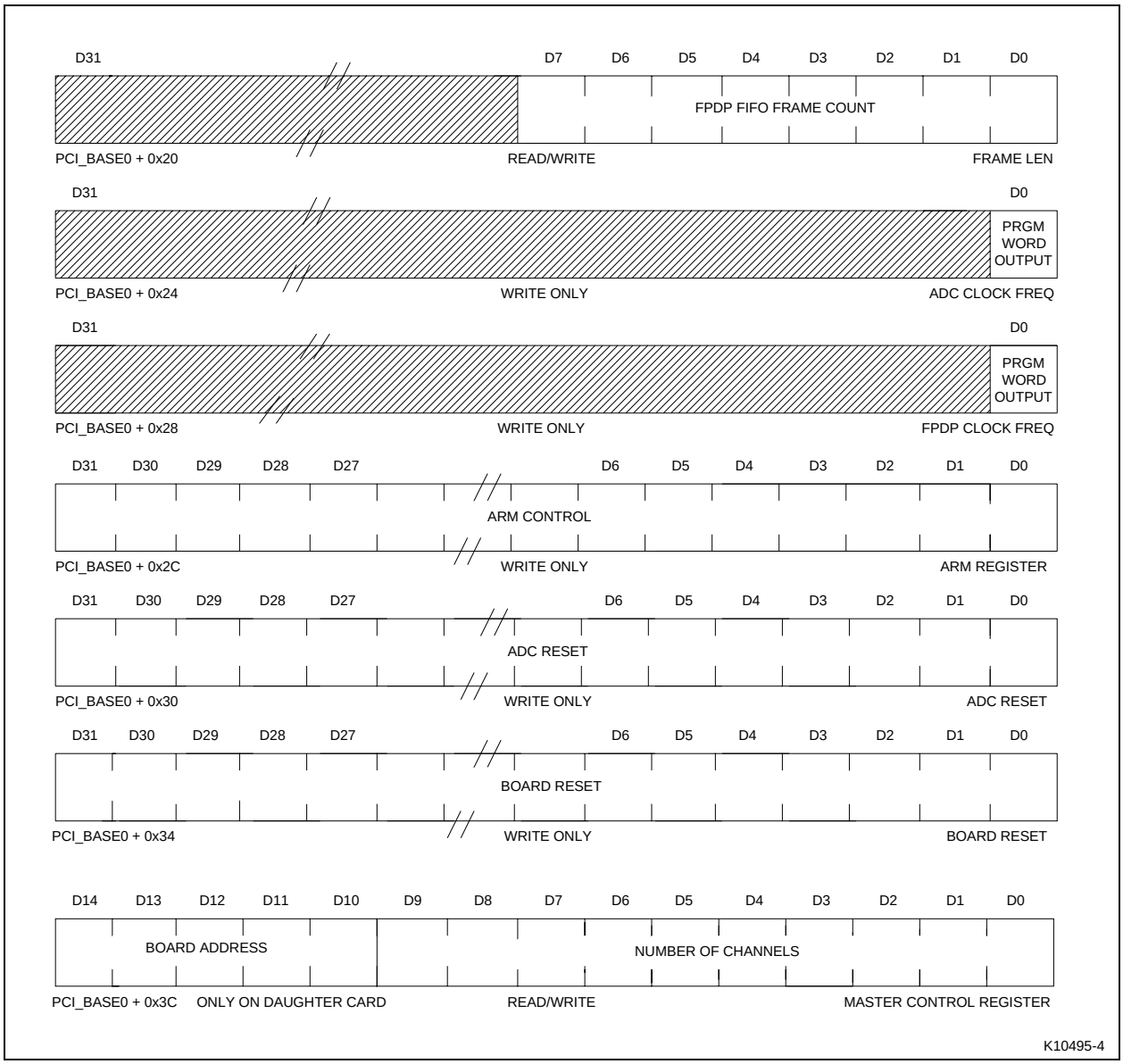


Figure 8 - ICS-610 Register Descriptions (Cont'd)

5.2 V360EPC Registers

The ICS-610 uses the V3 Semiconductor V360EPC PCI bus interface chip to handle all PCI bus communications. Full details of the V360EPC may be found in the V360EPC PCI Controller Data Book (see Reference [3]). Descriptions of the V360EPC registers, that may be needed when programming the ICS-610, are given in Table 5.2.

As with any PCI Bus device, the V360EPC has a unique 256-Byte region called the Configuration Header Space, or just Configuration Space (see Reference [3]). It is mandatory that portions of this configuration header are addressable in order for a PCI agent to be in full compliance with the PCI specification.

Following power-up, the V360EPC downloads the contents of the Configuration Space from an EEPROM device on the ICS-610. These values can be read at any time after power-up. The operating system may modify parts of them.

Five registers are used to define the PCI Bus base addresses and address ranges (sizes) of the three apertures used for access to the V360EPC and the ICS-610 register and data areas. The operating system must perform configuration of PCI Bus devices following power up in order to establish and configure these registers. The user cannot access the ICS-610 until this process has been completed.

PCI_IO_BASE:	Base address of Configuration Space. Points to the V360EPC register set. This register is referred to as PCI BAR0 in the PCI specification.
PCI_BASE0:	Base address of aperture 0. Points to the ICS-610 register set. This register is referred to as PCI BAR1 in the PCI specification.
PCI_BASE1:	Base address of aperture 1. Points to the ADC Data/Diagnostic area. This register is referred to as PCI BAR2 in the PCI specification.
PCI_MAP0:	Defines the range (size) of aperture 0 and mapping address.
PCI_MAP1:	Defines the range (size) of aperture 1 and mapping address.

The vendor and device identification information is contained in address offsets 0x2C and 0x2E, respectively, from the base of the configuration register area. These 16-bit read-only registers contain the following information:

Sub-Vendor Identification	0x1464
Sub-Device Identification	0x0610

Other relevant register descriptions are given in Table 5.2. For a full description of the V360EPC register set, consult Reference [3].

Each bit in the V360EPC registers is readable and writable according to one of the following designations. Those marked with an asterisk (*) apply to the PCI Configuration Registers only and comply with the PCI specification to provide the required PCI configuration header.

R: Read only – bits are internally driven and cannot be modified.

FR*: Firmware Initialized, Configuration Read Only – these bits are initialized after a system reset by downloading via the serial EEPROM device or by the local bus master. Once 'FR' bits are loaded they may be locked from further modification by setting the LOCK bit in the SYSTEM register.

W: Write only. Typically used to issue commands.

FRW*: Firmware Initialized, Configuration Read/Write – Initialized at boot-time but can be either read or written from the PCI and Local buses.

RW: Read and Write.

All reserved register bits read back as zeros.

Table 5.2 - V360EPC Operation Register Descriptions

Register	Mnemonic	Type	Reset Value	Offset	Description	
PCI_VENDOR	VENDOR	FR	11B0H	0x00	Vendor ID (V3 Semiconductor Inc.)	
PCI_DEVICE	DEVICE	FR	see text	0x02	Device ID Reads back as a value representing V360EPC.	
PCI_CMD				0x04	This is a register required by the PCI specification	
PCI Command Register	-	R	0H		PCI_CMD <15:10>	Reserved.
	FBB_EN	FRW	0H		PCI_CMD <09>	Fast Back-to-Back Enable. 1 = EPC will perform fast back-to-back transfers when bus master. 0 = EPC will not perform back-to-back transfers.
	SERR_EN	FRW	0H		PCI_CMD <08>	System Error Enable. Enable system error. If PAR_En (bit 6) is also enabled, then /SERR is driven in response to an address parity error.
	-	R	0H		PCI_CMD <07>	Reserved.
	PAR_EN	FRW	0H		PCI_CMD <06>	Parity Error Enabled. When set, EPC will report PCI parity errors.
	-	R	0H		PCI_CMD <05>	Reserved.
	-	R	0H		PCI_CMD <04>	Reserved.
	-	R	0H		PCI_CMD <03>	Reserved.
	MASTER_EN	FRW	0H		PCI_CMD <02>	PCI Master Enable. When set, V360EPC will act as PCI Bus master (i.e. assert /REQ). (Note: Clearing this bit effectively prohibits any local bus reads/writes to PCI space. If PCI Bus mastering is disabled, all local bus writes to PCI space, and all DMA transfers destined for PCI space, will be queued in the Local-to-PCI FIFO until this bit is set, or the FIFO is full).
	MEM_EN	FRW	0H		PCI_CMD <01>	Memory Access Enable. When set, V360EPC will respond to memory accesses on the PCI Bus.

Register	Mnemonic	Type	Reset Value	Offset	Description	
	IO_EN	FRW	0H		PCI_CMD <00>	I/O Access Enable. When set, V360EPC will respond to I/O accesses on the PCI Bus.
PCI_STAT	PAR_ERR	FRW	0H	0x06	PCI_STAT <15>	Parity Error Enable. Set (1) in response to a parity being detected on the PCI Bus. Cleared by writing '1' to this bit.
	SYS_ERR	FRW	0H		PCI_STAT <14>	System Error. Set (1) in response to system error being detected by this device and reported on the /SERR pin on the PCI Bus. Cleared by writing '1' to this bit.
	M_ABORT	FRW	0H		PCI_STAT <13>	Master Abort. Set (1) in response to a master abort being detected during transaction in which the EPC was acting as a bus master. Cleared by writing '1' to this bit.
	T_ABORT	FRW	0H		PCI_STAT <12>	Target Abort. Set (1) in response to target abort being detected during transaction in which the EPC was acting as a bus master. Cleared by writing '1' to this bit.
	-	R	0H		PCI_STAT <11>	Reserved.
	DEVSEL	FR	0H		PCI_STAT <10:09>	Device Select Timing. Programmable during initialization for the benefit of other PCI Bus masters. Doesn't affect the operation of the EPC.
	PAR_REP	FRW	0H		PCI_STAT <08>	Data Parity Error Report. Set (1) whenever the EPC acts as a bus master and observes the /PERR signal being driven. The PAR_EN bit in PCI_CMD must also be enabled for this bit to be set. Cleared by writing '1' to the bit
	FAST_BACK	FR	0H		PCI_STAT <07>	Fast-Back-to-Back Target Enable. Used to indicate to other bus masters the ability of this device to respond to fast back-to-back transfers. Note: the state of this bit will not effect the internal operation of the EPC and it will always respond properly to fast back-to-back transfers.

Register	Mnemonic	Type	Reset Value	Offset	Description	
	-	R	0H		PCI_STAT <06:00>	Reserved.
PCI_BASE0 (Only available when I2O mode is disabled)	ADR_BASE	FRW	0H	0x14	PCI_BASE0 <31:20>	Base Address. If the value of ADR_BASE matches that of AD[31:20] during the address phase of a PCI access then a match is detected. A larger address space can be decoded by changing the ADR_SIZE field in the PCI_MAP0 register. This will mask off some of the lower bits in this field to allow automatic configuration software to determine the size of the aperture.
	ADR_BASEL	FRW	0H		PCI_BASE0 <19:08>	Low order base address bits used for fine grain I/O decode only. These bits are only used when IO=1 and ADR_SIZE is set to 0100-0111 in the PCI_MAP0 register.
	-	R	0H		PCI_BASE0 <07:04>	Reserved.
	PREFETCH	FR	0H		PCI_BASE0 <03>	Prefetchable: 1= Enable read prefetching for this aperture. 0= Disable read prefetching for this aperture. When LOCK is disabled and both the IO and PREFETCH bits are written to '1', the PREFETCH bit will read '0' even though it is internally set to '1' and the aperture will exhibit prefetch behaviour.
PCI_BASE0 (Only available when I2O mode is disabled)	TYPE	R	0H		PCI_BASE0 <02:01>	Address Range type: These Read Only bits are hardwired to "00" to indicate that the device can be mapped anywhere in the 32 bit address space.
	IO	FR	0H		PCI_BASE0 <00>	1= The PCI-to-Local aperture 0 will respond to PCI IO space access (/CBE=2h, 3h). 0= The PCI-to-Local aperture 0 will respond to PCI memory space access (/CBE=6h, 7h, Ch, Eh, Fh).

Register	Mnemonic	Type	Reset Value	Offset	Description	
PCI_BASE1 (Only available when I2O mode is disabled)	ADR_BASE	FRW	0H	0x18	PCI_BASE1 <31:20>	Base Address. If the value of ADR_BASE matches that of AD[31;20] during the address phase of a PCI access then a match is detected. In legacy DOS mode the address comparison has increased granularity.
	ADR_BASEL	FRW R	0H		PCI_BASE1 <19:14>	Base address bits used only for DOS compatibility mode. These bits read back as '0' unless DOS mode is selected in the PCI_MAP1 register.
	-	R	0H		PCI_BASE1 <13-11>	Reserved
PCI_BASE1 (Only available when I2O mode is disabled) cont.	DOS_MEM	FRW R	0H		PCI_BASE1 <10:08>	DOS Mode Memory Size. When IO=0 and DOS mode is selected, these bits set the size of the real mode DOS memory hole: 100 = 16K bytes (A[31:14]); 101 = 32K bytes (A [31:15]); 110= 64K bytes (A[31:16]); 111 = 128K bytes (A[31:17]); Others = disabled. These bits read back as '0' unless DOS mode is selected in the PCI_MAP1 register.
	-	R	0H		PCI_BASE1 <07:04>	Reserved
	PREFETCH	FR	0H		PCI_BASE1 <03>	Prefetchable: 1 = Enable read prefetching for this aperture. 0 = Disable read prefetching for this aperture. When LOCK is disabled and both IO and PREFETCH bits are written to '1', the PREFETCH bit will read '0' even though it is internally set to '1' and the aperture will exhibit prefetch behaviour.
	TYPE	R	0H		PCI_BASE1 <02:01>	Address Range Type. These read only bits are hardwired to "00" to indicate that the device can be mapped anywhere in the 32 bit address space.

Register	Mnemonic	Type	Reset Value	Offset	Description
	IO	FR	0H		PCI_BASE1 <00> 1 = The PCI-to-Local aperture 0 is in PCI IO space. 0= The PCI-to-Local aperture 0 is in PCI memory space.
PCI_SUB_ VENDOR	VENDOR	FRW	0H	0x2C	Subsystem vendor ID. Reads as 0x1464 (Interactive Circuits & Systems Ltd.).
PCI_SUB_ID	ID	FRW	0H	0x2E	Subsystem ID Reads as 0x0610 (ICS-610).
PCI_MAP0	MAP_ADR	FRW	0H	0x40	PCI_MAP0 <31:20> Map Address. These bits correspond to bits LAD [31:20] in local address space when a PCI to Local access is made. The lower bits of MAP_ADR are masked off according to the ADR_SIZE bits in the PCI_MAP registers.
	-	R	0H		PCI_MAP0 <19:16> Reserved.
	RD_POST_INH	FRW	0H		PCI_MAP0 <15> Read Posting Inhibit. When set to '1', the very first read of a burst read from the corresponding aperture will not generate a /STOP regardless of the latency of the access.
	-	R	0H		PCI_MAP0 < 14:12> Reserved.
	ROM_SIZE	FRW	0H		PCI_MAP0 <11:10> ROM Size. Determines the size of the expansion ROM address decoder: 00 = expansion ROM base register disabled 01 = 4K byte expansion ROM (A[31:12] significant) 10 = 16K byte expansion ROM(A[31:14] significant) 11 = 64K byte expansion ROM(A[31:16] significant)
	SWAP	FRW	0H		PCI_MAP0 <09:08> Byte Swap Control. Selects byte lane swapping for read and write cycles according to Table 5.3. Auto Swap: When local bus /BE[3:0]= "1100" or "0011" then a 16 bit swap is done. When local bus /BE[3:0] = "1110", "1101", "1011" or "0111" then an 8-bit swap is done. Any other combination results in non-swapped data.

Register	Mnemonic	Type	Reset Value	Offset	Description	
	ADR_SIZE	FRW	0H		PCI_MAP0 <07:04>	Aperture Size. Legacy DOS mode Uses a different decoding scheme. See Table 5.4 for more information.
	-	R	0H		PCI_MAP0 <03:02>	Reserved.
	REG_EN (Must be written '0' when I2O mode is enabled)	FRW	0H		PCI_MAP0 <01>	PCI_BASE0 Register Enable. 1 = PCI_BASE0 enabled, 0 = PCI_BASE0 disabled (reads back as OH)
	ENABLE (Must be written '0' when I2O mode is enabled)	FRW	0H		PCI_MAP0 <00>	PCI_BASE0 Aperture Enable. 1 = PCI-to-Local aperture 0 is enabled, 0 = PCI- to-Local aperture 0 is disabled
PCI_MAP1	MAP_ADR	FRW	0H	0x44	PCI_MAP1 <31:20>	Map Address. These bits correspond to bits LAD(31:20) in local address space when a PCI to Local access is made. The lower bits of MAP_ADR are masked off according to the ADR_SIZE bits in the PCI_MAP registers.
	-	R	0H		PCI_MAP1 <19:16>	Reserved.
PCI_MAP1 cont.	RD_POST_INH	FRW	0H		PCI_MAP1 <15>	Read Posting Inhibit. When set '1', the very first read of a burst read from the corresponding aperture will not generate a /STOP regardless of the latency of the access.
	-	R	0H		PCI_MAP1 <14:10>	Reserved.
	ADR_SIZE	FRW	0H		PCI_MAP1 <07:04>	Aperture Size. Legacy DOS mode uses a different decoding scheme. See Table 5.4 for more information.
	-	R	0H		PCI_MAP1 <03:02>	Reserved
	REG_EN	FRW	0H		PCI_MAP1 <01>	PCI_BASE1 Register Enable. 1 = PCI_BASE1 enabled, 0 = PCI_BASE1 disabled (reads back as 0H from PCI and Local).

Register	Mnemonic	Type	Reset Value	Offset	Description
	ENABLE	FRW	0H		PCI_MAP1 <00> PCI_BASE1 Aperture Enable. 1 = PCI-to-Local aperture 1 is enabled, 0 = PCI-to-Local aperture 1 is disabled
DMA_PCI_ ADDR0	ADR	RW	0H	0x80	DMA_PCI_ADDR0<31:02> PCI Byte Address
DMA_PCI_ ADDR0	-	R	0H		DMA_PCI_ADDR0 <01:00> These low address bits read back zero since all DMA transfers are 32 bit aligned.
DMA_CSR0	CHAIN	RW	0H	0x08B	DMA_CSR0 <07> 1 = enable DMA chaining for this transfer. 0 = disable DMA chaining for this transfer
	CLR_LEN	RW	0H		DMA_CSR0 <06> Clear Length. When set (1), the DMA_LENGTH value in the memory based descriptor will be cleared after the transfer is complete.
	PRIORITY	RW	0H		DMA_CSR0 <05> Controls the relative priority of DMA channels.
	DIRECTION	RW	0H		DMA_CSR0 <04> DMA Direction: 0 = Local to PCI 1 = PCI to Local
	SWAP	RW	0H		DMA_CSR0 <03:02> Byte Swap Control: Selects byte order conversion options (see Table 5.5). (Note: Writing to DMA_CSRx with the ABORT bit set will cause all other bits in the register to maintain their previous value (they are not written). The transfer can be restarted by setting DMA_IPR again using a read-modify-write to maintain the contents of the other register bits.
	ABORT	W	0H		DMA_CSR0 <01> 1 = immediately abort current DMA transfer process (see Note in DMA_CSR0 <03:02> description section). 0 = no operation
DMA_CSR0	DMA_IPR	RW	0H		DMA_CSR0 <00> DMA Initiate Process: Write 1 = begin DMA operationWrite 0 = no operation Read 1 = DMA in Progress Read 0 = DMA Idle Automatically cleared when the transfer count expires and there are no chains to process.

Register	Mnemonic	Type	Reset Value	Offset	Description	
DMA_ LENGTH0	DREQ_EN	RW	0H	0x88	DMA_LENGTH0 <23>	External DMA Request Enable: When set (1) the DMA will be throttled by the state of the INTC# input pin (DMA Channel 0) or INTD# input pin (DMA Channel 1). The corresponding pin must low (0) to allow the DMA to fetch the data source.
	INTR_EN	RW	0H		DMA_LENGTH0 <22>	Interrupt on Link Complete: When set (1), an internal interrupt from the DMA controller will be generated whenever the data transfer portion of a link is complete. The internal DMA interrupt can be routed to PCI or local interrupt outputs by enabling them in the PCI_INT_CFG and/or LB_IMASK registers. An internal interrupt is always generated upon chain completion when the DMA_IPR bit is cleared by the hardware.
	-	R	0H		DMA_LENGTH0 <21:20>	Reserved
	COUNT	RW	0H		DMA_LENGTH0 <19:00>	Transfer Count Remaining. This register holds the initial transfer count (in 32-bit words) and is updated with the remaining count after each DMA transfer.
DMA_CSR0	DMA_IPR	RW	0H		DMA_CSR0 <00>	DMA Initiate Process: Write 1 = begin DMA operation Write 0 = no operation Read 1 = DMA in Progress Read 0 = DMA Idle Automatically cleared when the transfer count expires and there are no chains to process.
DMA_ LENGTH0	DREQ_EN	RW	0H	0x88	DMA_LENGTH0 <23>	External DMA Request Enable: When set (1) the DMA will be throttled by the state of the INTC# input pin (DMA Channel 0) or INTD# input pin (DMA Channel 1). The corresponding pin must low (0) to allow the DMA to fetch the data source.

Register	Mnemonic	Type	Reset Value	Offset	Description
	INTR_EN	RW	0H		DMA_LENGTH0 <22> Interrupt on Link Complete: When set (1), an internal interrupt from the DMA controller will be generated whenever the data transfer portion of a link is complete. The internal DMA interrupt can be routed to PCI or local interrupt outputs by enabling them in the PCI_INT_CFG and/or LB_IMASK registers. An internal interrupt is always generated upon chain completion when the DMA_IPR bit is cleared by the hardware.
	-	R	0H		DMA_LENGTH0 <21:20> Reserved
	COUNT	RW	0H		DMA_LENGTH0 <19:00> Transfer Count Remaining. This register holds the initial transfer count (in 32-bit words) and is updated with the remaining count after each DMA transfer.
DMA_CTLB_ADR0	CTLB_ADR	RW	0H	0x8C	DMA_CTLB_ADRO <31:04> DMA Control Block Address. The address of the first control block in a DMA chain. Must be aligned to a 16 byte boundary and reside in Local memory.
	-	R	0H		DMA_CTLB_ADRO <03:00> Reserved
DMA_PCI_ ADDR1	ADR	RW	0H	0x90	DMA_PCI_ADDR1 <31:02> PCI Byte Address
	-	R	0H		DMA_PCI_ADDR1 <01:00> These low address bits read back zero since all DMA transfers are 32 bit aligned.
DMA_CSR1	CHAIN	RW	0H	0x09B	DMA_CSR1 <07> 1 = enable DMA chaining for this transfer 0 = disable DMA chaining for this transfer
	CLR_LEN	RW	0H		DMA_CSR1 <06> Clear Length. When set (1), the DMA_LENGTH value in the memory based descriptor will be cleared after the transfer is complete.
	PRIORITY	RW	0H		DMA_CSR1 <05> Controls the relative priority of DMA channels.
	DIRECTION	RW	0H		DMA_CSR1 <04> DMA Direction 0 = Local to PCI 1 = PCI to Local

Register	Mnemonic	Type	Reset Value	Offset	Description	
DMA_CSR1	SWAP	RW	0H		DMA_CSR1 <03:02>	Byte Swap Control: Selects byte order conversion options (see Table 5.5). (Note: Writing to DMA_CSRx with the ABORT bit set will cause all other bits in the register to maintain their previous value (they are not written). The transfer can be restarted by setting DMA_IPR again using a ready-modify-write to maintain the contents of the register bits.
	ABORT	W	0H		DMA_CSR1 <01>	1 = immediately abort current DMA transfer process (see above Note). 0 = no operation
	DMA_IPR	RW	0H		DMA_CSR1 <00>	DMA Initiate Process: Write 1 = begin DMA operation; Write 0 = no operation Read 1 = DMA in Progress Read 0 = DMA Idle Automatically cleared when the transfer count expires and there are no further chains to process.
DMA_ LENGTH1	DREQ_EN	RW	0H	0x98	DMA_LENGTH1 < 23>	External DMA Request Enable: When set (1) the DMA will be throttled by the state of the INTC# input pin (DMA Channel 0) or INTD# input pin (DMA Channel 1). The corresponding pin must be low (0) to allow the DMA to fetch the data source.
DMA_ LENGTH1 cont.	INTR_EN	RW	0H		DMA_LENGTH1 <22>	Interrupt on Link Complete: When set (1), an internal interrupt from the DMA controller will be generated whenever the data transfer portion of a link is complete. The internal DMA interrupt can be routed to PCI or local interrupt outputs by enabling them in the PCI_INT_CFG and/or LB_IMASK registers. An internal interrupt is always generated upon chain completion when the DMA_IPR bit is cleared by the hardware.
	-	R	0H		DMA_LENGTH1 <21:20>	Reserved

Register	Mnemonic	Type	Reset Value	Offset	Description	
	COUNT	RW	0H		DMA_LENGTH1 <19:00>	Transfer Count Remaining. This register holds the initial transfer count (in 32-bit words) and is updated with the remaining count after each DMA transfer.
DMA_CTLB_ADR1	CTLB_ADR	RW	0H	0x9C	DMA_CTLB_ADR1 <31:04>	DMA Control Block Address. Address of the first control block in a DMA chain. Must be aligned to a 16 byte boundary and reside in Local memory.
	-	R	0H		DMA_CTLB_ADR1 <03:00>	Reserved
DMA_DELAY	DELAY	RW	0H	0xE0	DMA_DELAY <07:00>	Determines the delay between the completion of processing a DMA descriptor and the loading of the next DMA descriptor.

Table 5.3 – Byte Lane Swapping for Byte Swap Control

	SWAP	D[31:24]	D[23:26]	D[15:08]	D[07:00]
No swap, 32 bit	00	Q[31:24]	Q[23:16]	Q[15:08]	Q[07:00]
16 bit	01	Q[15:08]	Q[07:00]	Q[31:24]	Q[23:16]
8 bit	10	Q[07:00]	Q[15:08]	Q[23:16]	Q[31:24]
	11	Auto Swap			

Table 5.4 – Aperture Size

ADDR_SIZE	Size	Valid ADR BASE Bits
0000	1 MByte	31:20
0001	2 MBytes	31:21
0010	4 MBytes	31:22
0011	8 MBytes	31:23
0100	16 MBytes memory 256 Bytes I/O	31:24 (mem) 31:08 (IO)
0101	32 MBytes memory 512 Bytes I/O	31:25 (mem) 31:09 (IO)
0110	64 MBytes memory 1024 Bytes I/O	31:26 (mem) 31:10 (IO)
0111	128 MBytes memory 2048 Bytes I/O	31:27 (mem) 31:11 (IO)
1000	256 MBytes	31:28
1001	512 MBytes	31:29
1010	1 GByte	31:30
11x	1MByte DOS Mode (PCI_MAP1 Only)	31:20
others	-	reserved

Table 5.5 – Byte Order Conversion Options

	SWAP	**D[31:24]**	**D[23:26]**	**D[15:08]**	**D[07:00]**
No swap, 32 bit	00	Q[31:24]	Q[23:16]	Q[15:08]	Q[07:00]
16 bit	01	Q[15:08]	Q[07:00]	Q[31:24]	Q[23:16]
8 bit	10	Q[07:00]	Q[15:08]	Q[23:16]	Q[31:24]
reserved	11				

5.3 Performing DMA Transfers

When performing Direct Memory Access (DMA) transfers to read data from the ICS-610, it is important that the transfer count is correctly programmed. If not, data may be lost or invalid data may be included in the destination buffer. It is also important that the ADC Data/Diagnostic area size is not exceeded by using an incorrect transfer start address or length. If necessary, multiple DMA transfers may be used in order to reach the required swing buffer length. If the transfer count is less than the programmed swing buffer length, and if an ADC interrupts are re-enabled after the transfer has completed, an ADC interrupt will immediately occur, indicating that the read-side swing buffer is not empty. Swing buffer swap, and therefore normal operation of the board in continuous mode, cannot occur until the read-side swing buffer has been completely emptied.

Either the ICS-610 (V360EPC PCI bus interface) or the target device may be the master (initiator) for the transfer. In general, faster transfer rates will be achieved if the ICS-610 is used as the DMA master for the transfer.

5.3.1 PCI Bus DMA Master

This describes how to perform DMA transfers using the V360EPC device on the ICS-610 as the PCI bus master (initiator). For V360EPC register details, please refer to Table 5.2 above. For ICS-610 register details, refer to Figure 7 and Figure 8 above.

The V360EPC contains two identical DMA Controller channels, which may be independently programmed to transfer data to/from the ICS-610. In the register names given below, these are referred to as REGx, where the register name is REG and x is either 0 or 1 to indicate which channel is being used. In general, the user will need to use only one of these channels.

The V360EPC DMA Controller supports block transfers of up to the full ADC Data/Diagnostic area size (512K 32-bit words = one side of the swing buffer). On-the-fly bye-order conversion is supported, for transferring data to systems which do not use little-endian byte ordering. The PCI Bus addresses used for DMA transfer are independent of the PCI apertures (address ranges) used for access to the ICS-610.

The procedure for performing a DMA transfer using the ICS-610 (V360EPC) as Master is as follows. Full descriptions of the relevant V360EPC registers are given in Table 5.2 to Table 5.5.

1. Write the destination PCI Bus start address to register PCI_ADDRx. Only bits 31-2 are significant since addresses must be on 32-bit word boundaries.
2. Write 0x80000000 to the DMA_LOCAL_ADDRx register. This is the local bus start address. It should always be programmed as 0x80000000 for each block transferred.
3. Write the DMA transfer length, in 32-bit words, to register DMA_LENGTHx. If bit 22 is set, an interrupt will be generated when the transfer is complete.
4. Write to the DMA_CSRx register. Bit 7 must be cleared. The transfer direction must be set in bit 4 (0 = from ICS-610 to PCI Bus target). Byte swap control must be set in bits 3 – 2 (see Table 5.2). Bit 0 must be set; this causes the transfer to start immediately.

5.3.2 PCI Bus DMA Chaining

The V360EPC provides DMA block chaining. In other words, data from the ICS-610 swing buffer may be transferred to multiple destination buffers at diverse addresses on the PCI Bus target device. To support this feature, chaining descriptor blocks must be provided by the user. These must be programmed to the ICS-610 DMA chain memory area referenced in Table 5.1. The DMA Controller also supports single block DMA, in which case the transfer is completely described by the destination address and transfer count programmed to the V360EPC itself as described above, and there is no requirement to program the DMA chain memory.

The DMA chain memory blocks are structured as described in Table 5.6 below. The names of the data fields correspond to the V360EPC register names used for programming a single block DMA, and the fields should be programmed in the same way as those registers, as described above, with the following exceptions:

1. The address in local memory of the first control block must be programmed to V360EPC register DMA_CTLB_ADDRx. The address of each subsequent control block must be programmed in the DMA_CTLB_ADDRx field of the previous control block.
2. The CHAIN bit (bit 7) of register/field DMA_CSRx must be set in the V360EPC register and in this field of each control block except the last one. This will cause the transfer to terminate following the final control block.
3. The DMA_LOCAL_ADDRx field of each control block should always be programmed as 0x80000000, since the ICS-610 always reads data sequentially from the swing buffer regardless of local bus address.

Table 5.6 - DMA Chaining Control Block Layout

31	**0**		
Next DMA_PCI_ADDRx value		0	
Next DMA_LOCAL_ADDRx value		4	WORD
Next DMA_CSRx	Next DMA_LENGTHx value	8	OFFSET
Next DMA_CTLB_ADDRx value		C	

5.3.3 PCI Bus DMA Slave

When performing a DMA transfer with the ICS-610 as the slave device, no set-up activity is necessary on the ICS-610. The source address range for each read transfer must lie entirely within the ADC Data/Diagnostic area address range. The transfer count must not exceed 512K 32-bit words.

5.4 ADC Data/Diagnostics Area

This section of the ICS-610's PCI bus memory map is used to read data from the ADC memory over the PCI bus. This area of the memory map is 512K 32-bit words in length; no access should exceed this length. The ADC memory buffers are strictly read only. The same area of the memory map allows test pattern data to be written to the diagnostic FIFO, which is strictly write-only. See Section 5.20 for details on using the built-in diagnostic feature.

In unpacked mode, the data is organized as one sample in each 32-bit word, justified to the most significant 24 bits of the word. In packed mode, each sample is truncated to 16 bits, and two samples are packed in each 32-bit word, with ‘big endian’ ordering. For example, channel 1 occupies the most significant 16 bits and channel 2 occupies the least significant 16 bits of a 32 bit word.

The data area appears to the user as FIFO type memory. Random access to samples in the memory is not available. Data access is always sequential regardless of the address used for read or write, as long as the address used falls within the ADC Data area. Thus, when multiple slave DMA transfers are used to read data, each transfer may start from the base address for the area.

Each time a data word is read from the buffer, the data is removed from memory and buffer pointers are modified. The user must be careful to read the exact number of 32-bit words corresponding to the programmed buffer length, otherwise buffer overflow or underflow will occur. However, the data transfer may be done in more than one transfer sequence or DMA sequence.

The user should perform a reset of the memory (ADC Reset register) after programming the ADC configuration and before enabling acquisition. This is necessary to ensure that the buffer pointers are correctly aligned prior to buffer access by the ADC circuits.

Note: When performing a diagnostic read, the data readout is not the data the user writes into the FIFO. The data readout is a 32-bit serial version of the 16-bit parallel input word, with each bit representing one of the 32 channels. Details of the format are given in Section 5.20.

5.5 Status Register (SR)

Some bits Read only, some bits Read/Write

The Status Register contains information about the state of the ICS-610. It is used to determine the interrupt status of the ICS-610, and the source of the interrupt. It also indicates the state of the diagnostic FIFO.

5.5.1 SR<0> - ADC IRQ

Read Only

This bit reflects the status of the ADC control unit. When the Swing Buffer swaps (Continuous mode) or acquisition completes (Capture mode), the ADC control unit will assert this flag indicating that new data is available. If ADC interrupts are enabled, an interrupt request will occur.

SR<0>	ADC Interrupt Request
READ ONLY	
0	ADC control unit is not asserting IRQ
1	ADC control unit is asserting IRQ

5.5.2 SR<1> - ADC Interrupt Pending

Read Only

This bit indicates that an ADC IRQ has been asserted while ADC interrupts are enabled (IMR <0>). An ADC interrupt is therefore pending.

SR<1>	ADC Interrupt Pending
READ ONLY	
0	ADC Interrupt pending
1	ADC Interrupt not pending

5.5.3 SR<2> - Diagnostic FIFO Empty

Read Only

This bit indicates that the ICS-610 diagnostic FIFO is empty. The user may write more data until the FIFO is full when operating in diagnostic mode.

SR<2>	Diagnostic FIFO Empty
READ ONLY	
0	Diagnostic FIFO is not empty
1	Diagnostic FIFO is empty

5.5.4 SR<3> - ADC Offset Calibration

Read Only

This bit indicates that the ICS-610 ADC offset calibration is in progress. The ADC offset calibration cycle starts when the ADC reset signal goes high. The bit goes low after 8704 clock cycles when the ADC oversampling ratio is 128x mode or after 17408 clock cycles when the ADC oversampling radio is 64x mode.

SR<3>	ADC Offset Calibration
READ ONLY	
0	The offset calibration cycle is finished
1	The offset calibration cycle is in progress.

5.5.5 SR<5> - Daughter Card Present

Read Only

This read-only bit indicates whether the optional ICS-610 daughter card is present. The daughter card contains an FPDP interface and a Local Bus connector (P4). The latter is required for multiple board ICS-610 configurations, in order to route the required timing signals to the other boards.

SR<5>	Daughter Card Present
READ ONLY	
0	Daughter card not present
1	Daughter card present

5.5.6 SR<6> - Buffer Overflow

Read/Write

This bit indicates that swing buffer overflow has occurred. This happens when the application does not succeed in completely reading one side of the swing buffer before the next swing buffer swap occurs, resulting in data being lost. The bit is latched, and will therefore remain set until cleared by writing a zero to this bit. If the corresponding IMR bit is set, an interrupt will occur when this bit is asserted.

SR<6>	Buffer Overflow
READ/WRITE	
0	No buffer overflow has occurred
1	Buffer overflow has occurred

5.6 Interrupt Mask Register (IMR)

Read/Write

This register is used to enable PCI bus interrupts. Masked interrupts are still seen in the corresponding bit of the status register, but do not cause an interrupt to occur.

5.6.1 IMR<0> - ADC IRQ Mask

This bit enables the ICS-610 to generate a PCI Bus interrupt when the swing buffer completes or swaps.

IMR<0>	ADC IRQ Mask
READ/WRITE	
0	ADC interrupts are disabled
1	ADC interrupts are enabled

5.6.2 IMR<6> - Buffer Overflow IRQ Mask

This bit enables the ICS-610 to generate a PCI Bus interrupt when swing buffer overflow occurs.

IMR<6>	Buffer Overflow IRQ Mask
READ/WRITE	
0	Buffer overflow interrupts are disabled
1	Buffer overflow interrupts are enabled

5.7 Control Register (CR)

Read/Write

The control register allows the user to configure the following operating parameters:

- Acquisition start and stop control through software
- Sampling master/slave selection
- FPDP master/slave selection
- Internal/external trigger selection
- Output mode (PCI Bus packed/unpacked, FPDP)
- Internal/external clock selection
- Oversampling ratio selection
- Select acquisition mode
- Enable/disable converter high pass filter
- Select internal or external signal source for converter calibration
- Enable/disable diagnostic mode

The control register bits are discussed in detail below. Following power up, or after a write to the Board Reset register, the register is set to zero in used bits.

5.7.1 CR<00> - Trigger Select

This bit selects internal or external triggering of the board. When internal triggering is selected, the board must be triggered under software control by writing a 1 to CR<14>. When external triggering is selected, the board must be triggered using a TTL level signal applied to pin 2 of the analog input connector.

CR<00>	Trigger Select
0	Internal Trigger
1	External Trigger

5.7.2 CR<01> - ADC Sampling Clock Select

This bit selects internal or external sampling clock. When the internal sampling clock is selected, the user must program the required sampling frequency to the on-board programmable oscillator using the ADC Clock Frequency register. When external sampling clock is selected, the user must supply a TTL level clock to pin 1 of the analog input connector. In either case, the frequency of the clock signal must be at the oversampling frequency, which is 256x or 128x the required sample output rate per channel, depending on the converter oversampling ratio selected in CR<10>.

CR<01>	ADC Sampling Clock Select
0	Internal Sampling Clock
1	External Sampling Clock

5.7.3 CR<02> - Diagnostic Mode Enable/Disable

This bit enables diagnostic mode. In this mode, the user can write data to the ADC Data area, and subsequently read it back. This procedure allows the user to exercise nearly all aspects of operation of the digital part of the ICS-610. The correct procedure must be followed in order to user diagnostic mode (see Section 5.20).

CR<02>	Diagnostic Mode Enable
0	Disable Diagnostic Mode (Normal Acquisition Mode)
1	Enable Diagnostic Mode

5.7.4 CR<03> - FPDP Enable

This bit enables the FPDP port on the optional ICS-610 daughter card. It is mandatory to have a daughter card installed in order to use the FPDP port. The FPDP interface provides a high speed 32-bit parallel synchronous data path to DSP boards and other devices.

CR<03>	FPDP Enable
0	Disable FPDP Port (Only Use PCI Data Path)
1	Enable FPDP Port (PCI and FPDP Data Path)

5.7.5 CR<04> - Select Packed Data

This bit enables packing of data on the PCI and FPDP interfaces. If enabled, samples are truncated to 16 bits and packed two samples in each 32-bit PCI word; the lower channel number is presented in the most significant 16 bits of each 32-bit word. If disabled, samples are not packed, but presented as 24-bit values justified to the most significant 24 bits of each 32-bit word.

CR<04>	Select Packed Data
0	Unpacked data
1	Packed data

5.7.6 CR<05> - Select ADC Master

This bit selects the current board as the ADC Sampling Master. This bit must be set when the ICS-610 is a stand-alone board, and when it is the sampling master of a multiple ICS-610 configuration. Note that the optional daughter board must be installed on all boards in a multiple board configuration, since the required timing signals are generated and bussed using the daughter board. Only the first board on the local bus (P4) must be configured as the sampling master (see Section 4.1).

CR<05>	Select ADC Master
0	ADC Slave
1	ADC Master

5.7.7 CR<06> - ADC Terminations Enable

This bit enables ADC terminations on the local bus. It should be set on stand-alone boards and also on the last board (end slave) of multiple board configurations, in order to correctly terminate the local bus.

CR<06>	ADC Terminations Enable
0	Disable ADC Terminations
1	Enable ADC Terminations

5.7.8 CR<07> - Select FPDP Master

This bit selects the ICS-610 as FPDP Master. This bit must be set on stand-alone boards using the FPDP port, and on FPDP Master boards of multiple board configurations. Note that the optional daughter board must be installed on all boards in a multiple board configuration, since the FPDP signals are generated and bussed using the daughter board. There may be more than one FPDP master in a multiple board configuration; however it is more common to have only one (see Section 4.1).

CR<07>	Select FPDP Master
0	FPDP Slave
1	FPDP Master

5.7.9 CR<08> - FPDP Terminations Enable

This bit enables the ICS-610 terminations. This bit must be set on stand-alone boards using the FPDP port, and on FPDP Master boards of multiple board configurations. Note that the optional daughter board must be installed on all boards in a multiple board configuration, since the FPDP signals are generated and bussed using the daughter board. There may be more than one FPDP master in a multiple board configuration; however it is more common to have only one (see Section 4.1).

CR<08>	FPDP Terminations Enable
0	Disable FPDP Terminations
1	Enable FPDP Terminations

5.7.10 CR<10> - Oversampling Ratio

This bit sets the oversampling ratio of the converter. 128 times oversampling provides superior signal-to-noise ratio performance but is available only for output rates up to 54 kHz. 64 times oversampling is available for output rates up to 108 kHz.

CR<10>	Oversampling ratio
0	Oversampling ratio = 128 x
1	Oversampling ratio = 64 x

5.7.11 CR<11> - ADC HP Filter Enable

Setting this bit enables and disables the converters' high pass filters. The AKM AK5393 converter includes a first order high pass digital filter at the output, which may be used to remove DC offset. The filter 3 dB cut-off frequency is 1.0 Hz when the output rate is 48 kHz, and scales linearly with frequency.

CR<11>	ADC HP Filter Enable
0	ADC HP Filter Disabled
1	ADC HP Filter Enabled

5.7.12 CR<12> - Zero Calibration

The setting of this bit determines the way in which converter calibration is performed. A write to the ADC Reset register will cause calibration to occur (see Section 5.17); the effect of it is to remove any DC bias present in the converter at the time the calibration is performed. The inputs used during calibration may be selected using this bit as either the normal signal inputs or voltage reference values provided by the converters themselves. When this bit is set, calibration is performed using the converter internal reference voltages. When clear, calibration is performed using the signal inputs. Note that the latter is the case following power up. In general, the bit should be set when calibration is carried out. If it is decided to use the signal inputs rather than the converter reference voltages, the user must be sure of the presence of stable DC signals (usually 0 volts) at the input terminals at the time.

CR<12>	Zero Calibration
0	Calibration will use signal inputs
1	Calibration will use internal reference voltages

5.7.13 CR<13> - Acquisition Mode

This bit determines the acquisition mode of the board. Setting the bit selects Capture mode, while clearing the bit selects Continuous mode. See Section 3.9 for a description of these modes.

CR<13>	Acquisition Mode
1	Capture Mode
0	Continuous Mode

5.7.14 CR<14> - ADC Internal Trigger

Setting this bit triggers the board when internal triggering has been selected in CR<00>. In Continuous mode, this starts the writing of ADC data to the swing buffer memories. The number of data stored in each memory is determined by the buffer length register. In Capture mode, setting this bit starts the count down of the remaining data points to be stored into the memory before stopping. The remaining number of data points to be stored is determined by the Acquisition Length register.

Prior to setting this bit, pre-trigger data is stored in a circular fashion into the memory. The pre-trigger phase is enabled by a write to the Arm register. The board must be completely configured before setting this bit.

CR<14>	**ADC Trigger**
0	No effect
1	Trigger ADC

Note: In Capture mode, the internal trigger will be automatically cleared once acquisition is complete. While in Continuous mode, it will not be cleared until the ADC is disabled.

5.7.15 CR<15> - ADC Enable

Setting this bit enables sampling. Sampling does not start until the board is either Armed by writing to the Arm register (if using Capture mode with pre-trigger storage), or triggered internally or externally (other modes).

CR<15>	**ADC Enable**
0	ADCs Disabled
1	ADCs Enabled

5.8 Gain/ Bandwidth Control

Read/Write

5.8.1 GBCR <03:00> - Input Voltage Range

The Input Voltage Range register should be programmed with a four-bit value according to the following table. The same gain is applied to all channels:

Value Programmed (Hex)	Input Voltage, Vpp (each wire) ICS-610	Input Voltage, Vpp (each wire) ICS-610-32A
0x7	10	20
0xB	5	10
0xD	2	4
0xE	1	2

Note: The input required to produce a full scale output is expressed as a differential input, peak-to-peak voltage, ±6%, approximately.

Reset Default: 0xB

5.8.2 GBCR <05:04> - Bandwidth Selection

The two bits for the bandwidth selection should be programmed as follows. They select the bandwidth of the 2-pole low pass Chebyschev anti-alias filter. Refer to Section 3.17 for more details.

Value Programmed	Input Signal Bandwidth (kHz)	Filter Cut-off (kHz)
0	0 – 2	6.5
1	2 – 6	20
2	6 – 20	65
3	20 – 45	150

5.9 Channel Count Register

Read/Write

This register allows the user to set the number of channels to be acquired in each frame. Unused channels are discarded prior to storage in the ADC Swing Buffer. The number of channels selected for acquisition must be an even number, and not greater than the channel capacity of the board. The register must be set to the actual number of channels required less one. Thus, valid numbers written to this register are 1 (2 channels) to 31 (32 channels), in steps of 2 (see Table 5.6). When operating in packed mode (see Section 5.7.5 above), this register must be programmed as the required number of channels divided by two, less one.

In multiple board synchronous sampling configurations (i.e. P4 bussed), it is mandatory to allocate the full 32 channels on all boards except the End Slave.

Reset Default: None

5.10 Buffer Length Register

Read/Write

The Buffer Length register is used to determine the total number of samples stored in the ICS-610 Swing Buffer. The register must be programmed with the number of 32-bit words (i.e. pairs of samples in packed mode and number of samples in unpacked mode) to be acquired in the buffer prior to each interrupt or to completion. In Continuous mode, the 19-bit buffer length value determines the number of 32-bit words written to the swing buffer by the ADCs before the buffer banks are swapped. This must be equal to the number of active channels multiplied by the acquisition length (programmed to the Acquisition Length register) for unpacked mode, and that number divided by two for packed mode. In Capture mode, the value programmed determines the total number of samples (or sample pairs in packed mode) acquired for all active channels before acquisition terminates. The value must be written to this register as one less than the required buffer length. If the ADC interrupt is enabled, a PCI Bus interrupt will occur when the programmed length is reached. The valid range of numbers that may be programmed to this register is 0 to 524287 (see Table 5.6).

The user must perform an ADC Reset (by writing to the ADC Reset register) after loading the Buffer Length, Acquisition Length, Decimation and Frame Length registers in order for the new values to take effect.

Reset Default: None

5.11 Acquisition Length Register

Read/Write

In Continuous mode, the Acquisition Length register must be set to the number of samples per channel stored in the swing buffer by the ADCs before the buffer banks are swapped. In Capture mode, this Acquisition Length register determines the number of samples per channel to be acquired after each trigger. Note that the actual number of samples stored after the trigger will be reduced by approximately 39 samples and approximately 39 samples will be stored before the trigger. This is due to the inherent pipeline delay of the ADC. The valid range of numbers that may be programmed to this register is 1 to 524287. The user must perform an ADC Reset (by writing to the ADC Reset register) after loading the Buffer Length, Acquisition Length, Decimation and Frame Length registers in order for the new values to take effect.

The table below indicates the relationship between the values programmed to the Channel Count, Acquisition Length and Buffer Length registers. Note that, when using Capture mode with pre-trigger storage, the value programmed to the Acquisition Length register (NP) must correspond to the number of samples per channel acquired after the trigger, and may therefore be any number in the range 1 – NS.

Reset Default: None

Table 5.7 - Register Programming Values

	Continuous Mode		Capture Mode	
	Packed	**Unpacked**	**Packed**	**Unpacked**
Channel Count Register	(NC/2) –1	NC –1	(NC/2) -1	NC –1
Acquisition Length	NS	NS	NP	NP
Buffer Length	$\frac{(NC \times NS)}{2} - 1$	(NC x NS) –1	$\frac{(NC \times NS \times NA)}{2} - 1$	(NC x NS x NA) – 1

NC = Number of channels (2, 4, ...32)
NS = Number of samples per channel acquired in buffer at each trigger
NA = Number of triggers or acquisitions. When using pre-trigger storage, NA = 1 only
NP = Number of samples per channel acquired after each trigger. NP $\leq$ NS. When using post-trigger storage, NS = M x NP, where M is integer.

Note: The actual number of samples stored after the trigger is reduced by approximately 39 samples due to the inherent delay of the ADC.

5.12 Decimation Register

Write Only

This register is used to set the decimation factor. Decimation is done by periodically discarding a specified number of samples from each channel at the output of the converters and before the samples are written to the ADC Swing Buffer. The decimation is applied equally to all channels.

The register allows the user to specify the decimation factor in the range 1 to 255. The number programmed to the register must be the required decimation factor.

For example, when Decimation=1, no decimation of the output takes place. When Decimation=2, every second output frame of data is decimated.

Reset Default: None

5.13 Frame Length Register

Read/Write

Data for output to the FPDP interface is stored in two FIFO buffers which are arranged in a swing buffer mode of operation. One buffer receives the acquired data while the other is the source for the data transmitted on the FPDP interface. When the acquisition path completes the writing of N acquisition frames (a frame consists of a sample for each active channel), the two buffers are automatically swapped. In general, the user should use a frame length of one. The valid range of numbers that may be programmed to this register is 1 to 255.

The user must perform an ADC Reset (by writing to the ADC Reset register) after loading the Buffer Length, Acquisition Length, Decimation and Frame Length registers in order for the new values to take effect.

Reset Default: None

5.14 ADC Clock Frequency Register

Write Only

This register allows the user to program the internal sampling (conversion) frequency. This is accomplished by writing a 22-bit programming word to the on-board programmable oscillator. Data is written serially to the oscillator, least significant bit first. One write to the register must occur for each bit of data to be written to the oscillator, with the data to be programmed in bit 0. Note that the frequency should be 256 times the desired output sampling rate for 128x operation and 128 times the desired output rate for 64x operation. See Section A.7 for details on programming the oscillator.

Reset Default: None

5.15 FPDP Clock Frequency Register

Write Only

This register allows the user to program the FPDP Strobe (clock) frequency, when the FPDP is used for output. This is accomplished by writing a 22-bit programming word to the on-board programmable oscillator. Data is written serially to the oscillator, least significant bit first. One write must occur for each bit of data to be written to the oscillator, with the data to be programmed in bit 0. See APPENDIX A for details of programming the oscillator. The theoretical minimum FPDP Strobe frequency required is the sample output rate multiplied by the number of channels selected; this value can be divided by two if packed output mode is used (see Section 5.7.5). The actual frequency used must be at least 15% higher than the calculated minimum. Under certain conditions (e.g. small frame sizes), it may be necessary to further increase the Strobe frequency used.

Reset Default: None

5.16 Arm Register

Write Only

Writing to this register initiates pre-storage of data when the ICS-610 is used in Capture mode. The value written is unimportant. See Section 3.9 for details on using pre-trigger storage.

Reset Default: None

5.17 ADC Reset Register

Write only

A write to this register synchronizes all onboard ADCs, loads the acquisition count, buffer length and decimation values and performs an ADC calibration. It does not alter memory contents or the values of control registers. The data written to the register is unimportant. The register should be written to after the board is configured and before acquisition is enabled. After writing to this register, a delay must be observed before the board is enabled and triggered, to allow time for the calibration to complete. The length of the delay depends on the sampling rate programmed to the internal clock, if used, or the frequency of the external clock. The required delay is calculated as follows:

Delay (milliseconds) = 2560.0 / Oversampling clock frequency (MHz)

Note that the oversampling clock frequency is 128 x or 256 x the required sample output rate. At the maximum oversampling clock frequency of 25.6 MHz, the required delay is therefore 100 ms.

Calibration has the effect of removing any DC offset caused by the converter. It is important that the voltages present at the converter analog inputs are known when this is done. For this purpose, the user may select either the internal reference voltages supplied by the converters, or the normal signal inputs, using CR<12>. In general, the internal reference voltages should be used. Additional information is given in Section 5.7.12.

5.18 Board Reset Register

Write only

A write to this register masks all interrupts, resets all control register bits to their power-up defaults (zero) and resets all on-board memory. V360EPC registers and status are unaffected. The data written to the register is unimportant. The register should only be written to in order to perform a complete reset of the board prior to changing the board configuration.

5.19 Master Control Register (MCR)

Read/Write

This register is used to program the FPDP interface configuration. The term FPDP cluster refers to all ICS-610 boards connected on the same FPDP cable, which may be one or more. The End Slave is the final ICS-610 board on the cable, in multiple ICS-610 configurations. A Stand-alone Master is the name given to a single ICS-610 configuration.

5.19.1 MCR<09:00> - Frame Length

This field sets the number of words to be sent in a FPDP frame, which is related to the total number of active channels across all boards. This value is given by the following expression:

$W = (C \times P / 2) - 1$

where C = total number of channels selected on all ICS-610 boards in cluster
P = packing factor selected in CR<4>, either 2 for unpacked or 1 for packed data

The calculated value must be programmed to all ICS-610 boards in the cluster. Note that, in an FPDP Cluster, all boards except the End Slave must be programmed for 32 active channels. An End Slave or Stand-alone Master may have any number of active channels (multiples of two only, minimum of four). The valid range of values for this field is 0 to 1023.

5.19.2 MCR<14:10> - FPDP board address

These bits program the FPDP address for the current board in an FPDP cluster. The range is 0 to (N-1), where is N is the number of ICS-610 boards connected on the FPDP and P4 cables. The valid range of values for this field is 0 to 31. The FPDP Master or Stand-alone Master must have FPDP board address zero, and the other boards must have ascending board addresses in order of their positions on the cable.

Reset Default: None

5.20 Using Diagnostic Mode

The ICS-610 has digital diagnostic circuitry that allows the user to test all functionality of the board with the exception of the ADCs themselves. This is accomplished by feeding the ICS-610 with simulated ADC data from an on-board 16 KWord FIFO.

To use diagnostic mode, configure the ICS-610 for Capture mode acquisition with no pre-trigger storage. Any legal buffer length may be programmed, but the maximum acquisition length must be less than or equal to 16384. Note that the buffer length must be an integral multiple of the acquisition length. Either internal or external clock and trigger may be selected. Set the Diagnostic Enable bit (CR<2>). As usual, after configuring the board, the ADC Reset register must be written to.

An amount of data equal to the programmed acquisition length (maximum of 4096 32-bit words) should now be written to the ADC Data area. The format of data to be written to the board is different from the format in which it is read. Figure 9 shows the format of the data to be written. The board should then be enabled and triggered, using the desired clock and trigger modes (internal or external). The user must now poll the Diag FIFO Empty bit (SR<2>) until the diagnostic FIFO is empty. The acquisition should then be disabled (CR<15>). This sequence of writing data to the board, enabling acquisition and disabling the board may be repeated until a number of words equal to the buffer length has been written to the board. At this point, when acquisition is enabled, an ADC interrupt will occur, if enabled.

The data written to the board may then be read back and compared with the original data in order to verify correct operation of the digital circuits.

In order to return the board to normal operation, the Diagnostic Enable bit (CR<2>) should be cleared when the above operation has been completed.

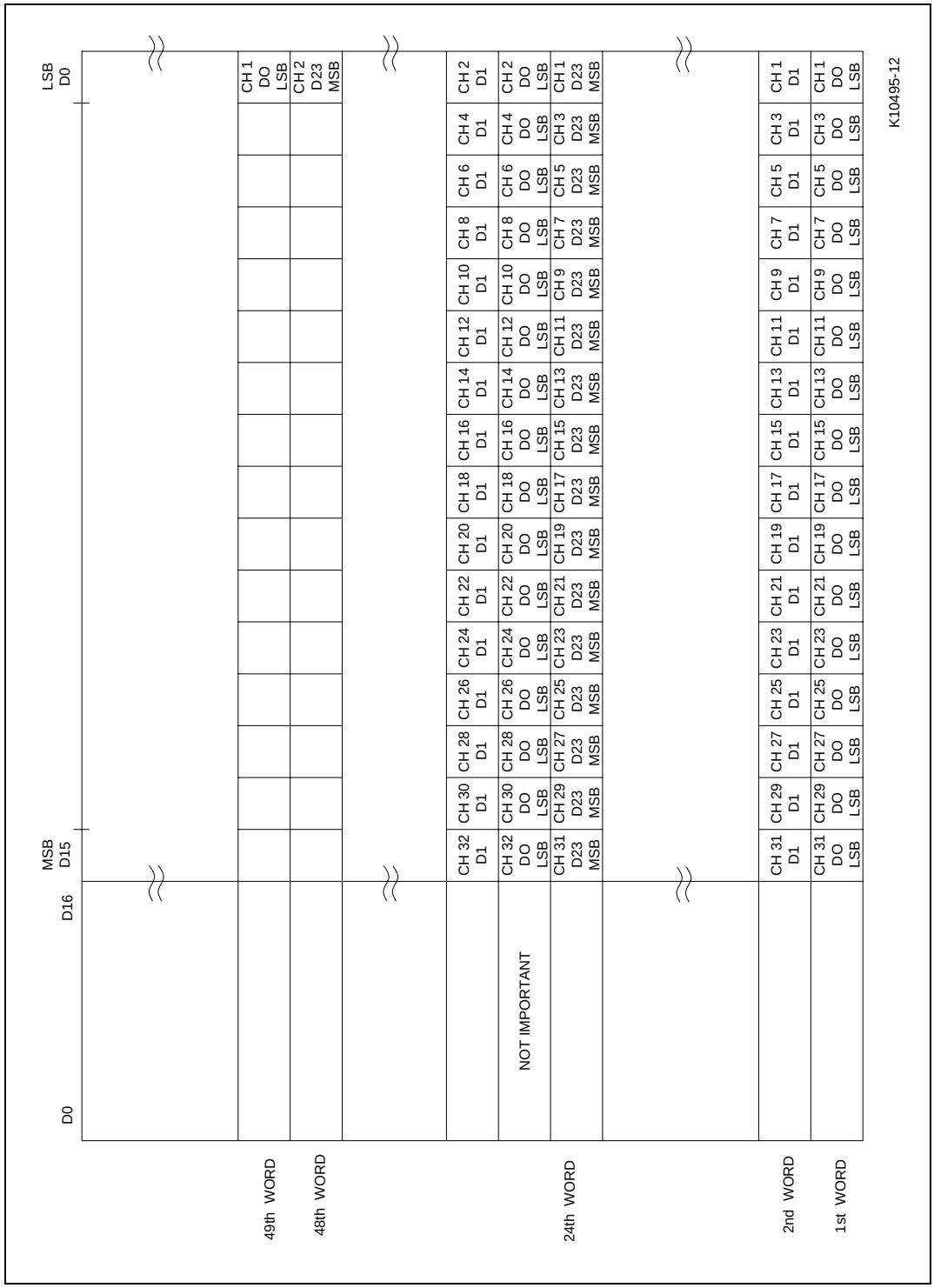


Figure 9 - Format of Diagnostic Data to be written to FIFO

Note: FIFO data is long word addressed, even though only bits 15 to bit 0 are effective.

5.21 Typical Order of Operations for Simple Acquisition

1. Configure switches if using external clock or trigger inputs. Install ICS-610 into system.
2. Configure V360EPC as appropriate (usually performed by operating system).
3. Reset board by writing to Board Reset register; clears control registers.
4. Program sample rate if using internal clock.
5. Set the Gain/ Bandwidth Control register to the desired input voltage range and signal bandwidth.
6. Set Control register:
   - 6.1 Select trigger source (internal / external)
   - 6.2 Select clock source (internal / external)
   - 6.3 Disable diagnostic mode (see Section 5.20)
   - 6.4 Select output interface
   - 6.5 Select packed/unpacked data
   - 6.6 Select ADC Master bit (set for master board)
   - 6.7 Select ADC Term bit (set for stand-alone master and end-slave boards)
   - 6.8 Select FPDP Master and Term bits, if using FPDP
   - 6.9 Select oversampling ratio (64x/128x)
   - 6.10 Select HP filter enable/disable
   - 6.11 Set Zero Cal bit, to select internal reference voltage for calibration
   - 6.12 Select operating mode (capture / continuous)
   - 6.13 Disable internal trigger
   - 6.14 Disable acquisition
7. Clear Interrupt Mask register.
8. Set Decimation register.
9. Set Acquisition Length register.
10. Set Buffer Length register.
11. Reset ADC (loads acquisition length and buffer length values and performs calibration).
12. Wait for calibration to complete.
13. Enable ADC.
14. If using pre storage, write to ARM register (starts pre-trigger storage).
15. If using internal trigger, set trigger bit in control register. If using external trigger, wait for external signal.
16. Enable ADC interrupt.
17. Wait for interrupt from ICS-610.
18. Disable ADC interrupt
19. Read back acquired data.
20. If using continuous mode:
21. IF enough data acquired, disable acquisition.
22. ELSE repeat steps 16... 21.
23. If using capture mode:
24. IF enough data acquired, disable acquisition.
25. ELSE repeat steps 14... 24.

6 USING THE ICS-610

This section provides an overview of the board operation through the use of examples.

6.1 ADC Swing Buffer Organization

This section discusses ADC Swing Buffer organization with respect to the different output modes.

6.1.1 PCI Bus Data Organization

Data from the ADC Swing Buffer may be read over the PCI Bus as 32-bit (longword) read operations from the ICS-610 PCI Bus ADC Data/ Diagnostics area at PCI Bus address PCI_BASE1+0x80000000. Table 6.1 shows the organization of the ADC Swing Buffer for unpacked output mode transfers.

Table 6.2 shows the organization of the ADC Swing Buffer for packed output mode transfers.

Table 6.1 - Unpacked Data Output Format (Eight Channels Selected)

	D31	**D08**	**D07**	**D00**
FIRST READ	CHANNEL 1 (T)		0	
SECOND READ	CHANNEL 2 (T)		0	
THIRD READ	CHANNEL 3 (T)		0	
•	CHANNEL 4 (T)		0	
•	CHANNEL 5 (T)		0	
•	CHANNEL 6 (T)		0	
•	CHANNEL 7 (T)		0	
•	CHANNEL 8 (T)		0	
•	CHANNEL 1 (T+1)		0	
•	CHANNEL 2 (T+1)		0	
•	CHANNEL 3 (T+1)		0	
•	CHANNEL 4 (T+1)		0	
•	CHANNEL 5 (T+1)		0	
•				

Table 6.2 - Packed Data Output Format (Eight Channels Selected)

	D31	D16	D15	D00
FIRST READ	CHANNEL 1 (T)		CHANNEL 2 (T)	
SECOND READ	CHANNEL 3 (T)		CHANNEL 4 (T)	
THIRD READ	CHANNEL 5 (T)		CHANNEL 6 (T)	
•	CHANNEL 7 (T)		CHANNEL 8 (T)	
•	CHANNEL 1 (T+1)		CHANNEL 2 (T+1)	
•	CHANNEL 3 (T+1)		CHANNEL 4 (T+1)	
•	CHANNEL 5 (T+1)		CHANNEL 6 (T+1)	
•	CHANNEL 7 (T+1)		CHANNEL 8 (T+1)	
•	CHANNEL 1 (T+2)		CHANNEL 2 (T+2)	
•	CHANNEL 3 (T+2)		CHANNEL 4 (T+2)	
•	CHANNEL 5 (T+2)		CHANNEL 6 (T+2)	
•	CHANNEL 7 (T+2)		CHANNEL 8 (T+2)	
•	CHANNEL 1 (T+3)		CHANNEL 2 (T+3)	
•				

6.1.2 FPDP Data Organization

The ICS-610 FPDP interface allows the user to move data at an aggregate rate of up to 40 MSamples/second (24-bit samples) or 80 MSample/second (16-bit truncated samples). This standard supports a 32-bit data bus, however the ICS-610 drives only 24 bits of the data bus (bits D31 through D08) in unpacked output mode.

Table 6.1 shows the unpacked data format, while **Table 6.2** summarizes the packed format.

6.2 Single-Board Real-Time PCI Bus Operating Example

In this configuration, data is converted and accessed over the PCI Bus using 32-bit read operations. The following example explains how to initialize the ICS-610, and how to access the data in real-time using the PCI Bus interrupt mechanism. A twenty channel configuration is assumed, operating at a 100 kHz output rate using the internal sampling clock in 64x oversampling mode. Acquisition control is internal using the ADC Trigger bit (CR<14>). Capture mode is used, and unpacked data is selected. 1K samples are acquired on each of the 20 channels. The input signal is a 1 Vpp differential signal with a 40 kHz bandwidth.

The board must be configured for Stand-Alone Master operation with internal clock and trigger.

1. Perform a board reset by writing to the Board Reset register.
2. Program the Clock Frequency register with a value calculated using the procedure in APPENDIX A to set the sampling clock frequency to 100,000 x 128 = 12.8 MHz. Note that because the required oversampling ratio is 64x, the clock frequency must be set to 128x the required output rate.
3. Set the Gain/Bandwidth Control to 62 for an input voltage range of 1 Vpp and a bandwidth of 40 kHz.
4. Configure the ICS-610 CR as follows:

    4.1 CR<00> TRIGGER SELECT=0.
    4.2 CR<01> ADC CLOCK SELECT=0.
    4.3 CR<02> DIAGNOSTIC MODE ENABLE=0.
    4.4 CR<03> FPDP ENABLE=0.
    4.5 CR<04> PACKED DATA=0

4.6 CR<05> ADC MASTER=1
4.7 CR<06> ADC TERMINATE=1.
4.8 CR<07> FPDP MASTER=0.
4.9 CR<08> FPDP TERMINATE=0.
4.10 CR<10> OVERSAMPLING RATIO=0 (64x)
4.11 CR<11> ADC HP FILTER ENABLE=0
4.12 CR<12> ZERO CAL = 1
4.13 CR<13> ACQ MODE=1
4.14 CR<14> ADC TRIGGER=0.
4.15 CR<15> ADC ENABLE=0

5. Set Channel Count Register =19.
6. Set Buffer Length = (20 x 1024 -1) = 20479
7. Set Acquisition Length = 1024 –1 = 1023
8. Set Decimation = 1
9. Write to the ADC Reset Register
10. Wait for Calibration delay to complete
11. Set CR<15> to enable board
12. To begin acquisition, set CR<14> ADC TRIGGER=1
13. Enable ADC interrupt.
14. Wait for an ADC interrupt.
15. Disable ADC interrupt.
16. When an interrupt occurs:
    16.1 Read 20480 32-bit words using standard reads or DMA Master/Slave cycles.
    16.2 Re-enable ADC Interrupt if further capture sequences are required

For real-time operation, repeat steps 12 through 16.

6.3 Two-Board Real-Time FPDP Operating Example

In this configuration, data is converted continuously by two ICS-610 boards and transmitted as unpacked data over the FPDP interface to a receiving board, for example a Digital Signal Processor. The optional daughter board must be installed on both boards in order to use this function. The following example explains how to initialize both ICS-610 boards, as well as prepare the FPDP interface. A 40-channel configuration is assumed using the internal clock and operating at an output rate of approximately 12 kHz in 128x oversampling mode. The input signal is a 5 Vpp differential with a 5 kHz bandwidth. Continuous mode is used. Acquisition control is external using the front panel analog input connector EXT_TRIG input.

The external trigger is applied to the EXT_TRIG signal (pin 2) of the front panel analog input connector. The FPDP bus and local bus cables must be connected between the two ICS-610 boards; the FPDP cable should extend to the FPDP receiver.

With a two ICS-610 board configuration, one of the boards should be configured as a Master, and the other ICS-610 should be configured as an End-Slave.

1. Perform a board reset by writing to the Board Reset register on both boards.
2. Program the Clock Frequency register on the motherboard with a value calculated using the procedure in APPENDIX A to set the sampling clock frequency to 12,000 x 128.
3. Set the Gain/Bandwidth register on both boards to 27 for an input voltage range of 5 Vpp and a signal bandwidth of 5 kHz.
4. Configure the ICS-610 Master CR as follows:

    4.1 CR<00> TRIGGER SELECT=1.
    4.2 CR<01> ADC CLOCK SELECT=0.

4.3 CR<02> DIAGNOSTIC MODE ENABLE=0.
4.4 CR<03> FPDP ENABLE=1.
4.5 CR<04> PACKED DATA=0.
4.6 CR<05> ADC MASTER=1.
4.7 CR<06> ADC TERMINATE=0.
4.8 CR<07> FPDP MASTER=1.
4.9 CR<08> FPDP TERMINATE=1.
4.10 CR<10> OVERSAMPLING RATIO=1.
4.11 CR<11> ADC HP FILTER ENABLE=0.
4.12 CR<12> ZERO CAL = 1
4.13 CR<13> ACQ MODE=0
4.14 CR<14> ADC TRIGGER=0.
4.15 CR<15> ADC ENABLE=0.

5. Configure the ICS-610 Slave CR as follows:

5.1 CR<00> TRIGGER SELECT=1.
5.2 CR<01> ADC CLOCK SELECT=0.
5.3 CR<02> DIAGNOSTIC MODE ENABLE=0.
5.4 CR<03> FPDP ENABLE=1.
5.5 CR<04> PACKED DATA=0
5.6 CR<05> ADC MASTER=0.
5.7 CR<06> ADC TERMINATE=1.
5.8 CR<07> FPDP MASTER=0.
5.9 CR<08> FPDP TERMINATE=0.
5.10 CR<10> OVERSAMPLING RATIO=1.
5.11 CR<11> ADC HP FILTER ENABLE=0
5.12 CR<12> ZERO CAL = 1
5.13 CR<13> ACQ MODE=0
5.14 CR<14> ADC TRIGGER=0.
5.15 CR<15> ADC ENABLE=0.

6. On the ICS-610 Master board, set Channel Count Register=31.
7. On the ICS-610 Slave board, set Channel Count Register=7.
8. On the ICS-610 Master board, set Frame Length Register=1.
9. On the ICS-610 Slave board, set Frame Length Register=1.
10. On both ICS-610 boards, set Decimation=1.
11. On the ICS-610 Master, set Master Control Board Address=0,
12. Master Control Number of Channels=39
13. On the ICS-610 Slave, set Master Control Board Address=1,
14. Master Control Number of Channels=39
15. Write to the ADC Reset register on both cards to reset the ADC Swing Buffers and start calibration
16. Wait for calibration to complete
17. Enable the Master and Slave boards.
18. To start acquisition, trigger the Master board using the external trigger signal.

After step 17, the ICS-610-x FPDP mechanism will begin to feed data over the FPDP bus to the FPDP receiver. The ICS-610-x Master will handshake with the receiver in order to ensure that the receiver's buffer does not overflow; this handshake is mediated by means of the SUSPEND* and DVALID* FPDP signals. However, it is the responsibility of the FPDP receiver to keep up with the output data rate of the ICS-610-x two-board system. Descriptions of FPDP signals are given in APPENDIX D of this manual.

7 TECHNICAL SUPPORT

Technical support for this product is available through ICS using the contact information given below.

When requesting technical support, please provide the following information:

- Product name - ICS-610 specific model
- Serial number of board (of the form 31425, given on a bar code label located on the board).
- Software device driver used, if any (e.g. Windows, Linux or VxWorks driver).
- Installation environment – type of chassis, type of CPU, and other boards installed.
- Nature of problem.

You may contact ICS Technical Support at:

Address: ICS Ltd.
Attn. Technical Support
5430 Canotek Road
Ottawa, Ontario
K1J 9G2

Phone: 613-749-9241 or (USA) 800-267-9794
Fax: 613-749-9461
Web: http://www.ics-ltd.com
E-mail: support@ics-ltd.com

8 REFERENCES

1. PCI Bus Specification, IEC821, ANSI/IEEE Std.

2. AK5393 Product Information, M0038-E-01/00, Asahi Kasei Microsystems Co. Ltd., http://www.akm.com.

3. V360EPC Product Information, Quicklogic, http://www.quicklogic.com

4. Front Panel Data Port Specification, ANSI/VITA 17-1997 Standard.

5. ICS Technical Note Number 16, http://www.ics-ltd.com

6. IEEE press publication "Oversampling Sigma-Delta Data Converters", James C. Candy and Gabor C. Temes

APPENDICES

APPENDIX A PROGRAMMING THE INTERNAL CLOCK GENERATOR

A.1 Introduction

The frequencies of the ICS-610 internal sampling clock and FPDP Strobe clock are controlled by programming the programmable oscillator through the ADC Clock Frequency and FPDP Clock Frequency registers of the PCI bus memory map (see Table 5.1 and Figure 7). The device is programmed not in engineering units, but by means of a complex programming word whose construction is described below; a series of control words must also be written to the device. Data is transferred to the device serially; it is necessary to write the data to the ICS-610 ADC Clock register one bit at a time; bit 0 of the register is the relevant bit. Thus the programming sequence should normally be done by repeatedly writing each control or programming word to the ADC Clock register, shifting the data right by one bit after each write, until all bits of the word have been written.

Automatic calculation of the programming word is provided by the ics610calcFoxWord() function and other functions in the 'C' language function library supplied with the optional ICS-610 software drivers, available for Windows environments. These routines generate a 22-bit formatted programming word for the oscillator equivalent to the nearest possible frequency to that supplied as input by the user (in MHz), and also supply the actual frequency represented by the programming word, as an output.

A.2 Programming Summary

The oscillator device contains two registers, the Control Register and the Programming Word Register. The programming sequence is as follows:

1. Write to Control Register to configure device and prepare the device to receive the Programming Word.
2. Write Programming Word.
3. Write to Control Register to load Programming Word data into device.
4. Wait at least 10 ms for device Voltage Controlled Oscillator (VCO) frequency to stabilize.
5. Write to Control Register to enable device output of new frequency.

A.3 Control Register

When writing data to the Control Register, it is necessary to include a Protocol Field to identify the data as Control Register data.

Protocol Field (6 bits) = 0 1 1 1 1 0

It is important that the sequence of four ones contained in the protocol field never be sent except as part of the Protocol Field. Thus, when writing programming word data to the device, it is necessary to use a technique of inserting an extra zero after a run of three ones; this technique is called ‘bit stuffing’, and is described in more detail in Section A.4.

The control register contains eight bits, which are defined as shown in Table A.1.

Table A.1 - Control Register

Bit Number	Description	Function	Power-up Default
0	Enable Programming Word register to be written by next data	0 = Program Register Disabled 1 = Program Register Enabled to Receive Data	0
1	Internal Output Disable	0 = Output is VCO or f_{REF} 1 = Output is tri-stated	0
2	Internal Multiplexer	0 = Output is VCO frequency 1 = Output is f_{REF}	1
3	Device pin 7 usage	Set to zero only	0
4 - 7	Reserved	Set to 0	0000

Control register data is written to the device starting with bit 0 of the control word, continuing to bit 7 of the control word, and followed by the 6 bits of the Protocol field, for a total of 14 bits.

Note that the default configuration of the device following power-up results in the output being at the frequency of the reference oscillator which is 14.31818 MHz.

A.4 Programming Register

The Programming register is written with a 22-bit word describing the required frequency of the output. However, it is essential that programming words do not mimic the Control word Protocol field (see Section A.3 above) by containing runs of four consecutive ones. Thus, the device specification requires that a zero must be inserted in the word after each occasion when three one's have been transmitted to the device, regardless of whether the next bit is a 0 or a 1. This procedure is known as ‘bit stuffing’. For this reason, the actual length of a programming word may vary between 22 and 29 bits.

For example, to send this programming data:

Last Bit				First Bit
1111	0101	0111	1110	111111

Transmit this serial bit stream:

Last Bit				First Bit
10111	0101	00111	01110	01110111

The fields of the programming word are described in Table A.2.

Table A.2 - Fields of Programming Words

Field	Bits	# of Bits	Notes
P Counter value (P)	<21:15>	7	MSB (Most Significant Bits)
Duty Cycle Adjust Up (D)	<14>	1	Set to logic 0
Mux (M)	<13:11>	3	
Q Counter Value (Q)	<10:4>	7	
Index (I)	<3:0>	4	LSB (Least Significant Bits)

The frequency of the programmable oscillator f_{VCO}, and the output frequency f_{OUT} are determined by these fields as follows:

$$f_{VCO} = 2 * f_{REF} * (P+3)/(Q+2)$$

where, f_{REF} = Reference frequency (i.e. 14.31818 MHz)

$$f_{OUT} = f_{VCO} / 2^{M}$$

The values of the P and Q parameters must be selected so that f_{VCO} remains between 50 MHz and 150 MHz, inclusive. The value programmed to the M field programs a division register to allow sub-multiples of the VCO frequency to be obtained at the output; the maximum divisor possible is 128.

The Index field 'I' is used to preset the VCO to an appropriate range. The value for this field should be chosen from the following table. (Note that this table is referenced to f_{VCO} rather than to the desired output frequency.)

I	**f_{vco} (MHz)**
0000	50 – 80
1000	80 - 150

If the desired VCO frequency is exactly 80 MHz, then either index value may be used (since both limits are tested). However, the manufacturer recommends using the setting corresponding to the higher frequency range.

A.5 VCO Programming Constraints

There are three primary programming constraints the user must be aware of:

1. 50 MHz <= Fvco <= 150 MHz
2. 1 <= P <= 127
3. 1 <= Q <= 127

The constraints have to do with the trade-offs between optimum speed with lowest noise, VCO stability and factors affecting the loop equation.

A.6 Program Register Example

The following is an example of how to calculate a clock programming word:

1. Derive the proper programming word for 12.8 MHz clock frequency:
   1.1 Since 12.8 MHz < 50 MHz, quadruple it to 51.2 MHz
2. Set M to 0102
3. Set I to 00002

The result:

$$Fout = 12.8 = (2*14.31818*(P+3)/(Q+2))/2^M$$

where M = 0, 1, 2, 3, 4, 5, 6, 7
since M = 2: (P+3)/(Q+2) = 1.787936735

The two choices of P and Q giving the nearest to the required frequency are:

P	Q	f_{VCO}	Error (PPM)
56	31	51.19834	32
115	64	51.19834	32
90	50	51.21503	293

Taking the first set of values, i.e. (P,Q) = (56,31):

P = 56 decimal = 0111000 binary = 0(0)111000

Q = 31 decimal = 0011111 binary = 0011(0)111

Note: The presence of three ones in a row in both P and Q values causes zero bit-stuff values to be inserted in each. However, it is necessary to examine the values in the previous (I) field before inserting a zero in the least significant bits of the Q value. If the I field had contained a 1 in the most significant position the inserted zero would have been in a different position.

The full programming word, W is therefore:

W = P, D, M, Q, I = 00111000, 0, 010, 00110111, 0000 = 001110000010001101110000 (382370 Hex)

A.7 Oscillator Programming Example

The oscillator requires three control words plus the programming word in order to program a new output frequency (see programming sequence given in Section A.2 above). The following paragraphs provide an overview of how the control words are build along side the programming word.

All data is written to the oscillator serially through the ICS-610 ADC Clock Frequency or FPDP Clock Frequency register bit 0. The data is written least significant bit first. An example of programming the oscillator to an initial or new frequency is as follows:

1. Load Control register to enable loading of the Programming word register, enable the output and select the reference frequency for output from the Internal Multiplexer. The Protocol word follows the control word. All data is shifted in LSB (Least Significant Bit) first.

	Last Bit First Bit
Control word	0 1 1 1 1 0 0 0 0 0 0 0 1 0 1
	Protocol Word Control Reg. Data

2. Shift in the desired output frequency value via a programming word that is 22 bits in length, plus any required bit stuffs. (Up to 29 bits can be obtained with bit-stuffing). The example programming word for 12.8 MHz, calculated in Section A.6 above, is shown below.

	Last Bit First Bit
Programming word for 12.8 MHz (0x382370)	0 0 1 1 1 0 0 0 0 0 1 0 0 0 1 1 0 1 1 1 0 0 0 0

3. Load the Control register to disable further loading of the Programming word register. This causes the required output frequency value to be programmed while keeping the output set to the reference frequency for the time being.

	Last Bit First Bit
Control word	0 1 1 1 1 0 0 0 0 0 0 1 0 0
	Protocol Word Control Reg. Data

4. Wait at least 10ms for the VCO to settle to the new frequency. The value will be accurate to within 0.1% within this time.

5. Load the Control register to disable the Internal Multiplexer. This will cause the output to immediately swing to the new frequency.

	Last Bit First Bit
Control word	0 1 1 1 1 0 0 0 0 0 0 0 0 0
	Protocol Word Control Reg. Data

APPENDIX B ANALOG INPUT 1-32 CONNECTOR DETAILS

Connector on board: AMP 748483-5
Mating connector: AMP 748368-1 (Specify pins and shells required)
Manufacturer: AMP Inc., 1-800-522-6752

PIN	SIGNAL	PIN	SIGNAL
1	EXT CLK	40	Digital GND
2	EXT TRIG	41	Analog GND
3	Analog GND	42	Channel 10+
4	Channel 2+	43	Channel 10-
5	Channel 2-	44	Channel 12+
6	Channel 4+	45	Channel 12-
7	Channel 4-	46	Channel 14+
8	Channel 6+	47	Channel 14-
9	Channel 6-	48	Channel 16+
10	Channel 8+	49	Channel 16-
11	Channel 8-	50	Channel 26+
12	Channel 18+	51	Channel 26-
13	Channel 18-	52	Channel 28+
14	Channel 20+	53	Channel 28-
15	Channel 20-	54	Channel 30+
16	Channel 22+	55	Channel 30-
17	Channel 22-	56	Channel 32+
18	Channel 24+	57	Channel 32-
19	Channel 24-	58	Analog GND
20	Analog GND	59	Digital GND
21	Digital GND	60	Analog GND
22	Analog GND	61	Channel 9+
23	Channel 1+	62	Channel 9-
24	Channel 1-	63	Channel 11+
25	Channel 3+	64	Channel 11-
26	Channel 3-	65	Channel 13+
27	Channel 5+	66	Channel 13-
28	Channel 5-	67	Channel 15+
29	Channel 7+	68	Channel 15-
30	Channel 7-	69	Channel 25+
31	Channel 17+	70	Channel 25-
32	Channel 17-	71	Channel 27+
33	Channel 19+	72	Channel 27-
34	Channel 19-	73	Channel 29+
35	Channel 21+	74	Channel 29-
36	Channel 21-	75	Channel 31+
37	Channel 23+	76	Channel 31-
38	Channel 23-	77	Analog GND
39	Analog GND	78	ADC CLK OUT

Note: All other pins are connected to analog ground on the board.

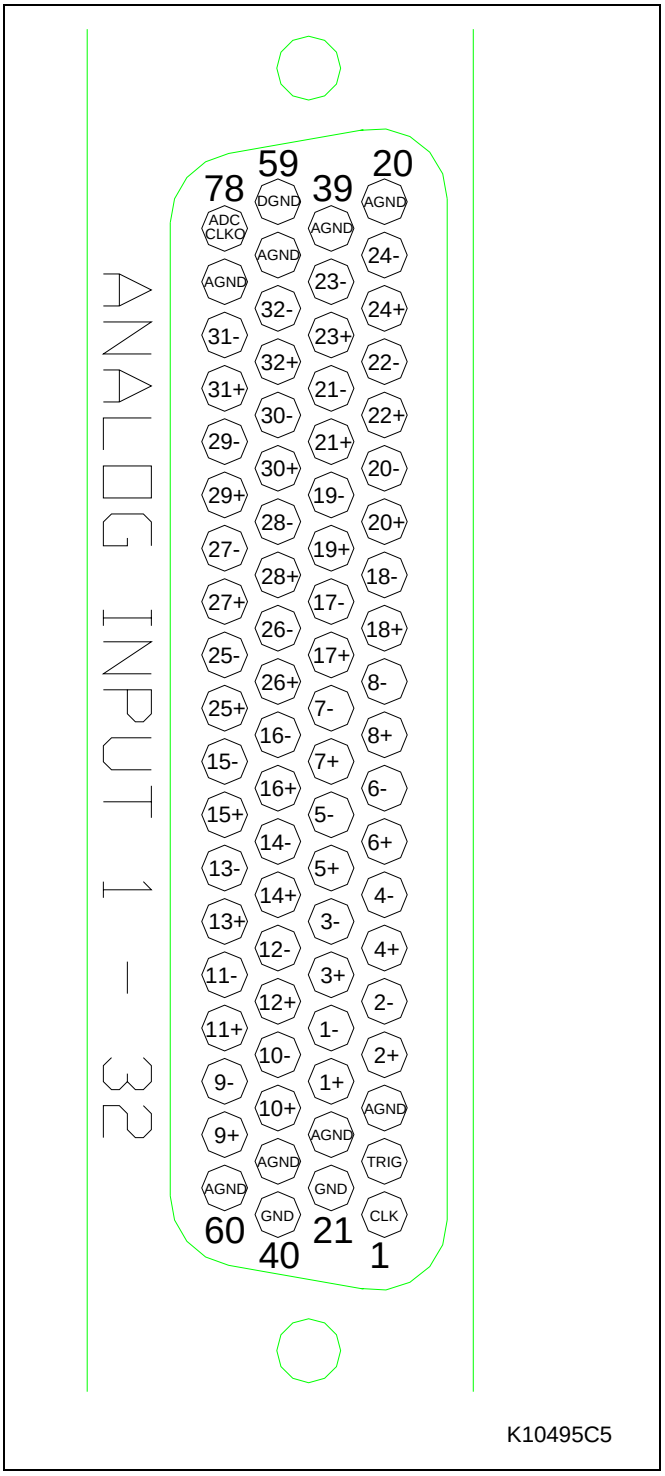


Figure 8 - ICS-610 Analog Connector Pinout

APPENDIX C P4 LOCAL BUS CONNECTOR DETAILS

Suitable mating connectors are available from a number of manufacturers. The one listed is an example only.

Connector on board:	8831E-026-170L (KEL Corporation) P50E-026P1-RR1-TG (Robinson-Nugent)
Mating connector:	8825E-026-175 KEL (with strain relief) 8825R-026-175 KEL (without strain relief) P25E-026S-TG Robinson-Nugent
Manufacturers:	KEL Corporation, (408)720-9044 Robinson-Nugent, (812)945-0211

Pin Number	Signal Name	Description
1	ADC_CLK	Distribution ADC Clock +ve. This PECL signal is used by sampling master to ensure all slaves sample at the same time. This signal is bussed from the sampling master to all slaves, and is driven by the master only.
2	/ADC_CLK	Distribution ADC Clock -ve. This PECL signal is used by sampling master to ensure all slaves sample at the same time. This signal is bussed from the sampling master to all slaves, and is driven by the master only.
3	GND	Digital Ground
4	SYNC	ADC Frame Sync. In multiple board systems, this signal is used by the sampling master to ensure the ADC's output synchronization on all boards. This signal is bussed from the sampling master to all slaves, and is driven by the master only.
5	GND	Digital Ground
6	BX_SYNC*	Swing Buffer Sync. This is used by the sampling master to ensure the swing buffers on all slaves in sync. The signal is bussed from the sampling master to all slaves, and is driven by the master only.
7	GND	Digital Ground
8	FSYNC	Decimation Sync. In multiple board systems, this signal is used by the sampling master to ensure all boards decimate on the same sample. This signal is bussed from the sampling master to all slaves, and is driven by the master only.
9	GND	Digital Ground
10	TRIG	Distribution Trigger. This signal is used by the sampling master to ensure all boards trigger at the same time. This signal is bussed from the sampling master to all slaves, and is driven by the master only.
11	GND	Digital Ground
12	FP_CLK	Distribution FPDP Clock +ve. This PECL signal is used by FPDP master to ensure FPDP data transfers. This signal is bussed from the FPDF master to all slaves, and is driven by the master only.
13	PECL /FP_CLK	Distribution FPDP Clock -ve. This PECL signal is used by FPDP master to ensure FPDP data transfers. This signal is bussed from the FPDF master to all slaves, and is driven by the master only.
14	GND	Digital Ground

Pin Number	Signal Name	Description
15	/FP_DV	FPDP Data Valid. This line is asserted by the FPDP transmitter. It signals valid data on the FPDP bus.
16	GND	Digital Ground
17	CHAN5	Signal used in FPDF board addressing
18	CHAN6	Signal used in FPDF board addressing
19	CHAN7	Signal used in FPDF board addressing
20	CHAN8	Signal used in FPDF board addressing
21	CHAN9	Signal used in FPDF board addressing
23	-	Not Used
24	GND	Digital Ground
25	-	Not Used
26	GND	Digital Ground

Note: When operating multiple boards, and reading data over PCI Bus (not FPDP), the last board to be read following each swing buffer swap interrupt should be the master board.

APPENDIX D P5 FPDP DETAILS

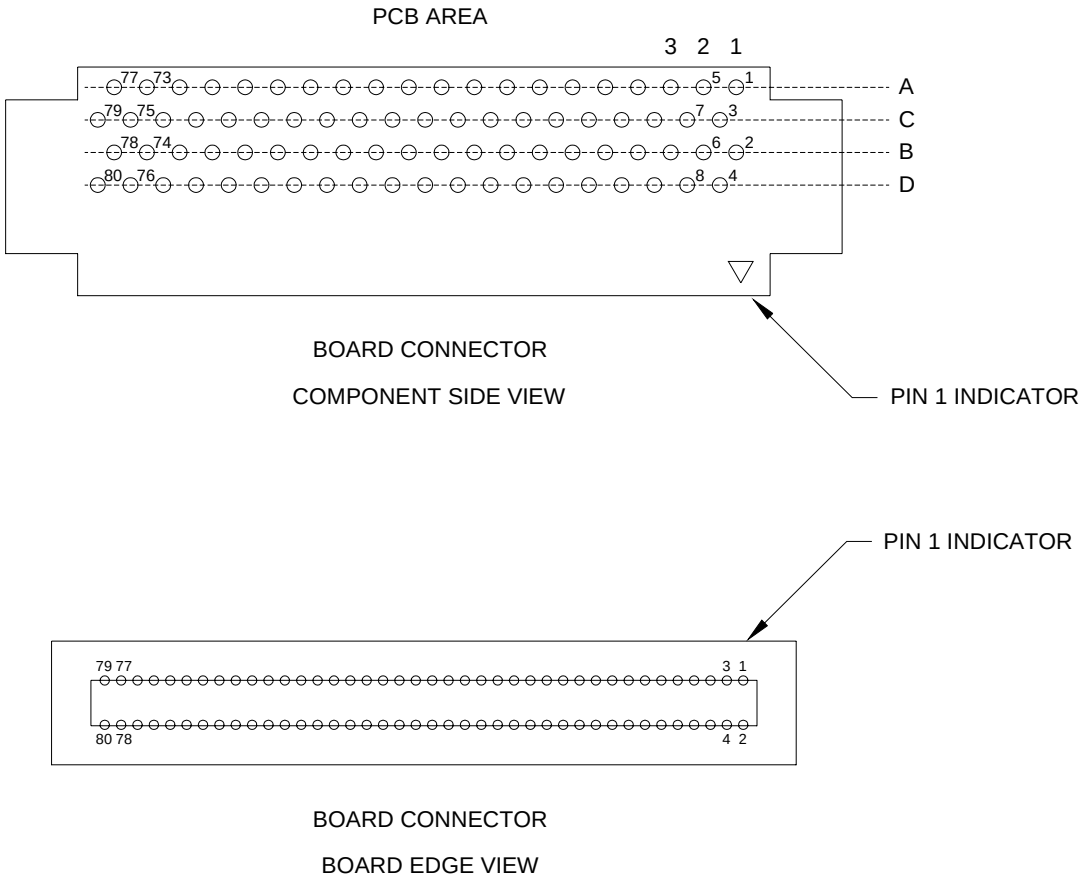
Connector on board:	KEL 8831E-080-170L
Mating connector:	KEL 8825E-080-175 (with strain relief)
	KEL 8825R-080-175 (without strain relief)
	R-N P25E-080S-TG
Manufacturers:	KEL Corporation, (408) 720-9044
	Robinson-Nugent, (812) 945-0211

Note 1: The ICS-610 uses 24 bits of the 32 bit data bus width available on the FPDP (D31:D00) when generating unpacked data. The bits used are D31:D08. When generating packed data, all 32 bits are driven and contain two 16-bit samples. The unused pins are driven low.

Note 2: When connecting one or more ICS-610 boards to a DSP board, the user should be aware that some DSP implementations have the FPDP connector and pinouts inverted. For the ICS-610, the connector index mark appears at the connector end nearest the panel; cable conductor #1 is adjacent to this mark. In order to prevent the need to fold the FPDP ribbon cable when connecting to a DSP board with an inverted FPDP configuration, the cable must have connectors that are inverted with respect to one another. The pinouts at the DSP FPDP connector are therefore reversed, compared to the ones given below. In other words, at the DSP, connector pin 1 connects to pin 80 at the ICS-610, while pin 79 connects to pin 2 at the ICS-610.

The FPDP is a high performance 32 bit parallel interface configured with a ribbon cable to connect boards or systems together. The simple and well-defined physical and electrical interface provides the basis for integrating many different types of boards and sub-systems. The maximum clock rate of the ICS-610 FPDP interface is 20 MHz, providing a sustained data rate of up to 80 MBytes/second. Since multiple FPDP buses are possible, the total data path bus bandwidth may be scaled to system requirements.

D.1 FPDP Connector Pin Assignments



Connector row and column designations are shown outside connector outline.

Cable numbers are shown inside connector outline.

FPDP BOARD-MOUNTED CONNECTOR
KEL 8831E-080-170L
or
Robinson-Nugent P50E-080P1-SR1-TG

K10128B2

Figure 10 - FPDP Board Connector

The FPDP interface connector is an 80-pin high density connector available from KEL and Robinson-Nugent. The connector on the board is a KEL 8831E-080-170L or R-N P50E-080P1-SR1-TG and is shown in Figure 10. The mating cable connector is a KEL 8825E-080-175S or R-N P25E-080S-TG, and takes a single ribbon cable of 80 conductors on 0.025 inch pitch. Table D.1 defines the connector pin assignments.

Table D.1 - ICS-610 FPDP P5 Connector Pin Assignments

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	GND	2	STROBE	3	GND	4	GND
5	GND	6	GND	7	NRDY*	8	GND
9	DIR*	10	GND	11	RESERVED	12	GND
13	SUSPEND*	14	GND	15	GND	16	GND
17	PIO2	18	GND	19	PIO1	20	GND
21	RESERVED	22	GND	23	RESERVED	24	GND
25	PSTROBE	26	GND	27	PSTROBE*	28	GND
29	SYNC*	30	GND	31	DVALID*	32	GND
33	D31	34	D30	35	GND	36	D29
37	D28	38	GND	39	D27	40	D26
41	GND	42	D25	43	D24	44	GND
45	D23	46	D22	47	GND	48	D21
49	D20	50	GND	51	D19	52	D18
53	GND	54	D17	55	D16	56	GND
57	D15	58	D14	59	GND	60	D13
61	D12	62	GND	63	D11	64	D10
65	GND	66	D09	67	D08	68	GND
69	D07	70	D06	71	GND	72	D05
73	D04	74	GND	75	D03	76	D02
77	GND	78	D01	79	D00	80	GND

D.2 FPDP Signals

A description of FPDP signals is given in Table D.2 .

Further details concerning the FPDP design are given in Reference [5].

Table D.2 - ICS-610 FPDP Signal Descriptions

Signal/s	Signal Name	Description
D31:00	Data Bus	32 bit data bus driven by the data source.
DIR*	Data Direction	The data source asserts DIR* low.
DVALID*	Data Valid	When asserted, DVALID* indicates that the data bus has valid data. This signal is generated by the data source with each data sample.
STROB	Data Strobe	STROB is a free running clock supplied by the data source. The receiving end should clock the data with the rising edge of STROB.
NRDY*	Not Ready	NRDY* is asserted by the receiver when it is not ready to receive data. The data source must sample this signal until the receiver brings it high, at which time the transfer can commence. Since NRDY* is asynchronous to STROB, the data source should double-synchronize to it before sampling its state; this avoid metastability problems.
PIO1,PIO2	Prog. I/O	The PIO signals are programmable I/O lines for user-defined functions. They can be configured as inputs or outputs.
PSTROBE	+ PECL Data Strobe	This signal along with PSTROBE* are generated by the data source as an optional differential PECL (Positive Emitter-Coupled Logic) data strobe. PSTROBE is the positive version of the differential clock and has the same polarity as STROB. For high data rate applications, the differential PECL data strobe should be used instead of STROB. The user must configure the board appropriately; see Section 4.2.
PSTROBE*	- PECL Data Strobe	This signal is the negative version of the differential PECL data strobe.
RESERVED		Do not connect to reserved signals.
SUSPEND*	Suspend Data	SUSPEND* is generated by the receiver to inform the data source of a pending FIFO overflow condition. The data source is allowed as many as 16 cycles before suspending the transfer. Since SUSPEND* is asynchronous to STROB, the data source should be double-synchronized to it before sampling its state; this avoids metastability problems.
SYNC*	Sync Pulse	The data source can provide a sync pulse to the receiver to synchronize data transfers. The receiver waits for the sync pulse before accepting data. The receiver starts accepting data on the first Data Valid period following the sync pulse.

