VMIC VMIVME-1160A-123

32-Bit Optically Coupled Digital Input Module

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VMIVME-1160A

32-bit OPTICALLY COUPLED DIGITAL INPUT BOARD WITH CHANGE-OF-STATE DETECTION

INSTRUCTION MANUAL

DOCUMENT NO. 500-101160-000 C

Revised June 18, 1999

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(I/O man figure)

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RECORD OF REVISIONS

REVISION LETTER	DATE	PAGES INVOLVED	CHANGE NUMBER
A	07/7/92	Release Manual	92-0232
B	02/16/94	Cover, pages ii and 5-5	94-0210
C	06/18/99	Cover, pages ii, v, vi, vii, 5-2, 5-3, and Section 6	99-0551

VMIC
SAFETY SUMMARY

THE FOLLOWING GENERAL SAFETY PRECAUTIONS MUST BE OBSERVED DURING ALL PHASES OF THE OPERATION, SERVICE, AND REPAIR OF THIS PRODUCT. FAILURE TO COMPLY WITH THESE PRECAUTIONS OR WITH SPECIFIC WARNINGS ELSEWHERE IN THIS MANUAL VIOLATES SAFETY STANDARDS OF DESIGN, MANUFACTURE, AND INTENDED USE OF THIS PRODUCT. VME MICROSYSTEMS INTERNATIONAL CORPORATION ASSUMES NO LIABILITY FOR THE CUSTOMER'S FAILURE TO COMPLY WITH THESE REQUIREMENTS.

GROUND THE SYSTEM

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY SYSTEM

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to VME Microsystems International Corporation for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS

Warnings, such as the example below, precede only potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

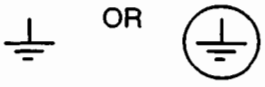
DANGEROUS VOLTAGES, CAPABLE OF CAUSING DEATH, ARE PRESENT IN THIS SYSTEM. USE EXTREME CAUTION WHEN HANDLING, TESTING, AND ADJUSTING.

SAFETY SYMBOLS

GENERAL DEFINITIONS OF SAFETY SYMBOLS USED IN THIS MANUAL

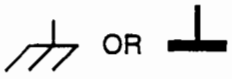
Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect against damage to the system.

Indicates dangerous voltage (terminals fed from the interior by voltage exceeding 1000 volts are so marked).



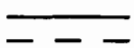
Protective conductor terminal. For protection against electrical shock in case of a fault. Used with field wiring terminals to indicate the terminal which must be connected to ground before operating equipment.

Low-noise or noiseless, clean ground (earth) terminal. Used for a signal common, as well as providing protection against electrical shock in case of a fault. Before operating the equipment, terminal marked with this symbol must be connected to ground in the manner described in the installation (operation) manual.

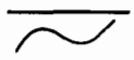


Frame or chassis terminal. A connection to the frame (chassis) of the equipment which normally includes all exposed metal structures.

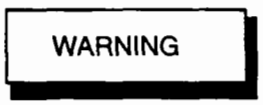
Alternating current (power line).



Direct current (power line).



Alternating or direct current (power line).



The WARNING sign denotes a hazard. It calls attention to a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

The CAUTION sign denotes a hazard. It calls attention to an operating a procedure, a practice, a condition, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the system.

NOTE: The NOTE sign denotes important information. It calls attention to a procedure, a practice, a condition or the like, which is essential to highlight.

VMIVME-1160A

32-bit OPTICALLY COUPLED DIGITAL INPUT BOARD WITH CHANGE-OF-STATE DETECTION

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SECTION 1

INTRODUCTION

1.1 INTRODUCTION

The VMIVME-1160A is designed with standard Change-of-State (COS) control and interrupt logic that detects any COS and provides an interrupt vector to the byte level. It incorporates an MC68153 Bus Interrupter Module (BIM) and interrupts are supported on any of seven levels.

Each byte (8 bits) of input may have a unique interrupt vector that is generated upon a COS in any bit of that byte. This product also has an Interrupt Enable Register which is used to allow interrupts to be enabled on a byte-by-byte basis. The input data may be accessed as a D8 or D16 transfer.

A functional block diagram of this product is shown in Figure 1.1-1. Interrupts are generated on any COS (positive or negative transition). Polarity is determined by reading the input port after the COS interrupt.

NOTE

STATE CHANGES THAT OCCUR DURING THE INTERRUPT PROCESSING WINDOW (INTERNAL REQUEST TO INTERRUPT ACKNOWLEDGE CYCLE COMPLETE) WILL NOT BE DETECTED. THE TIME BETWEEN USER INPUT STATE CHANGES MUST NOT BE LESS THAN THE COMPUTER INTERRUPT PROCESSING TIME; OTHERWISE, THE STATE CHANGES WILL BE LOST.

A Change-of-State Application Guide that describes the complete COSMODULE™ product line, VMIC's Document No. 825-000000-002, is available from VMIC. A summary of the COSMODULE™ product line is provided in Table 1.1-1 for reference.

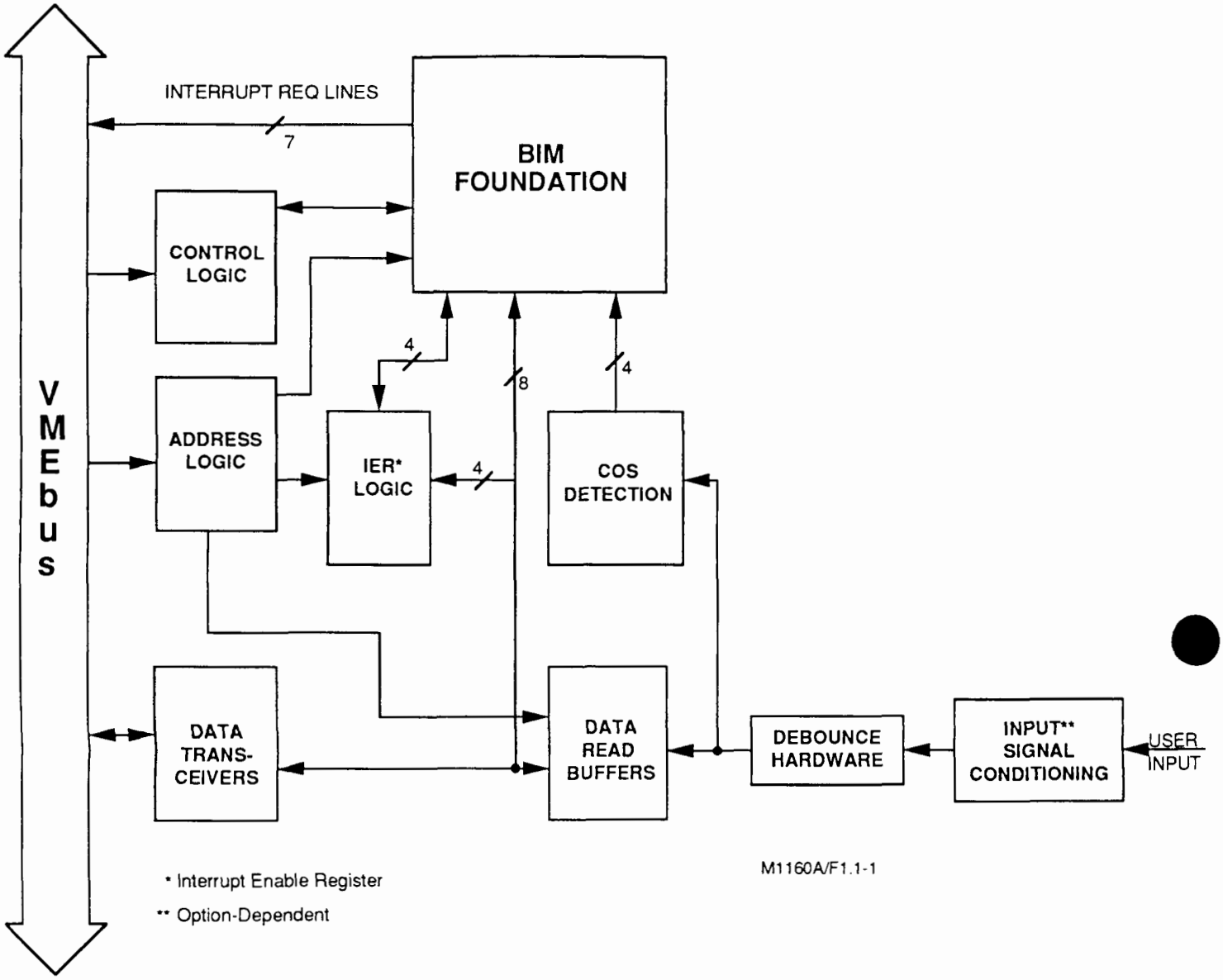


Figure 1.1-1. Typical COSMODULE™ Functional Block Diagram

Table 1.1-1. COSMODULE™ Product Line Summary

ITEM NO.	DESCRIPTION	MODEL NO.	TRANSFER TYPE
1.	16-Channel AC or DC High Voltage (5 V to 240 V) Optically Coupled Input with Change-of-State Interrupt	VMIVME-1001	D8,D16
2.	32-bit TTL Digital Input with Change-of-State Interrupt	VMIVME-1101	D8,D16
3.	32-bit High Voltage (5 to 50 V) Digital Input with Change-of-State Interrupt	VMIVME-1180	D8,D16
4.	32-bit High Voltage (1 to 66 V) COS board with Data Capture Registers and Built-in-Test	VMIVME-1181	D8,D16,D32
5.	32-bit Optically Coupled Digital Input with Change-of-State Interrupt	VMIVME-1160A	D8,D16

M1160A/T1.1-1

1.2 FUNCTIONAL DESCRIPTION

The VMIVME-1160A provides 32 high voltage, optically coupled inputs with change-of-state detection and vectoring to the byte level. The interrupt functions are supported by an MC68153 Bus Interrupter Module. The major features of the VMIVME-1160A are:

a. Quad 8-bit ports
b. Change-of-State port identified with interrupt vector
c. Voltage sourcing or contact sensing signal conditioning
d. Double-height Eurocard form factor with front panel
e. 8- or 16-bit data transfers
f. 64-pin DIN type input connector
g. Jumper-selectable nonprivileged short I/O, supervisory short I/O, or both
h. 32 optically coupled inputs

1.3 REFERENCE MATERIAL LIST

The reader should refer to "The VMEbus Specification" for a detailed explanation of the VMEbus. "The VMEbus Specification" is available from the following source:

VITA
VMEbus International Trade Association
10229 N. Scottsdale Road
Scottsdale, AZ 85253
(602) 951-8866

The following Application and Configuration Guides are available from VMIC to assist the user in the selection, specification, and implementation of systems based on VMIC's products:

TITLE	DOCUMENT NO.
Digital Input Board Application Guide	825-000000-000
Change-of-State Application Guide	825-000000-002
Digital I/O (with Built-in-Test) Product Line Description	825-000000-003
Connector and I/O Cable Application Guide	825-000000-006

SECTION 2

PHYSICAL DESCRIPTION AND SPECIFICATIONS

REFER TO 800-101160-000 SPECIFICATION

SECTION 3

THEORY OF OPERATION

3.1 BLOCK DIAGRAMS

The VMIVME-1160A consists of eight functional building blocks as illustrated in Figure 3.1-1. The eight sections of the VMIVME-1160A are: (1) Address Logic; (2) Control Logic; (3) Data Logic; (4) Bus Interrupter Module (BIM) Logic; (5) Interrupt Enable Logic; (6) Change-of-State Detection Logic; (7) Input Data Registers; and (8) Input Buffers. Each section of the design is illustrated in further detail in Figures 3.1-2 through 3.1-10.

3.2 INTERRUPT FUNCTIONS

Interrupts are generated on any Change-of-State (positive or negative transition). The polarity is determined by reading the input port after a Change-of-State interrupt occurs.

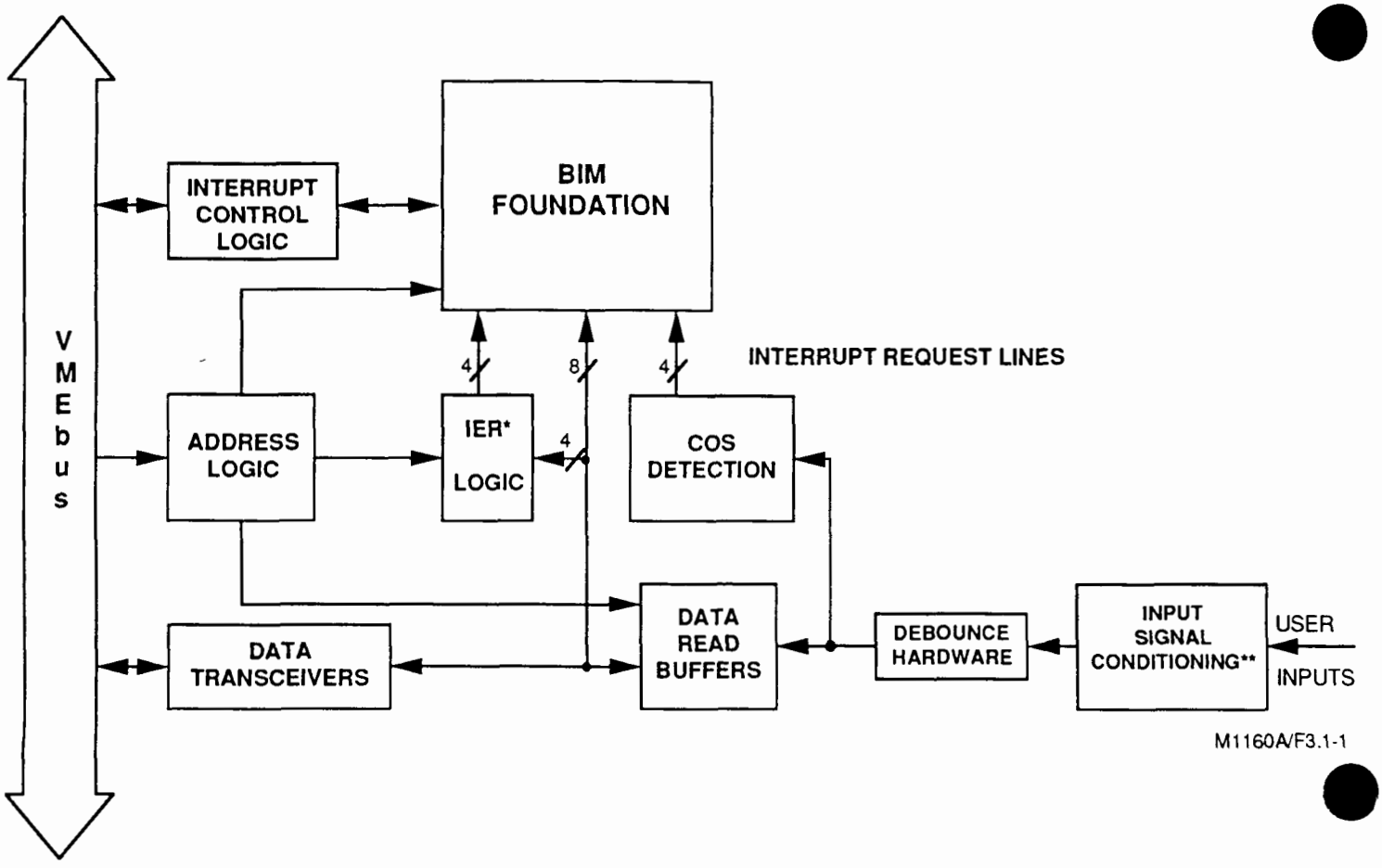
NOTE

STATE CHANGES THAT OCCUR DURING THE INTERRUPT PROCESSING WINDOW (INTERNAL REQUEST TO INTERRUPT ACKNOWLEDGE CYCLE COMPLETE) WILL NOT BE DETECTED. THE TIME BETWEEN USER INPUT STATE CHANGES MUST NOT BE LESS THAN THE COMPUTER INTERRUPT PROCESSING TIME; OTHERWISE, THE STATE CHANGES WILL BE LOST.

The reader should refer to "The VMEbus Specification" for a detailed explanation of the priority interrupt bus. "The VMEbus Specification" is available from the following source:

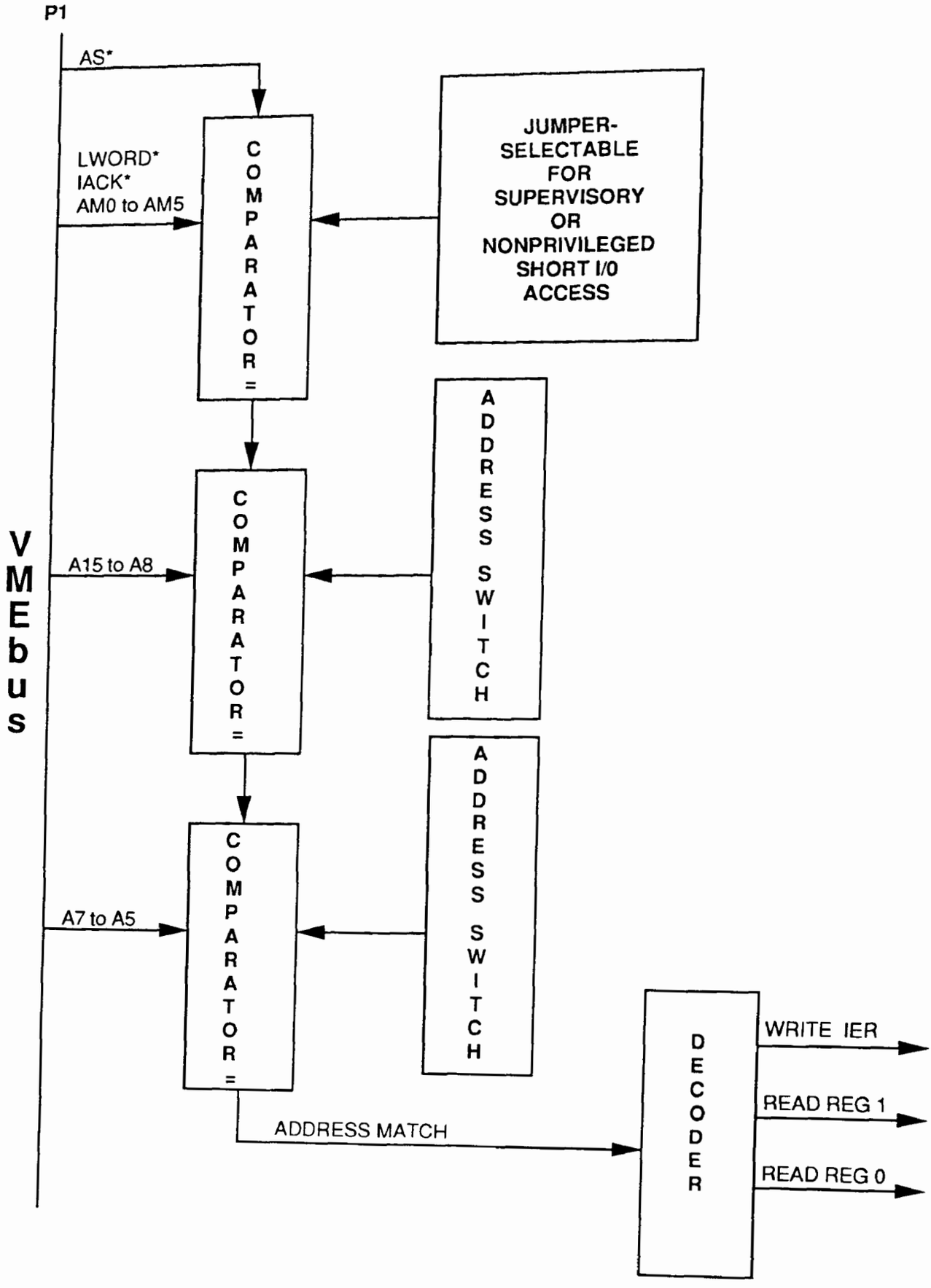
VITA
VMEbus International Trade Association
10229 N. Scottsdale Road
Scottsdale, AZ 85253
(602) 951-8866

The data transfer bus, the arbitration bus, and the interrupt bus are all used in the process of generating and handling bus interrupts.



*Internal Enable Register
**Option Dependent

Figure 3.1-1. VMIVME-1160A Functional Block Diagram



M1160A/F3.1-2

Figure 3.1-2. Address Section Block Diagram

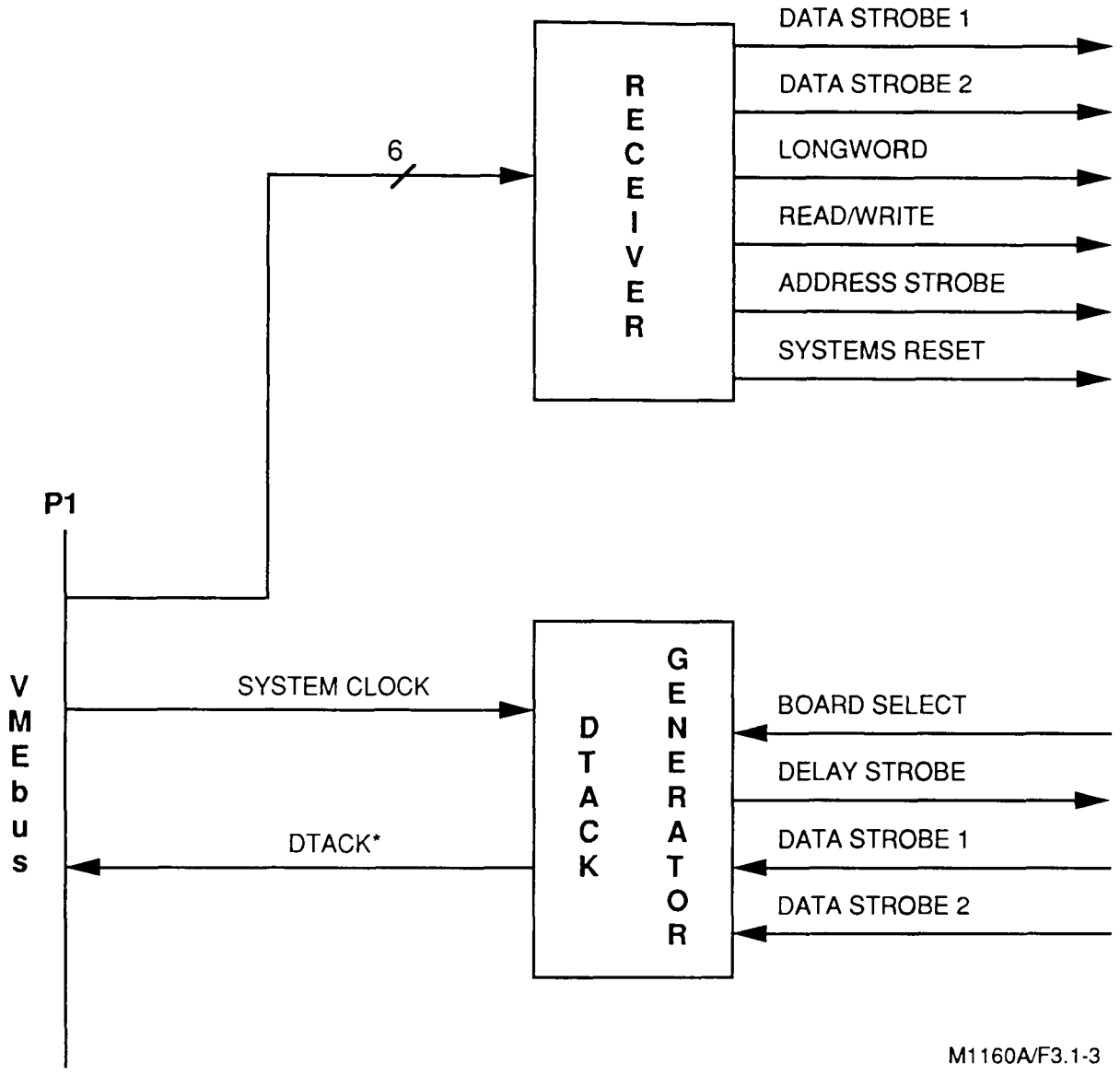


Figure 3.1-3. Control Section Block Diagram

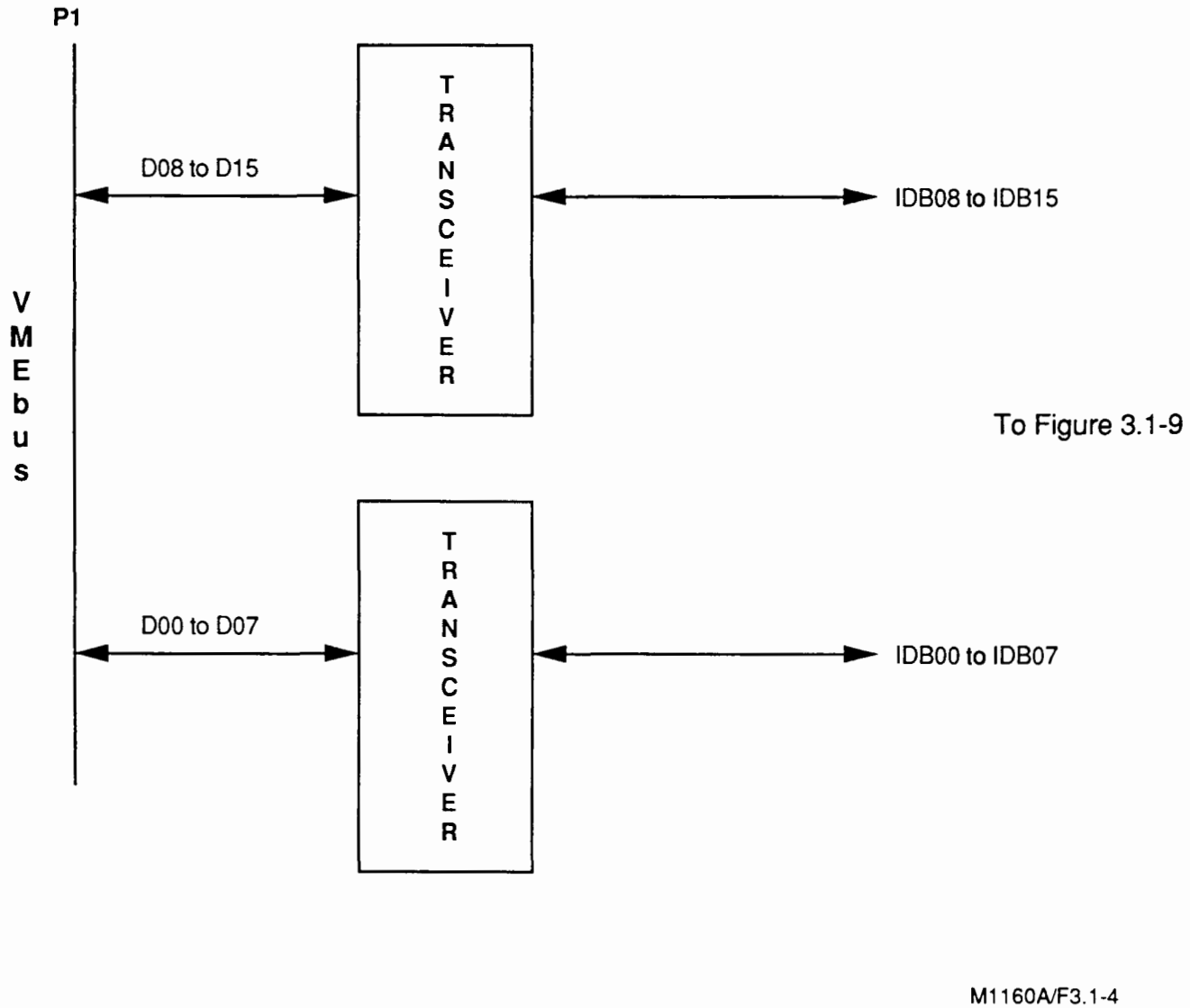


Figure 3.1-4. Data Section Block Diagram

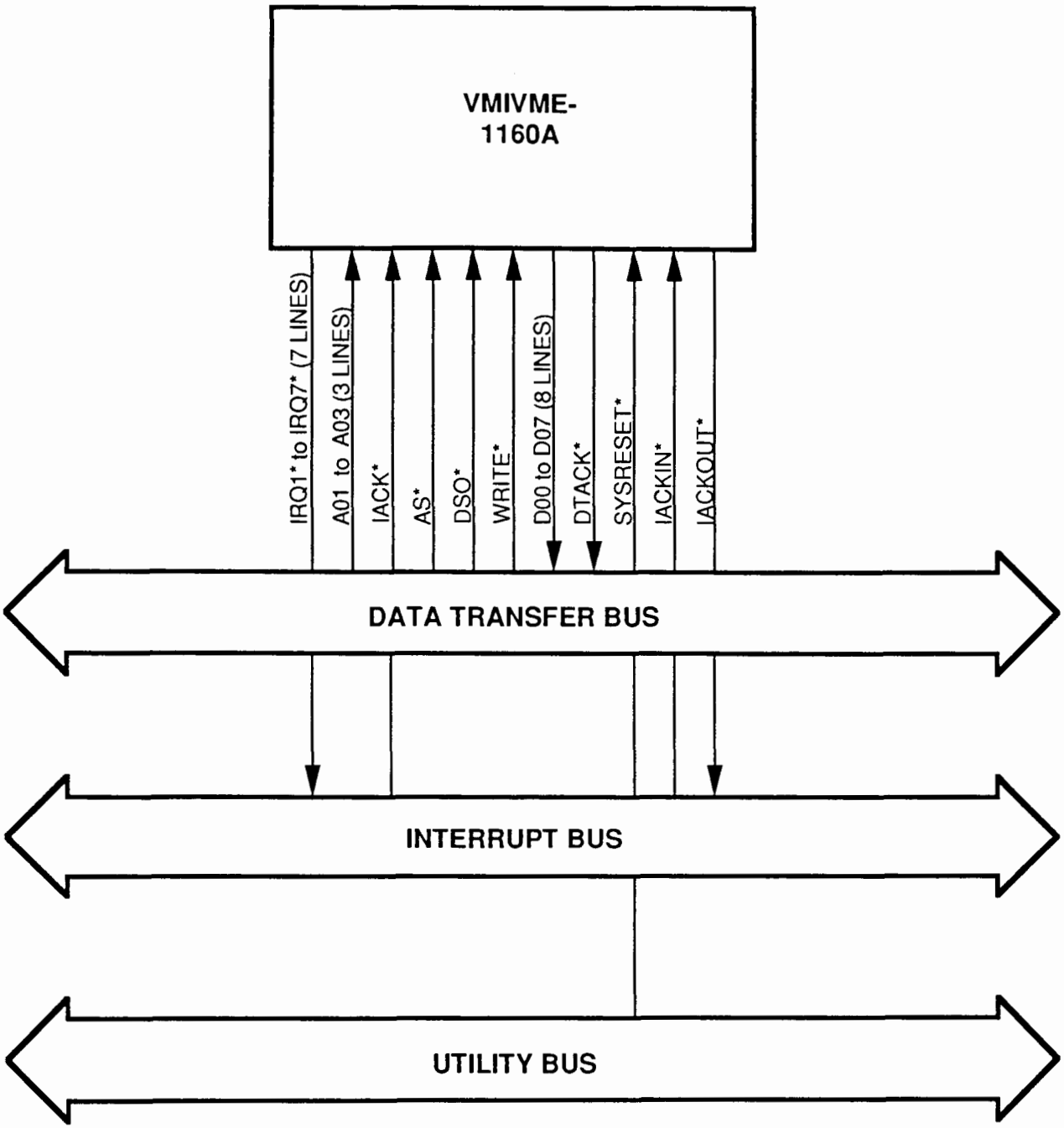


Figure 3.1-5. VMEbus Signal Lines Used by the VMIVME-1160A

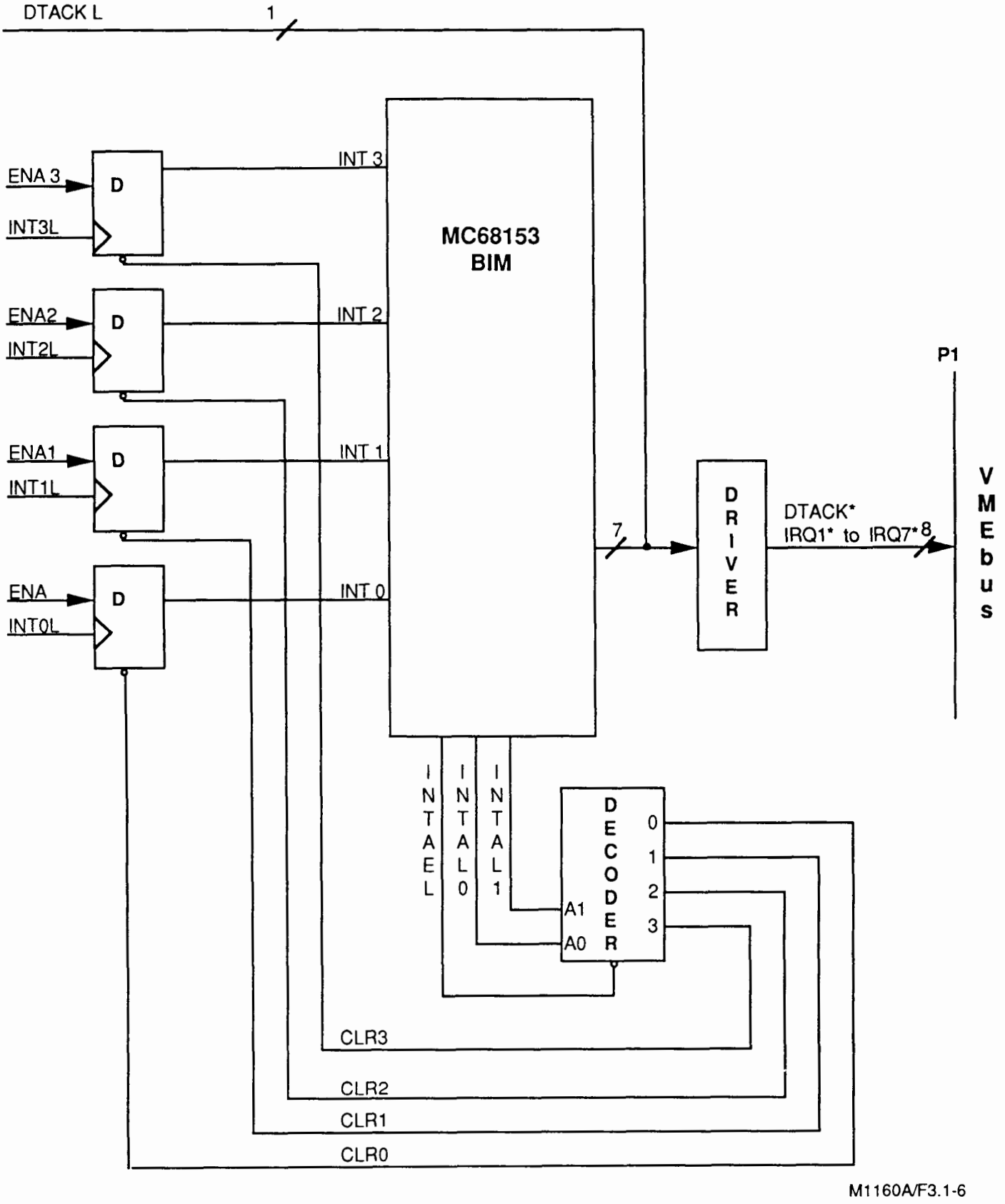


Figure 3.1-6. BIM Foundation Section Block Diagram

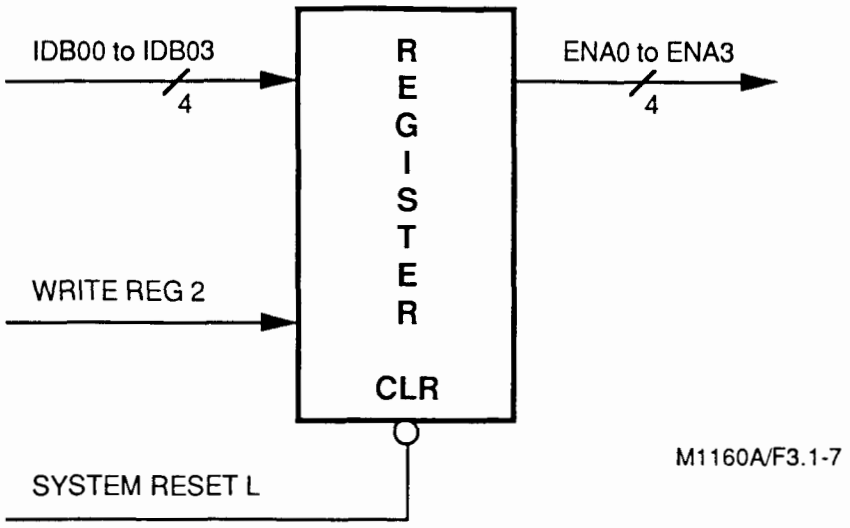


Figure 3.1-7. Typical IER Logic Section

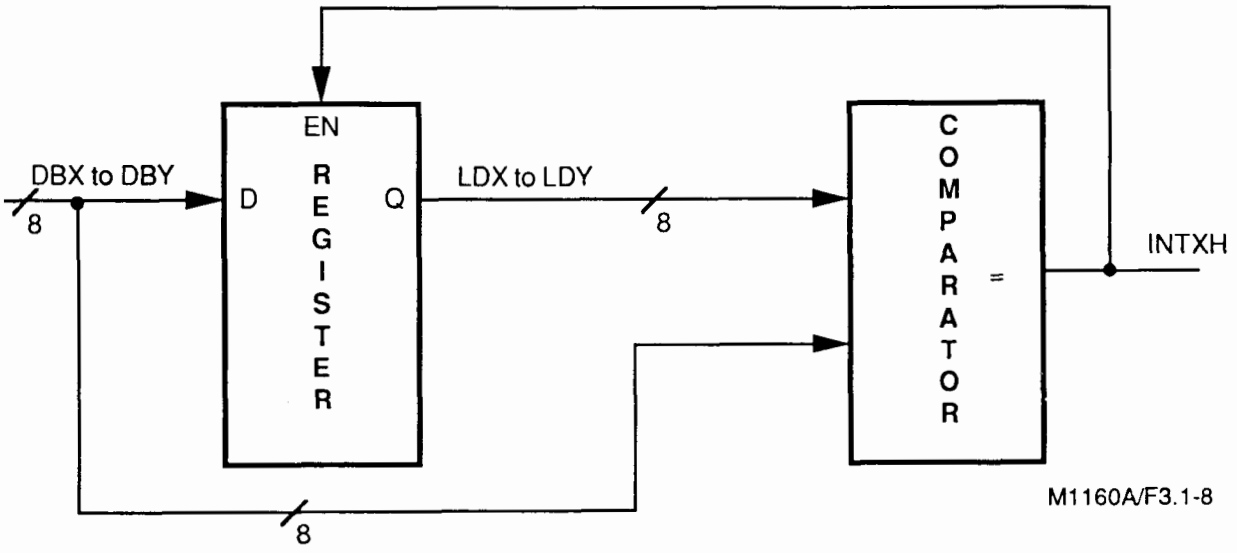


Figure 3.1-8. Typical Change-of-State Detection Logic Section

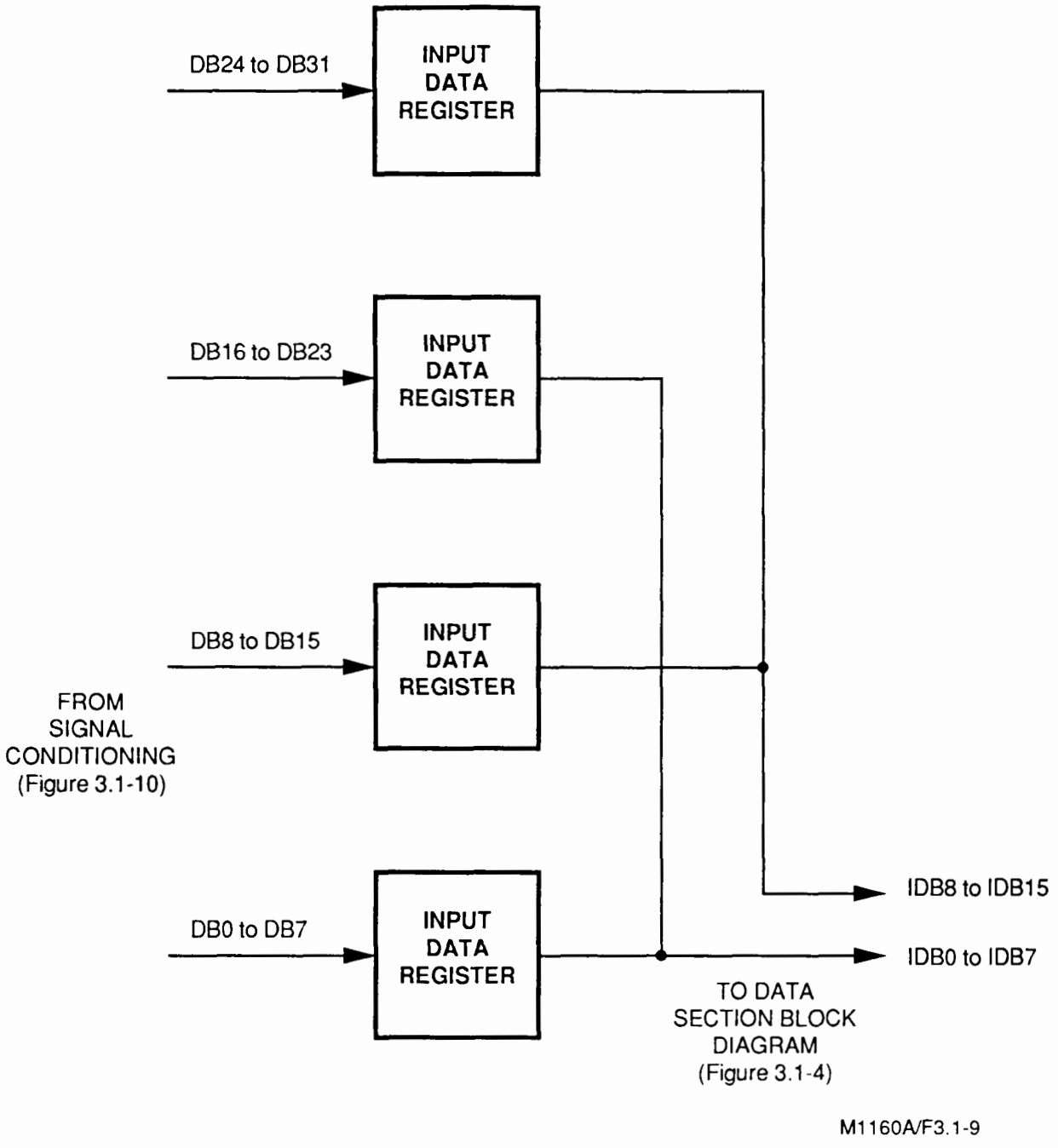


Figure 3.1-9. Input Data Registers Block Diagram

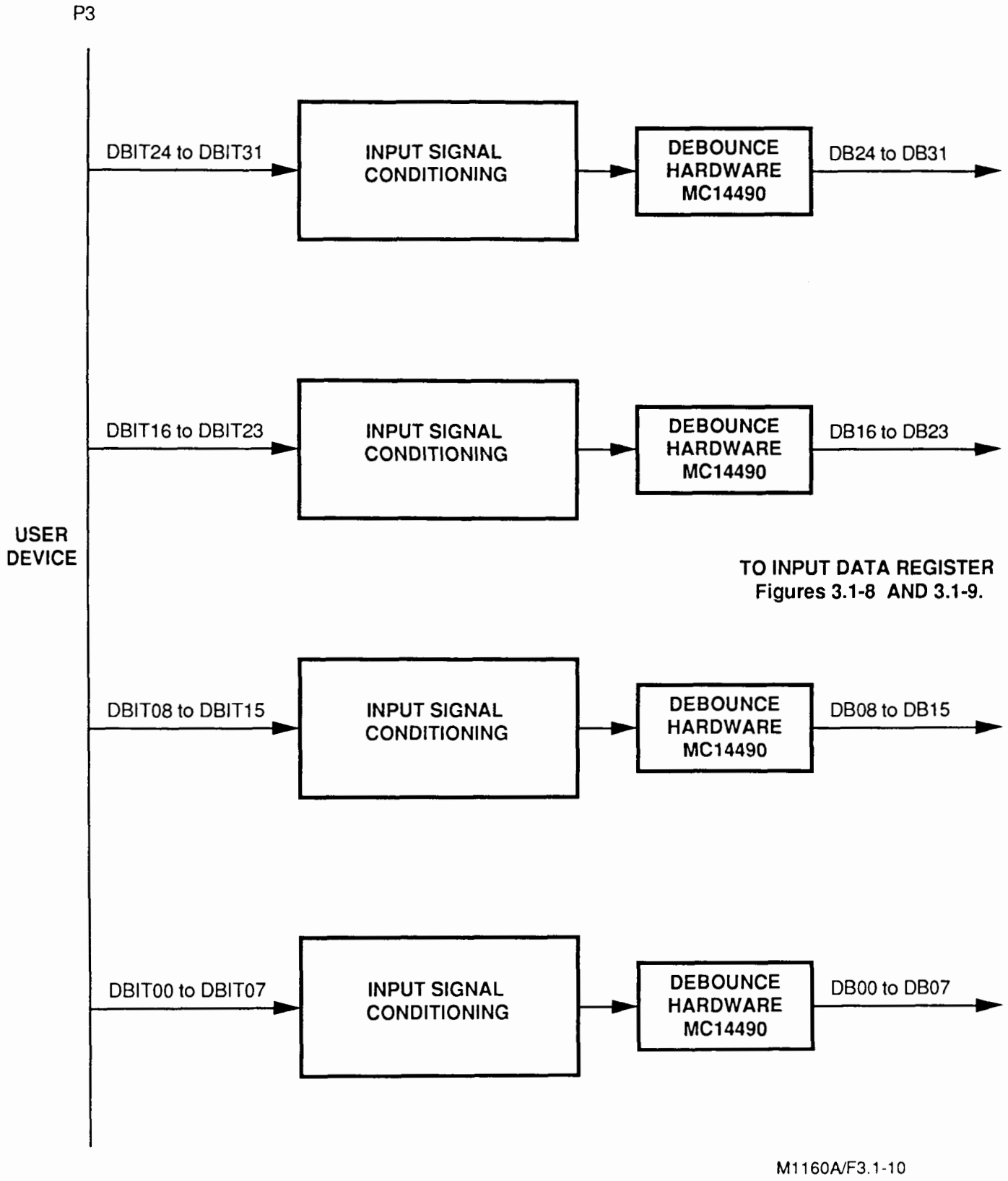


Figure 3.1-10. Signal Conditioning Block Diagram

3.3 PRIORITY INTERRUPT SUBSYSTEM

The following overview of the priority interrupt subsystem assumes that the reader understands the operation of both the data transfer bus and the arbitration bus.

The interrupt bus consists of seven interrupt request signal lines, one daisy-chain signal line, and one interrupt acknowledge line:

IRQ1*	IRQ4*	IRQ7*
IRQ2*	IRQ5*	IACK*
IRQ3*	IRQ6*	IACKIN*/IACKOUT*

Each interrupt request line may be driven low by the VMIVME-1160A Board or other interrupter to request an interrupt. In a single handler system, these interrupt request lines are prioritized, with IRQ7* having the highest priority.

The IACK* line runs the full length of the bus and is connected to the IACKIN* pin of slot A1. When it is driven low, it initiates a low-going transition down the interrupt acknowledge daisy-chain. This may not occur immediately, since additional constraints are placed on the propagation of IACKIN*/IACKOUT*.

Each of the seven interrupt request lines may be shared by two or more interrupter boards. Because of this, some method must be provided to ensure that only one of the boards is acknowledged. This is done by means of the interrupt acknowledge daisy-chain. The daisy-chain line passes through each board on the VMEbus. When an interrupt is acknowledged, IACKIN* is driven low at slot A1. Each board that is driving an interrupt request line low must wait for the low level down the daisy-chain, thereby guaranteeing that only one board will be acknowledged.

The VMIVME-1160A uses one of the seven IRQX* lines to request an interrupt. It then monitors the DTB address bus, IACK*, and the IACKIN*/IACKOUT* daisy-chain to determine when its interrupt is being acknowledged. When acknowledged, it places its status/ID byte on the lower eight lines of the data bus and signals the byte's validity to the interrupt handler via the DTACK* line.

The VMEbus signal lines used by the VMIVME-1160A are shown in Figure 3.1-4.

The reader should refer to Appendix B, which contains Motorola's application note on the MC68153, for a detailed explanation of the Bus Interrupter Module (BIM).

SECTION 4

PROGRAMMING

4.1 OPERATIONAL OVERVIEW

The VMIVME-1160A is designed to provide 32 channels of high voltage, optically coupled inputs with change-of-state detection. Each eight bits (byte) of input may have a unique interrupt vector that is generated upon a change-of-state of any bit in that byte. The VMIVME-1160A also has an Interrupt Enable Register which is used to allow interrupts on change-of-state to be enabled on a byte basis. The channels of input data may be accessed as two 16-bit words or four 8-bit bytes.

A register map is shown in Table 4.1-1. Detailed register bit definitions are shown in Tables 4.1-2, 4.1-3, and 4.1-4. A typical flow diagram is shown in Figure 4.1-1.

Table 4.1-1. Register Map

RELATIVE ADDRESS	MNEMONIC	NAME/FUNCTION	
$XX00	DR0	Data Register 0	
$XX01	DR1	Data Register 1	
$XX02	DR2	Data Register 2	
$XX03	DR3	Data Register 3	
$XX05	IER	Interrupt Enable Register	
$XX11	CR0	Control Register 0	MC68153 BIM REGISTERS
$XX13	CR1	Control Register 1	
$XX15	CR2	Control Register 2	
$XX17	CR3	Control Register 3	
$XX19	VR0	Vector Register 0	
$XX1B	VR1	Vector Register 1	
$XX1D	VR2	Vector Register 2	
$XX1F	VR3	Vector Register 3	

M1160A/T4.1-1

The reader may want to refer to Appendix B for detailed programming characteristics of the MC68153 BIM.

Table 4.1-2. Typical Input Data Register Bit Maps

$XX00 DR0

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
INPUT DATA							
ID31	ID30	ID29	ID28	ID27	ID26	ID25	ID24

$XX01 DR1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INPUT DATA							
ID23	ID22	ID21	ID20	ID19	ID18	ID17	ID16

$XX02 DR2

BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
INPUT DATA							
ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8

$XX03 DR3

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INPUT DATA							
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

$XX05 IER

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
				INTERRUPT ENABLE*			
RESERVED				DR0	DR1	DR2	DR3

M1160A/T4.1-2

* A "one" in the BIT location will enable the interrupts for the stated Data Register.

Table 4.1-3. Typical BIM Control Register Map

$XX11 CONTROL REGISTER 0 (Control for DR3 Inputs)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FLAG	FLAG AUTO CLEAR	VECTOR	INT ENABLE	INT AUTO CLEAR	INTERRUPT LEVEL		
F	FAC	0=INTERNAL 1=EXTERNAL	IRE	1=AUTO 0=NO	L2	L1	L0

$XX13 CONTROL REGISTER 1 (Control for DR2 Inputs)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FLAG	FLAG AUTO CLEAR	VECTOR	INT ENABLE	INT AUTO CLEAR	INTERRUPT LEVEL		
F	FAC	0=INTERNAL 1=EXTERNAL	IRE	1=AUTO 0=NO	L2	L1	L0

$XX15 CONTROL REGISTER 2 (Control for DR1 Inputs)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FLAG	FLAG AUTO CLEAR	VECTOR	INT ENABLE	INT AUTO CLEAR	INTERRUPT LEVEL		
F	FAC	0=INTERNAL 1=EXTERNAL	IRE	1=AUTO 0=NO	L2	L1	L0

$XX17 CONTROL REGISTER 3 (Control for DR0 Inputs)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FLAG	FLAG AUTO CLEAR	VECTOR	INT ENABLE	INT AUTO CLEAR	INTERRUPT LEVEL		
F	FAC	0=INTERNAL 1=EXTERNAL	IRE	1=AUTO 0=NO	L2	L1	L0

M1160A/T4.1-3

Table 4.1-4. Typical BIM Vector Register Map

$XX19 VR0 (Vector for DR3 COS)*

VECTOR REGISTER							
V7	V6	V5	V4	V3	V2	V1	V0

$XX1B VR1 (Vector for DR2 COS)*

VECTOR REGISTER							
V7	V6	V5	V4	V3	V2	V1	V0

$XX1D VR2 (Vector for DR1 COS)*

VECTOR REGISTER							
V7	V6	V5	V4	V3	V2	V1	V0

$XX1F VR3 (Vector for DR0 COS)*

VECTOR REGISTER							
V7	V6	V5	V4	V3	V2	V1	V0

M1160A/T4.1-4

*COS = Change-of-State

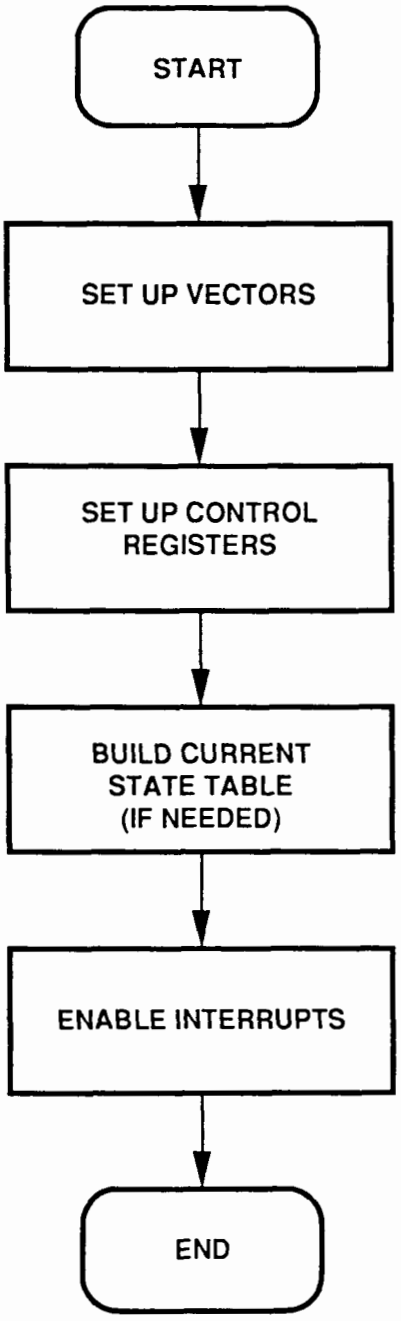


Figure 4.1-1. VMIVME-1160A Programming Flow Diagram

4.2 TYPICAL PROGRAMMING EXAMPLE

The following example code enables interrupts, processes interrupts, and displays the current input data when a change-of-state occurs.

```
/*
**  1160.h
**
**  VMIVME-1160 32 BIT OPTICALLY COUPLED DIGITAL INPUT W/COS
*/

struct vmivme_1160_registers {
  unsigned char offset[32];
};

typedef struct vmivme_1160_registers v1160_t;


/*
**  register offset definitions
**
**  note: defining register offsets using the above
**        structure/array and defines facilitates
**        skipping unused addresses in the board map.
*/

#define   dr0       offset[0x00]
#define   dr1       offset[0x01]
#define   dr2       offset[0x02]
#define   dr3       offset[0x03]
#define   ier       offset[0x05]
#define   cr0       offset[0x11]
#define   cr1       offset[0x13]
#define   cr2       offset[0x15]
#define   cr3       offset[0x17]
#define   vr0       offset[0x19]
#define   vr1       offset[0x1b]
#define   vr2       offset[0x1d]
#define   vr3       offset[0x1f]

/*
**  interrupt enable control bits
*/

#define   IE_DR3    0x08
#define   IE_DR2    0x04
#define   IE_DR1    0x02
#define   IE_DR0    0x01
```

```
/*
**  BIM control bits
*/

#define   FLAG_BIT            0x80
#define   FLAG_AUTO_CLEAR     0x40
#define   EXTERNAL_VECTOR     0x20      /* don't use ! - see manual */
#define   INTERRUPT_ENABLE    0x10
#define   INTR_AUTO_CLEAR     0x08
#define   REQUEST_LEVEL_7     0x07
#define   REQUEST_LEVEL_6     0x06
#define   REQUEST_LEVEL_5     0x05
#define   REQUEST_LEVEL_4     0x04
#define   REQUEST_LEVEL_3     0x03
#define   REQUEST_LEVEL_2     0x02
#define   REQUEST_LEVEL_1     0x01
#define   INTERRUPTS_OFF      0x00
```

```
/*
**  1160.c
**
**  VMIVME-1160 32 BIT OPTICALLY COUPLED DIGITAL INPUT W/COS
*/

#include  <stdio.h>
#include  "1160.h"

/*
**  System dependent definitions ( Force Cpu-33 SBC )
*/

#define   SHORTIO   0xfbff0000          /* short io window */

#define   USER_VECTOR( v )  v + 0x54    /* 1st available user vector
*/


/*
**  Define global pointer to vmivme 1160 board
*/

#define   BASE_ADDR_1160  0x0000    /* see manual section 5 */

v1160_t * board = (( v1160_t * )( SHORTIO + BASE_ADDR_1160 ));


/*
**  Define Global Change of State Flags and Data Storage
**
**  Note: COS flags and data variables are modified in the
**        Interrupt Service Routines (ISR's) and therefore
**        need to be global and/or visable to them.
*/

unsigned  char    cos_flags;

#define   COS_0   0x01
#define   COS_1   0x02
#define   COS_2   0x04
#define   COS_3   0x08

unsigned  char    cos_0_data;
unsigned  char    cos_1_data;
unsigned  char    cos_2_data;
unsigned  char    cos_3_data;
```

```
/*
**  Declare external functions ( ISR's )
**
**  Note: The interrupt service routines are written
**        in assembler and linked to the main C program.
**        They modify the globally defined variables
**        above that are visable to main and the ISR's.
*/

void  cos0isr( void );
void  cos1isr( void );
void  cos2isr( void );
void  cos3isr( void );


/*
**  INITIALIZE 1160 BOARD AND DISPLAY CHANGE OF STATE INPUTS
*/

main()
{

  /*
  **  Install ISR Addresses into CPU-33 Vector Table
  **
  **  Note: Vector installation is system dependent. Our
  **        method is through a libarary call that installs
  **        the ISR addresses according to the vector used.
  */

  setvect( USER_VECTOR( 0 ), &cos0isr );
  setvect( USER_VECTOR( 1 ), &cos1isr );
  setvect( USER_VECTOR( 2 ), &cos2isr );
  setvect( USER_VECTOR( 3 ), &cos3isr );

  /*
  **  Initialize Vector Registers
  **
  **  Note: Vectors available to the user are system dependent.
  */

  board->vr0 = USER_VECTOR( 0 );
  board->vr1 = USER_VECTOR( 1 );
  board->vr2 = USER_VECTOR( 2 );
  board->vr3 = USER_VECTOR( 3 );

  /*
  **  Initialize Interrupt Control Registers
  **
  **  The change of state interrupts are enabled with request
  **  levels 3 through 6 where 6 is the highest priority. This
  **  is an arbitrary level selection that could have been a mix
  **  or all the same level depending on the application ...
  */
```

```
  board->cr0 = ( INTERRUPT_ENABLE | INTR_AUTO_CLEAR | REQUEST_LEVEL_3 );
  board->cr1 = ( INTERRUPT_ENABLE | INTR_AUTO_CLEAR | REQUEST_LEVEL_4 );
  board->cr2 = ( INTERRUPT_ENABLE | INTR_AUTO_CLEAR | REQUEST_LEVEL_5 );
  board->cr3 = ( INTERRUPT_ENABLE | INTR_AUTO_CLEAR | REQUEST_LEVEL_6 );

  /*
  **  Initialize Interrupt Enable Register
  **
  **  Writing this register is necessary to enable COS information
  **  to cause interrupts. Each port has an associated interrupt
  **  enable control bit so that COS interrupts may be enabled on
  **  each bytewide port. This simple application enables interrupts
  **  and leaves them enabled. These enables could be used to switch
  **  interrupts on and off to capture or ignore data according to
  **  the application.
  */

  board->ier = ( IE_DR3 | IE_DR2 | IE_DR1 | IE_DR0 );

  /*
  **  Monitor Change of States and Print Input Data
  */

  for( ;; ) {       /* loop forever */

    if( cos_flags &  COS_3 ) {
      printf("\r\nDR3 COS data = %.2X", cos_3_data );
      cos_flags &= ~COS_3;
    }

    if( cos_flags &  COS_2 ) {
      printf("\r\nDR2 COS data = %.2X", cos_2_data );
      cos_flags &= ~COS_2;
    }

    if( cos_flags &  COS_1 ) {
      printf("\r\nDR1 COS data = %.2X", cos_1_data );
      cos_flags &= ~COS_1;
    }

    if( cos_flags &  COS_0 ) {
      printf("\r\nDR0 COS data = %.2X", cos_0_data );
      cos_flags &= ~COS_0;
    }
  }
}
```

```
**  1160isr.sa
**
**  VMIVME-1160 32 BIT OPTICALLY COUPLED DIGITAL INPUT W/COS
**

*    external references and declarations

          xref      _board
          xref      _cos_flags
          xref      _cos_3_data
          xref      _cos_2_data
          xref      _cos_1_data
          xref      _cos_0_data

          xdef      _cos0isr
          xdef      _cos1isr
          xdef      _cos2isr
          xdef      _cos3isr

*    offsets to board data registers

dr0       equ       $00
dr1       equ       $01
dr2       equ       $02
dr3       equ       $03

*    offsets to board intr ctrl registers

cr0       equ       $11
cr1       equ       $13
cr2       equ       $15
cr3       equ       $17

          section   code

*    service dr3 / cos3 interrupt

_cos3isr  movem.l   a0,-(a7)            preserve registers
          move.l    _board,a0           get pointer to board
          move.b    (dr3,a0),_cos_3_data read COS data
          bset      #4,(cr3,a0)         re-enable interrupt
          bset      #3,_cos_flags       set COS intr flag
          movem.l   (a7)+,a0            restore registers
          rte                           return from exception

*    service dr2 / cos2 interrupt

_cos2isr  movem.l   a0,-(a7)            preserve registers
          move.l    _board,a0           get pointer to board
          move.b    (dr2,a0),_cos_2_data read COS data
          bset      #4,(cr2,a0)         re-enable interrupt
          bset      #2,_cos_flags       set COS intr flag
          movem.l   (a7)+,a0            restore registers
          rte                           return from exception
```

```
*     service dr1 / cos1 interrupt

_cos1isr  movem.l   a0,-(a7)            preserve registers
          move.l    _board,a0           get pointer to board
          move.b    (dr1,a0),_cos_1_data read COS data
          bset      #4,(cr1,a0)         re-enable interrupt
          bset      #1,_cos_flags       set COS intr flag
          movem.l   (a7)+,a0            restore registers
          rte                           return from exception

*     service dr0 / cos0 interrupt

_cos0isr  movem.l   a0,-(a7)            preserve registers
          move.l    _board,a0           get pointer to board
          move.b    (dr0,a0),_cos_0_data read COS data
          bset      #4,(cr0,a0)         re-enable interrupt
          bset      #0,_cos_flags       set COS intr flag
          movem.l   (a7)+,a0            restore registers
          rte                           return from exception
```

SECTION 5

CONFIGURATION AND INSTALLATION

5.1 UNPACKING PROCEDURES

CAUTION

SOME OF THE COMPONENTS ASSEMBLED ON VMIC's PRODUCTS MAY BE SENSITIVE TO ELECTROSTATIC DISCHARGE AND DAMAGE MAY OCCUR ON BOARDS THAT ARE SUBJECTED TO A HIGH ENERGY ELECTROSTATIC FIELD. UNUSED BOARDS SHOULD BE STORED IN THE SAME PROTECTIVE BOXES IN WHICH THEY WERE SHIPPED. WHEN THE BOARD IS TO BE LAID ON A BENCH FOR CONFIGURING, etc., IT IS SUGGESTED THAT CONDUCTIVE MATERIAL BE INSERTED UNDER THE BOARD TO PROVIDE A CONDUCTIVE SHUNT.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to VMIC together with a request for advice concerning disposition of the damaged item(s).

5.2 PHYSICAL INSTALLATION

CAUTION

DO NOT INSTALL OR REMOVE BOARDS WHILE POWER IS APPLIED.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

5.3 CONFIGURATION SWITCHES

The reader should refer to Figure 5.3-1 for the locations of jumpers and address switches.

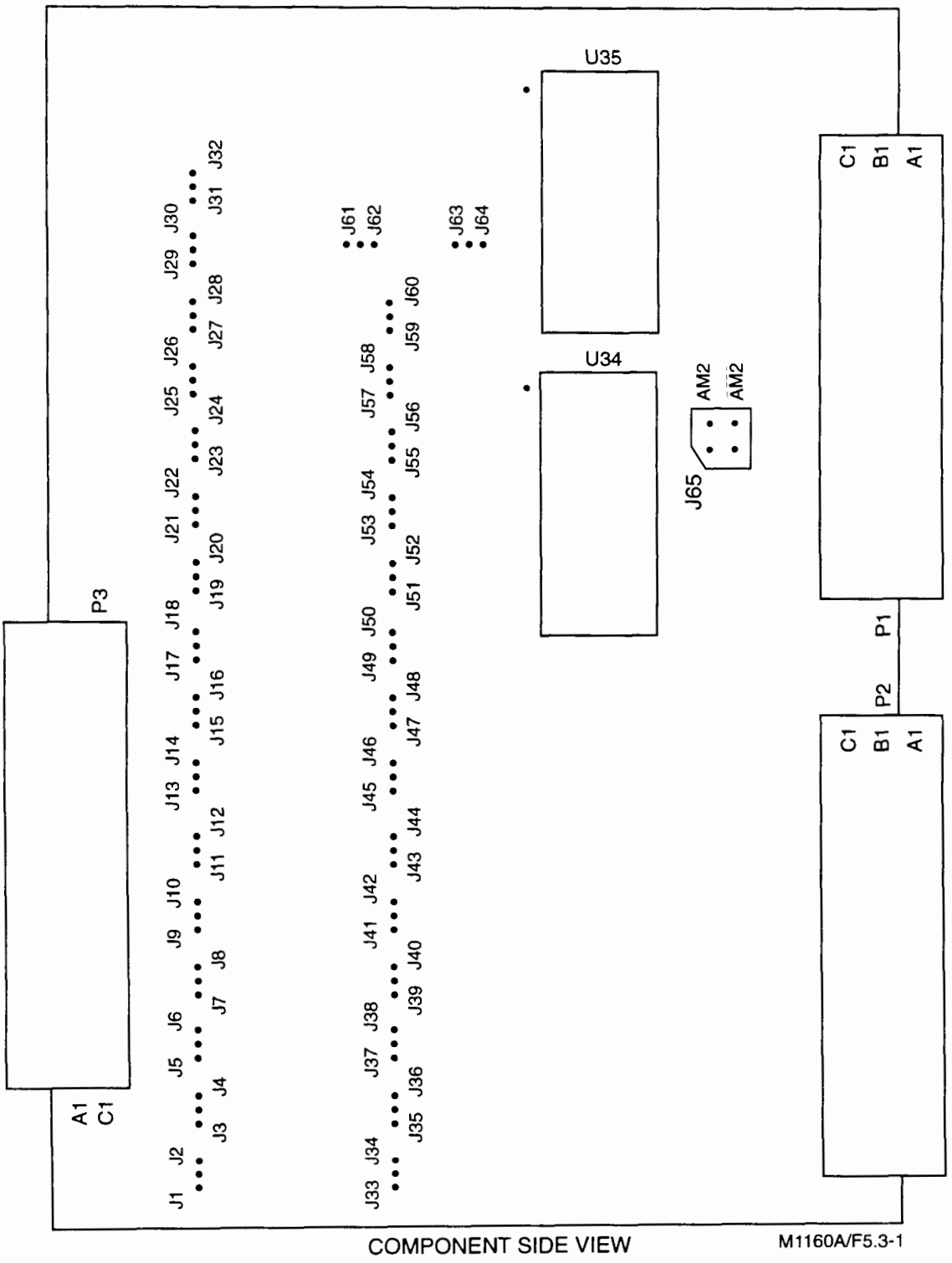


Figure 5.3-1. Location of Jumpers and Address Switches

5.4 CONTACT SENSE, VOLTAGE SOURCE SELECTION

The VMIVME-1160A may be ordered with its input signal conditioning electronics factory configured for voltage source or contact sense input options. A wide range of input V (5 to 48 V) are supported, and the user may select from a variety of input filters. Refer to the document number 800-101160-000 for complete ordering information.

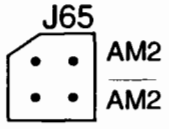
In Figure 5.8-1 Jx is the contact sense jumper. This jumper is installed at the factory when a contact sense board is ordered. Jx corresponds to the even numbered jumpers (J2, J4, etc.) on the schematic in the appendix of this manual. Jy is the voltage source jumper. It is installed for voltage source boards and corresponds to the odd numbered jumpers (J3, J5, etc.) except for jumper J65, which is the address modifier jumper.

5.5 EXTERNAL PULL-UP VOLTAGE

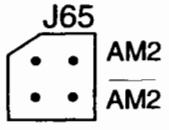
External voltage is connected through the P2 connector on pins C30, and C31 (VPOS uses P2 pin C30, VNEG uses P2 pin C31). This voltage is required on contact sense configurations only.

5.6 ADDRESS MODIFIERS

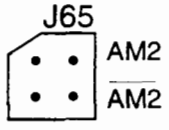
I/O Access Mode is configured by a dual header jumper post J65. Figures 5.6-1a, 5.6-1b, and 5.6-1c show how J65 can be configured for short supervisory I/O access, short I/O nonprivileged I/O access, or both. The VMIVME-1160A is factory configured to respond to short nonprivileged I/O access.



a. Configuration for Short Supervisory I/O Access, AM = 2D



b. Configuration for Short Nonprovileged I/O Acess, AM = 29



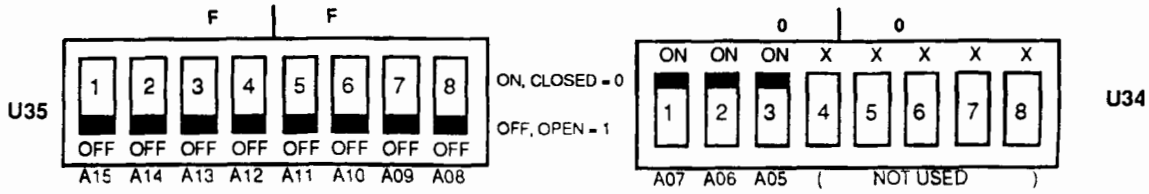
c. Configuration for both Short Supervisory I/O Access or Short Nonprvileged I/O Access

M1160A/F5.6-1

Figure 5.6-1. I/O Access Mode Selection

5.7 ADDRESS SELECTION SWITCHES

Figure 5.7-1 shows the two addressing DIP switches on board the VMIVME-1160A and their use in the addressing scheme.



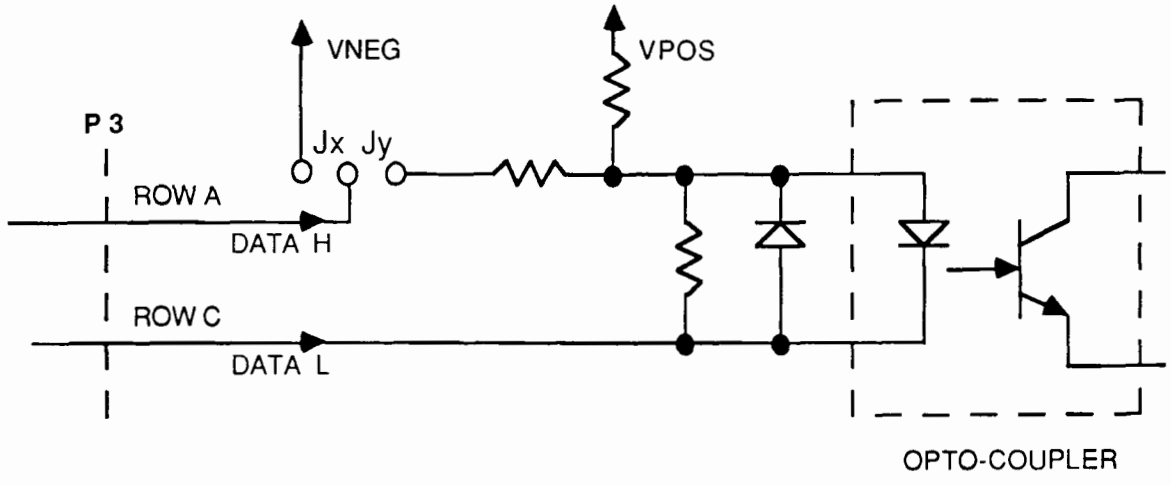
A base address FF00 HEX is shown in this example.

M1160A/F5.7-1

Figure 5.7-1. Data Register Address Select Switches

5.8 CONNECTOR PIN CONFIGURATION

Figure 5.8-1 below shows a typical input channel.



M1160A/F5.8-1

Figure 5.8-1. Typical Input Channel

The input connector, P3, is a 64-pin connector designed with pins in two rows, Row A and Row C. Connection is accomplished by connecting the appropriate row pin to the appropriate user signal. For example, in the voltage source case the user is recommended to connect the equipment ground to the Row C pins, and bring each signal input in through Row A pins.

5.9 I/O CABLE AND FRONT PANEL CONNECTOR CONFIGURATION

The I/O connector (P3) on the VMIVME-1160A is a 64-pin DIN standard and was selected by VMIC because of its high quality. Although these connectors are generally used with flat-ribbon cables, a variety of cables and mating connectors are available for most user requirements. The user should refer to VMIC's Connector and I/O Cable Application Guide (VMIC's Document 825-000000-006) for additional information concerning the variety of possible cabling and connector types available.

Details concerning I/O connections are shown in Figure 5.9-1. Conductor No. 1 is shown at the bottom of the connector as it plugs into the header, because pin No. 1 of P3 is mounted as shown.

A compatible flat-ribbon cable connector for the VMIVME-1160A is Panduit No. 120-964-435E, and strain relief, Panduit No. 100-000-032. The Header Connector soldered to the PC board is Panduit No. 120-964-033A. Figure 5.9-2 shows the pin out of connector P3. Table 5.9-2 shows the P3 connector pin assignments for the inputs to the board. Figure 5.9-3 shows the pin out of connector P2. Table 5.9-1 shows the pertinent pin assignments for connector P2.

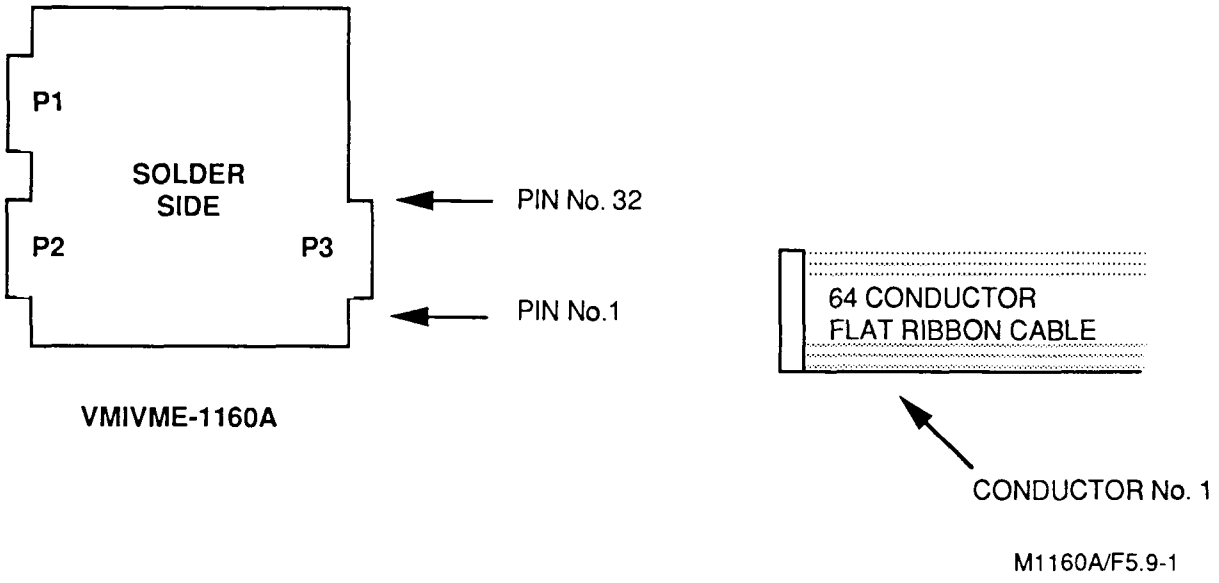


Figure 5.9-1. Cable Connector Configuration

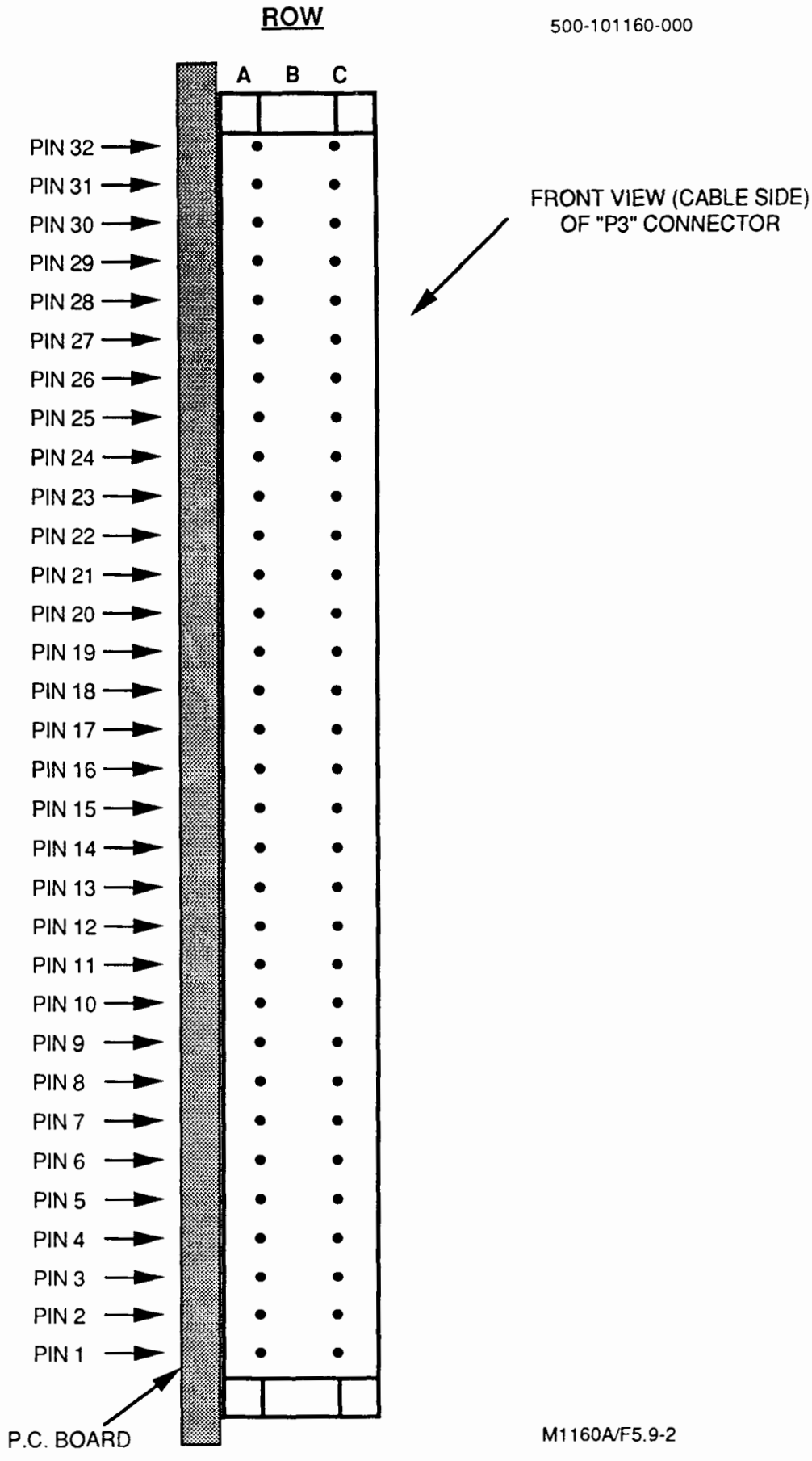


Figure 5.9-2. P3 Connector Pin Layout

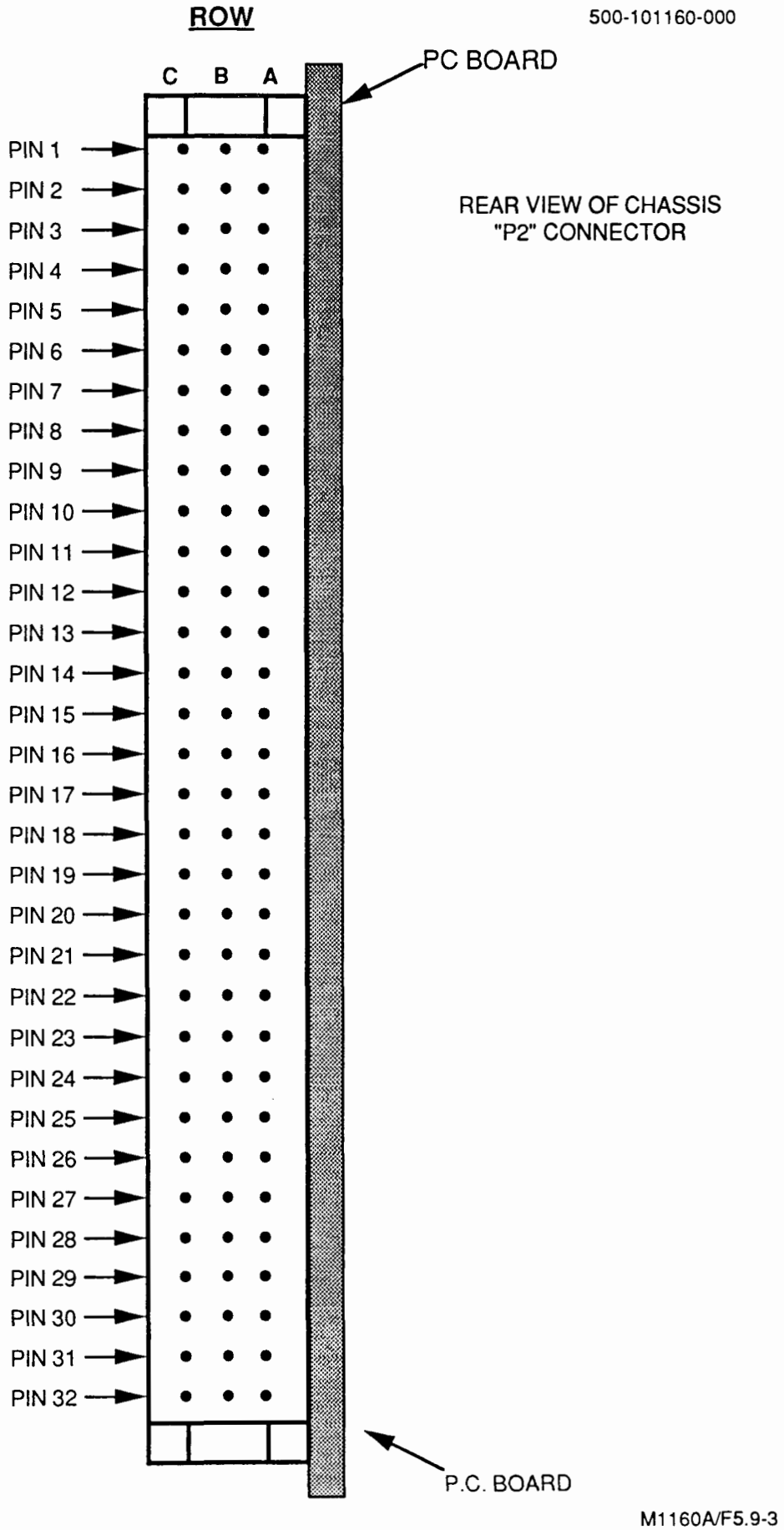


Figure 5.9-3. P2 Connector Pin Layout

Table 5.9-1. P2 Connector Pin Assignment

PIN NO.	ROW A[1]	ROW B[2]	ROW C
1		+5 VOLTS	
2		GND	
3			
4			
5			
6			
7			
8			
9			
10			
11			
12		GND	
13		+5 VOLTS	
14			
15			
16			
17			
18			
19			
20			
21			
22		GND	
23			
24			
25			
26			
27			
28			
29			
30			V POS
31		GND	V NEG
32		+5 VOLTS	

M1160A/T5.9-1

NOTES: 1. External Reference is supplied by the user.
2. Inputs to the Board - not required.

Table 5.9-2. P3 Pin-Channel Assignment

P3	
ROW A PIN	CHANNEL NO.
32	31
31	30
30	29
29	28
28	27
27	26
26	25
25	24
24	23
23	22
22	21
21	20
20	19
19	18
18	17
17	16

P3	
ROW A PIN	CHANNEL NO.
16	15
15	14
14	13
13	12
12	11
11	10
10	09
09	08
08	07
07	06
06	05
05	04
04	03
03	02
02	01
01	00

M1160A/T 5.9-2

SECTION 6

MAINTENANCE

6.1 MAINTENANCE

This section of the technical manual provides information relative to the care and maintenance of VMIC's products. Should the products malfunction, the user should verify the following:

a. Software
b. System configuration
c. Electrical connections
d. Jumper or configuration options
e. Boards fully inserted into their proper connector location
f. Connector pins are clean and free from contamination
g. No components of adjacent boards are disturbed when inserting or removing the board from the VMEbus card cage
h. Quality of cables and I/O connections

User level repairs are not recommended. Contact VMIC for a Return Material Authorization (RMA) Number. This RMA Number must be obtained prior to any return.

6.2 MAINTENANCE PRINTS

The appendix(ices) to this manual contain(s) drawings and diagrams for reference purposes.

APPENDIX A

ASSEMBLY DRAWING, PARTS LIST, AND SCHEMATIC

NOTES:

* ASTERISK DENOTES OPTIONAL PART
  REFER TO PARTS LIST FOR APPLICATION AND VALUE.

REVISIONS

REV.	DESCRIPTION	BY	DATE	APPR.
A	RELEASE PER ECO 92-0027	E.M.GREEN	2/14/92	A.JORDAN
B	CHANGED JUMPER FIELD BIM FIX PER ECO 92-0028	E.M.GREEN	2/14/92	A.JORDAN
C	CHANGED PER ECO 94-0330	S.E.O'NEAL	6/24/94	A.JORDAN
D	CHANGE PER ECO 95-0179	E.M. GREEN	4/7/95	[illegible]

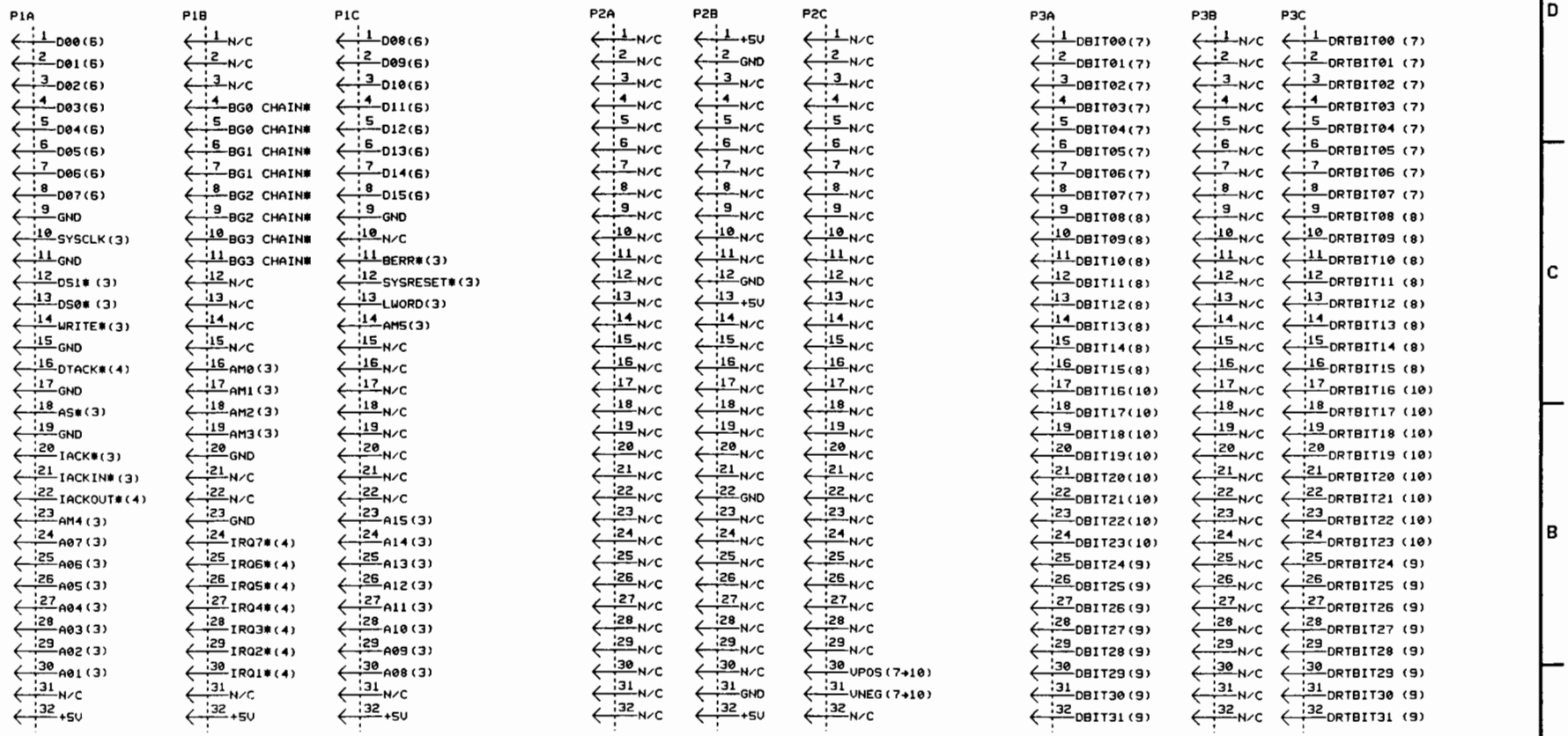
SIGNATURES		DATE
DRAWN	E.M.GREEN	5/10/91
PROJ. ENG.	A. JORDAN	7/30/91
ENG. MGR.	G. MEARES	7/30/91
PROD.		
Q.A.		

VMIC® 12090 SO. MEM. PKWY.
HUNTSVILLE, AL. 35803-3308
VME MICROSYSTEMS INTERNATIONAL CORPORATION

VMIVME-1160A

SIZE		DWG NO.	REV.
B	0BPH5	141-101160-000	D

SCALE | SHEET 1

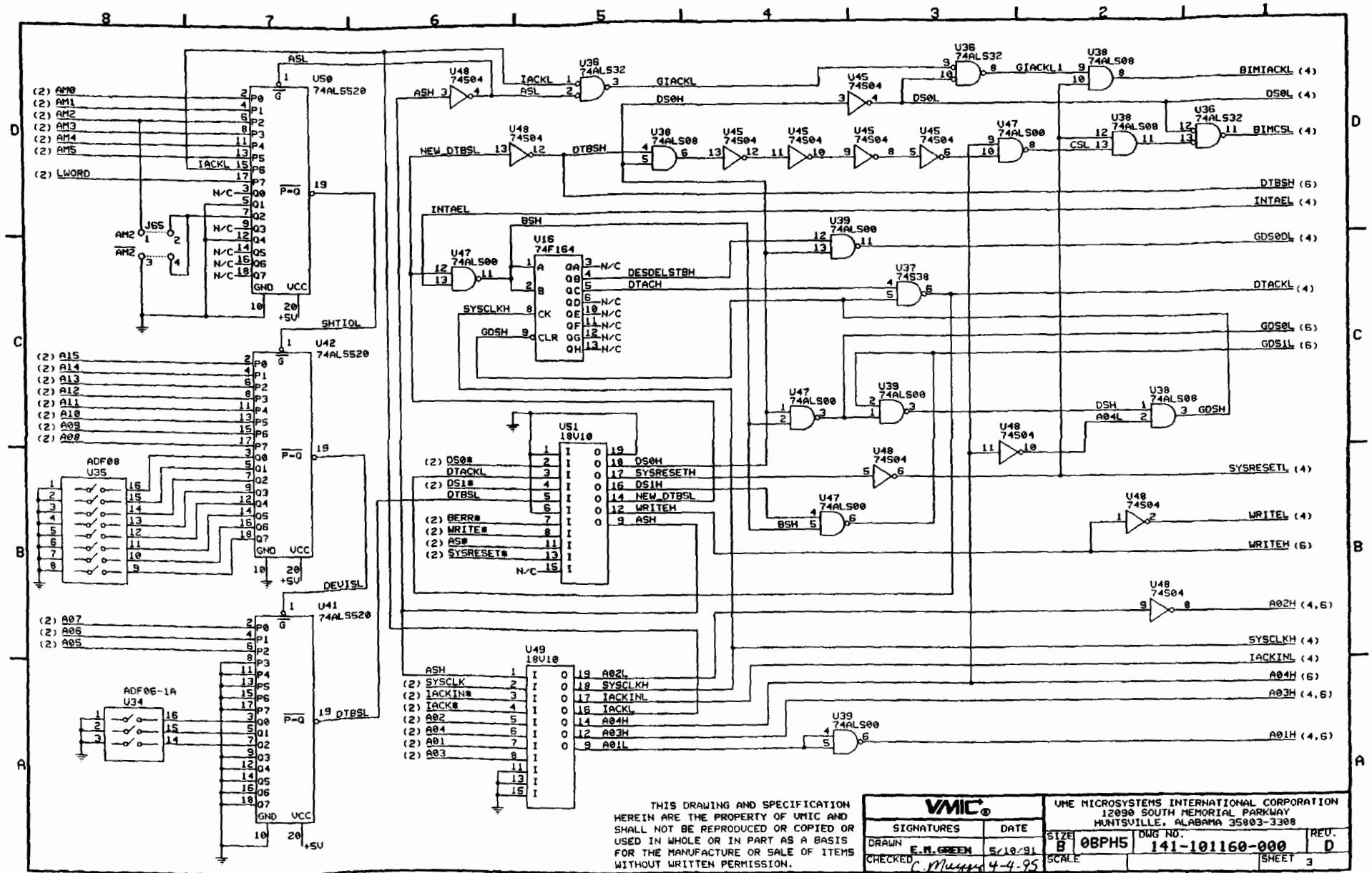


VMIC®	SIGNATURES	DATE
DRAWN	E.M.GREEN	5/10/91
CHECKED	C. Musser	4-4-95

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

SIZE	DWG NO.	REV.
B	0BPH5 141-101160-000	D

SCALE | SHEET 2



SIGNATURES	DATE
DRAWN E.M.GREEN	5/10/91
CHECKED C. Murray	4-4-95

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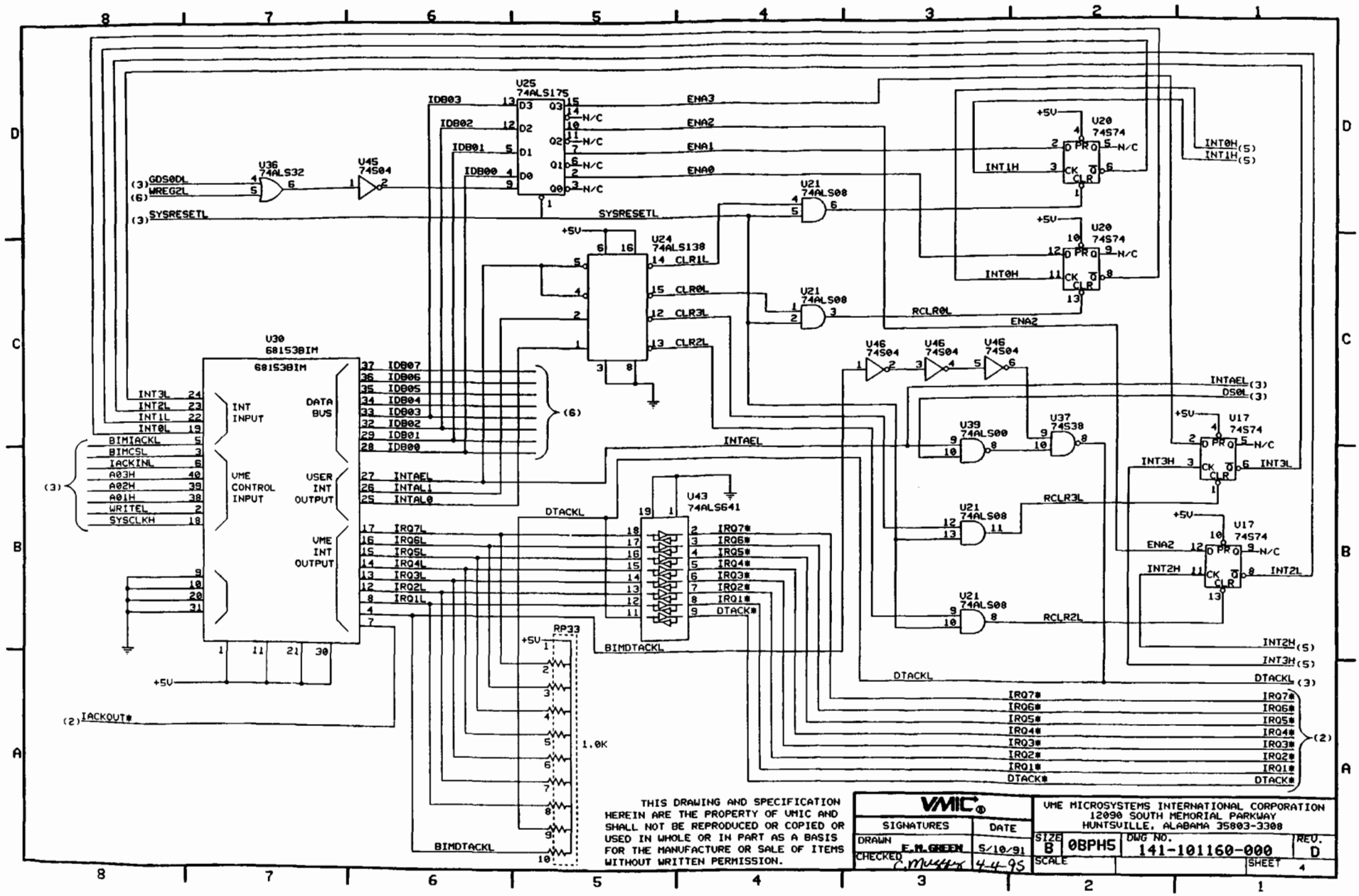
SIZE	DWG NO.	REV.
B	0BPH5 141-101160-000	D
SCALE		SHEET 3



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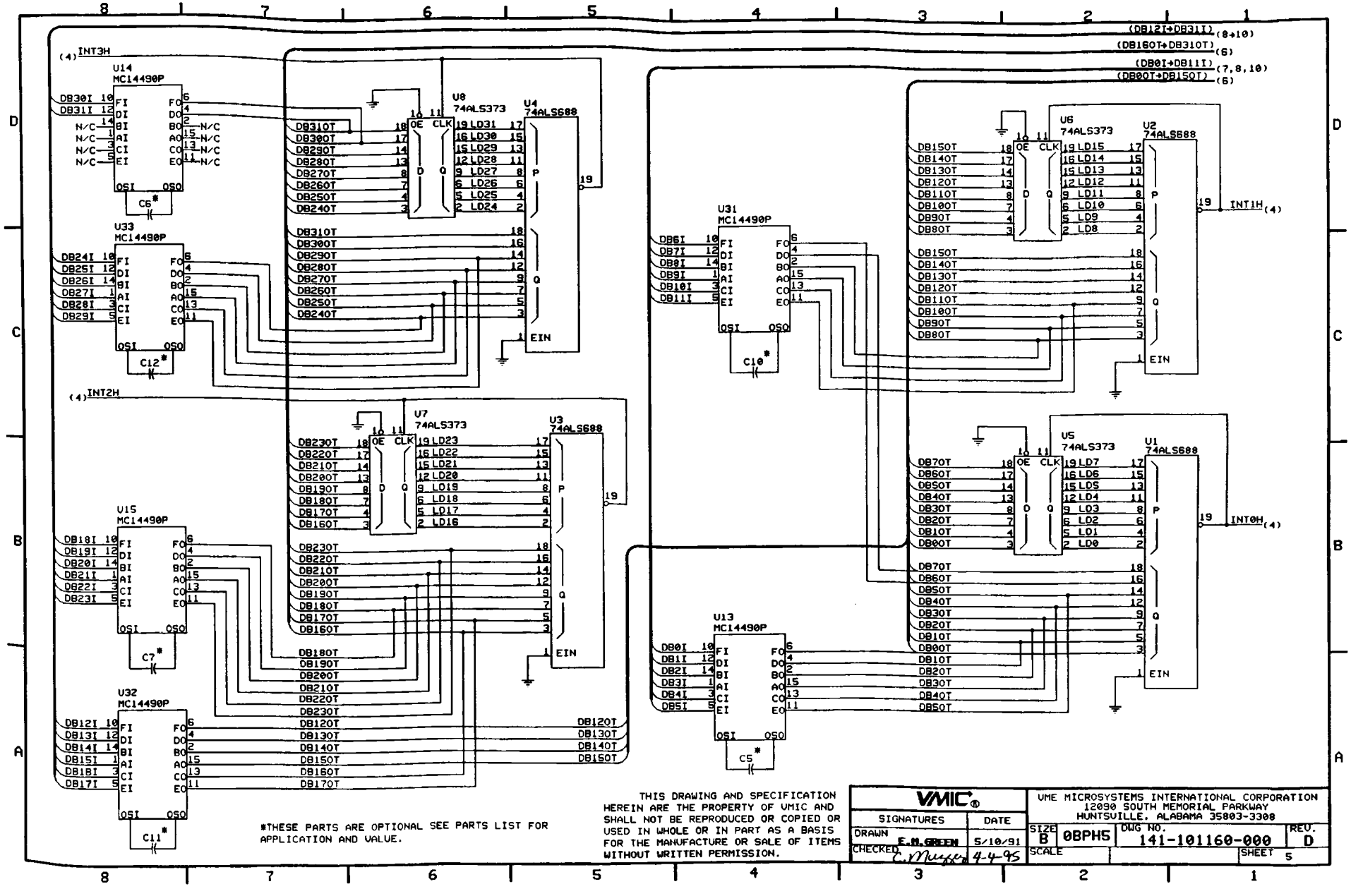
SIZE	DWG NO.	REV.
B	0BPH5 141-101160-000	D
SCALE		SHEET 4


(4)INT3H
(4)INT2H
U14 MC14490P
U33 MC14490P
U15 MC14490P
U32 MC14490P
U31 MC14490P
U13 MC14490P
U8 74ALS373
U7 74ALS373
U6 74ALS373
U5 74ALS373
U4 74ALS688
U3 74ALS688
U2 74ALS688
U1 74ALS688
C6*
C12*
C7*
C11*
C10*
C5*
(DB12I→DB31I) (8+10)
(DB16OT→DB31OT) (6)
(DB0I→DB11I) (7,8,10)
(DB0OT→DB15OT) (6)
INT1H (4)
INT0H (4)
*THESE PARTS ARE OPTIONAL SEE PARTS LIST FOR APPLICATION AND VALUE.
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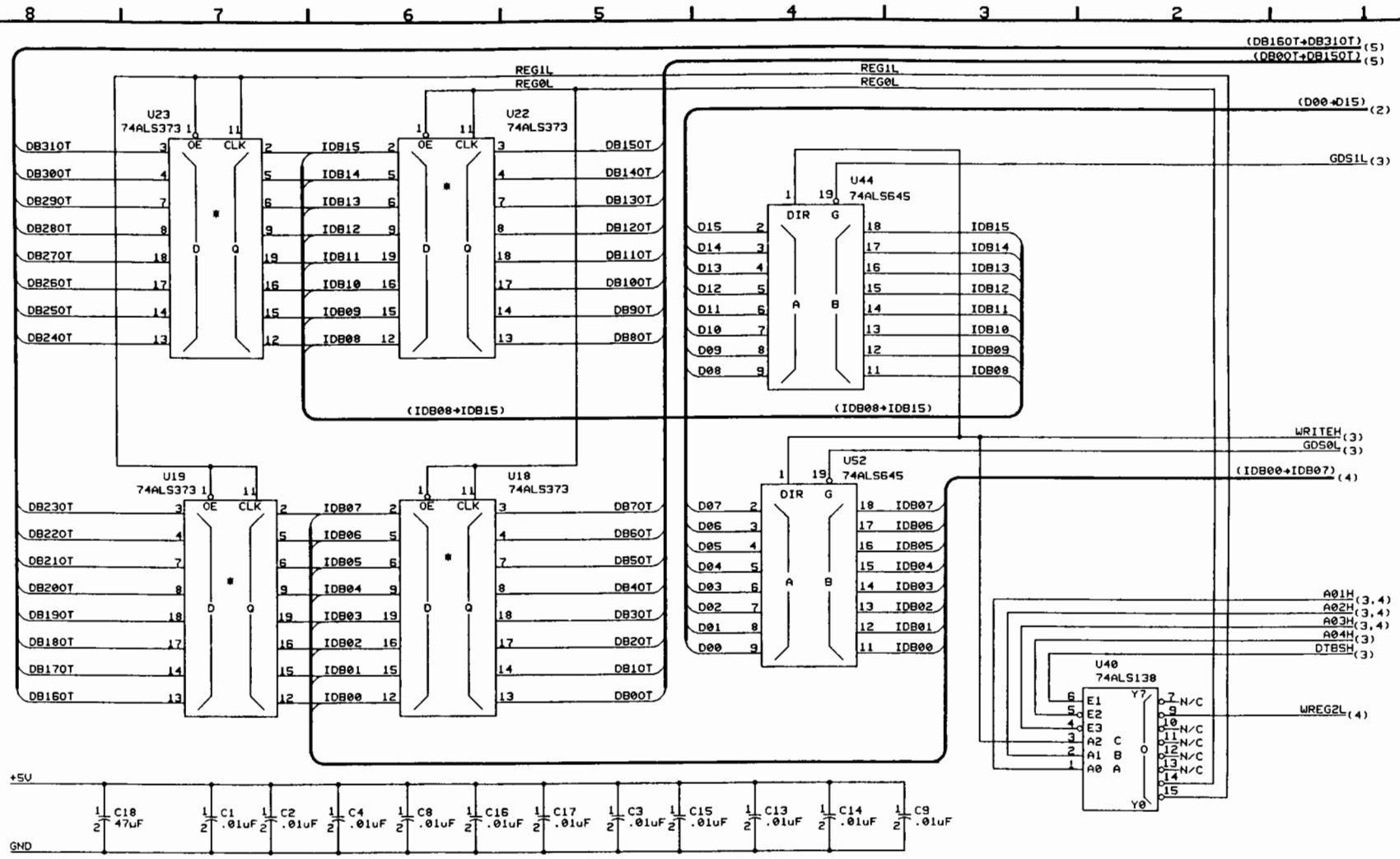
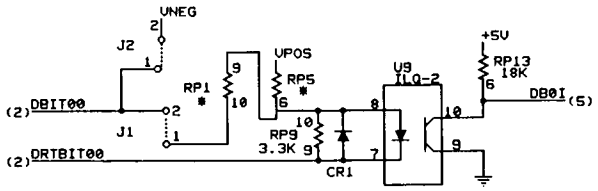
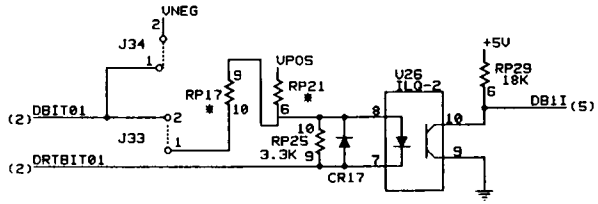
VMIC®
SIGNATURES
DATE
DRAWN E.M.GREEN 5/10/91
CHECKED C. Musser 4-4-95
VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308
SIZE B
0BPH5
DWG NO. 141-101160-000
REV. D
SCALE
SHEET 5

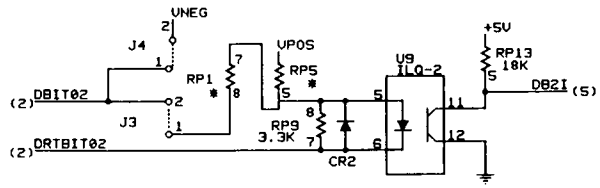


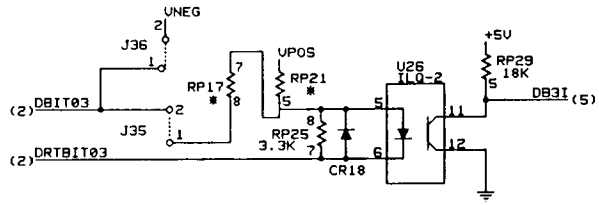
*THESE PARTS ARE OPTIONAL SEE PARTS LIST FOR APPLICATION AND VALUE.

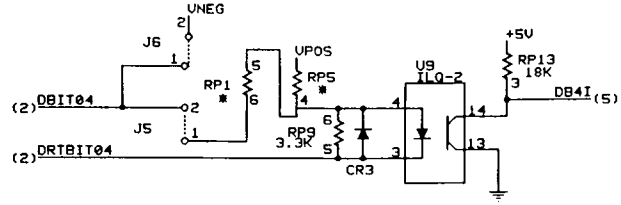
VMIC®		VME MICROSYSTEMS INTERNATIONAL CORPORATION 12090 SOUTH MEMORIAL PARKWAY HUNTSVILLE, ALABAMA 35803-3308		
SIGNATURES	DATE	SIZE	DWG NO.	REV.
DRAWN E.M.GREEN	5/10/91	B 0BPH5	141-101160-000	D
CHECKED C. Mussa	4-4-95	SCALE	SHEET	6

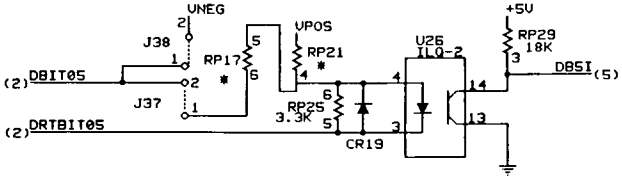


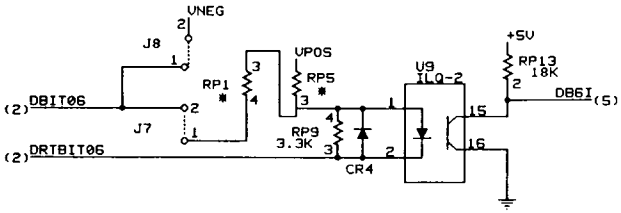


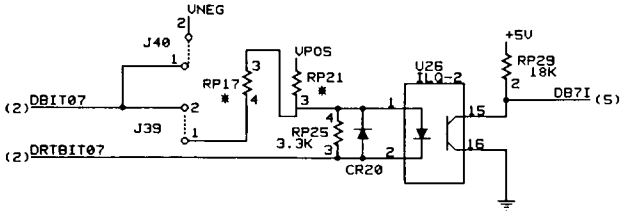






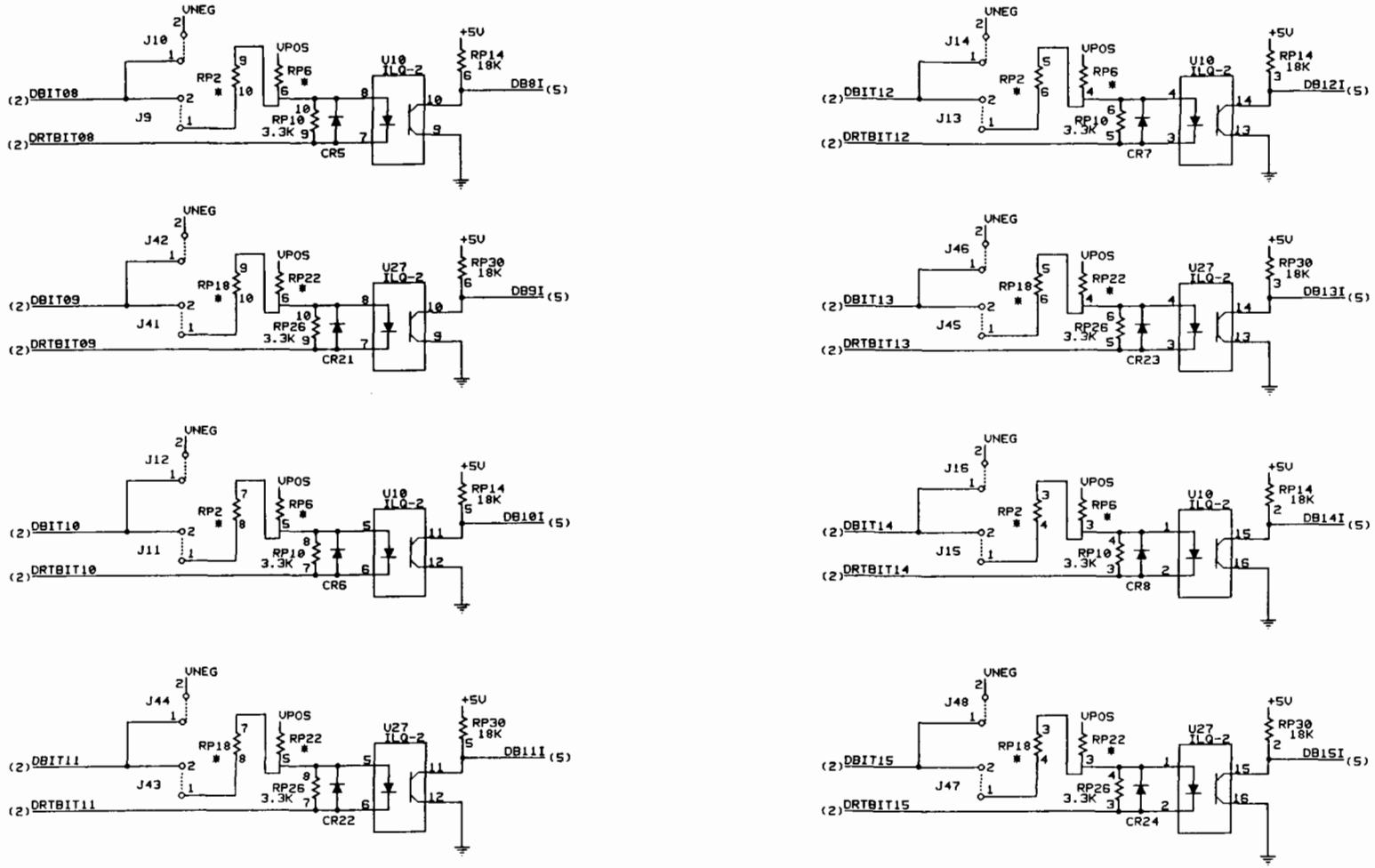






*THESE PARTS ARE OPTIONAL SEE PARTS LIST FOR APPLICATION AND VALUE.

VMIC®		VME MICROSYSTEMS INTERNATIONAL CORPORATION 12090 SOUTH MEMORIAL PARKWAY HUNTSVILLE, ALABAMA 35803-3308		
SIGNATURES	DATE	SIZE B	0BPH5	DWG NO. 141-101160-000	REV. D
DRAWN E.M.GREEN	5/10/91	SCALE		SHEET 7
CHECKED C. Mussey	4-4-95			



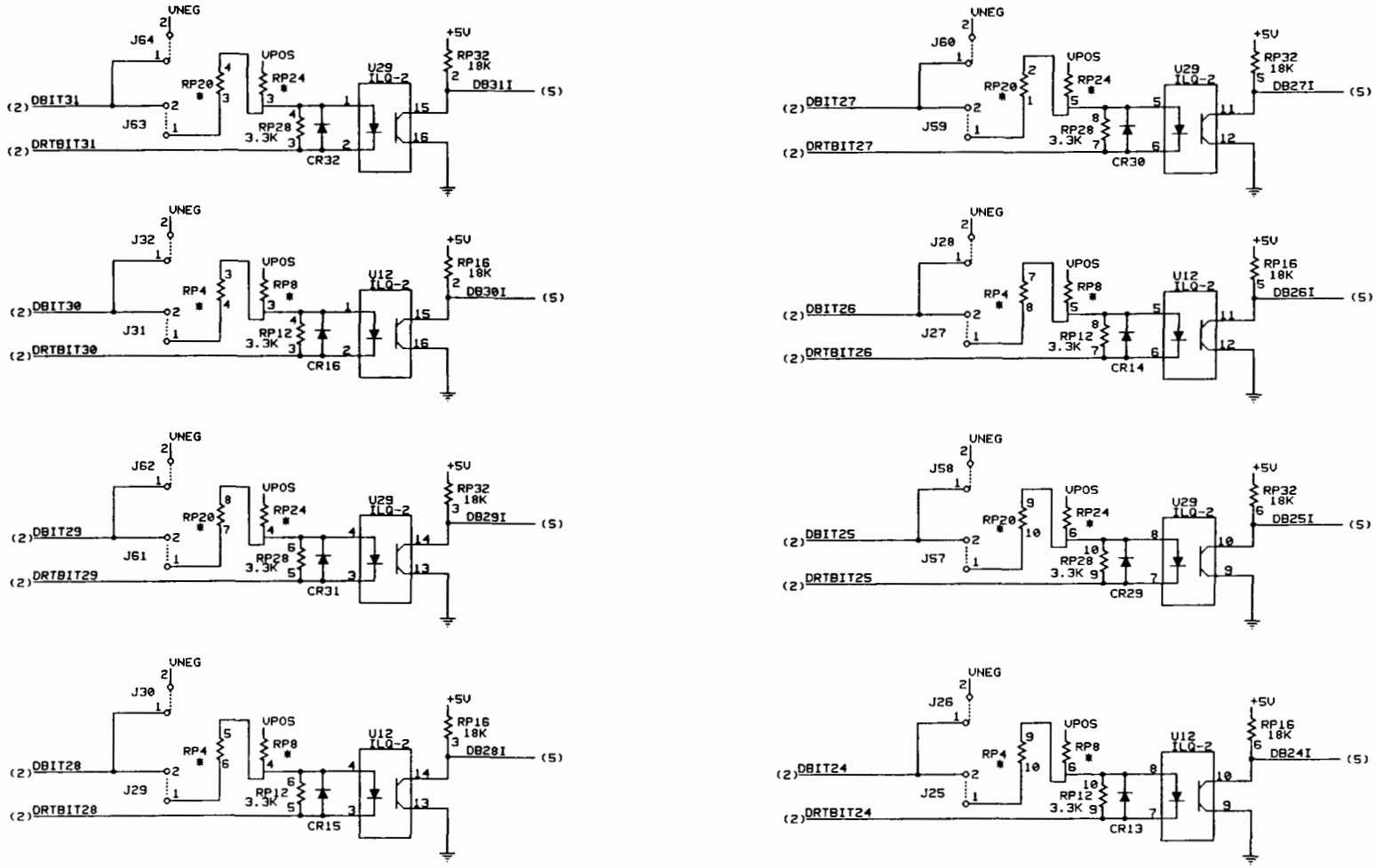
*THESE PARTS ARE OPTIONAL SEE PARTS LIST FOR APPLICATION AND VALUE.

VMIC®	SIGNATURES	DATE
DRAWN	E.M.GREEN	5/10/91
CHECKED	C. Murphy	4-4-95

VME MICROSYSTEMS INTERNATIONAL CORPORATION
12090 SOUTH MEMORIAL PARKWAY
HUNTSVILLE, ALABAMA 35803-3308

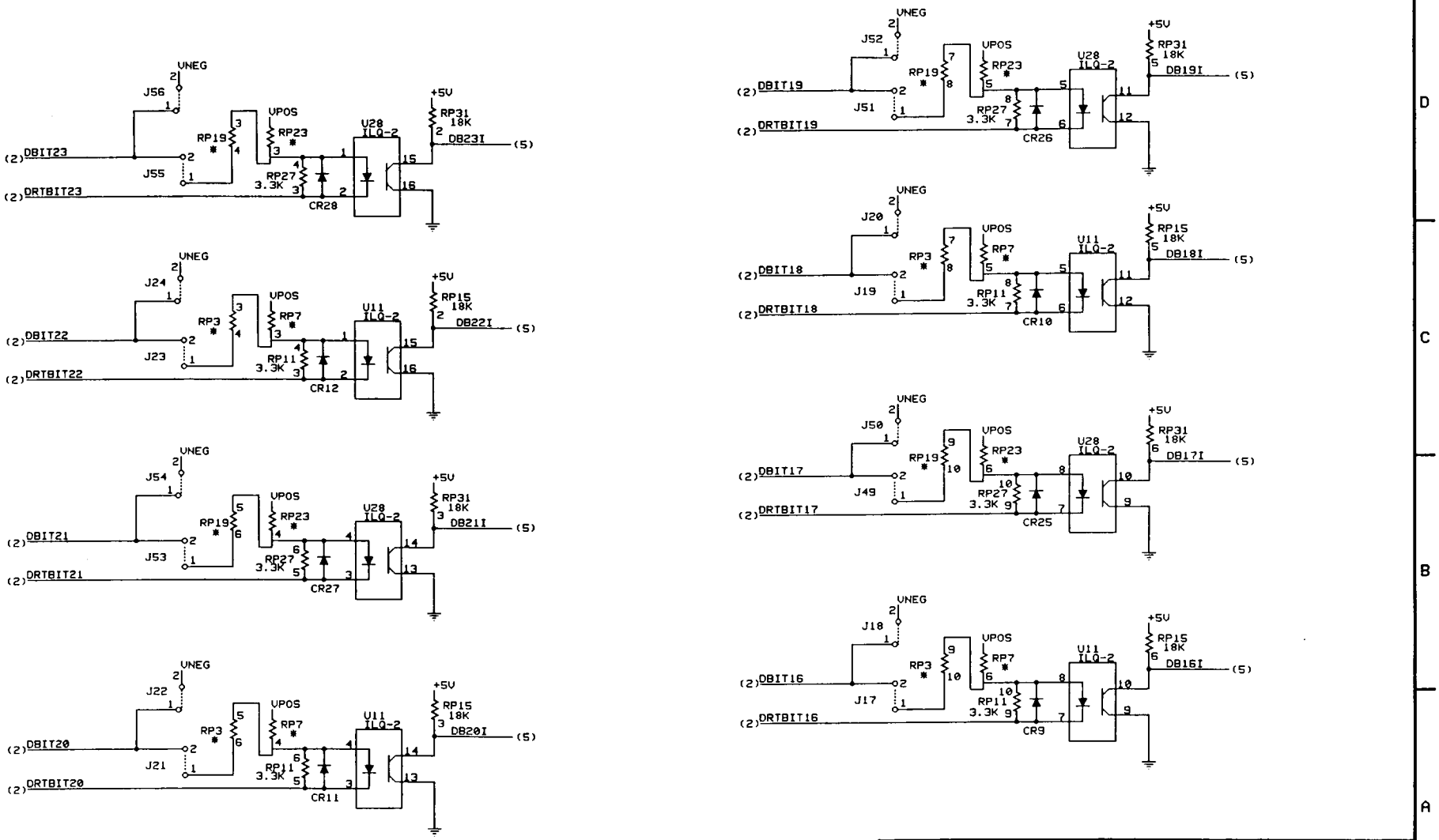
SIZE	DWG NO.	REV.
B	141-101160-000	D

SCALE | SHEET 8



*THESE PARTS ARE OPTIONAL SEE PARTS LIST FOR APPLICATION AND VALUE.

VMIC		VME MICROSYSTEMS INTERNATIONAL CORPORATION 12090 SOUTH MEMORIAL PARKWAY HUNTSVILLE, ALABAMA 35803-3308	
SIGNATURES	DATE	SIZE	DWG NO.	REV.
DRAWN E.M.GREEN	5/10/91	B	0BPH5	141-101160-000	D
CHECKED P. Musser	4-4-95	SCALE		SHEET 9



*THESE PARTS ARE OPTIONAL SEE PARTS LIST FOR APPLICATION AND VALUE.

VMIC®		VME MICROSYSTEMS INTERNATIONAL CORPORATION 12090 SOUTH MEMORIAL PARKWAY HUNTSVILLE, ALABAMA 35803-3308		
SIGNATURES	DATE	SIZE B	0BPH5	DWG NO. 141-101160-000	REV. D
DRAWN E.M.GREEN	5/10/91	SCALE		SHEET 10 OF 10
CHECKED C. Murphy	4-4-95			

SIZE	DWG NO	SH	REV
A	132-101160-000	1	K

NOTES:

1. FOR SCHEMATIC DIAGRAM SEE 141-101160-000.
2. FOR TEST PROCEDURE SEE 510-001160-000.
3. FOR DOCUMENT SET SEE 110-101160-000.

REVISION STATUS OF 332
A
B
C
C
C
D
D
D
D
D

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	RELEASE PER ECO 92-0027	2/14/92	A.J.
B	MX BIM COPPER UPDATE PER ECO 92-0028	2/14/92	A.J.
C	RP 5-8, 21-24 OPTION CORRECTION PER ECO 92-0158	6/10/92	T.L.T.
D	DOCUMENT CHANGE TO NOTE 2 PER ECO 93-0575	8/3/93	A.J.
E	ADD EXTRUDED FP PER ECO 93-0830	1/13/94	D.F.
F	SUPPORT ADDRESS PIPELINE ECO 94-0330	7/6/94	A.J.
G	CORRECT DESCRIPTION U51,49 ECO 94-0367	7/6/94	A.J.
H	CHANGE PER ECO 94-0451	7/6/94	A.J.
J	CHANGE PER ECO 94-0727	3/21/95	D.F.
K	CHANGE TERM. TO CORRECT QTY. PER ECO 97-0087	2/21/97	

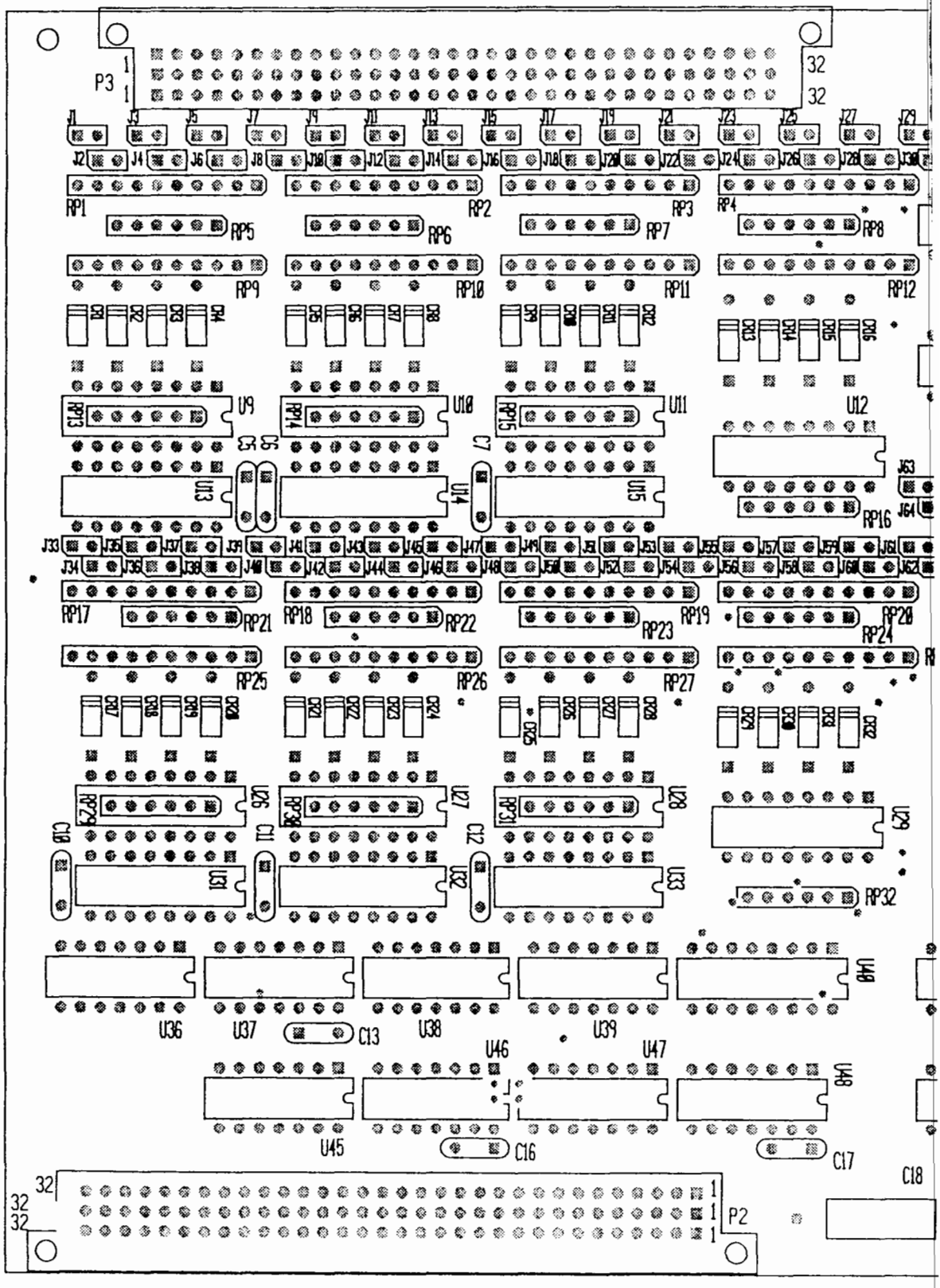
UNLESS OTHERWISE SPECIFIED	SIGNATURES	DATE
DIMENSIONS ARE IN INCHES TOLERANCES ON: 2 PL DECIMALS ± 3 PL DECIMALS ± ANGLES ± FRACTIONS ±	DRAWN: E.M. GREEN	7/24/91
	PROJ.ENG.: A. JORDAN	10/3/91
	ENG.MGR.: G. MEARES	10/3/91
	PROD.: D. FOWLER	2/19/92
	Q.A.: S. KEAGLE	2/21/92
	MAGNETIC MEDIA FILENAME FOR PACKAGE: A101160K.EXE	

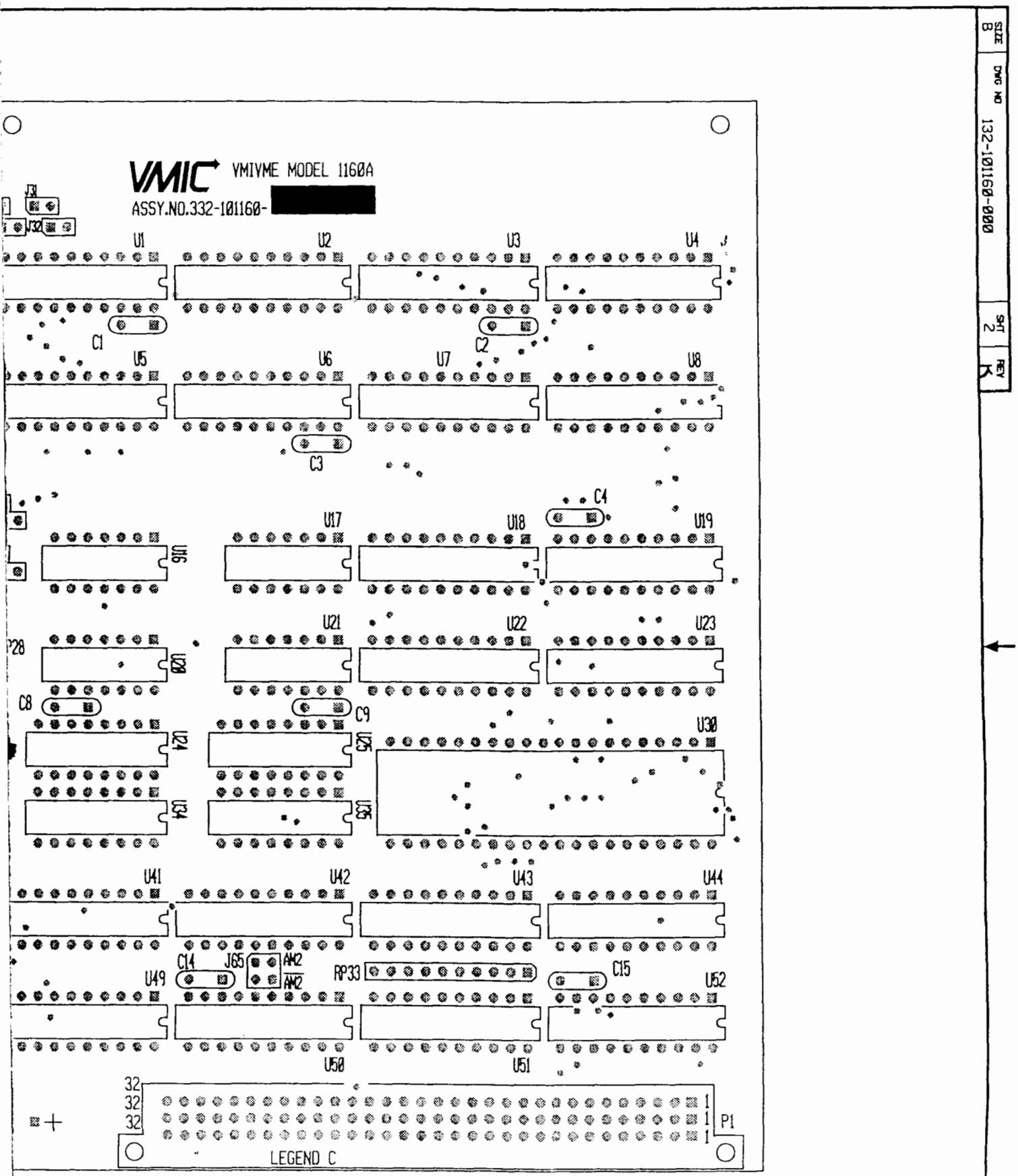
VMIC® HUNTSVILLE, ALABAMA 35803-3308
VME MICROSYSTEMS INTERNATIONAL CORPORATION

ASSEMBLY DRAWING
VMIVME-1160A

SIZE	FSCM NO.	DWG NO.
A	OBPH5	132-101160-000

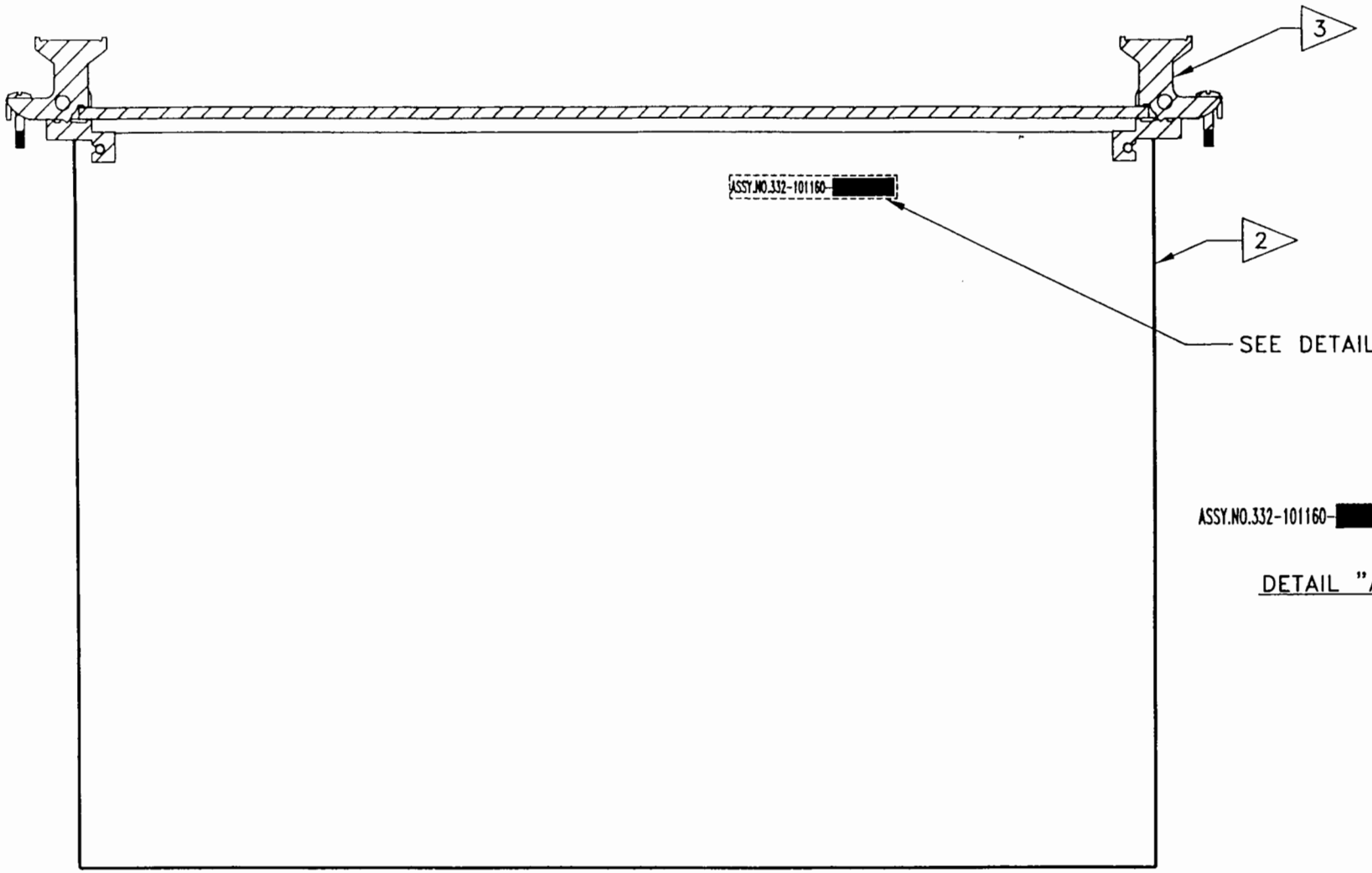
SCALE		SHEET
NONE		1 OF 8


P3
P2
RP1
RP2
RP3
RP4
RP5
RP6
RP7
RP8
RP9
RP10
RP11
RP12
RP16
RP17
RP18
RP19
RP20
RP21
RP22
RP23
RP24
RP25
RP26
RP27
RP32
U9
U10
U11
U12
U13
U14
U15
U26
U27
U28
U29
U33
U36
U37
U38
U39
U40
U45
U46
U47
U48
C13
C16
C17
C18



SIZE B | DWG NO 132-101160-000 | SHT 2 | REV K

SIZE	DWG NO	SH	REV
A	132-101160-000	2A	K



DETAIL "A"

VMIC® HUNTSVILLE, AL 35803-3308 VME MICROSYSTEMS INTERNATIONAL CORP.	SIZE: A	FSCM NO.: 0BPH5	DWG NO.: 132-101160-000
DRAWN: E. JORY			
CHECKED: C. Mussey 2-18-97	SCALE: .75=1		SHEET: 2A

REWORK LEGEND:

A. REWORK INSTRUCTIONS SHALL BE ACCOMPLISHED ON THE COPPER REVISION(S) INDICATED AND WILL BECOME A PART OF THE ASSEMBLED BOARD.

B. REWORK INSTRUCTION SYMBOLS:

1. PIN ONE DOT ■
2. DRILL HOLE ●
3. DISCONNECT TRACE ×
4. TRACE ON INTERNAL LAYER ------
5. TRACE ON EXTERNAL LAYER ———

INSTRUCTIONS:

NOTES:

1> A. ALL ASSEMBLED BOARDS SHALL BE IDENTIFIED WITH THE ASSEMBLED BOARD PART NUMBER. THIS NUMBER INCLUDES THE CURRENT REVISION LETTER LISTED IN THE "REVISION STATUS OF 332" BLOCK (SEE SHEET 1). THE RESULTING PART SHALL BECOME A 332-101160-ABC (REV).

B. THE PART NUMBER FIELDS "ABC" WILL COINCIDE WITH THE OPTIONAL PARTS INSTALLED IN THE COMPLETED ASSEMBLY. IF NO OPTIONAL PARTS ARE USED IN A FIELD, THAT FIELD WILL DEFAULT TO "0".

C. IF NECESSARY, REMOVE AND REPLACE 332 REVISION LETTER WITH CURRENT REVISION LETTER USING EITHER A REMOVABLE NON-SMEARING BLACK INK OR A LABEL.

2> SOLDER COMPOSITION COMPLIES WITH MIL-STD-2000.

3> SEE DRAWING 150-000022-000 FOR THE ASSEMBLY AND INSTALLATION OF THE FRONT PANEL.

4> SEE REWORK INSTRUCTIONS, EFFECTIVITY: 333-101160-000 REV N/R AND REV B, BEFORE INSTALLING U13, U14, U15, U31, U32, AND U33.

5> SEE REWORK INSTRUCTIONS, EFFECTIVITY: 333-101160-000 REV A AND EARLIER, BEFORE INSTALLING SOCKETS AT LOCATIONS U49 AND U51.

EFFECTIVITY: DCO III-1160A (333-101160-000 REV N/R AND B, NOT REQ'D FOR REV A)

INSTRUCTIONS: REWORK U13, U14, U15, U31, U32, U33

STEP 1

PULL SIX-16 PIN ELEVATED SOCKETS (PART # 321-001316-081).

STEP 2

CUT PART, BUT NOT ALL, OF PINS 16 AND 8 OF THE ELEVATED SOCKET SO THAT PINS 16 AND 8 WILL NOT COME INTO CONTACT WITH THE PCB BOARD WHEN IT IS INSTALLED.

STEP 3

USING 30 GUAGE WIRE, CONNECT PIN 8 OF PCB BOARD TO PIN 16 OF SOCKET. (FOR U13, U14, U15, U31, U32, U33)

STEP 4

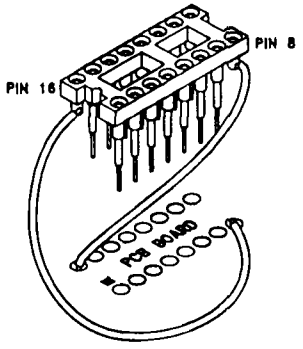
USING 30 GUAGE WIRE, CONNECT PIN 16 OF PCB BOARD TO PIN 8 OF SOCKET. (FOR U13, U14, U15, U31, U32, U33)

STEP 5

INSTALL SOCKETS INTO BOARD.

STEP 6

INSTALL PART INTO SOCKET.



STEPS 1 THRU 6

EFFECTIVITY: ECO 92-0028 (333-101160-000 REV N/R)

INSTRUCTIONS: REWORK

STEP 1

DISCONNECT U38 PIN 11 FROM U30 PIN 3 BY CUTTING TRACE ON LAYER 1 (COMPONENT SIDE) AS SHOWN.
THE TRACE IS THE FIRST TRACE TO THE RIGHT OF U30 PIN 1.

STEP 2 (SOLDER SIDE)

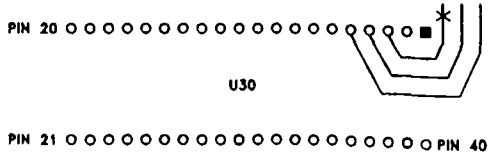
CONNECT U38 PIN 11 TO U36 PIN 13.

STEP 3 (SOLDER SIDE)

CONNECT U36 PIN 10 TO U36 PIN 12.

STEP 4 (SOLDER SIDE)

CONNECT U36 PIN 11 TO U30 PIN 3.



STEP 1

VMIC® HUNTSVILLE, AL 35803-3308 VME MICROSYSTEMS INTERNATIONAL CORP.	SIZE A	FSCM NO. 0BPH5	DWG NO. 132-101160-000
DRAWN: E. JORY			
CHECKED: C. Musser 2-18-97	SCALE		SHEET 3A

EFFECTIVITY: ECO 94-0330 (332-101160-000 REV C & EARLIER)

INSTRUCTIONS: REWORK

STEP 1

INSPECT U49; IF U49 IS A 74-244 TYPE, THEN REMOVE.

STEP 2

INSPECT U51; IF U51 IS A 74-240 TYPE, THEN REMOVE.

EFFECTIVITY: ECO 94-0330 (333-101160-000 REV A & EARLIER)

INSTRUCTIONS: REWORK

STEP 1 (SOLDER SIDE)

CUT P1A PIN 29 FROM U51 PIN 15.

STEP 2 (SOLDER SIDE)

CUT P1A PIN 30 FROM U51 PIN 17.

STEP 3 (COMPONENT SIDE)

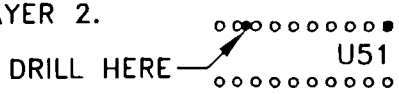
CUT U51 PIN 7 FROM U48 PIN 5.

STEP 4 (COMPONENT SIDE)

CUT U51 PIN 5 FROM U48 PIN 9.

STEP 5 (COMPONENT SIDE)

DRILL AT U51 BETWEEN U51 PIN 8 AND U51 PIN 9 TO DISCONNECT U51 PIN 3 FROM U39 PIN 4. THE TRACE IS CONNECTED ON LAYER 2.



STEP 6 (COMPONENT SIDE)

CUT P1A PIN 21 FROM U49 PIN 17.

STEP 7 (SOLDER SIDE)

CUT U49 PIN 3 FROM U30 PIN 6.

STEP 8 (COMPONENT SIDE)

CUT U41 PIN 19 FROM U48 PIN 13.

STEP 9

TAKE A 20 PIN SOCKET, P/N 321-001320-000, AND INSERT AT U51.

STEP 10

TAKE A 20 PIN SOCKET, P/N 321-001320-000, REMOVE PINS 1 AND 19 FROM SOCKET, SO THAT WHEN INSTALLED THE SOCKET AT PINS 1 AND 19 WILL NOT COME INTO CONTACT WITH THE COPPER, AND INSTALL AT LOCATION U49.

STEP 11 (SOLDER SIDE)

CONNECT U41 PIN 19 TO U51 PIN 5.

STEP 12 (SOLDER SIDE)

CONNECT U51 PIN 14 TO U48 PIN 13.

STEP 13 (SOLDER SIDE)

CONNECT U51 PIN 3 TO U37 PIN 6.

STEP 14 (SOLDER SIDE)

CONNECT U51 PIN 17 TO U48 PIN 5.

STEP 15 (SOLDER SIDE)

CONNECT U51 PIN 7 TO P1C PIN 11.

STEP 16 (SOLDER SIDE)

CONNECT U49 PIN 3 TO P1A PIN 21.

STEP 17 (SOLDER SIDE)

CONNECT U49 PIN 17 TO U30 PIN 6.

EFFECTIVITY: ECO 94-0330 (333-101160-000 REV A & EARLIER)

INSTRUCTIONS: REWORK (CONTINUED)

STEP 18 (SOLDER SIDE)
CONNECT U49 PIN 5 TO P1A PIN 29.

STEP 19 (SOLDER SIDE)
CONNECT U49 PIN 7 TO P1A PIN 30.

STEP 20 (SOLDER SIDE)
CONNECT U49 PIN 9 TO U39 PIN 4.

EFFECTIVITY: ECO 94-0330 (332-101160-000 REV C & EARLIER)

INSTRUCTIONS: REWORK

STEP 1
REMOVE RP33, A 4.7K OHM SIP, P/N 347-001002-472, AND REPLACE WITH A 1K OHM SIP, P/N 347-001002-102.

STEP 2
INSTALL PAL 1160A51A, P/N 303-001137-000 INTO LOCATION U51.

STEP 3
INSTALL PAL 1160A49A, P/N 303-001136-000, INTO SOCKET AT U49.

EFFECTIVITY: ECO 94-0330 (333-101160-000 REV A & EARLIER)

INSTRUCTIONS: REWORK

STEP 1
CONNECT A MOD WIRE TO PIN 1 OF PAL U49. ROUTE MOD WIRE THROUGH EMPTY SOCKET HOLE AND PC BOARD AND CONNECT TO U48 PIN 3 ON THE SOLDER SIDE.

STEP 2
CONNECT A MOD WIRE TO PIN 19 OF PAL U49. ROUTE MOD WIRE THROUGH EMPTY SOCKET HOLE AND PC BOARD AND CONNECT TO U48 PIN 9 ON THE SOLDER SIDE.

END OF REWORK INSTRUCTIONS

PARTS LIST

VME Microsystems In'tl Corporation

CODE OBPH5 | DRAWING NUMBER 132-101160-000 REV: K | CHECKER/DATE C. Muggs 2-18-97

ITEM	ABC	REF. DES.	QTY.	PART NO:	DESCRIPTION	MANUFACTURER
1			1	333-101160-000	BOARD: PC, RAW, 6 LAYERS (VMIVME-1160A)	
2			1	317-000119-000	F/P ASSY: EXTRUDED EJECTOR, ONE LOWER POSITION 64 PIN CUTOUT (SEE NOTE 3)	
3				DELETED		
4			1	324-101160-100	LABEL: ID, 1160A, FRONT PANEL (SEE NOTE 3)	
5				DELETED		
6				DELETED		
7				DELETED		
8				DELETED		
9		P1-3	6	328-250000-010	SCREW: M2.5, PAN HEAD, PHILLIPS, CROSS RECESSED SS, 10MM LENGTH	OPEN SOURCE
10		P1-3	6	328-250001-025	NUT: METRIC, 2.5MM, HEX, SS	OPEN SOURCE
11		REF.P1-3	A/R	316-000002-000	LOCTITE: SMALL SCREW THREADLOCKER 222	
12				DELETED		
13		C1-4,8,9,13-17	11	315-205001-103	CAP: .01uF, .200 LEAD SPACE, 20%, 50V, Z5U CERAMIC MONOLYTHIC	C317C103M5U5CA (KEMET)
14		C18	1	315-902000-476	CAP: 47uF, AXIAL, 20%, 35V, ALUMINUM ELECTROLYTIC	ECEB1VU470 (PANASONIC)
15		P3	1	321-000013-105	CONNECTOR: FLAT CABLE, 64 PIN, RIGHT ANGLE MALE W/ EJECTOR LATCHES, TYPE C, SERIES 120	120-964-033A (PANDUIT)
16			32	321-000015-001	JUMPER: PC BOARD, 2 POSITION, FEMALE GOLD PLATED CONTACT, BLACK	MSB-2360-G-C-STP (McKENZIE)

ITEM	ABC	REF. DES.	QTY.	PART NO:	DESCRIPTION	MANUFACTURER
17		J65	1	321-000017-021	TERMINAL: PC BOARD, DUAL ROW, .025 THICK, GOLD PLATED, TWO POST	PEG04DS-(T,F)BR (CRANE)
18		P1	1	321-000054-001	CONNECTOR: DIN, 96 PIN, WAVE SOLDER, ANGLED TYPE C, MALE	100-096-033 (PANDUIT)
19		P2	1	321-000054-002	CONNECTOR: DIN, 96 PIN, WAVE SOLDER, ANGLED TYPE C, MALE	100-096-033 (PANDUIT)
20		U12,29	2	321-001316-001	SOCKET: DIP, 16 PIN, .300 ROW, STAMPED & FORMED	2-641600-(3,1,5) (AMP)
21		U9-11,26-28	6	321-001316-081	SOCKET: DIP, 16 PIN, .300 ROW, ELEVATED	ICA-316-E(TT,GT) (SAMTEC)
22		U30	1	321-001640-001	SOCKET: DIP, 40 PIN, .600 ROW, STAMPED & FORMED	2-641606-(3,1,5) (AMP)
23		U39,47	2	331-300400-100	IC: DIGITAL, QUAD 2-INPUT NAND GATE, PLASTIC DIP	SN74ALS00AN (TI)
24		U45,46,48	3	331-300404-100	IC: DIGITAL, HEX INVERTER, PLASTIC DIP	SN74ALS04BN (TI)
25		U21,38	2	331-300408-100	IC: DIGITAL, QUAD 2-INPUT AND GATE, PLASTIC DIP	SN74ALS08N (TI)
26		U36	1	331-300432-100	IC: DIGITAL, QUAD 2-INPUT OR GATE, PLASTIC DIP	SN74ALS32N (TI)
27		U37	1	331-300438-700	IC: DIGITAL, QUAD 2-INPUT NAND BUFFER, PLASTIC DIP	SN74S38N (TI)
28		U17,20	2	331-300474-700	IC: DIGITAL, DUAL D FLIP FLOP, PLASTIC DIP	SN74S74N (TI)
29		U24,40	2	331-304138-100	IC: DIGITAL, 1 OF 8 DECODER/DEMULTIPLEXER, PLASTIC DIP	SN74ALS138N (TI)
30		U16	1	331-304164-400	IC: DIGITAL, 8-BIT GATED SERIAL-IN, PARALLEL-OUT, FAST, PLASTIC DIP	MC74F164P (MOTOROLA)
31		U25	1	331-304175-100	IC: DIGITAL, QUAD D FLIP FLOP W/CLEAR, PLASTIC DIP	SN74ALS175N (TI)
32		U51	1	303-001137-000	PROGRAMMED PAL: FILE: 1160A51A.PLD A PROGRAMMED 18V10 (331-300132-200)	

ITEM	ABC	REF. DES.	QTY.	PART NO:	DESCRIPTION	MANUFACTURER
33		U49	1	303-001136-000	PROGRAMMED PAL: FILE: 1160A49A.PLD A PROGRAMMED 18V10 (331-300132-200)	
34		U5-8	4	331-304373-100	IC: DIGITAL, OCTAL TRANSPARENT LATCH, PLASTIC DIP	SN74ALS373N (TI)
35		U41,42,50	3	331-304520-100	IC: DIGITAL, 8-BIT IDENTITY COMPARATOR, PLASTIC DIP	SN74ALS520N (TI)
36		U43	1	331-304641-110	IC: DIGITAL, OCTAL BUS TRANSCEIVER, PLASTIC DIP	SN74(ALS,AS)641A-1N (TI)
37		U44,52	2	331-304645-110	IC: DIGITAL, OCTAL BUS TRANSCEIVER, PLASTIC DIP	SN74(ALS,AS)645A-1N (TI)
38		U1-4	4	331-304688-100	IC: DIGITAL, 8-BIT MAGNITUDE COMPARATOR, PLASTIC DIP	SN74ALS688N (TI)
39		U13-15,31-33	6	331-309034-012	IC: DIGITAL, HEX CONTACT BOUNCE ELIMINATOR, PLASTIC DIP (SEE NOTE 4)	MC14490P (MOTOROLA)
40		U30	1	331-309099-000	IC: INTERFACE, CMOS VMEBUS INTERRUPTER MODULE, PLASTIC DIP	MX68C153 (MACRONIX)
41		U9-12,26-29	8	337-000000-300	TRANSISTOR: PHOTO, QUAD CHANNEL, 16 PIN	ILQ-2 (SIEMENS)
42		RP13-16,29-32	8	347-001000-183	SIP: 18K OHM, BUSSED, 6 PIN, LOW PROFILE	4606X-101-183 (BOURNS)
43		RP33	1	347-001002-102	SIP: 1K OHM, BUSSED, 10 PIN, LOW PROFILE	4610X-101-102 (BOURNS)
44		RP9-12,25-28	8	347-001005-332	SIP: 3.3K OHM, ISOLATED, 10 PIN, LOW PROFILE	4610X-102-332 (BOURNS)
45		CR1-32	32	348-104148-000	DIODE: SWITCHING, HIGH CONDUCTANCE, ULTRA FAST, DO-35 OUTLINE	1N4148 (AMPEREX)
46		U34,35	2	351-000000-080	SWITCH: DIP, 8 POSITION, LOW PROFILE, PC MOUNT, TAPE SEAL	ADF-08PCT (AUGAT)
47		U49,51	2	321-001320-000	SOCKET: DIP, 20 PIN, .300 ROW, MACHINED (SEE NOTE 5)	ICA-320-S(TT,ST,GT) (SAMTEC)
48						

ITEM	ABC	REF. DES.	QTY.	PART NO:	DESCRIPTION	MANUFACTURER	
49							
50							
51	1BC	ALL ODD J'S	32	321-000017-011	TERMINAL: PC BOARD, DUAL ROW, .025 THICK, GOLD PLATED, ONE POST	PEG02DS-(T,F)BR	(CRANE)
52	1BC	U18,19,22,23	4	331-304533-400	IC: DIGITAL, 8-BIT, TRANSPARENT, D-TYPE, INVERTING TRI-STATE, FAST, PLASTIC DIP	SN74F533N	(TI)
53	2BC	ALL ODD J'S	32	321-000017-011	TERMINAL: PC BOARD, DUAL ROW, .025 THICK, GOLD PLATED, ONE POST	PEG02DS-(T,F)BR	(CRANE)
54	2BC	U18,19,22,23	4	331-304373-100	IC: DIGITAL, OCTAL TRANSPARENT LATCH, PLASTIC DIP	SN74ALS373N	(TI)
55	3BC	ALL EVEN J'S	32	321-000017-011	TERMINAL: PC BOARD, DUAL ROW, .025 THICK, GOLD PLATED, ONE POST	PEG02DS-(T,F)BR	(CRANE)
56	3BC	U18,19,22,23	4	331-304533-400	IC: DIGITAL, 8-BIT, TRANSPARENT, D-TYPE, INVERTING TRI-STATE, FAST, PLASTIC DIP	SN74F533N	(TI)
57	4BC	ALL EVEN J'S	32	321-000017-011	TERMINAL: PC BOARD, DUAL ROW, .025 THICK, GOLD PLATED, ONE POST	PEG02DS-(T,F)BR	(CRANE)
58	4BC	U18,19,22,23	4	331-304373-100	IC: DIGITAL, OCTAL TRANSPARENT LATCH, PLASTIC DIP	SN74ALS373N	(TI)
59							
60	30C	RP5-8,21-24	8	347-001000-102	SIP: 1K OHM, BUSSED, 6 PIN, LOW PROFILE	4606X-101-102	(BOURNS)
61	A0C	RP1-4,17-20	8	347-001005-102	SIP: 1K OHM, ISOLATED, 10 PIN, LOW PROFILE	4610X-102-102	(BOURNS)
62	31C	RP5-8,21-24	8	347-001000-332	SIP: 3.3K OHM, BUSSED, 6 PIN, LOW PROFILE	4606X-101-332	(BOURNS)
63	A1C	RP1-4,17-20	8	347-001005-332	SIP: 3.3K OHM, ISOLATED, 10 PIN, LOW PROFILE	4610X-102-332	(BOURNS)
64	32C	RP5-8,21-24	8	347-001000-822	SIP: 8.2K OHM, BUSSED, 6 PIN, LOW PROFILE	4606X-101-822	(BOURNS)
65	A2C	RP1-4,17-20	8	347-001005-822	SIP: 8.2K OHM, ISOLATED, 10 PIN, LOW PROFILE	4610X-102-822	(BOURNS)

ITEM	ABC	REF. DES.	QTY.	PART NO:	DESCRIPTION	MANUFACTURER
66	33C	RP5-8,21-24	8	347-001000-183	SIP: 18K OHM, BUSSED, 6 PIN, LOW PROFILE	4606X-101-183 (BOURNS)
67	A3C	RP1-4,17-20	8	347-001005-183	SIP: 18K OHM, ISOLATED, 10 PIN, LOW PROFILE	4610X-102-183 (BOURNS)
68						
69						
70	AB2	C5-7,10-12	6	315-220001-229	CAP: 2.2pF, .200 LEAD SPACE, +/-.5pF, 200V, NPO CERAMIC MONOLYTHIC	C317C229D2G5CA (KEMET)
71	AB3	C5-7,10-12	6	315-210001-182	CAP: .0018uF, .200 LEAD SPACE, 20%, 100V, X7R CERAMIC MONOLYTHIC	C317C182M1R5CA (KEMET)
72	AB4	C5-7,10-12	6	315-220002-471	CAP: 470pF, .200 LEAD SPACE, 10%, 200V, NPO CERAMIC MONOLYTHIC	C3(17,22,23)C471K2G5CA (KEMET)
73	40C	RP5-8,21-24	8	347-001000-102	SIP: 1K OHM, BUSSED, 6 PIN, LOW PROFILE	4606X-101-102 (BOURNS)
74	41C	RP5-8,21-24	8	347-001000-332	SIP: 3.3K OHM, BUSSED, 6 PIN, LOW PROFILE	4606X-101-332 (BOURNS)
75	42C	RP5-8,21-24	8	347-001000-822	SIP: 8.2K OHM, BUSSED, 6 PIN, LOW PROFILE	4606X-101-822 (BOURNS)
76	43C	RP5-8,21-24	8	347-001000-183	SIP: 18K OHM, BUSSED, 6 PIN, LOW PROFILE	4606X-101-183 (BOURNS)

APPENDIX B

MC68153 BIM Data Sheet

MOTOROLA

SEMICONDUCTORS

PO BOX 20912 • PHOENIX ARIZONA 85036

MC68153

Advance Information

BUS INTERRUPTER MODULE

The bipolar LSI MC68153 Bus Interrupter interfaces a microcomputer system bus to multiple slave devices requiring interrupt capabilities. It handles up to 4 independent sources of interrupt requests and is fully programmable.

- VERSAbus/VMEbus Compatible
- MC68000 Compatible
- Handles 4 Independent Interrupt Sources
- 8 Programmable Read/Write Registers
- Programmable Interrupt Request Levels
- Programmable Interrupt Vectors
- Supports Interrupt Acknowledge Daisy Chain
- Control Registers Contain Flag Bits
- Single +5.0 Volt Supply
- Total Power Dissipation = 1.5 W Typical
- Temperature Range of 0°C to 70°C
- Chip Access Time = 200 ns Typical with 16 MHz Clock
- 40-Pin Dual-In-Line Package

TTL

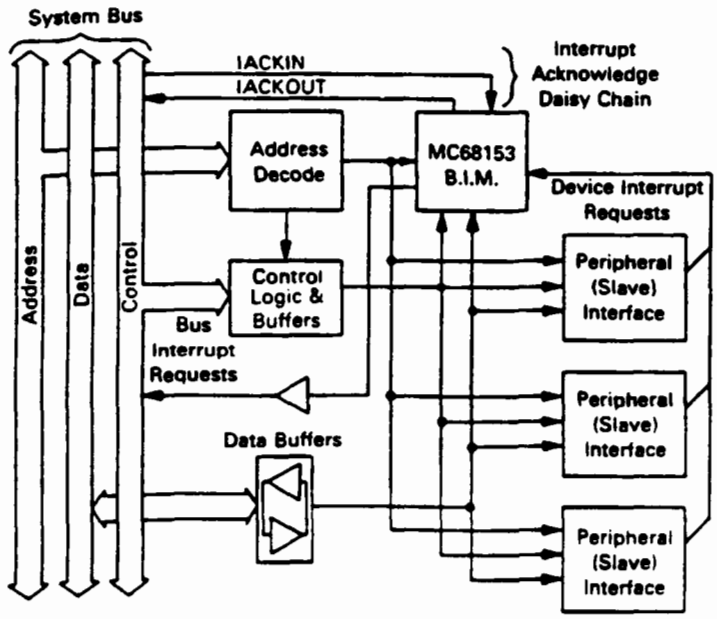
BUS INTERRUPTER MODULE

ADVANCED LOW POWER SCHOTTKY

P SUFFIX
PLASTIC PACKAGE
CASE 711-03

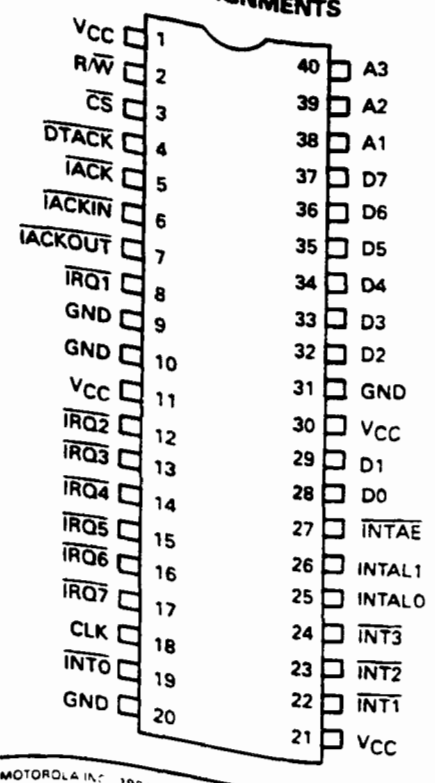
L SUFFIX
CERAMIC PACKAGE
CASE 734-04

FIGURE 1 — MC68153 SYSTEM BLOCK DIAGRAM



VERSAbus is a trademark of Motorola.

PIN ASSIGNMENTS



ABSOLUTE MAXIMUM RATINGS (Beyond which useful life may be impaired.)

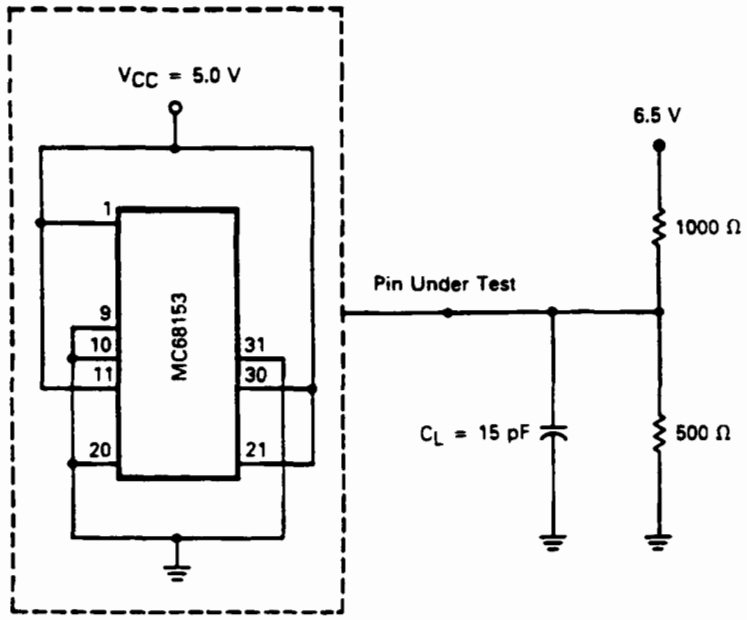
Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{in}	−0.5 to +7.0	V
Input Current	I_{in}	−30 to +5.0	mA
Output Voltage	V_{out}	−0.5 to +5.5	V
Output Current	I_{OL}	Twice Rated I_{OL}	mA
Storage Temperature	T_{stg}	−65 to +140	°C
Junction Operating Temperature	T_J	−55 to +140	°C

BURN-IN LIMITS: A maximum T_J of +175°C may be used for periods not to exceed 250 hours.

DC ELECTRICAL SPECIFICATIONS (V_{CC} = 5.0 V ±5%, T_A = 0°C to 70°C)

Parameter	Symbol	Min	Max	Unit	Test Conditions
High Level Input Voltage	V_{IH}	2.0	—	V	
Low Level Input Voltage	V_{IL}	—	0.8	V	
Input Clamp Voltage	V_{IK}	—	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
High Level Output Voltage(1)	V_{OH}	2.7	—	V	V_{CC} = MIN, I_{OH} = −400 μA
Low Level Output Voltage	V_{OL}	—	0.4	V	V_{CC} = MIN, I_{OL} = 8.0 mA
Output Short Circuit Current(2)	I_{OS}	−15	−130	mA	V_{CC} = MAX, V_{OUT} = 0 V
High Level Input Current	I_{IH}	—	20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
Low Level Input Current	I_{IL}	—	−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
Supply Current	I_{CC}	225	385	mA	V_{CC} = MAX
Output Off Current (High)	I_{OZH}	—	20	μA	V_{CC} = MAX, V_{OUT} = 2.4 V
Output Off Current (Low)	I_{OZL}	—	−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V

AC TEST CIRCUIT — AC Testing of All Outputs



NOTES:
1. Not applicable to *open-collector outputs*.
2. Not more than one output should be shorted at a time for longer than one second.
3. $\overline{CS}$ Low to CLK High (Setup Time) of 15 ns Min must be observed.
4. IACK Low to CLK High and $\overline{IACKIN}$ Low to CLK High (Setup Times) of 15 ns Min must be observed.
5. See Table 1 for additional performance guidelines.

AC ELECTRICAL SPECIFICATIONS (V_{CC} = 5.0 V ±5%, T_A = 0°C to 70°C)

Parameter	Test Number[5]	Max (ns)
CLK High to Data Out Valid (Delay)[3]	1	55
CLK High to $\overline{\text{DTACK}}$ Low (Delay)[3]	2	40
$\overline{\text{CS}}$ High to $\overline{\text{DTACK}}$ High (Delay)	3	35
CLK High to Data Out Valid (Delay)[4]	4	55
CLK High to $\overline{\text{INTAE}}$ Low (Delay)[4]	5	40
$\overline{\text{IACK}}$ High to Data Out High Impedance (Delay)	6	60
$\overline{\text{IACK}}$ High to $\overline{\text{DTACK}}$ High (Delay)	7	45
$\overline{\text{CS}}$ High to Data Out High (Delay)	8	45
$\overline{\text{CS}}$ High to $\overline{\text{IRQ}}$ High (Delay)	9	60
$\overline{\text{IACK}}$ High to $\overline{\text{INTAE}}$ High (Delay)	10	35

GENERAL DESCRIPTION

The MC68153 Bus Interrupter Module (BIM) is designed to serve as an interrupt requester for peripheral devices in a microcomputer system. Up to 4 independent devices can be interfaced to the system bus by the MC68153. Intended for asynchronous master/slave bus operation, the BIM is compatible with VERSAbus, VMEbus, MC68000 device bus, and other system buses. Figure 1 shows a block diagram of a typical configuration. In this example, three peripheral devices (bus slaves) are connected to the system data bus. Each of these devices could be parallel I/O, serial I/O, or some other function. An interrupt request from any device is routed to the MC68153, and the BIM handles all interface to the system bus. It generates a bus interrupt request as a result of the device interrupt request. When the system interrupt handler or processor responds with an interrupt acknowledge cycle, the MC68153 can answer supplying an interrupt vector and handling all timing.

The functional block diagram of the MC68153 is shown in Figure 2. The device contains circuitry to accept four separate interrupt sources ($\overline{\text{INT0}}$ – $\overline{\text{INT3}}$). Interface to the system bus includes generation of bus interrupt requests ($\overline{\text{IRQ1}}$ – $\overline{\text{IRQ7}}$), response to a bus interrupt acknowledge cycle (either supplying a vector or passing on a daisy chain signal), and releasing the bus interrupt request signal at the proper time. The BIM has flexibility provided by eight programmable read/write registers. Four 8-bit vector registers (VR0 – VR3) contain status/address information and supply a byte vector in response to an interrupt acknowledge cycle for the corresponding interrupt source. Four other 8-bit control registers (CR0 – CR3) contain information that oversees operation of the interrupt circuitry. The control information is programmable and includes interrupt request level and interrupt enable and disable. Also contained in the control registers are flag-bits. These flags are useful for task coordination, resource management, and interprocessor communication.

SIGNAL DESCRIPTION

Throughout the data sheet, signals are presented using the terms asserted and negated independent of whether the signal is asserted in the high voltage or low voltage state. Active low signals are denoted by a superscript bar.

BIDIRECTIONAL DATA BUS — D0 – D7

Pins D0 – D7 form an 8-bit bidirectional data bus to/from the system bus. These are active high, 3-state pins. D7 is the most significant bit.

ADDRESS INPUTS — A1 – A3

These active high inputs serve two functions. One function is to select one of the eight possible registers during a read or write cycle. Secondly, during an interrupt acknowledge A1 – A3 show the level of interrupt being acknowledged, and the BIM uses these to determine if a match exists with an internal level.

CHIP SELECT — $\overline{\text{CS}}$

$\overline{\text{CS}}$ is an active low input used to select the BIM's registers for the current bus cycle. Address strobe, data strobe, and appropriate address bits must be included in the chip select equation.

READ/WRITE — R/$\overline{\text{W}}$

The R/$\overline{\text{W}}$ input is a signal from the system bus used to determine if the current bus cycle is a read (high) or write (low).

DATA TRANSFER ACKNOWLEDGE — $\overline{\text{DTACK}}$

$\overline{\text{DTACK}}$ is an open-collector, active low output that signals the completion of a read, write, or interrupt acknowledge cycle. During read or interrupt acknowledge cycles, $\overline{\text{DTACK}}$ is asserted by the MC68153 after data has been provided on the data bus; during write cycles it is asserted after data has been accepted from the data bus. A pullup resistor is required to maintain $\overline{\text{DTACK}}$ high between bus cycles.

FIGURE 2 — MC68153 FUNCTIONAL BLOCK DIAGRAM

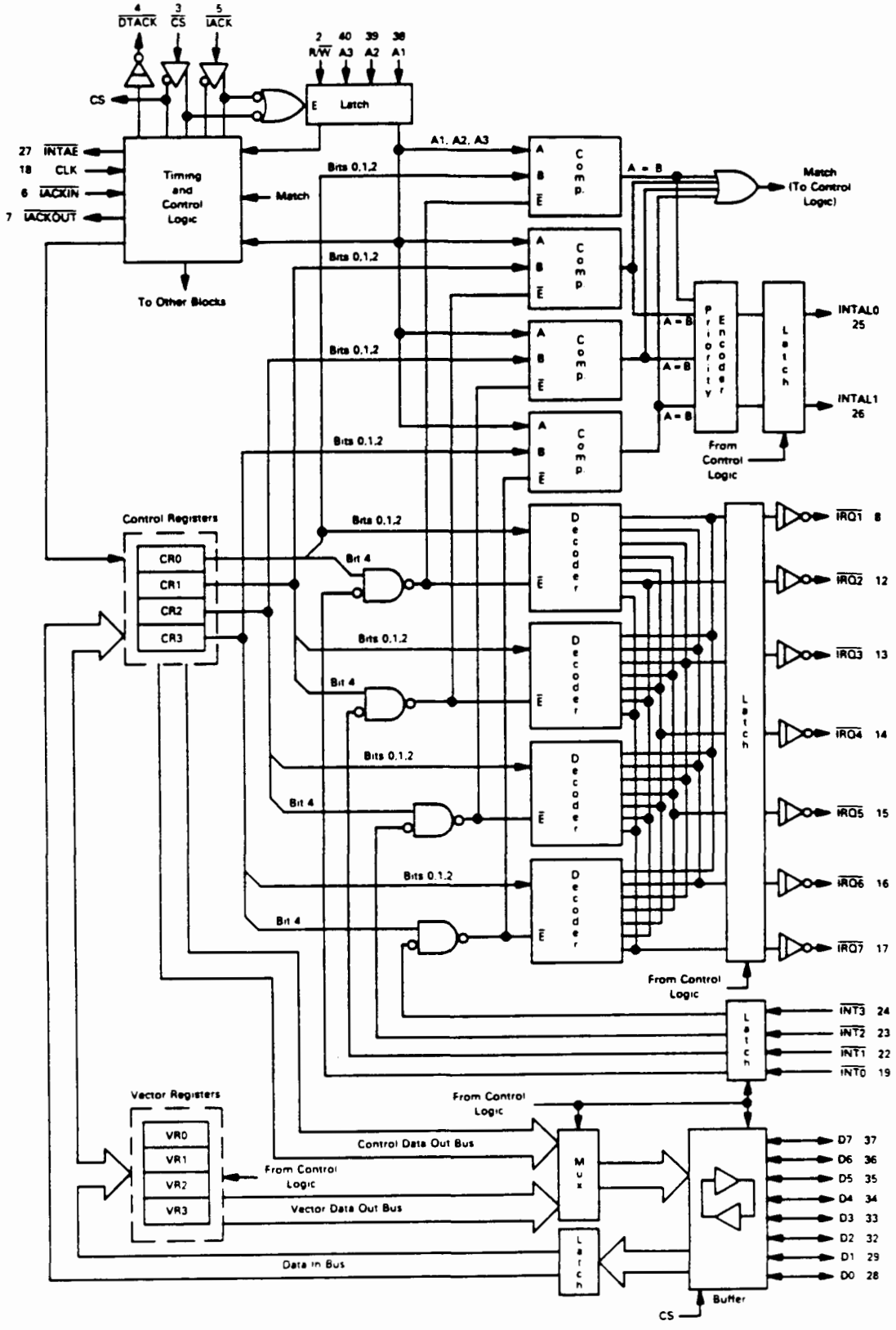
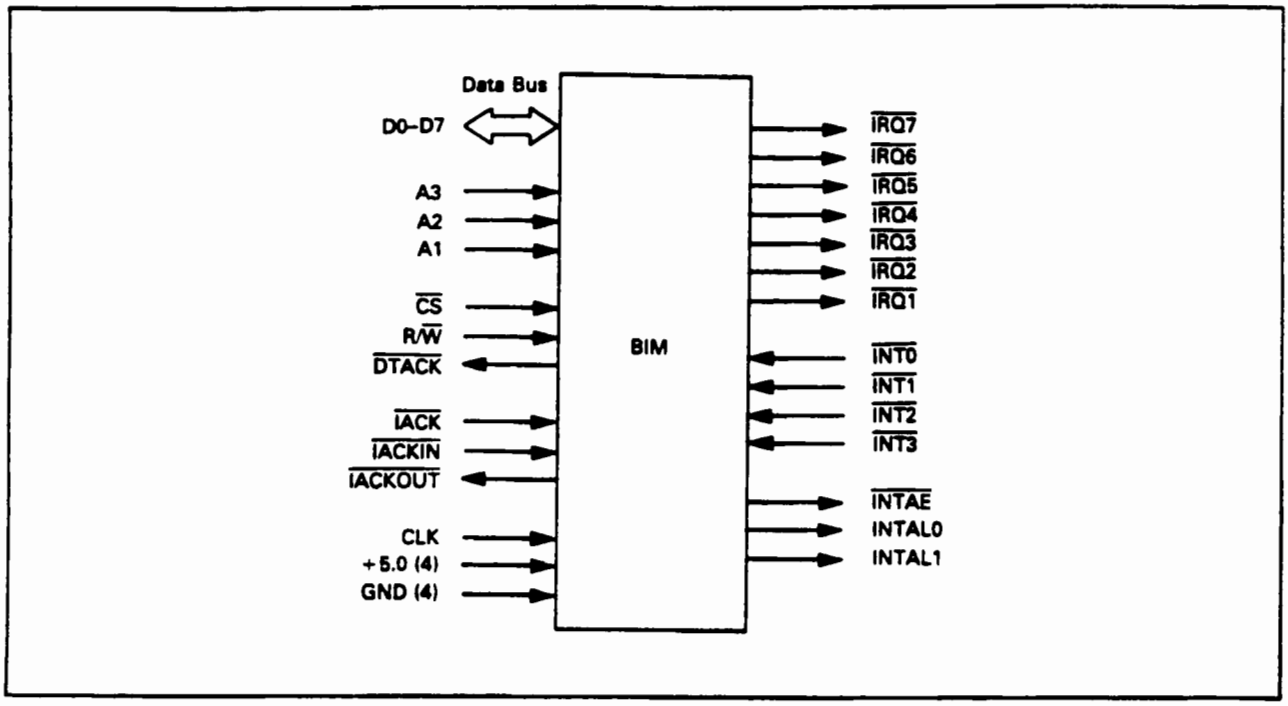


FIGURE 3 — LOGICAL PIN ASSIGNMENT



INTERRUPT ACKNOWLEDGE SIGNALS — $\overline{IACK}$, $\overline{IACKIN}$, $\overline{IACKOUT}$

These three pins support the interrupt acknowledge cycle. A low level on the $\overline{IACK}$ input indicates an interrupt acknowledge cycle has been initiated. This signal is conditioned externally with Address Strobe and the lower data strobe of an MC68000 type bus. After $\overline{IACK}$ is asserted the BIM compares the interrupt level presented on address lines A1, A2, and A3 with the current levels generated internally and determines if a match exists. Then, if input $\overline{IACKIN}$ is asserted (driven low), the BIM will either complete the interrupt acknowledge cycle if a match exists or assert output $\overline{IACKOUT}$ if *no* match exists.

$\overline{IACKIN}$ and $\overline{IACKOUT}$ form part of a prioritized interrupt acknowledge daisy chain. The daisy chain prioritizes interrupters and guarantees that two or more devices requesting an interrupt on the same level will not respond to the same cycle. The requesting device (or interrupter) must wait until $\overline{IACKIN}$ is asserted and not pass the signal on (assert $\overline{IACKOUT}$) if it is to complete the interrupt acknowledge cycle.

BUS INTERRUPT REQUEST SIGNALS — $\overline{IRQ1}$ – $\overline{IRQ7}$

These open-collector outputs are low when asserted, indicating a bus interrupt is requested at the corresponding level. An open-collector buffer is normally required for sufficient drive when interfacing to a system bus. A pullup resistor is required to maintain $\overline{IRQ1}$ – $\overline{IRQ7}$ high between interrupt requests.

DEVICE INTERRUPT REQUEST SIGNALS — $\overline{INT0}$ – $\overline{INT3}$

$\overline{INT0}$ – $\overline{INT3}$ are active low inputs used to indicate to the BIM that a device wants a bus interrupt.

INTERRUPT ACKNOWLEDGE ENABLE — $\overline{INTAE}$

During an interrupt acknowledge cycle, this output pin is asserted low to indicate that outputs INTAL0 and INTAL1 are valid. These two outputs contain an encoded number (x) corresponding to the interrupt ($\overline{INTx}$) being acknowledged. This feature can be used to signal interrupting devices, which supply their own vector, when to respond to the interrupt acknowledge cycle with the vector and a $\overline{DTACK}$ signal.

INTERRUPT ACKNOWLEDGE LEVEL — INTAL0, INTAL1

These active high outputs contain an encoded number corresponding to the interrupt level being acknowledged. They are valid only when $\overline{INTAE}$ is asserted low.

CLOCK — CLK

The CLK input is used to supply the clock for internal operations of the MC68153.

RESET — $\overline{CS}$, $\overline{IACK}$

Although a reset input is not supplied, an on-board reset is performed if $\overline{CS}$ and $\overline{IACK}$ are asserted simultaneously.

FIGURE 4 — MC68153 REGISTER MODEL

ADDRESS BIT A3	A2	A1	FLAG	FLAG AUTO-CLEAR	EXTERNAL/INTERNAL	INTERRUPT ENABLE	INTERRUPT AUTO-CLEAR	INTERRUPT LEVEL			REGISTER NAME
0	0	0	F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 0
0	0	1	F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 1
0	1	0	F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 2
1	1	1	F	FAC	X/$\overline{IN}$	IRE	IRAC	L2	L1	L0	CONTROL REGISTER 3
1	0	0	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 0
1	0	1	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 1
1	1	0	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 2
1	1	1	V7	V6	V5	V4	V3	V2	V1	V0	VECTOR REGISTER 3
			7	6	5	4	3	2	1	0	REGISTER NAME
			REGISTER BIT								

REGISTER DESCRIPTION

The MC68153 contains 8 programmable read/write registers. There are four control registers (CR0 – CR3) that govern operation of the device. The other four (VR0 – VR3) are vector registers that contain the vector data used during an interrupt acknowledge cycle. Figure 4 illustrates the device register model.

CONTROL REGISTERS

There is a control register for each interrupt source, i.e., CR0 controls $\overline{INT0}$, CR1 controls $\overline{INT1}$, etc. The control registers are divided into several fields:

1. Interrupt level (L2, L1, L0) — The least significant 3-bit field of the register determines the level at which an interrupt will be generated:

L2	L1	L0	IRQ LEVEL
0	0	0	DISABLED
0	0	1	IRQ1
0	1	0	IRQ2
0	1	1	IRQ3
1	0	0	IRQ4
1	0	1	IRQ5
1	1	0	IRQ6
1	1	1	IRQ7

   A value of zero in the field disables the interrupt.

2. Interrupt Enable (IRE) — This field (Bit 4) must be set (high level) to enable the bus interrupt request associated with the control register. Thus, if the $\overline{INTX}$ line is asserted and IRE is cleared, *no* interrupt request ($\overline{IRQX}$) will be asserted.
3. Interrupt Auto-Clear (IRAC) — If the IRAC is set (Bit 3), IRE (Bit 4) is cleared during an interrupt acknowledge cycle responding to this request. This action of clearing IRE disables the interrupt request. To re-enable the interrupt associated with this register, IRE must be set again by writing to the control register.
4. External/Internal (X/$\overline{IN}$) — Bit 5 of the control register determines the response of the MC68153 during an interrupt acknowledge cycle. If the X/$\overline{IN}$ bit is clear (low level) the BIM will respond with vector data and a $\overline{DTACK}$ signal, i.e., an internal response. If X/$\overline{IN}$ is set, the vector is not supplied and no $\overline{DTACK}$ is given by the BIM, i.e., an external device should respond.
5. Flag (F) — Bit 7 is a flag that can be used in conjunction with the test and set instruction of the MC68000. It can be changed without affecting chip operation. It is useful for processor-to-processor communication and resource allocation.
6. Flag Auto-Clear (FAC) — If FAC (Bit 6) is set, the Flag bit is automatically cleared during an interrupt acknowledge cycle.

VECTOR REGISTERS

Each interrupt input has its own associated vector register. Each register is 8 bits wide and supplies a data byte during its interrupt acknowledge cycle if the associated External/Internal (X/$\overline{IN}$) control register bit is clear (zero). This data can be status, identification, or address information depending on system usage. The information is programmed by the system user.

DEVICE RESET

When the MC68153 is reset, the registers are set to a known condition. The control registers are set to all zeros (low). The vector registers are set to $0F. This value is the MC68000 vector for an uninitialized interrupt vector.

FUNCTIONAL DESCRIPTION

SYSTEM OVERVIEW

The MC68153 can be used with many system buses, however, it is primarily intended for VMEbus, VERSAbus and MC68000 applications. Figure 5 shows a system configuration similar to VMEbus. In the figure only one system Data Transfer Bus (DTB) master is used. The Priority Interrupt structure provides a means for peripheral slave devices to ask for an interrupt of other processor (DTB master) activity and receive service from the processor. The MC68153 BIM acts as an interface device requesting and responding to interrupt acknowledge cycles for up to 4 independent slaves.

In Figure 5, functional modules are identified as Interrupters and an Interrupt Handler. An Interrupter (such as the MC68153) receives slave requests for an interrupt and handles all interface to the system bus required to ask for and respond to interrupt requests. The Interrupt Handler receives the bus interrupt requests, determines when an interrupt acknowledge will occur and at which level, and finally either performs the interrupt acknowledge (IACK) cycle or tells the DTB master to execute the IACK cycle.

The signal lines in the Priority Interrupt structure include (* — indicates active low):

1. IRQ1*–IRQ7* — seven prioritized interrupt request lines.
2. IACK* — signal line that indicates an interrupt acknowledge cycle is occurring.
3. IACKIN*/IACKOUT* — two signals that form part of a daisy chain that prioritizes interrupters.

In addition Data Transfer Bus control signals are involved in the IACK bus cycle:

1. AS* — the Address Strobe asserted low indicates a valid address is on the bus.
2. DSO* — the lower Data Strobe asserted low indicates a data transfer will occur on bus bits D00–D07.
3. WRITE* — the Read/Write is negated indicating the data is to be read from the Interrupter.
4. A01–A03 — Address lines A01–A03 contain the encoded priority level of the IACK cycle.
5. D00–D07 — Data bus lines D00–D07 are used to pass the interrupt vector from the responding Interrupter to the Interrupt Handler.
6. DTACK* — Data Transfer Acknowledge asserted low signals that the Interrupter has put the vector on the data bus.

FIGURE 5 — SIMPLE VMEbus CONFIGURATION

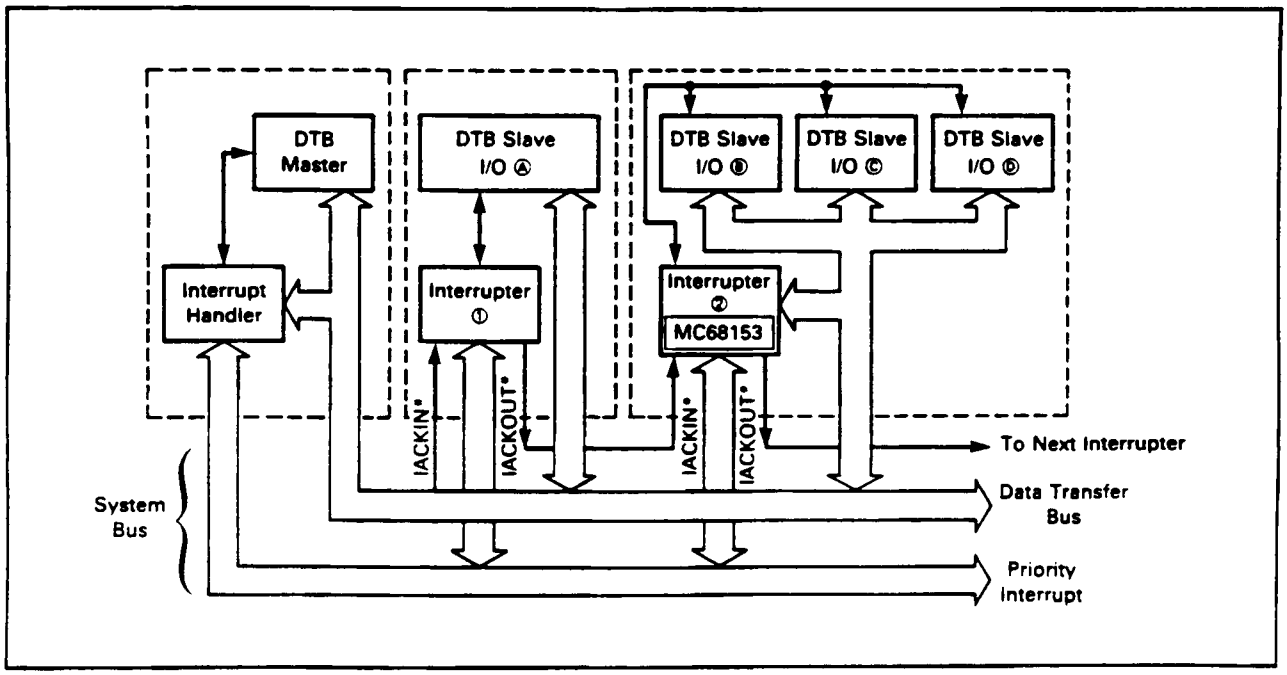
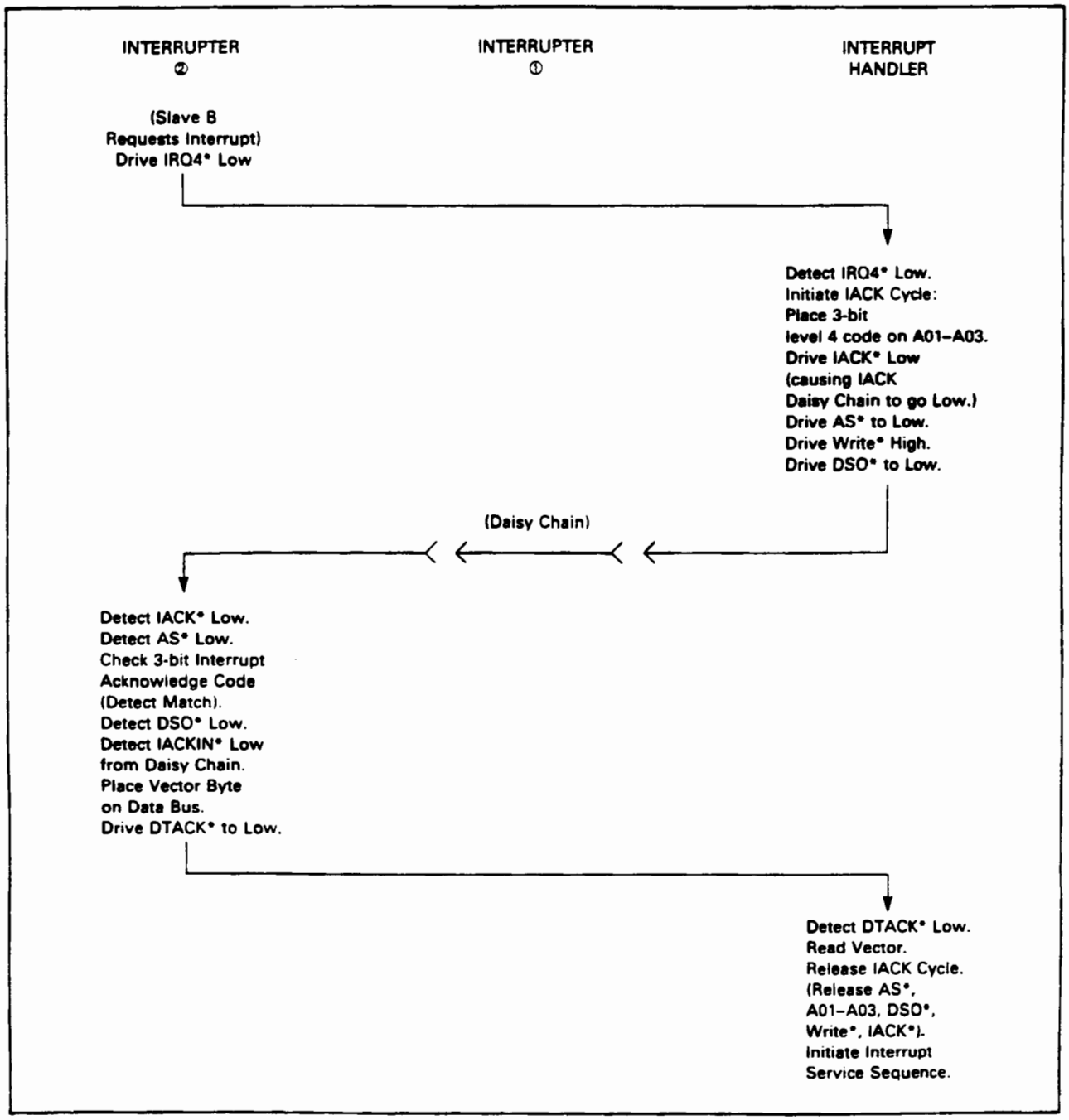


Figure 6 shows a flow diagram of a typical interrupt request and acknowledge operation. Briefly, the sequence of events is first, an Interrupter makes a request, next the Handler responds with an IACK cycle, then the Interrupter passes a vector to the Handler completing the IACK cycle, and finally the Handler uses the vector to determine additional action. Typically, an interrupt service routine is stored in software and the vector determines where its starting address is stored.

Note the daisy chain operation. If the IACK level (on A01–A03) does not match the Interrupter's request level or if no request is pending, the Interrupter passes the IACKIN* signal on and asserts IACKOUT*. This sequential action automatically prioritizes Requesters on the same level (first one in line with a request pending gets serviced) and prevents two or more Interrupters from responding simultaneously.

FIGURE 6 — INTERRUPT REQUEST AND ACKNOWLEDGE OPERATION FLOW DIAGRAM



This discussion is a very cursory look at the bus operation. For more details including situations with multiple bus masters, the user is directed to the VMEbus Specification MVMEBS or VERSAbus Specification M68KVBS. Also, the MC68153 can be used with other buses having similar interrupt structures.

BIM BUS INTERFACE

Figure 7 shows a simplified block diagram of the MC68153 interface to VERSAbus or VMEbus. Address Decode and Control Logic are dependent on the application and must be designed to guarantee BIM ac specifications. It is possible in most cases that the decode logic can be shared with the slave devices. Buffers are provided where shown to comply with bus loading and drive specifications. It is also possible that buffers can be shared with the slave bus interface.

READ/WRITE OPERATION

All eight BIM registers can be accessed from the system bus in both read and write modes. The BIM has an asynchronous bus interface, primarily designed for MC68000-like buses. The following BIM signals generate read and write cycles: Chip Select ($\overline{CS}$), Read/Write (R/$\overline{W}$), Address Inputs (A1–A3), Data Bus (D0–D7), and Data Transfer Acknowledge ($\overline{DTACK}$). During read and write cycles the internal registers are selected by A1, A2, and A3 in compliance with the Figure 4 Truth Table.

Figure 8 shows the device timing for a read cycle. R/$\overline{W}$ and A1–A3 are latched on the falling edge of $\overline{CS}$ and must meet specified setup and hold times. Chip access time for valid data and $\overline{DTACK}$ are dependent on the clock frequency as shown in the figure.

Figure 9 shows the device timing for a write cycle. R/$\overline{W}$, A1–A3, and D0–D7 are latched on the falling edge of $\overline{CS}$ and must meet specified setup and hold times. Chip access time for $\overline{DTACK}$ is dependent on the clock frequency as shown in the figure.

FIGURE 7 — VMEbus/VERSAbus INTERFACE BLOCK DIAGRAM

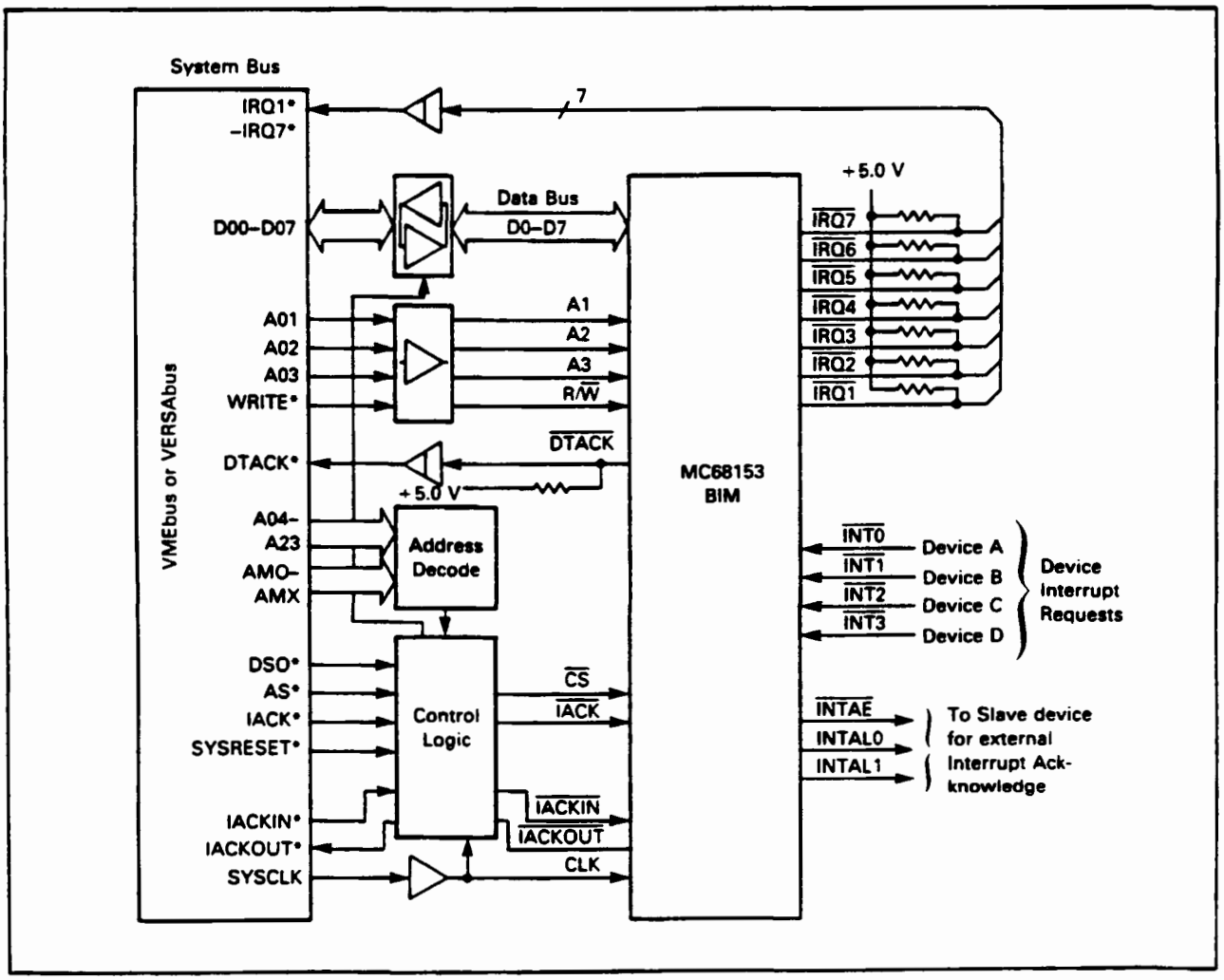


FIGURE 8 — READ CYCLE

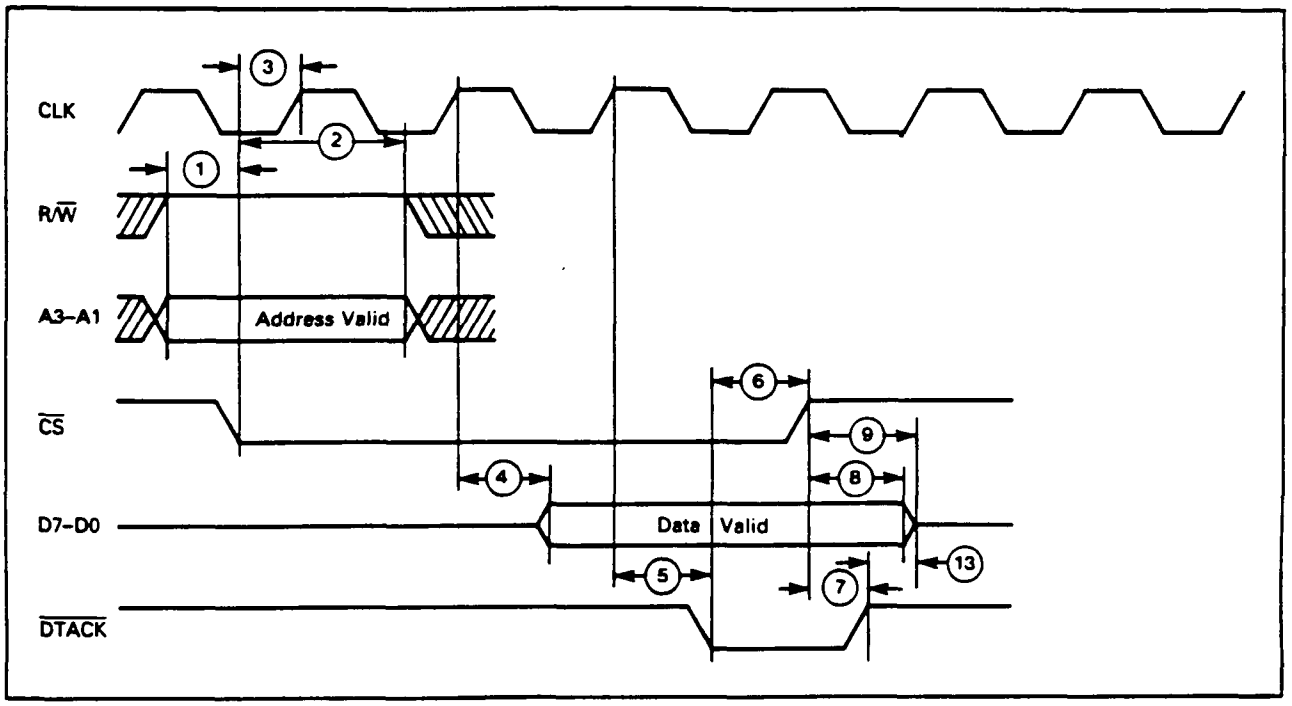
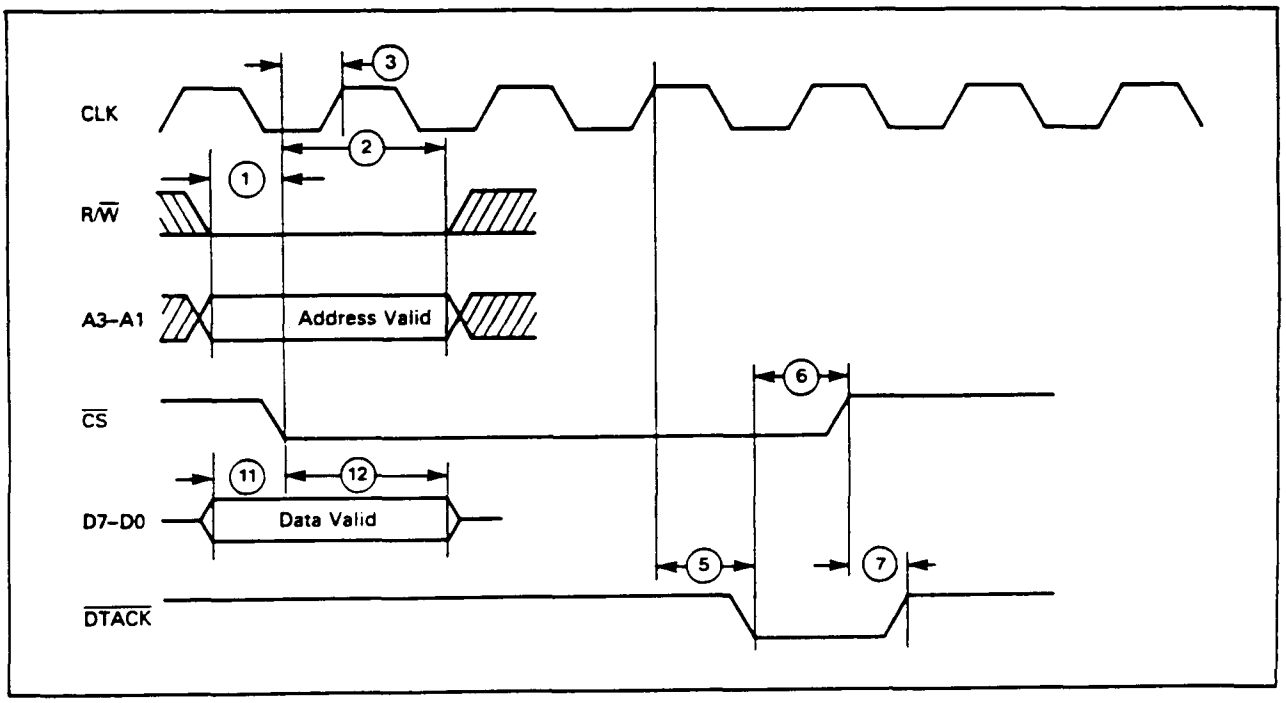


FIGURE 9 — WRITE CYCLE



INTERRUPT REQUESTS

The MC68153 accepts device interrupt requests on inputs $\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, and $\overline{INT3}$. Each input is regulated by Bit 4 (IRE) of the associated control register (CR0 controls $\overline{INT0}$, CR1 controls $\overline{INT1}$, etc). If IRE (Interrupt Enable) is set and a device input is asserted, an Interrupt Request open-collector output ($\overline{IRQ1}$–$\overline{IRQ7}$) is asserted. The asserted $\overline{IRQX}$ output is selected by the value programmed in Bits 0, 1, and 2 of the control register (L0, L1, and L2). This 3-bit field determines the interrupt request level as set by software.

Two or more interrupt sources can be programmed to the same request level. The corresponding $\overline{IRQX}$ output will remain asserted until multiple interrupt acknowledge cycles respond to all requests.

If the interrupt request level is set to zero, the interrupt is disabled because there is no corresponding IRQ output.

INTERRUPT ACKNOWLEDGE

The response of an Interrupt Handler to a bus interrupt request is an interrupt acknowledge cycle. The IACK cycle is initiated in the MC68153 by receiving $\overline{IACK}$ low. R/$\overline{W}$, A1, A2, A3 are latched, and the interrupt level on line A1–A3 is compared with any interrupt requests pending in the chip. Further activity can be one of four cases:

1. No further action required — This occurs if $\overline{IACKIN}$ is not asserted. Asserting $\overline{IACK}$ only starts the BIM activity. If the daisy chain signal never reaches the MC68153 ($\overline{IACKIN}$ is not asserted), another Interrupter has responded to the $\overline{IACK}$ cycle. The cycle will end, the chip $\overline{IACK}$ is negated, and no additional action is required.

2. Pass on the interrupt acknowledge daisy chain — For this case, $\overline{IACKIN}$ input is asserted by the preceding daisy chain Interrupter, and $\overline{IACKOUT}$ output is in turn asserted. The daisy chain signal is passed on when no interrupts are pending on a matching level or when any possible interrupts are disabled. The Interrupt Enable (IRE) bit of a control register can disable any interrupt requests, and in turn, any possible matches.

3. Respond internally — For this case, $\overline{IACKIN}$ is asserted and a match is found. The MC68153 completes the IACK cycle by supplying an interrupt vector from the proper vector register followed by a $\overline{DTACK}$ signal asserted. $\overline{IACKOUT}$ is not asserted because the interrupt acknowledge cycle is completed by this device.

   For the MC68153 to respond in this mode of operation, the EXTERNAL/$\overline{INTERNAL}$ control register bit (X/$\overline{IN}$) must be zero. For each source of interrupt request, the associated control register determines the BIM response to an IACK cycle, and the X/$\overline{IN}$ bit sets this response either internally (X/$\overline{IN}$ = 0) or externally (X/$\overline{IN}$ = 1).

4. Respond externally — For the final case, $\overline{IACKIN}$ is also asserted, a match is found and the associated control register has X/$\overline{IN}$ bit set to one. The MC68153 does not assert $\overline{IACKOUT}$ and does assert $\overline{INTAE}$ low. $\overline{INTAE}$ signals that the requesting device must complete the IACK cycle (supplying a vector and $\overline{DTACK}$) and that the 2-bit code contained on outputs INTAL0 and INTAL1 shows which interrupt source is being acknowledged.

These cases are discussed in more detail in the following paragraphs.

Internal Interrupt Acknowledge

For an internal interrupt acknowledge to occur, the following conditions must be met:

1. One or more device interrupt inputs ($\overline{INT0}$–$\overline{INT3}$) has been asserted and corresponding control bit IRE value is one.

2. $\overline{IACK}$ asserted.

3. A match exists between [A3, A2, A1] and the [L2, L1, L0] field of an enabled, requesting control register. If two or more devices are requesting at the same interrupt level, preference is given to the *highest number requester*, that is, $\overline{INT3}$ has highest priority and $\overline{INT0}$ has lowest.

4. Control register bit X/$\overline{IN}$ of matching interrupt source must be zero.

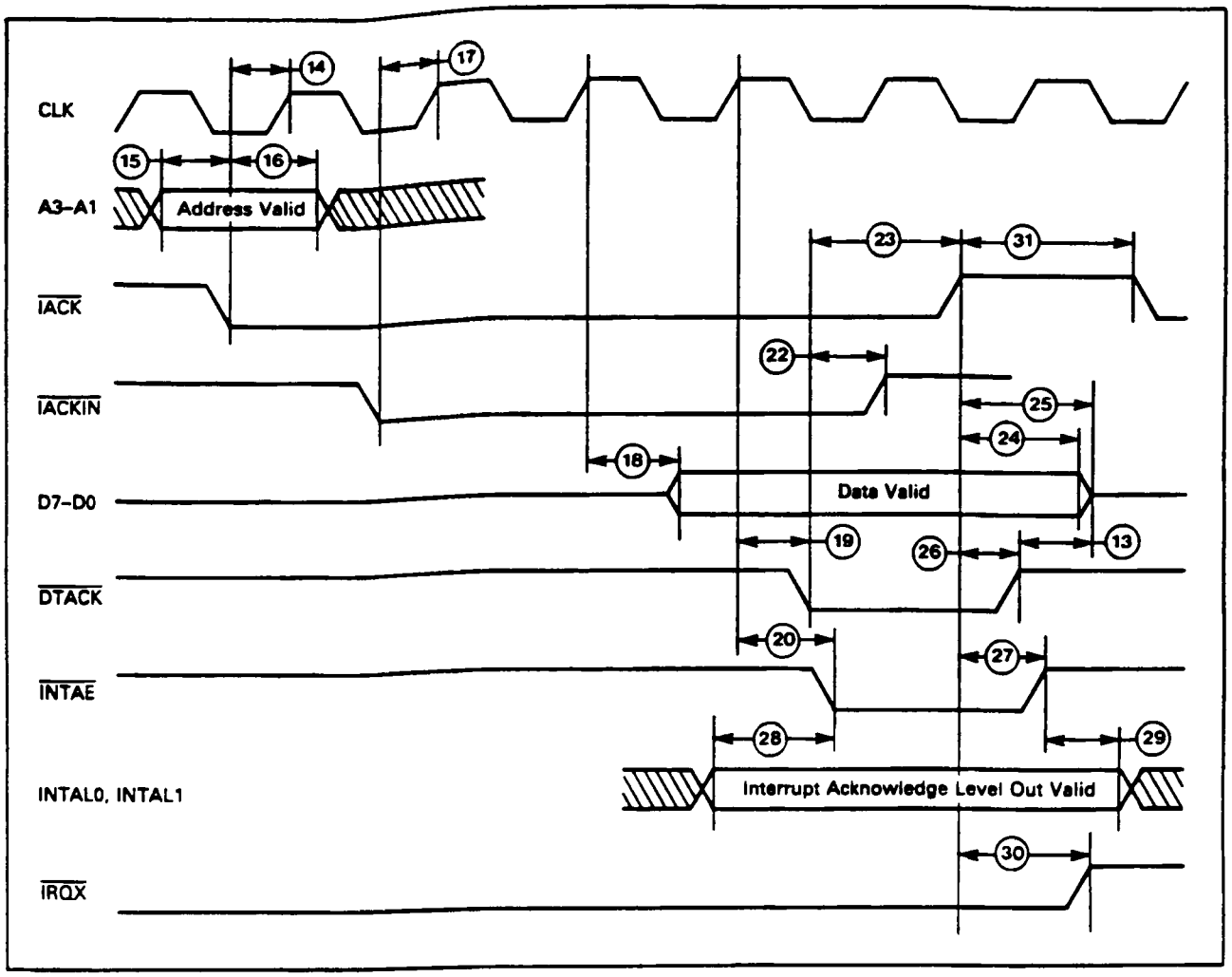
5. $\overline{IACKIN}$ asserted.

The internal interrupt acknowledge cycle timing is shown in Figure 10. The 8-bit interrupt acknowledge vector is presented to the data bus and $\overline{DTACK}$ is asserted. Note also that INTAL0 and INTAL1 are valid and $\overline{INTAE}$ is asserted during this cycle although they would normally not be used. The cycle is terminated (data and $\overline{DTACK}$ released) after $\overline{IACK}$ is negated.

During the IACK cycle, the INTERRUPT AUTO-CLEAR control bit (IRAC) comes into play. If the IRAC = one for the responding interrupt source, the INTERRUPT ENABLE (IRE) bit is automatically cleared during the IACK cycle, thus disabling the associated interrupt input and any $\overline{IRQX}$ output asserted due to this interrupt input. Before another interrupt can be requested from this source, IRE must be set to one by writing to the control register.

Note that $\overline{IACKOUT}$ is not asserted because this device is responding to the IACK and does not pass the daisy chain signal on. Also, new device interrupt requests occurring on $\overline{INT0}$–$\overline{INT3}$ after $\overline{IACK}$ is asserted are locked out to prevent any race conditions on the daisy chain.

FIGURE 10 — INTERRUPT ACKNOWLEDGE CYCLE — INTERNAL VECTOR



External Interrupt Acknowledge

For an external interrupt acknowledge, the same conditions as listed above are met with one exception. Control register bit X/$\overline{IN}$ of matching interrupt source must be set to one. The timing is shown in Figure 11. For this cycle, the interrupt vector and $\overline{DTACK}$ must be supplied by an external device. $\overline{INTAE}$ is asserted indicating that INTAL0 and INTAL1 are valid. The external device can use these signals to enable the vector and $\overline{DTACK}$. The cycle is terminated after $\overline{IACK}$ is negated.

The IRAC control bit acts in the external interrupt acknowledge the same as described for the internal response (see above). Also, $\overline{IACKOUT}$ is not asserted and new device interrupts are disabled for reasons discussed above.

Pass On IACK Daisy Chain

If the MC68153 has no interrupt request pending at the same level as the interrupt acknowledge, the IACK daisy chain signal is passed on to the next device if $\overline{IACKIN}$ is asserted. The following conditions are thus met:

1. $\overline{IACK}$ asserted.
2. No match exists between [A3, A2, A1] and the [L2, L1, L0] field of an enabled, requesting control register.
3. $\overline{IACKIN}$ is asserted.

$\overline{IACKOUT}$ is asserted if these conditions are valid. This output drives $\overline{IACKIN}$ of the next Interrupter on the daisy chain, passing the signal along. Figure 12 shows the timing for this case. $\overline{IACKOUT}$ is negated after $\overline{IACK}$ is negated.

FIGURE 11 — INTERRUPT ACKNOWLEDGE CYCLE — EXTERNAL VECTOR

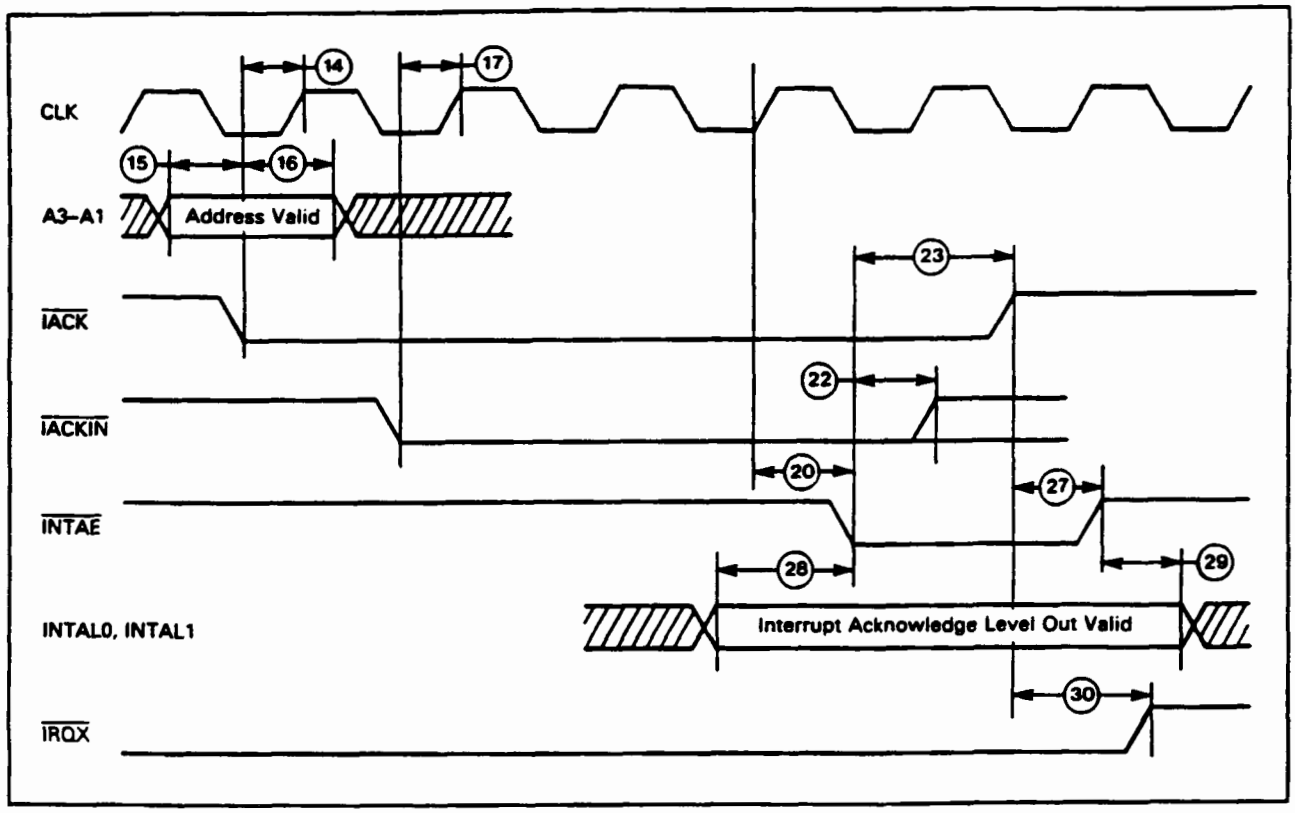
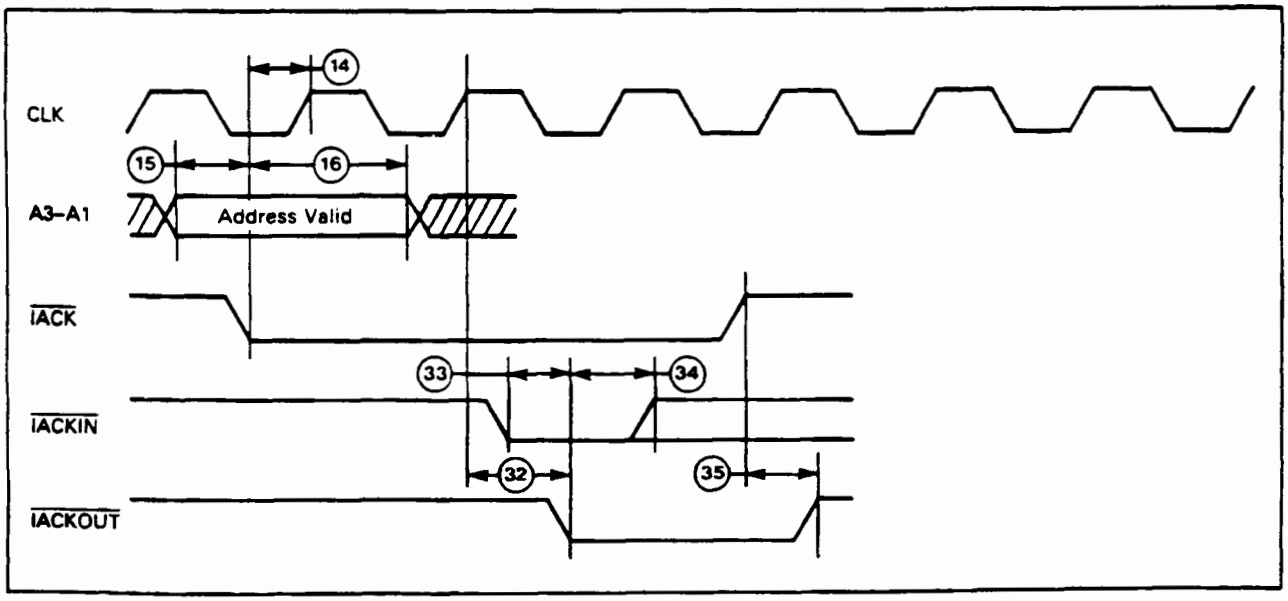


FIGURE 12 — INTERRUPT ACKNOWLEDGE CYCLE — $\overline{\text{IACKOUT}}$



CONTROL REGISTER FLAGS

Each control register contains a Flag bit (F) and a Flag Auto-Clear bit (FAC). Both bits can be read or altered via a register write without affecting the interrupt operation of the device. The Flag is useful as a status indicator for resource management and as a semaphor in multitasking or multiprocessor systems. Flag (F) is located in bit position 7 and can be used with the MC68000 Test and Set (TAS) instruction.

The Flag Auto-Clear (FAC) is used to manipulate the Flag bit. If the Flag is set to one and the FAC is also one, an interrupt acknowledge cycle to the associated interrupt source clears the Flag bit. This feature is useful in determining the interrupt status and passing messages.

RESET

There is no reset input, however, a chip reset is activated by asserting both $\overline{CS}$ and $\overline{IACK}$ simultaneously (Figure 13). These inputs should be held low for a minimum of two clock cycles for a full reset function. The control registers are reset to all zeroes and the Vector Registers are set to a value of $0F. This vector value is the uninitialized vector for the MC68000. See the MC68000 Users Manual for more details on this vector.

CLOCK

The chip clock is required for internal operation to occur. Typical frequency is 16 MHz in VMEbus and VERSAbus applications derived from the system clock. Any frequency can be used, however, up to 25 MHz (Figure 14).

FIGURE 13 — RESET

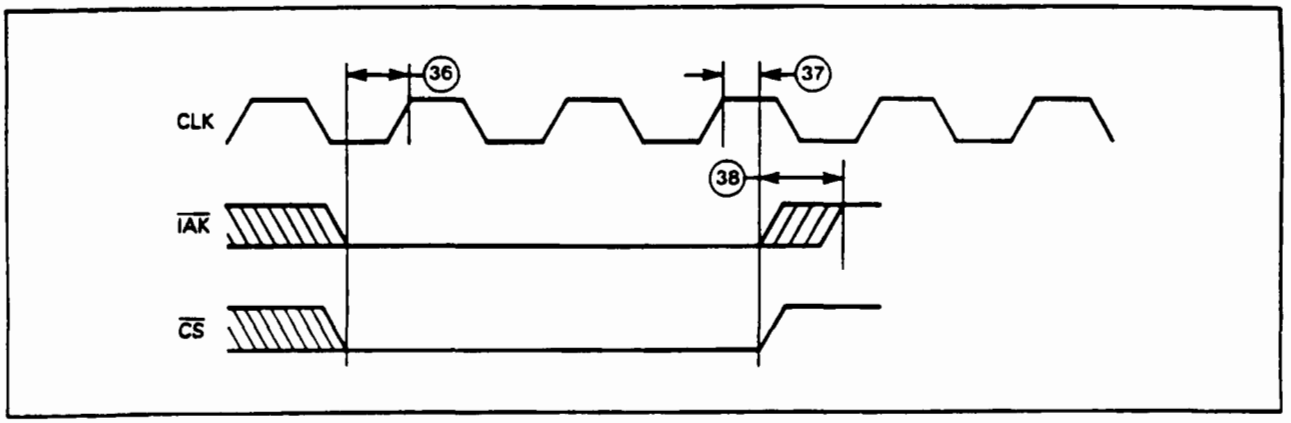


FIGURE 14 — CLOCK WAVEFORM

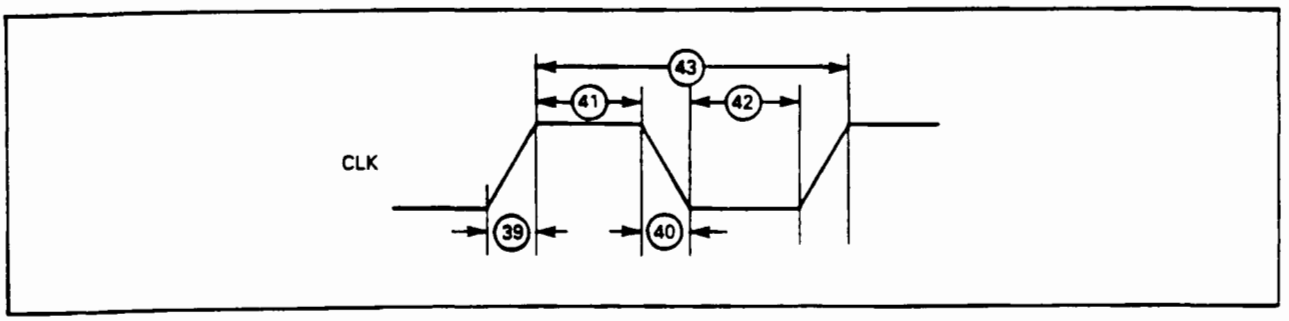


TABLE 1
AC PERFORMANCE SPECIFICATIONS
(V_{CC} = 5.0 V ±5%, T_A = 0°C to 70°C)

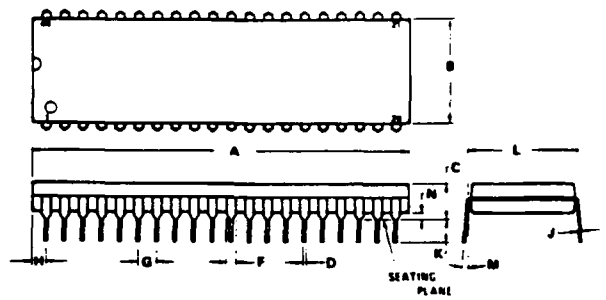
Number	Characteristic	Min	Max	Units	Notes
1	R/$\overline{W}$, A1–A3 Valid to $\overline{CS}$ Low (Setup Time)	10	—	ns	
2	$\overline{CS}$ Low to R/$\overline{W}$, A1–A3 Invalid (Hold Time)	5.0	—	ns	
3	$\overline{CS}$ Low to CLK High (Setup Time)	15	—	ns	1
4	CLK High to Data Out Valid (Delay)	—	55	ns	2
5	CLK High to $\overline{DTACK}$ Low (Delay)	—	40	ns	2
6	$\overline{DTACK}$ Low to $\overline{CS}$ High	0		ns	
7	$\overline{CS}$ High to $\overline{DTACK}$ High (Delay)	—	35	ns	10
8	$\overline{CS}$ High to Data Out Invalid (Hold Time)	0	—	ns	
9	$\overline{CS}$ High to Data Out High-Impedance (Hold Time)	—	50	ns	
10	$\overline{CS}$ High to $\overline{CS}$ or $\overline{IACK}$ Low	20	—	ns	
11	Data In Valid to $\overline{CS}$ Low (Setup Time)	10	—	ns	
12	$\overline{CS}$ Low to Data In Invalid (Hold Time)	5.0	—	ns	
13	$\overline{DTACK}$ High to Data Out High-Impedance	—	25	ns	10
14	$\overline{IACK}$ Low to CLK High (Setup Time)	15	—	ns	1
15	A1–A3 Valid to $\overline{IACK}$ Low (Setup Time)	10	—	ns	
16	$\overline{IACK}$ Low to A1–A3 Invalid (Hold Time)	5.0	—	ns	
17	$\overline{IACKIN}$ Low to CLK High (Setup Time)	15	—	ns	1, 8
18	CLK High to Data Out Valid (Delay)	—	55	ns	3
19	CLK High to $\overline{DTACK}$ Low (Delay)	—	40	ns	3
20	CLK High to $\overline{INTAE}$ Low (Delay)	—	40	ns	3
22	$\overline{DTACK}$ Low to $\overline{IACKIN}$ High	0	—	ns	8
23	$\overline{DTACK}$ Low to $\overline{IACK}$ High	0	—	ns	
24	$\overline{IACK}$ High to Data Out Invalid (Hold Time)	0	—	ns	
25	$\overline{IACK}$ High to Data Out High Impedance (Delay)	—	60	ns	
26	$\overline{IACK}$ High to $\overline{DTACK}$ High (Delay)	—	45	ns	10
27	$\overline{IACK}$ High to $\overline{INTAE}$ High (Delay)	—	35	ns	
28	INTAL0, INTAL1 Valid to $\overline{INTAE}$ Low (Setup Time)	1.0	2.0	CLK Per	
29	$\overline{INTAE}$ High to INTAL0, INTAL1 Invalid (Hold Time)	1.0	2.0	CLK Per	
30	$\overline{IACK}$ High to $\overline{IRQx}$ High (Delay)	—	50	ns	7, 10
31	$\overline{IACK}$ High to $\overline{IACK}$ or $\overline{CS}$ Low	20	—	ns	
32	CLK High to $\overline{IACKOUT}$ Low (Delay)	—	40	ns	5
33	$\overline{IACKIN}$ Low to $\overline{IACKOUT}$ Low (Delay)	—	30	ns	4, 8
34	$\overline{IACKOUT}$ Low to $\overline{IACKIN}$, $\overline{IACK}$ High	0	—	ns	8
35	$\overline{IACK}$ High to $\overline{IACKOUT}$ High (Delay)	—	35	ns	
36	$\overline{IACK}$ and $\overline{CS}$ both Low to CLK High (Setup Time)	15	—	ns	9
37	CLK High to $\overline{IACK}$ or $\overline{CS}$ High (Hold Time)	0	—	ns	
38	$\overline{IACK}$ or $\overline{CS}$ High to $\overline{IACK}$ and $\overline{CS}$ High (Skew)	—	1.0	CLK Per	6
39	Clock Rise Time	—	10	ns	
40	Clock Fall Time	—	10	ns	
41	Clock High Time	20	—	ns	
42	Clock Low Time	20	—	ns	
43	Clock Period	40	—	ns	

NOTES:

1. This specification only applies if the VBIM had completed all operations initiated by the previous bus cycle when $\overline{CS}$ or $\overline{IACK}$ was asserted. Following a normal bus cycle, all operations are completed within 2 clock cycles after $\overline{CS}$ or $\overline{IACK}$ have been negated. If $\overline{IACK}$ or $\overline{CS}$ is asserted prior to completion of these operations, the new cycle, and hence, $\overline{DTACK}$ is postponed.

   If the $\overline{IACK}$, $\overline{IACKIN}$ or $\overline{CS}$ setup time is violated, $\overline{DTACK}$ may be asserted as shown, or may be asserted one clock cycle later (i.e. $\overline{IACK}$ will not be recognized until the next rising edge of the clock).
2. Assumes that 3 has been met.
3. Assumes that 14 and 17 have both been met.
4. Assumes that 14 has been met. ($\overline{IACKOUT}$ cannot go low prior to $\overline{IACKIN}$ going low).
5. Assumes that 14 has been met and $\overline{IACKIN}$ has been low for at least the amount of time specified by 33.
6. 38 is the minimum skew between the last moment when both $\overline{IACK}$ and $\overline{CS}$ are asserted to when both are negated, to insure that an access cycle is not unintentionally started.
7. Assumes no other $\overline{INTx}$ input is causing $\overline{IRQx}$ to be driven low.
8. In non-daisy chain systems, $\overline{IACKIN}$ may be tied low.
9. Failure to meet this spec. causes RESET to be ignored for 1 clock period. It is then necessary to keep these signals low for 3 clock periods instead of 2.
10. Delay time is specified from input signal to Open-Collector Output pulled High thru 1.0 kΩ resistor to +6.5 V.

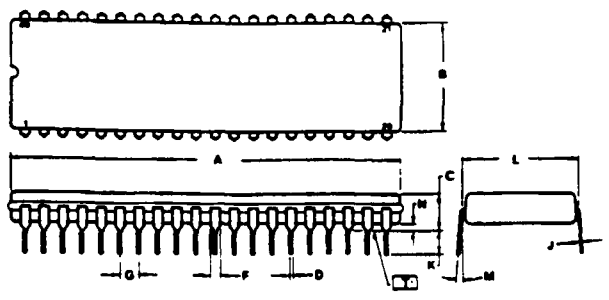
OUTLINE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

CASE 711-03
PLASTIC PACKAGE



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	51.31	53.24	2.020	2.096
B	12.70	15.49	0.500	0.610
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

NOTES
1. DIM -A- IS DATUM
2. POSITIONAL TOLERANCE FOR LEADS ⌖ Ø 0.25(0.010) Ⓜ T A Ⓢ
3. -T- IS SEATING PLANE
4. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL
5. DIMENSIONS A AND B INCLUDE MENISCUS
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973

CASE 734-04
CERAMIC PACKAGE

TYPICAL THERMAL CHARACTERISTICS

Package	θJA (Junction to Ambient) Still Air	Junction Temperature Still Air @ 70°C Ambient
L Suffix	40°C/W	147°C
P Suffix[1]	35°C/W	137°C

NOTES:
1. For reliable system operation the maximum allowable junction temperature (T_J) for plastic encapsulated packages has been limited to +140°C. Exceeding this limit will accellerate "wear-out" mechanisms associated with industry standard assembly methods using thermosonic ball bonds to attach gold (Aμ) bond wire to aluminum (Al) bond pads on the die surface.
2. At T_J = 140°C, time to 0.1% failure due to Aμ/Al interconnect = 8,920 Hours.

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