SBS VP74221-P0BC

Pentium All-In-One 6U VMEbus Embedded Computer

Limited Availability
Used and in Excellent Condition

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VP7

PC/AT compatible Processor Module
and Multifunction I/O Module

Hardware User's Manual

Revision 1.1

Revision	By	Date	Chapter	Comments
1.0	BG	02/18/02		First Release
1.1	PS	04/16/02	1.1-1.3	New CPUs added, new thermal specification

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Unpacking and Handling Instructions

1. Please read this manual carefully before unpacking the module or fitting it into your system. This will certainly save time and avoid trouble.
2. Please observe the precautions for electrostatic sensitive modules.
3. If the product contains batteries, please do not place the board on conductive surfaces or anti-static plastic or sponge, which can cause shorts and lead to battery or board trace damage.
4. Please do not exceed the specified operational temperatures. Please note that batteries might have temperature restrictions.
5. Keep all original packaging material for future storage or warranty shipments of the board.

Caution

Danger of explosion if battery is incorrectly replaced.
Replace only with the same or equivalent type recommended by SBS Technologies. Dispose of used batteries according to the instructions of SBS Technologies.

Notes

Drain static electricity before you install or remove any parts. Installing or removing modules without observing this precaution could result in damage to this and/or other modules in your system.

Installation

Use the following steps to install your SBS Technologies hardware.

General Advisories

1. Before installing or removing any board, please ensure that the system power and external supplies have been turned off.
2. Check that the jumpers and piggybacks are correctly configured for your application.
3. Mount the board/piggyback/transition module very carefully. See also additional advisories for VMEbus and CompactPCI products below.
4. Connect all I/O cables.
5. Once you are certain that all modules are correctly fitted into the system and all connections have been made properly, restore the power.

Advisories for VMEbus products

On a standard VMEbus backplane, remove the jumpers on the IACKIN - IACKOUT interrupt daisy chain (1 jumper) and on the BGxIN - BGxOUT busgrant daisy chains (4 jumpers) for the slot where the board is to be mounted. The daisy chain jumpers on the VMEbus backplane should be mounted on all free slots.

Setting jumpers is not necessary for the SBS Technologies Auto-Daisy-Chain VMEbus backplane (order number: VBUSxxAD). Please read additional advisories within the manual.

A board with system controller functionality must be fitted at slot 1 (for SBS Technologies products, see additional notes within the manual).

Advisories for Compact PCI products

Mount the CPU board carefully on the first CPCIbus slot (called system slot). Note that on some boards connectors are used for I/O purposes which must not be inserted into a CPCIbus backplane. A transition module must be used instead.

Disclaimer

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SBS Technologies do not accept any liability concerning the use of their products in life support systems.

Warranty

SBS Technologies grants the original purchaser of SBS Technologies products a warranty of 12 month from the date of delivery. For details refer to the "Allgemeine Geschäftsbedingungen".

In the event of repair, please return the product together with additional written information about

the kind of defect
is the defect restricted to certain environmental conditions
what was the hardware environment when the defect appeared
were there input signals; if yes which
warranty/no warranty repair

Please use the error report form sheet at the end of this manual and use the original packing material to avoid damage. Otherwise warranty may be lost.

Trademarks

Product and company names listed are trademarks or trade names of their respective companies owners.

Table of Contents

1 General Information

1.1 Features

• Microprozessor	Intel Celeron 333 up to 566 MHz running at 66 MHz bus clock Intel Pentium II 350, 400, 450 MHz running at 100 MHz bus clock Intel Pentium III 500 up to 1000 MHz running at 100 MHz bus clock Intel mobile Pentium III 500, 700 MHz running at 100 MHz bus clock
• Clocks	Front side bus clock 100 MHz (Pentium II >=350MHz) Front side bus clock 66 MHz (Pentium II <=333MHz, Celeron) PCI clock 33 MHz
• Cache RAM	16 Kbyte instruction + 16 Kbyte data first level cache up to 512 Kbyte second level cache depending on Microprocessor used L1 and L2 cache on CPU module
• DRAM	32 - 512 Mbyte DRAM SIMM module, optional with ECC
• Flash BIOS	256Kbyte easy updating, in-system programmable Includes: AMI BIOS SCSI BIOS VGA BIOS Ethernet BOOT module
• Silicon Disk	Up to 220 Mbyte with ATA Flash drive
• CMOS RAM	114 byte non-volatile RTC, MC146818 compatible RTC with onboard Lithium battery
• Keyboard	IBM PC/AT compatible keyboard controller with PS/2 style connector
• Mouse	PS/2 compatible mouse connector
• USB	2 high-speed 12 Mbit/sec USB ports
• Watchdog	Watchdog activates reset under software control
• NMI-Timer	User programmable timer, allows "Real Time Functions" with Windows 3.11, Windows 95 and Windows NT
• LCD/VGA	PCI VGA with 64-bit Windows accelerator and LCD flat panel interface. Resolution up to 1600x1200 on CRT, 65536/16.7 Mio colors, 135 MHz, 2/4MB RAM, color and monochrome TFT or STN panel, supports SS and DD type with max. 24-bit interfaces
• Fast Ethernet	High speed PCIbus Ethernet controller (AM79C972) with 10BaseT and 100BaseTX interface and integrated FIFO buffer

• SCSI-2, 40 MB/s	PCI Ultra Wide SCSI-2 controller (SYM53C875) with up to 40 Mbyte/s transfer rate
• Floppy	Supported formats: 3.5 inch, 720 Kbyte - 1.44 Mbyte
• Enhanced EIDE/ATAPI	PCI EIDE/ATAPI interface with up to 33 MB/s transfer rate, for two devices. 32 byte data buffer for 132 Mbyte/sec PCIbus burst transfers
• Serial I/O	Up to four async. 16550 compatible channels with 16 byte FIFO Transfer rates up to 115.2 Kbaud
• Parallel I/O	Two fully bi-directional IEEE 1284 enhanced parallel port support ECP and EPP modes
• VME bus	Tundra Universe-II Industry standard CA91C142 Universe-II PCI to VMEbus controller Full VMEbus system controller 20 Mbytes/sec transfer rate FIFOs for write posting, DMA controller with linked list support
• PMC extension slot	32-bit PCIbus interface with front panel I/O
• Temperature Sensor	Software readable in 0.5 °C increments from -55 to +125 °C
• EEPROM	Serial EEPROM for non-volatile user data
• Frontpanel I/O	VGA, 10/100baseTX, keyboard, mouse, 2xUSB, reset/NMI switch, COM1,2,3,4, LPT1, LPT2 or LCD connector, LED
• Backpanel I/O	SCSI, FDC, speaker, reset, watchdog, Transition Module for 1:1 PC compatible connectors available

1.2 Board Types

There are many versions of the CP7 board available. Please contact SBS Technologies for more info and a approriate solution for your needs.

1.3 Specification

- **PCB** FR4 Multilayer
- **Size** Total size: 6U, occupying 2 VME slots,8 TE
- **Dimensions** 160.93 mm x 233.35 mm without front panel
- **Weight:** max 1000 g
- **Battery**: onboard Lithium battery CR2450 for a expected lifetime of at least 10 years (45ºC)
- **Power Consumption**

The table below helps customers calculate the power consumption of each VP7 system. For measurement, the VP7 is mounted on a VME backplane, without keyboard and hard disk. The operating system (MSDOS) comes up from floppy disk. During measurement, the power consumption of the backplane and the floppy drive can be ignored.

Typical Current in A (+5V)		Description
With Power-Management	Without Power-Management	
2.2A	4.5A	Pentium II 350 MHz
2.3A	5.6A	Pentium III 500 MHz
1.9A	4.0A	Celeron 300 MHz
1.9A	4.1A	Celeron 333 MHz
2.1A	4.7A	Celeron 400 MHz
1.7A	2.8A	Mobile Pentium III 500MHz
1.8A	3.2A	Mobile Pentium III 700MHz
1.9A	5.0A	Pentium III 850MHz
2.6A	6.6A	Pentium III 1000MHz (D-Step, 1.75V)

☞ For keyboard connected add 100 mA (typical value)

☞ Fused VCC (+5V)

The following connectors provide a fused VCC voltage (+5V):
P1700(USB), P2000(KBD), P2001(Mouse), P2100(LPT1), P2600(LPT2), P2302(COM2), P4200(VGA), P2700(COM3), P2701(COM4)
The total current drawn from this VCC voltage may not exceed 1.5 Amperes.

The methods for measurements are defined as follows:

DOS prompt with power management :

BOOT disk with DOS 6.22
config.sys: device=power.exe adv, no autoexec.bat
wait until CPU enters HLT state
measure current on DOS prompt

DOS prompt without power management:

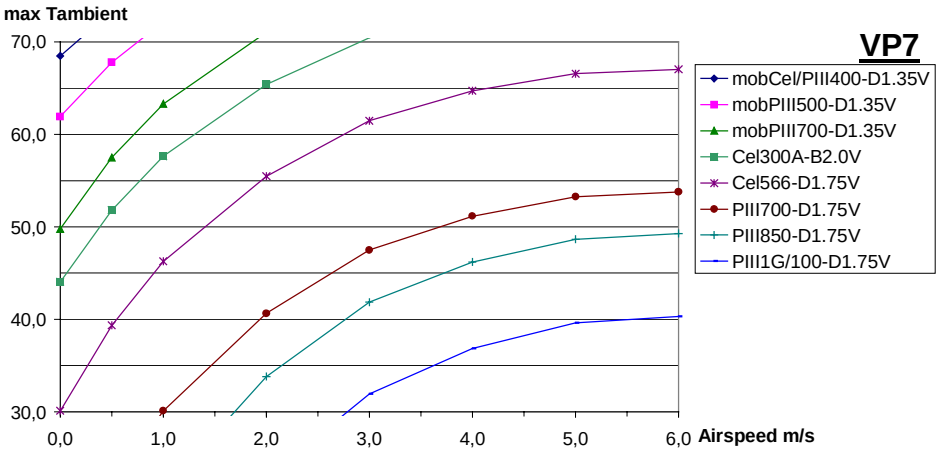
BOOT disk with DOS 6.22
config.sys: device=power.exe off, no autoexec.bat
measure current on DOS prompt

Environment	C-Style	I-Style

High Temperature [°C]

Storage: +70 +85

For the required airflow at a planned operating temperature, please check following diagram:



Low Temperature [°C]

Storage	-40	-40
Operating	+0	-40

Rel. Humidity

Storage	up to 95 %, 40°C non-condensing
Operating	up to 95 %, 40°C non-condensing

Vibration

Spectrum	5 to 100 Hz	5 to 100 Hz
Acceleration	2 g	2 g

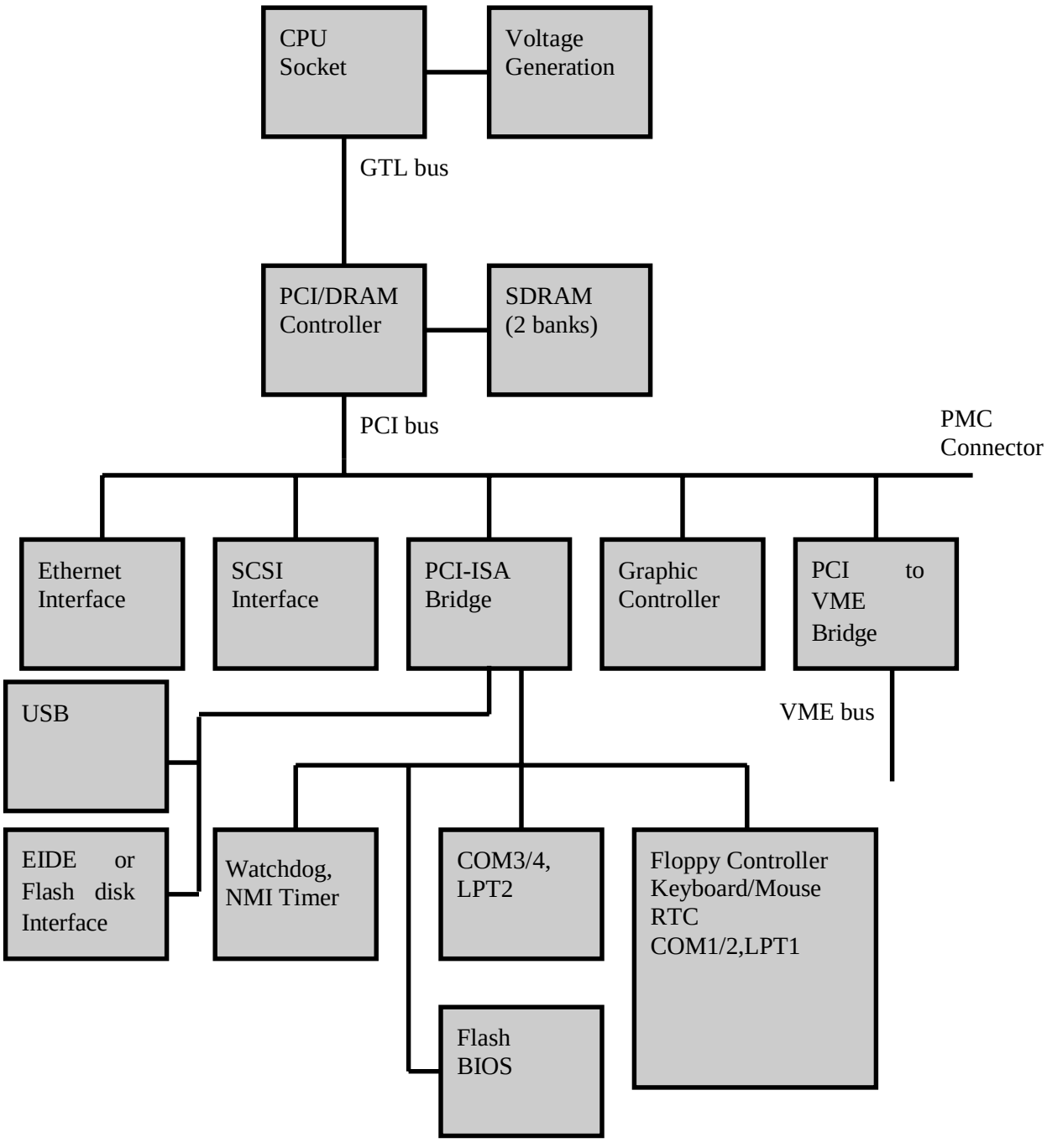
Shock

Amplitude	12 g	12 g
Duration	6 ms	6 ms

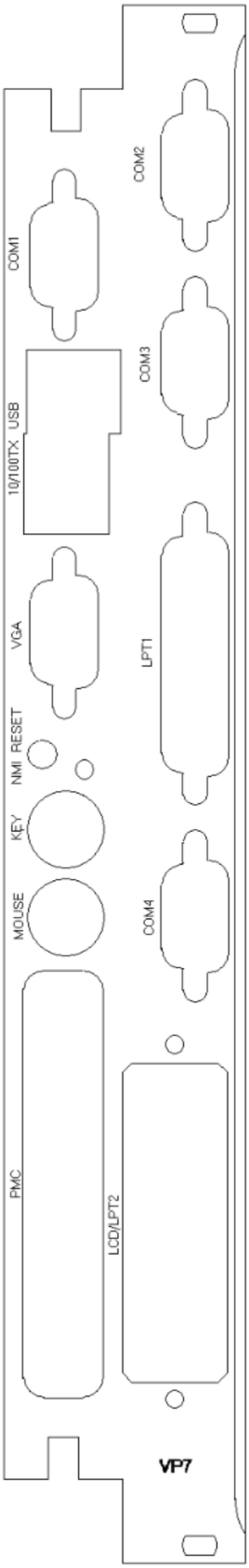
2 Hardware Installation

The VP7 is a fully IBM-AT compatible stand-alone PC. It is equipped with all functions a conventional Personal Computer can only offer with several add-on cards. Extension boards can be connected via the VME interface. The minimized board size and the large number of interfaces and functions enable the VP7 for use in many applications.

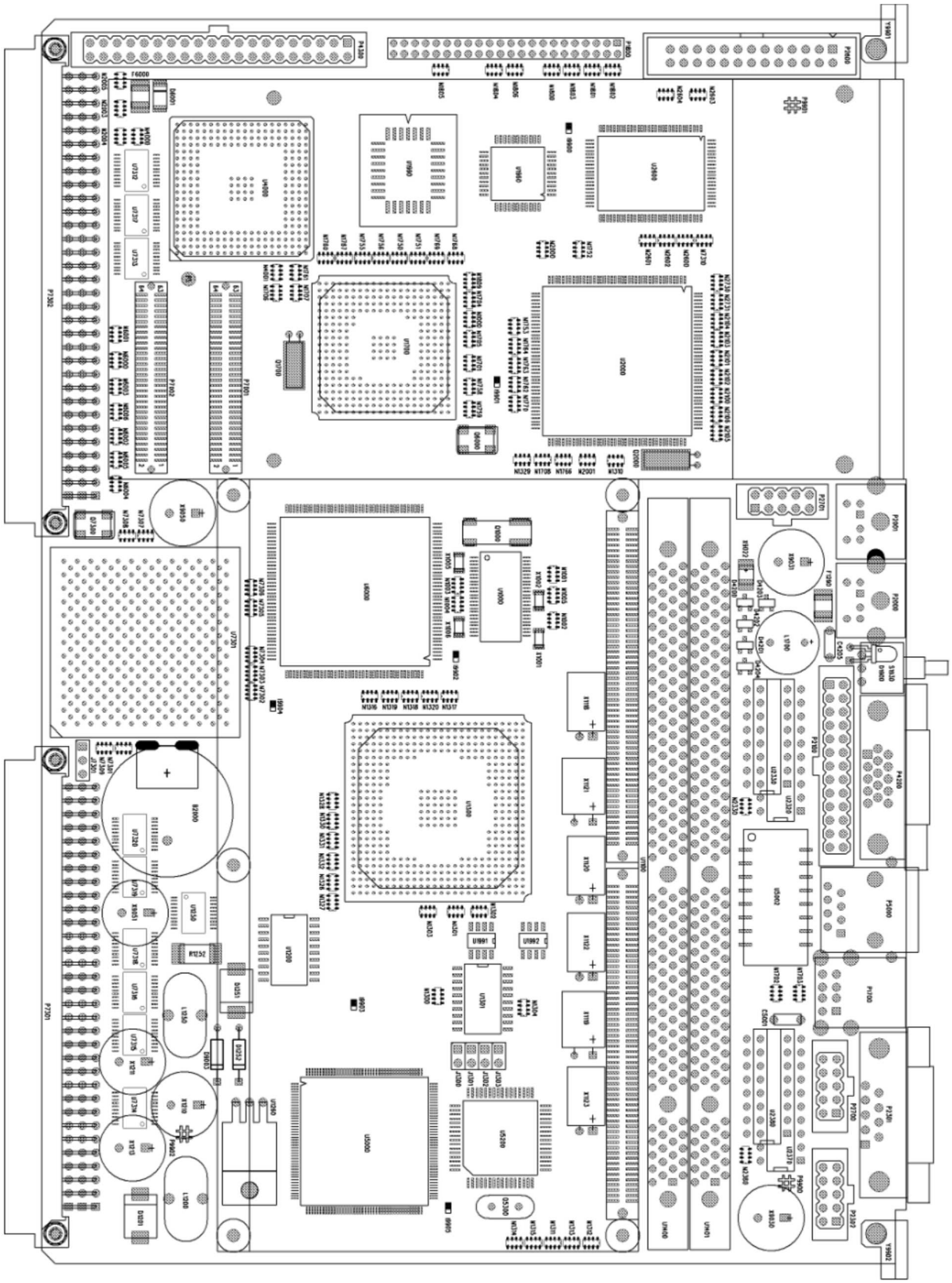
2.1 Block Diagram



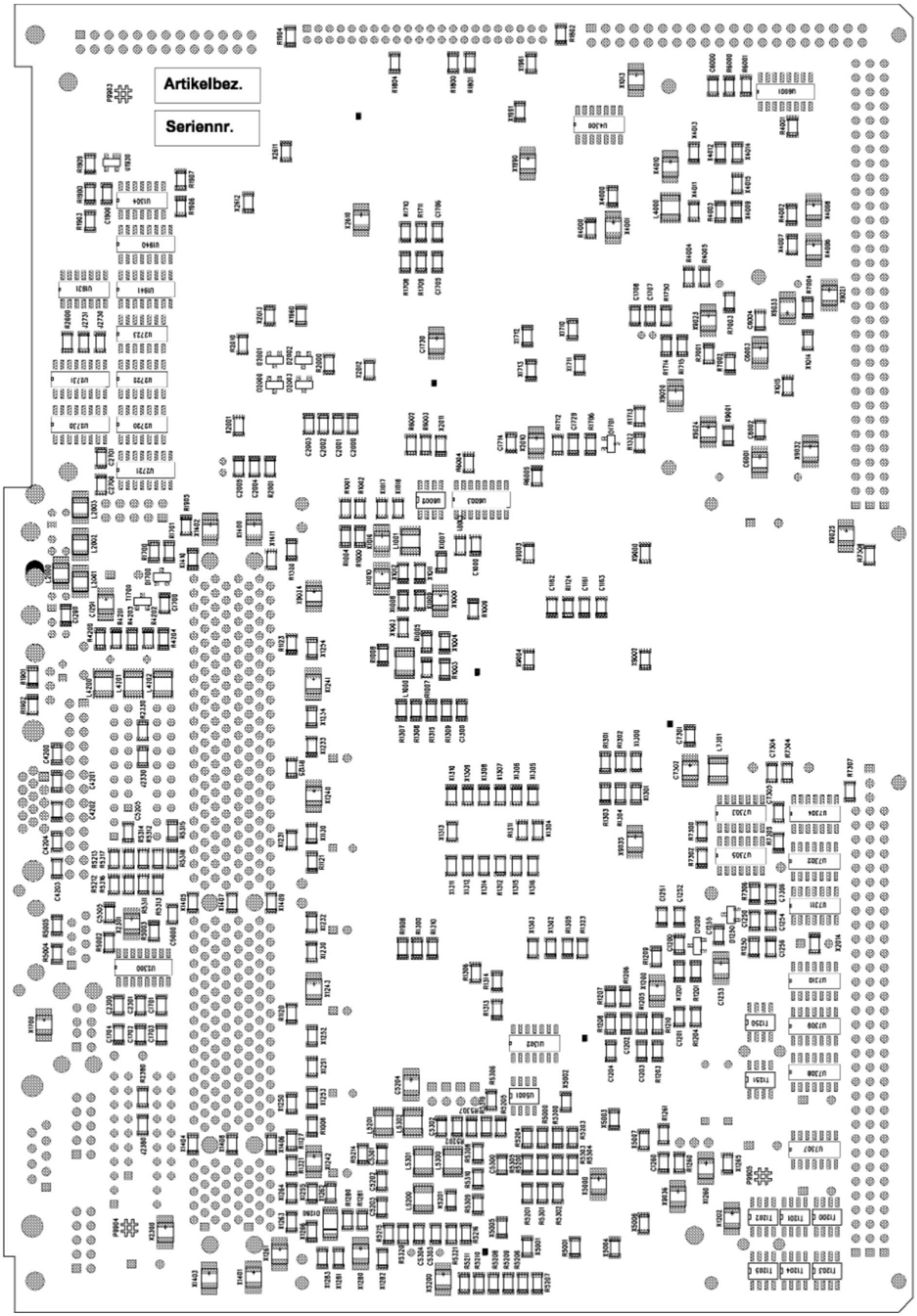
2.2 Front Panel



2.3 Placement Plan Component Side



2.4 Placement Plan Solder Side



2.5 Socket Installation

This chapter describes the user configurable sockets which are visible in the placement plan.

2.5.1 Memory

The VP7 offers two sockets for 168-pin compatible memory modules called SDRAM DIMMs. These sockets are U1400 and U1401. The VP7 supports Parity and ECC (Error Detection and Correction) when using 72-bit wide (ECC-) SDRAM DIMMs.

☞ The VP7 requires using SDRAM DIMMs with access time of 8 ns or faster compliant to PC100 specification.

2.5.2 Serial Port Configuration for COM1 and COM2

The serial ports COM1 and COM2 are user configurable for either RS232 or RS422 operation. Operation mode is selected by installing the appropriate transceiver in the corresponding socket.

	COM1 RS232	**COM1 RS422**	**COM2 RS232**	**COM2 RS422**
U2320	X			
U2330		X		
U2370			X	
U2380				X

U2320, U2370 = SN75C185
U2330, U2380 = SN75C1167

2.6 Jumper Configuration

The only user accessible jumper of the VP7 is J7301. This jumper defines the strategy for VME bus resets.

J7301 1-2	VME bus reset (SYSRES*) generated only when Universe chip is setup for VME bus system controller. If the VP7 is not set as system controller, a reset will only affect on the VP7 board. ☞ In this setting the SYSRES* signal has no steady state at low state. During pressed reset button the SYSRES* is inactive after releasing of the reset button the reset line will toggle for 270ms with a frequency of 1MHz. This is caused by the Universe chip. Please check if the used VME cards can tolerate such SYSRES* signal waveform.
J7301 2-3	VME bus reset is generated by Power On or Reset button (factory default setting).
J7301 open	VME bus reset is never generated.

System controller:
As specified by the VME64 specification the First Slot Detector module on the Universe VME controller samples BG3IN* immediately after reset to determine whether the Universe's host board resides in slot 1. The VMEbus specification requires that BG[3:0]* lines be driven high after reset. This means that if a card is preceded by another card in the VMEbus system, it will always sample BG3IN* high after reset. BG3IN* can only be sampled low after reset by the first card in the system (there is no preceding card to drive BG3IN* high). If BG3IN* is sampled at logic low immediately after reset (due to the Universe's internal pull-down), then the Universe's host board is in slot 1 and the Universe becomes system controller. This mechanism may be overridden by the system BIOS setup.

2.7 Connectors

2.7.1 VME bus Connector P1 (P7301)

The following table lists the pin assignments of connector P7301. The connector is compatible to the P1 connector of the VME bus specification ANSI/IEEE STD 1014-1987 and IEC 821 and 297.

	a	b	c
1	D00	BBSY*	D08
2	D01	BCLR*	D09
3	D02	ACFAIL*	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	SYSFAIL*
11	GND	BG3OUT*	BERR*
12	DS1*	BR0*	SYSRESET*
13	DS0*	BR1*	LWORD*
14	WRITE*	BR2*	AM5
15	GND	BR3*	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	N.C.	A17
22	IACKOUT*	N.C.	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	-12V	+5V STDBY	+12V
32	+5V	+5V	+5V

If the ACFAIL* function is not served by the power supply, ACFAIL* should be strapped to V_{CC} on the VME bus backplane to avoid spurious interrupts caused by cross talking.

2.7.2 VME bus Connector P2 (P7302)

The following table lists the pin assignments of connector P2. The b row of the connector is compatible to the P2 connector of the VME bus specification ANSI/IEEE STD 1014-1987 and IEC 821 and 297.

	a	b	C
1	\S_D10	+5V	\S_D11
2	\S_D08	GND	\S_D09
3	\S_REQ	Reserved	\S_IO
4	\S_SEL	A24	\S_C/D
5	\S_RST	A25	\S_MSG
6	\S_BUSY	A26	\S_ACK
7	\S_ATN	A27	GND
8	\S_DP0	A28	S_TERMPW
9	\S_D06	A29	\S_D07
10	\S_D04	A30	\S_D05
11	\S_D02	A31	\S_D03
12	\S_D00	GND	\S_D01
13	\S_D15	+5V	\S_DP1
14	\S_D13	D16	\S_D14
15	GND	D17	\S_D12
16	N.C.	D18	N.C.
17	N.C.	D19	N.C.
18	N.C.	D20	N.C.
19	N.C.	D21	N.C.
20	N.C.	D22	N.C.
21	N.C.	D23	N.C.
22	N.C.	GND	N.C.
23	N.C.	D24	N.C.
24	N.C.	D25	N.C.
25	SPEAKER	D26	\RST_BUT
26	GND	D27	WDG_REL
27	\FD_RDAT	D28	\FD_HDSL
28	\FD_TRK0	D29	\FD_WPRT
29	\FD_WDAT	D30	\FD_WGAT
30	\FD_DIR	D31	\FD_STEP
31	\FD_DCHG	GND	\FD_MTR0
32	\FD_INDX	+5V	\FD_DRV0

☞ Do not connect anything to **Reserved Pins!**

Signal groups for I/O signals:

floppy disk controller signals : \FD....
SCSI signals: \S_... and S_....
Misc signals: \SPEAKER,WDG_REL,\RST_BUT

2.7.3 PMC (P7001, P7002)

The following table lists the pin assignments of the PMC connector.

Pin #	P7001	P7002	Pin #	P7001	P7002
01	N.C.	+12V	33	/FRAME	GND
02	-12V	NC	34	GND	RES.
03	GND	NC	35	GND	/TRDY
04	/INTD	NC	36	/IRDY	+3.3V
05	/INTA	NC	37	/DEVSEL	GND
06	/INTB	GND	38	Vcc	/STOP
07	N.C.	GND	39	GND	/PERR
08	Vcc	RES.	40	/LOCK	GND
09	/INTC	RES.	41	SDONE	+3.3V
10	RES.	RES.	42	/SBO	/SERR
11	GND	Vcc	43	PAR	C/BE1
12	RES.	+3.3V	44	GND	GND
13	PCLK_PMC	/PCIRST	45	Vcc	AD14
14	GND	GND	46	AD15	AD13
15	GND	+3.3V	47	AD12	GND
16	/GNT0	GND	48	AD11	AD10
17	/REQ0	RES.	49	AD9	AD8
18	Vcc	GND	50	Vcc	+3.3V
19	Vcc	AD30	51	GND	AD7
20	AD31	AD29	52	C/BE0	RES.
21	AD28	GND	53	AD6	+3.3V
22	AD27	AD26	54	AD5	RES.
23	AD25	AD24	55	AD4	RES.
24	GND	+3.3V	56	GND	GND
25	GND	AD20	57	Vcc	N.C.
26	C/BE3	AD23	58	AD3	N.C.
27	AD22	+3.3V	59	AD2	GND
28	AD21	AD20	60	AD1	GND
29	AD19	AD18	61	AD0	/ACK64
30	Vcc	GND	62	Vcc	+3.3V
31	Vcc	AD16	63	GND	GND
32	AD17	C/BE2	64	/REQ64	RES.

N.C. Not connected
RES. Reserved. Do not connect anything!
+12V/-12V Only available if connected to VME bus backplane.

2.7.4 Hard Disk Connector (P1800)

The hard disk connector is designed as a 44-pin 2mm pitch connector to connect a 2.5” IDE hard disk or FlashDisk.

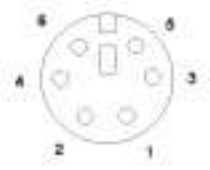
PIN	SIGNAL	PIN	SIGNAL
1	\RST_DRV	2	GND
3	HD_D7	4	HD_D8
5	HD_D6	6	HD_D9
7	HD_D5	8	HD_D10
9	HD_D4	10	HD_D11
11	HD_D3	12	HD_D12
13	HD_D2	14	HD_D13
15	HD_D1	16	HD_D14
17	HD_D0	18	HD_D15
19	GND	20	n.c.
21	HD_DRQ0	22	GND
23	\HD_IOW	24	GND
25	\HD_IOR	26	GND
27	HD_RDY	28	n.c.
29	HD_DAK0	30	GND
31	HD_IRQ	32	n.c.
33	HD_A1	34	n.c.
35	HD_A0	36	HD_A2
37	\HD_CS1	38	\HD_CS3
39	n.c.	40	GND
41	+5V	42	+5V
43	GND	44	n.c.

☞ Pin 1 is marked on the PCB.

2.7.5 PS/2 Mouse Interface (P2001)

The VP7 provides a standard 6-pin MINI-DIN connector for PS/2 compatible mouse.

Name	
Mouse Data	1
GND	3
FUSE_VCC	4
Mouse Clk	5
not connected	2,6

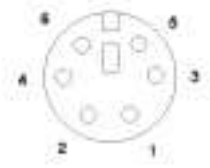


☞ The maximum load for FUSE_VCC (+5V) is **300 mA**.

2.7.6 Keyboard Interface (P2000)

The VP7 provides a standard 6-pin MINI-DIN connector for a compatible keyboard.

Name	
Keyb. Data	1
GND	3
FUSE_VCC	4
Keyb. Clk	5
not connected	2,6

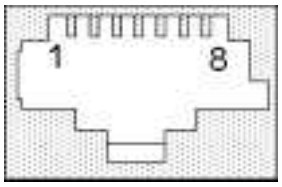


☞ The maximum load for FUSE_VCC (+5V) is **300 mA**.

2.7.7 Ethernet Interface 10BaseT and 100BaseTX (P5000)

The Ethernet interface requires usage of CAT 5 cable which contains separate transmit and receive pairs for proper operation with 100BaseTX. For operation with 10BaseT, a CAT 3 cable or better is required.

Name	P5400
TXD+	1
TXD-	2
RXD+	3
BIAS1	4
BIAS1	5
RXD-	6
BIAS2	7
BIAS2	8



BIAS1 and BIAS2 are the center tabs of the input and output transformers.

2.7.8 Parallel Interfaces LPT1 (P2100, P2600)

Parallel port 1 is connected to a standard 25-pin female D-Sub connector on the front panel. The D-Sub connector is wired to an onboard 2 x 13 header (P2100).

Name	**LPT1 P2100** (2x13 pin header)	**LPT1 P2100 Front Panel** Connector (25-pin female D-Sub)	**LPT2 P2600** (2x13 pin header)	**LPT2 P2600 Front Panel** Connector (25-pin female D-Sub)
\Strobe	1	1	1	1
D0	3	2	3	2
D1	5	3	5	3
D2	7	4	7	4
D3	9	5	9	5
D4	11	6	11	6
D5	13	7	13	7
D6	15	8	15	8
D7	17	9	17	9
\ACK	19	10	19	10
BUSY	21	11	21	11
PE	23	12	23	12
SLCT	25	13	25	13
\AUTOFEED	2	14	2	14
\ERROR	4	15	4	15
\INIT	6	16	6	16
\SLCTIN	8	17	8	17
GND	10,12,14,16,18, 20,22,24	18,19,20,21,22,23, 24,25	10,12,14,16,18,20, 22,24	18,19,20,21,22,23, 24,25
FUSE_VCC	26	-	26	-

☞ The maximum load for FUSE_VCC (+5V) is **100 mA** each.

2.7.9 Serial Interfaces (P2301, P2302, P2700, P2701)

The VP7 offers four serial ports, two are optional (COM3 and COM4). COM1 and COM2 have socketed line drivers configured for RS232 and can be reconfigured for RS422 by the user. COM3 and COM4 can be ordered with RS232 or RS422 transceivers. COM1,COM2,COM3 and COM4 are accessible via the front panel connectors which are D-Sub type.

Name (RS232)	**Name (RS422)**	**Onboard 2x5-pin headers for COM1..4**	**Front Panel COM1..4**
\DCD	-TXD	1	1
\DSR	+TXD	2	6
RXD	-RTS	3	2
\RTS	+RTS	4	7
TXD	+CTS	5	3
\CTS	-CTS	6	8
\DTR	+RXD	7	4
\RI	-RXD	8	9
GND		9	5
FUSE_VCC		10	-

☞ The maximum load for FUSE_VCC (+5V) is **100 mA** each.

2.7.10 VGA Interface (P4200)

The monitor signals are available at the front panel on a standard 15-pin female D-Sub connector.

Name	**P4200**
RED	1
GREEN	2
BLUE	3
HSYNC	13
VSYNC	14
DDC-Data	12
DDC-Clock	15
FUSE_VCC	9
GND	5, 6, 7, 8, 10
NC	4, 11

☞ The maximum load for FUSE_VCC (+5V) is **300 mA**.

2.7.11 USB Interface (P1700)

Two USB channels are available at the front panel.

Name	P1700
FUSE_VCC	1
USB0-	2
USB0+	3
GND	4
FUSE_VCC	5
USB1-	6
USB1+	7
GND	8

☞ The maximum load for FUSE_VCC (+5V) is **500 mA**.

2.7.12 LCD Interface (P4300)

For operation with monochrome and color displays an onboard 2 x 20 pin header is available. The signals on this header are connected to a 36-pin Centronics connector on the Front Panel.

Name	P4300 (Centronics Connector)	P4300 (2x20-pin onboard header)	Name	P4300 (Centronics Connector)	P4300 (2x20-pin onboard header)
not connected	36	-	not connected	18	-
C2_TXD	35	1	C2_RXD	17	2
KCLK	34	3	KDATA	16	4
\LC_VCC	33	5	LC_VEE	15	6
LC_BACKL	32	7	LC_DE	14	8
GND	31	9	LC_P04	13	10
LC_P03	30	11	LC_P02	12	12
LC_P01	29	13	LC_P00	11	14
LC_P17	28	15	GND	10	16
LC_P10	27	17	LC_P09	9	18
LC_P08	26	19	LC_P07	8	20
LC_P06	25	21	LC_P05	7	22
GND	24	23	LC_P15	6	24
LC_P14	23	25	LC_P13	5	26
LC_P12	22	27	LC_P11	4	28
LC_P16	21	29	GND	3	30
LC_VSYNC	20	31	LC_HSYNC	2	32
LC_CLK	19	33	GND	1	34
LC_P18	-	35	LC_P19	-	36
LC_P20	-	37	LC_P21	-	38
LC_P22	-	39	LC_P23	-	40

2.8 Memory Map

The table below shows the memory address area used by the VP7.

Start address (in hexadecimal)	used by	Size
0000 0000	DRAM	640 Kbytes
000A 0000	Video RAM	128 Kbytes
000C 0000	PCI BIOS ROMs (Video, SCSI, Ethernet etc.)	128 Kbytes
000E 0000	System BIOS	128 Kbytes
0010 0000	Extended Memory	depending on DRAM size
8000 0000	PCI devices	
FFFF 8000	BIOS Extension	256 Kbytes
FFFF C000	System BIOS	256 Kbytes

2.9 Register Set

The following chapter provides an overview of the registers located in the I/O address area of the VP7.

☞ The address location of PCI devices such as SCSI or Ethernet are not described in the following tables because the System BIOS automatically configures (PnP, Plug and Play) each PCI device to avoid address conflicts. Many device drivers show the actual address locations after installation and loading.

2.9.1 Standard Register Set

The standard register set is equal to all standard PC/AT systems. The table below provides an overview of the address ranges occupied by these registers.

I/O Address Range (Hex)	Function
0000 - 000F	DMA Controller 1
0020 - 0021	Interrupt Controller 1
0040 - 0043	Counter/Timer
0060	Keyboard Controller
0061	NMI Status and Control
0064	Keyboard Controller
0070 - 0071	RTC, NMI Mask
0080 - 008F	DMA Page register
00A0 - 00A1	Interrupt Controller 2
00B2 - 00B3	Power Management
00C0 - 00DE	DMA Controller 2
00F0 - 00F1	Coprocessor
01F0 - 01F7	EIDE/ATAPI
0278 - 027F	LPT [1)]
02E8 - 02EF	COM4 [2) 1)]
02F8 - 02FF	COM2 [1)]
0378 - 037F	LPT [1)]
03BC - 03BF	LPT [1)]
03C0 - 03DA	Graphic Controller
03E8 - 03EF	COM3 [2) 1)]
03F2 - 03F7	Floppy, EIDE/ATAPI
03F8 - 03FF	COM1 [1)]

☞ [1)]Via setup three address ranges can be defined for up to two parallel interfaces and four address ranges for four serial interfaces.
[2)]These I/O addresses are only used by optional devices.

2.9.2 Extended Register Set

The extended register set is specific to the VP7. To protect the system against illegal register accesses, the extended register set can be locked by using the LOCKR register.

I/O Address Range (Hex)	Name	Function
0160	WCR	Watchdog Control Register
0161	NMITCR	NMI Timer Control Register
0162-0167		Reserved
0168	LEDCR	LED Control Register
0169	LOCKR	Lock Register
0861	-	NMI Timer Recharge

A detailed description of the registers above can be found in the chapter Additional features / Extended registers of the manual and in "SBS Tech. Onboard I/O (Plug & Play capable systems) Programmers Manual" (M_PGM_IOPNPSYS).

2.9.3 Interrupts

The interrupt routing for standard components such as COM1/2, LPT1, ... is in compliance with standard PC/AT systems. Unused interrupts can be used for add-on cards or other board specific PCI devices such as SCSI and Ethernet.

Hardware IRQ		IRQ Source
INTC1	IRQ00	System Timer
	IRQ01	Keyboard
	IRQ02	Cascade from INTC2
	IRQ03	COM2 [1)]
	IRQ04	COM1 [1)]
	IRQ05	LPT2 [1)]
	IRQ06	Floppy Disk Controller
	IRQ07	LPT1 [1)]
INTC2	IRQ08	Real Time Clock
	IRQ09	unused
	IRQ10	COM4 [1)]
	IRQ11	COM3 [1)]
	IRQ12	PS/2 Mouse [2)]
	IRQ13	Numeric Coprocessor
	IRQ14	Flash disk
	IRQ15	unused
NMI	IOCHCK	NMI-Timer Reset Switch
	Parity Error, ECC Error, System Error	Memory Controller

☞ [1)] This interrupt is available when no ISR (Interrupt Service Routine) is installed.

[2)] This interrupt is available when PS/2 mouse is not connected.

2.9.4 DMA

The DMA routing for standard components such as floppy and parallel port is in compliance with other PC/AT systems.

DMA Channel		DMA Source
DMAC1	Channel 0	unused
	Channel 1	LPT2 in ECP mode
	Channel 2	Floppy Disk Controller
	Channel 3	LPT1 in ECP mode
DMAC2	Channel 4	Cascade from DMAC1
	Channel 5	Unused
	Channel 6	Unused
	Channel 7	Unused

3 Function Blocks

3.1 Standard AT-Devices

3.1.1 DMA Controller

In standard AT compatible PCs, as well as on the VP7 two DMA controllers integrated on the board are internally cascaded. Both controllers are compatible with the Intel 8237A. The DMA Controller 1 (DMAC1) is used for byte-wide transfers while the DMAC2 is used for word-wide transfers.

3.1.2 Interrupt Controller

The Interrupt controller on a standard PC consists of two 82C59A devices with eight interrupt request lines each. The two controllers are cascaded to provide 14 external and two internal interrupt sources.

The master interrupt controller provides IRQ[7..1] and the slave interrupt controller provides IRQ[15..8]. IRQ2 is used to cascade the two controllers, IRQ0 is used as a system timer interrupt and is tied to interval timer 1, counter 0. The remaining 14 interrupt lines are mapped to various onboard devices.

Each 82C59A provides several internal registers. The interrupts at the IRQ input lines are handled by two registers, the interrupt request register IRR and the in-service register ISR. For programming details see the 82C59A data sheet.

3.1.3 Timer

Standard PCs as well as the VP7 are equipped with a 8254 compatible timer. This timer contains three counters. Each counter output provides a key system function. Counter 0 is connected to interrupt controller input IRQ0 and provides a system timer interrupt for time-of-day, floppy disk timeout and other system timing functions. Counter 1 generates a refresh request signal and Counter 2 generates the sound for the speaker. The following table gives an overview of the 8254 functions.

Interval Timer Functions	
Function: Gate: Clock In: Out:	Counter 0 (System Timer) Always On 1.193 MHz(OSC/12) IRQ0 (INT1)
Function: Gate: Clock In: Out:	Counter 1 (Refresh Request) Always On 1.193 MHz(OSC/12) Refresh Request
Function: Gate: Clock In: Out:	Counter 2 (Speaker Tone) Programmable via Port $061 1.193 MHz(OSC/12) Speaker

The counter/timers are programmed by I/O accesses. A single control word register controls the operation of all three counters. The register map is shown in the following table:

I/O Address	**Access Type**	**Function**	**Name**
$0040	W	Write Initial Count to Counter 0	WIC0
$0041	W	Write Initial Count to Counter 1	WIC1
$0042	W	Write Initial Count to Counter 2	WIC2
$0043	W	Write Control Word	WCW
$0040	R	Read Status of Counter 0	RSC0
$0041	R	Read Status of Counter 1	RSC1
$0042	R	Read Status of Counter 2	RSC2
$0043	R	no function	

For more information on programming and a more detailed register description see the 8254 data sheet.

3.1.4 Real Time Clock

The RTC is a low-power clock that provides a time-of day clock and a 100-year calendar with alarm features and battery backed operation. The time-of-day function includes 14 control registers. Other features include maskable interrupt sources and 242 byte of general purpose CMOS RAM. Valid RAM data and time can be maintained after power down through the use of an external battery source. The RTC is software compatible to the Dallas DS1287 and the Motorola MC146818. The RTC function is mapped to I/O locations $70 (index) and $71 (data).

The table below shows the address location of the clock registers in the battery backed RAM area.

Name	Adr. (Index)	Length
current second in BCD	$00	1
second alarm in BCD	$01	1
current minute in BCD	$02	1
minute alarm in BCD	$03	1
current hour in BCD	$04	1
hour alarm in BCD	$05	1
current day of week in 1-7 (1=sunday)	$06	1
current day of month in 1-31 BCD	$07	1
current month in 1-12 BCD (1=January)	$08	1
current year in BCD (00=1900)	$09	1
control register A	$0A	1
control register B	$0B	1
control register C	$0C	1
control register D	$0D	1
BCD value for current century (19 or 20)	$032	1

Apart from the RTC information the RAM also contains system information as listed below:

Name	Adr. (Index)	Length
AT errors	$0E	1
shutdown status byte	$0F	1
diskette drive types	$10	1
fixed disk types	$12	1
equipment byte	$14	1
amount of base memory	$15	2
expansion memory	$17	2
extended fixed disk type	$19	2
Checksum	$2E	2

The general purpose CMOS RAM is reserved and must not be changed. Any change of the reserved RAM area may result in undesirable functionality of the system.

The RTC is addressable via the two registers listed below:

	7	6	5	4	3	2	1	0
RTCADD	NMIM	ADDR[6..0]						

I/O RTC Address Register

070_w NMIM NMI Mask. When set, the NMI is disabled.

ADDR[..] Address selection. This bit field defines the address location within the CMOS RAM for all consecutive accesses to the RTC Data register RTCDAT.

	7	6	5	4	3	2	1	0
RTCDAT	Data[7..0]							

I/O RTC Data Register

$071 DATA[..] This register allows access to the CMOS RAM at the location previously defined in the ADDR[..] field of the RTC address register RTCADD.

Note that writing to RTCADD must preserve the status of the NMIM bit in the RTCADD register.

3.2 Keyboard and Mouse Controller

The communication between the PC and the keyboard is managed by a device compatible to the Intel 8042 microcontroller, which also provides the PS/2 mouse interface.
The functions of this device are I/O mapped and communicate with the chip set via two ports:

Adr.	**Description**	**Command**
$060	Output buffer	Read
$060	Input buffer	Write
$064	Status register	Read
$064	Command register	Write

3.3 EIDE/ATAPI Interface

The VP7 offers one EIDE/ATAPI Interfaces. The device is logically connected to the primary PCI bus. Therefore a high data transfer rate is achievable. The signals of the EIDE interface are available at the connector P1800.

The registers used for the primary EIDE interface are I/O-mapped as shown below

Address	Name	Function
$01F0	Data Register	Read/Write
$01F1	Error Register	Read only
$01F1	Write Command Register	Write only
$01F2	Sector Count Register	Read/Write
$01F3	Sector Number Register	Read/Write
$01F4	Cylinder Number Register LSB	Read/Write
$01F5	Cylinder Number Register MSB	Read/Write
$01F6	Drive Head Register	Read/Write
$01F7	Status Register	Read only
$03F6	Fixed Disk Register	Write only
$03F7	Digital Input Register Def.	Read only

The VP7 System BIOS automatically detects a connected EIDE HDD or flash disk and enters the corresponding drive parameters into the BIOS setup. This feature allows faster and easier handling of varying types of EIDE hard disks. At the EIDE interface two hard disks can be connected. In this case one HDD must be configured as master and the other one as slave. Read the hard disk manual to find out where these jumpers are located on your drive. The optional flash disk is connected to an EIDE connector too.

Using EIDE and SCSI devices.
MS-DOS 6.22 can handle up to seven hard disks. The PC allows the simultaneous use of EIDE and SCSI hard disks. In BIOS setup, you can select whether to boot from the first EIDE or the first SCSI device.

☞ For correct operation of the EIDE interface, a maximum cable length of 8 inch (20 cm) must not be exceeded.

3.4 Serial Interfaces

The VP7 serial ports are fully compatible with the NS16450 and NS16550. This means that each serial interface provides a 16 byte FIFO and therefore offers a higher performance than earlier used standard serial interfaces. The UARTs have programmable baud rate generators capable of 50 to 115200 baud. There are four address locations defined for serial interfaces on standard PCs. The serial interfaces are I/O mapped and can occupy the following address ranges:

Name	Address
COM1	$03F8 - $03FF
COM2	$02F8 - $02FF
COM3	$03E8 - $03FF
COM4	$02E8 - $02FF

Each serial channel provides an identical register set as shown in the table below:

Address Offset	Divisor Latch Bit 1	Name
$00	0	Receiver Buffer (Read) Transmitter Holding (Write)
$01	0	Interrupt Enable
$02	0	Interrupt Identification (Read) FIFO Control (Write)
$03	x	Line Control
$04	x	Modem Control
$05	x	Line Status
$06	x	Modem Status
$07	x	Scratch register
$00	1	Divisor Latch (LSB)
$01	1	Divisor Latch (MSB)

3.5 Parallel Interfaces

The parallel ports are fully compatible with the new IEEE 1284 standard, including level 2 support. The parallel port consists of an Enhanced Parallel Port (EPP1.7/1.9) and an Extended Capabilities Port (ECP 16Byte FIFO + DMA support). The new modes allow higher transfer rates up to 1 Mbyte/s. Via BIOS Setup, the operating modes of the parallel interface can be selected.
The following modes are supported:

Mode	Average transfer rate (Read)	Average transfer rate (Write)
Standard	100 Kbyte/s	200 Kbyte/s
EPP	1 Mbyte/s	1 Mbyte/s
ECP	1 Mbyte/s	1 Mbyte/s

On a standard PC, three address areas are defined for a parallel interface. The parallel interface is I/O-mapped to one of the following addresses:

Name	Address
LPT1	$03BC
LPT2	$0378
LPT3	$0278

The address range $3BC cannot be used with EPP operation.

Each parallel channel provides the identical register set shown in the table below.

Address Offset	Standard	EPP	only important for ECP Mode # ECR(5-7)	ECP
$000	Data (R/W)	Data(R/W)	000,001	Data Register(R/W)
$000	"	"	011	
$001	Status(R)	Status(R)	ALL	ECP Address FIFO(W)
$002	Control(R/W)	Control(R/W)	ALL	Status Register(R)
$003		Address(R/W)		Control Register(R/W)
$004		Data Port 0 (R/W)		
$005		Data Port 1 (R/W)		
$006		Data Port 2 (R/W)		
$007		Data Port 3 (R/W)		
$400			010	Parallel Port Data FIFO(W)
$400			011	ECP Data FIFO(R/W)
$400			110	Test FIFO(R/W)
$400			111	Configuration Register A(R)
$401			111	Configuration Register B(R)
$402			ALL	Ext. Control Register(R/W)

3.6 Floppy Controller

The VP7 floppy controller is fully compatible with the PC8477, containing a superset of the NEC µPD72065B and the N82077.

The following formats are supported:

Format	Disk Size	Disk Media	formatted Tracks
720 Kbyte	3.5	Double Density 96 tpi	80
1.44 Mbyte	3.5	High Density 135 tpi	80

The floppy controller uses various I/O addresses in the PC I/O address space. The table below summarizes the standard floppy controller registers:

Address	Name	Function
$03F2	Digital Output Register	Write only
$03F4	Main Status Register	Read only
$03F5	Data Register	Read/Write
$03F7	Configuration Control Register	Write only

3.7 Graphics Controller

3.7.1 Features

Here are the major features of the Chips and Technology 69000 graphic controller chip.

- Highly integrated Flat Panel and CRT GUI, max. Pixel clock 135 MHz
- Accelerator & Multimedia Engine, Palette/DAC, Clock Synthesizer, and integrated frame buffer
- Integrated High Performance SDRAM memory
  • 2MB integrated memory, 83 MHz SDRAM operation
- Hardware Windows Acceleration
  • 64-bit Graphics Engine with 2D acceleration
- Hardware Multimedia Support
- Display centering and stretching features for optimal fit of VGA graphics and text on 800x600 and 1024x768 panels
- PCI Bus with Burst Mode capability
- Flat Panel modes

horizontal x vertical	**maximum bit per pixel**
640x480	24 bpp
800x600	24 bpp
1024x768	16 bpp
1280x1024	8 bpp
1600x1200	4 bpp

- CRT modes

horizontal x vertical	**max number of bits per pixel**	**vertical refresh rate**
640x480	24	60, 75, 85
800x600	24	60, 75, 85
1024x768	16	60, 75, 85
1280x1024	8	60, 75
1600x1200	8	60

- Flexible Panel Support
  • Support for a wide variety of monochrome and color panels
  • Single-Panel, Single-Drive (SS)
  • Dual-Panel, Dual Drive (DD) passive STN
  • Active matrix TFT/MIM LCD
  • EL panels
  • Plasma panels
  • interface to color and monochrome, single drive (SS), and dual drive (DD), STN & TFT panels
- Advanced Power Management feature minimizes power usage
- Fully Compatible with IBM® VGA

3.7.2 Supported Video Modes

3.7.2.1 IBM Standard Video Modes

Mode No.	No. of Colors	Char. x Rows	Char. Cell	Screen Format	Display Mode	Dot Clock MHz	Horiz. Freq. kHz	Vert. Freq. Hz
0,1 0*,1* 0+,1+	16	40x25	8x8 8x14 8x8	360x400 320x350 320x200	Text	28.322 25.175 25.175	31.5	70
2,3 2*,3* 2+,3+	16	80x25	9x16 8x14 8x8	720x400 640x350 640x200	Text	28.322 25.175 25.175	31.5	70
4	4	40x25	8x8	320x200	Graphics	25.175	31.5	70
5	4	40x25	8x8	320x200	Graphics	25.175	31.5	
6	2	80x25	8x8	640x200	Graphics	25.175	31.5	70
7 7+	Mono	80x25	9x16 9x14	720x400 720x350	Text	28.322	31.5	70
D	16	40x25	8x8	320x200	Planar	25.175	31.5	70
E	16	80x25	8x8	640x200	Planar	25.175	31.5	70
F	Mono	80x25	8x14	640x350	Planar	25.175	31.5	70
10	16	80x25	8x14	640x350	Planar	25.175	31.5	70
11	2	80x30	8x16	640x480	Planar	25.175	31.5	60
12	16	80x30	8x16	640x480	Planar	25.175	31.5	60
13	256	40x25	8x8	320x200	Packed Pixel	25.175	31.5	70

3.7.2.2 Extended Video Modes

For detail information see data sheet of 69000.

3.7.3 Supported Panel Types

The following displays have been tested successfully with the VP7:

3.7.3.1 Monochrome Displays

Manufacturer	Part Number	Resolution	Technology	Panel Drive	Interface
Hitachi	LMG7550XUFC	640x480	LCD	DD	8 Bit

3.7.3.2 STN Color Displays

Manufacturer	Part Number	Resolution	Technology	Panel Drive	Interface
Kyocera	KCS6448BSTT	640x480	STN	DD	16 Bit

3.7.3.3 TFT Color Displays

Manufacturer	Part Number	Resolution	Technology	Panel Drive	Interface
NEC	NL6448AC33-18	640x480	TFT	SS	18 Bit
Sharp	LQ10S21	800x600	TFT	SS	18 Bit

3.7.3.4 LCD Signal Mapping

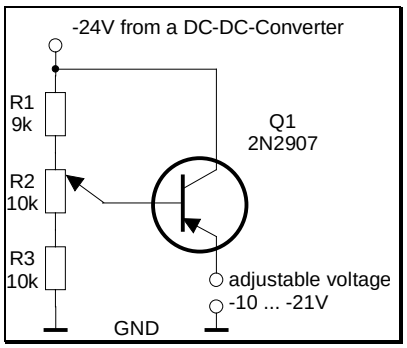
Pin Name	MONO SS 8 Bit	MONO DD 8 Bit	MONO DD 16 Bit	COLOR TFT 9/12/16 Bit	COLOR TFT 18/24 Bit
LC_P00	P0	UD3	UD7	---/---/B0	---/B0
LC_P01	P1	UD2	UD6	---/B0/B1	---/B1
LC_P02	P2	UD1	UD5	B0/B1/B2	B0/B2
LC_P03	P3	UD0	UD4	B1B2//B3	B1/B3
LC_P04	P4	LD3	UD3	B2/B3/B4	B2/B4
LC_P05	P5	LD2	UD2	---/---/G0	B3/B5
LC_P06	P6	LD1	UD1	---/---/G1	B4/B6
LC_P07	P7	LD0	UD0	---/G0/G2	B5/B7
LC_P08			LD7	G0/G1/G3	---/G0
LC_P09			LD6	G1/G2/G4	---/G1
LC_P10			LD5	G2/G3/G5	G0/G2
LC_P11			LD4	---/---/R0	G1/G3
LC_P12			LD3	---/R0/R1	G2/G4
LC_P13			LD2	R0/R1/R2	G3/G5
LC_P14			LD1	R1/R2/R3	G4/G6
LC_P15			LD0	R2/R3/R4	G5/G7
LC_P16					---/R0
LC_P17					---/R1
LC_P18					R0/R2
LC_P19					R1/R3
LC_P20					R2/R4
LC_P21					R3/R5
LC_P22					R4/R6
LC_P23					R5/R7

Pin Name	COLOR TFT HiRes 18/24 Bit	COLOR STN SS 8 Bit	COLOR STN SS 16 Bit	COLOR STN-DD 8 Bit	COLOR STN DD 16 Bit	COLOR STN DD 24-Bit
LC_P00	---/B00	R1	R1	UR1	UR0	UR0
LC_P01	---/B01	B1	G1	UG1	UG0	UG0
LC_P02	B00/B02	G2	B1	UB1	UB0	UB0
LC_P03	B01/B03	R3	R2	UR2	UR1	LR0
LC_P04	B02/B10	B3	G2	LR1	LR0	LG0
LC_P05	B03/B11	G4	B2	LG1	LG0	LB0
LC_P06	B10/B12	R5	R3	LB1	LB0	UR1
LC_P07	B11/B13	B5	G3	LR2	LR1	UG1
LC_P08	---/G00		B3		UG1	UB1
LC_P09	---/G01		R4		UB1	LR1
LC_P10	G00/G02		G4		UR2	LG1
LC_P11	G01/G03		B4		UG2	LB1
LC_P12	G02/G10		R5		LG1	UR2
LC_P13	G03/G11		G5		LB1	UG2
LC_P14	G10/G12		B5		LR2	UB2
LC_P15	G11/G13		R6		LG2	LR2
LC_P16	---/R00					LG2
LC_P17	---/R01					LB2
LC_P18	R00/R02					UR3
LC_P19	R01/R03					UG3
LC_P20	R02/R10					UB3
LC_P21	R03/R11					LR3
LC_P22	R10/R12					LG3
LC_P23	R11/R13					LB3

☞ When using 9 or 12 bit TFT displays, connect the data lines as for 16 bit TFT displays, starting with the most significant bit (MSB).

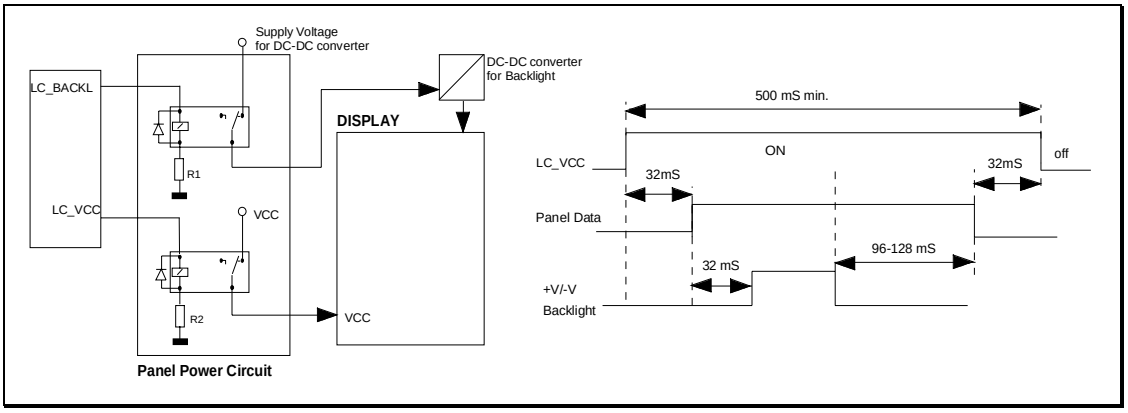
3.7.4 Schematic Diagram for Contrast Adjustment

STN color and monochrome displays have a lower contrast ratio than TFT Displays. To compensate for different environmental light conditions, a contrast adjustment circuit is necessary. For each display a matching DC-DC-converter is required because there is neither a standard for voltage nor for the polarity. The example below shows a simple schematic diagram for a negative voltage contrast adjustment.



3.7.4.1 Power Supply for Panels

Most of the display manufacturers recommend a special power on/off sequence for their panels. This sequence is important for correct operation of the panel. The diagram below shows the timing of the input signals and the supply voltage. The graphics controller provides two signals for controlling the power supply timing.



3.7.5 Software Installation

The following table provides an overview of the display drivers available for the Graphic Controller.

Program	**Version**
Windows 95	
WIN NT	3.51
WIN NT	4.0
OS2	3.0, 4.0
Windows 98	
Xfree86	3.3.3

Since the Chips and Technologies 69000 is used on a large number of computers, many operating systems like OS/2, Windows NT, Windows 95 and Windows 98 already include high resolution drivers.

3.8 SCSI Interface

The SCSI interface on the VP7 consisting of the PCI Bus SCSI controller Symbios 53C875. This controller chip drives the SCSI protocol in accordance to the ANSI X3.131-1986 (SCSI-1) and ANSI X3.131-199x (SCSI-2) specification, with the following functions:

- Arbitration
- Selection
- Message Handling
- Disconnect/Reconnect
- Data Bus Parity Checking

The SCSI controller can operate the SCSI bus at a maximum speed of 14 Mbytes/s asynchronously or 40 Mbytes/s synchronously and burst data 32bit wide to the host CPU at full PCI speeds.

- Termination of the SCSI Signals

  The SCSI interface is terminated on both sides of the connector cable. The terminator on the VP7 is an active terminator. The other usually on the peripheral unit must be also an active type. If more than one unit is connected to the host adapter, all terminators on the peripheral units must be removed or disabled, except for the one at the far end of the SCSI cable chain.

- Number of SCSI Devices

  All units connected to the SCSI bus (also peripheral controller and the host adapter) must have an address with which they may be accessed. Sixteen addresses (0..15), named ID numbers, can be assigned on the SCSI bus. These ID numbers can be changed by jumpers or switches located on the device. The SCSI controller on the VP7 usually reserves the ID number 7, meaning that ID numbers 0 .. 6 and 8 .. 15 (Wide SCSI devices only) can be assigned to the peripheral devices. The VP7 SCSI controller device ID can be altered from the SCSI BIOS configuration menu. When using more than two devices on the SCSI bus make sure that they all have unique IDs. If there are more SCSI hard disks in the system, the hard disk with the lowest ID number is the first hard disk and is given the logical drive name "C:\". The VP7 tries to startup the operating system from the first hard disk. SCSI scan order can be changed from the SCSI BIOS configuration. EIDE versus SCSI scan order can be altered in the system BIOS Setup.

- Cable characteristic

  The characteristic impedance of the cable is shown below:

Characteristic impedance:	SCSI-2	90 Ω to 132 Ω
	Ultra Fast-20	90 Ω+/-10 Ω
Signal attenuation:	0.095 dB maximum per meter at 5 MHz	
Pair-to-pair propagation delay delta:	0.20 ns maximum per meter	
DC resistance:	0.230 Ω maximum per meter at 20	

For correct operation of the SCSI bus, the cable length shown in the table below must not be exceeded.

SCSI-Type	Mbyte/s	No. of devices	cable length
SCSI-2	≤5	8	6m
SCSI-2	10	8	3m
Ultra Fast-20	20	≤4	3m
Ultra Fast-20	20	8	1.5m

☞ Using cables within the specified characteristics is necessary for reliable system operation.

☞ The active Terminator on the VP7 can not be disabled.

☞ The minimum cable length is 20 cm.

☞ The devices should be evenly spaced on the SCSI cable. Min. distance between devices is 20cm.

3.8.1 Software Installation

The 53C875 SCSI controller provides a total SCSI solution in PC environments with the Symbios SCSI Device Management System (SDMS). SDMS provides driver support for hard disk, removable media and CD-ROM peripherals for the DOS, Windows 3.xx, Windows95, OS/2 and Novell 3.x, 4.x and various UNIX environments.

The CDROM supplied with the VP7 include the most commonly used software drivers and utilities. More software is available from the Internet or BBS.

3.9 Ethernet Interface

The Ethernet controller Am79C972 used with the VP7 is a high performance Fast Ethernet PCI controller compatible to the Novell NE2100 and NE1500 standard devices.

For registration and identification of a workstation in a LAN, a unique ID number is required. Each network card is assigned an unique ID number, which resides in an Ethernet address ROM on the VP7. This ID number can be viewed by a software utility. The VP7 BIOS setup provides permission of an Ethernet boot option.

3.9.1 Software Installation

The drivers available for the Ethernet controller AM79C972 support a large number of operating systems. The VP7 BIOS also allows Ethernet remote boot from the following servers:

- IBM LAN SERVER 2.x/3.x
- IBM LAN SERVER 4.x
- Microsoft LAN SERVER
- Novell SERVER

Type	**System**
ODI	DOS, OS/2
NDIS	DOS, OS/2 2.01
NDIS	WfW 3.11 Windows NT 3.1 Windows NT 3.5 Windows NT 3.51, 4.0 Windows 95
SCO UNIX	SCO ODT 3.0 SCO Open Server 5.0
SUN Solaris	SUN Solaris Drive 2.4
Novell Unixware	Novell Unixware driver 1.2 Novell Unixware driver 2.0

The table shows operating systems

Supported by the available software.

The CDROM supplied with the VP7 include the most commonly used software drivers and utilities. More software is available from Internet or BBS. For detailed information, read the chapter "Update Information".

3.10 VMEbus Interface

The VP7 contains the UNIVERSE VMEbus interface chip. It contains a complete high performance 64-bit VMEbus interface with 32-bit PCI master/slave capability. Furthermore a system controller is implemented to allow the VP7 to reside in slot 1 without the necessity of an extra system controller.

☞ Slot 1 auto detection may be overridden by Setup.

Universe Register
All of the controlling registers are located in the UNIVERSE. The registers are memory mapped and after Power-On the base address is assigned dynamically by BIOS. 4 Kbytes address space are reserved for these registers.

Universe PCIbus Address Space
By default the VMEbus interface is disabled. If the VP7 needs to access the VMEbus, the VMEbus logic must be enabled and the PCI address spaces must be defined. Multiple PCI to VMEbus address space mappings with different attributes (A16, A24, D16, D32, User, ...) are possible. The size of available address space can be adjusted by BIOS Setup.

Universe VMEbus Address Space
VMEbus address space may be defined when another VMEbus master needs to access internal memory. Any location accessible over the PCIbus can be used.

Local Interrupt
UNIVERSE Interrupt line LINT 0 may be assigned by BIOS to a local interrupt line. Interrupt sharing with other PCI devices may be allowed when all interrupt lines support level driven mode (typical for PCI devices) and all interrupt service handlers know of this feature. The other seven interrupt lines LINT 1 .. LINT 7 are not connected.

☞ The driver software (onboard SCSI and Ethernet controller) of the most common operating systems, support interrupt sharing.

Features
- Fully compliant, 32-bit, 33 MHz PCI local bus interface
- fully compliant, high performance 64-bit VMEbus interface
- integral FIFOs for write posting to maximise bandwidth utilisation
- programmable DMA controller with linked list support
- VMEbus transfer rates of 60-70 Mbytes/sec
- complete suite of VMEbus address and transfer modes
    - A32/A24/A16 master and slave
    - D64 (MBLT)/D32/D16/D8 master and slave
    - BLT, ADOH, RMW, LOCK
- flexible register set, programmable from both the PCI and VMEbus ports
- full VMEbus system controller functionality

Programming
For detailed information about programming the UNIVERSE refer to 'VMEbus Interface Components Manual UNIVERSE' available from Tundra Semiconductor Corporation. This manual can be download from the Tundra web site (http://www.Tundra.com/) in PDF-Format. The web site also contains sample code for the first intialization. Please read also the “BIOS Application Note Tundra Universe PCI-to-VMEbus Bridge” available through SBS Technologies support, or on the VP7 utility CD.

SBS Technologies also recommend to read carefully the device errata available on the VP7 utility CD.

SBS Technologies provides complete DLLs for the VMEbus Interface for the most common operating systems like Windows 95, Windows NT, QNX. Contact SBS Technologies for more information.

3.11 Additional Features / Extended Registers

This chapter describes the extended registers in the I/O address space necessary for programming the additional features of the VP7. The extended register set is specific to the VP7. To protect the system against illegal accesses to these registers, the extended registers set can be locked completely. Writing $05 to the Lock Register LOCKR enables access, writing $04 disables access to the extended configuration register set.
Software using the Extended Reg. Set must comply to the methods described in M-PGM_IOPNPSYS.

	7	6	5	4	3	2	1	0
LOCKR								

I/O Lock Register

169_W LBP[] Lock Bit Pattern. Writing $05 to this register enables access to the extended registers. Writing $04 disables access to this registers. Any other values have no effect. The values written can not be read back.

3.11.1 SMB bus devices

The VP7 uses a serial 2-wire bus to communicate with several onboard devices:

Device	Designator	SMB address (binary)
Clock generator (*)	U1000	1101000X
PIX4 slave port (*)	U1700	0001000X
Serial EEprom (24C04)	U1991	1010100X
Temperature sensor (LM75)	U1992	1001111X
SDRAM bank 0 (*)	U1400	1010000X
SDRAM bank 1 (*)	U1401	1010001X

The Temperature sensor from National Semiconductor LM75 is located close to the processor and therefore has a comparable temperature.
In the serial EEprom 24C04 a board identifier or other board unique information can be stored.
For details on accessing these devices see the appropriate data sheets.

For further information see data sheet of LM75 and 24C04.

Access to devices marked by (*) is done by BIOS. It is strongly recommended not to access these devices by user software.

3.11.1.1 Temperature Sensor

A National Semiconductors LM75 temperature sensor is implemented on the VP7 board. Its interface is connected to the I2C control signals of the SMB. The sensor is located below the CPU and shows the air temperature between board and CPU. The sensor has an over-temperature output integrated, which can be used to take actions like reducing the CPU speed.
More information can be found in the LM75 datasheet from National Semiconductors.

3.11.1.2 Serial EEPROM

For storage of user data a serial EEPROM is implemented on the VP7 board. It is a standard 24C04 type EEPROM with 512 bytes. More information about writing and reading the contents can be found in the datasheets from the manufacturer (e.g. Microchip Technology, SGS Thomson, Atmel, Catalyst and many others).

3.11.2 Watchdog, Powerfail Monitor

For security of application software, the VP7 offers a software controlled hardware watchdog capable of issuing a reset signal if its time-out interval expires. To prevent the watchdog from generating a reset signal, it must be re-triggered within a 0.5 second interval by reading the Watchdog Control Register WCR.
Since standard software doesn't trigger the watchdog periodically, it is disabled after reset. The watchdog function can be enabled via the Watchdog Control Register WCR. If the watchdog is enabled, it must be reset periodically by reading WCR within 0.5 seconds. Otherwise, a reset pulse with a duration of 200msec is generated to restart the system. A watchdog reset which has occurred and reset the system can be detected by monitoring the WDG_REL line and the state of the WCR register bit 2.

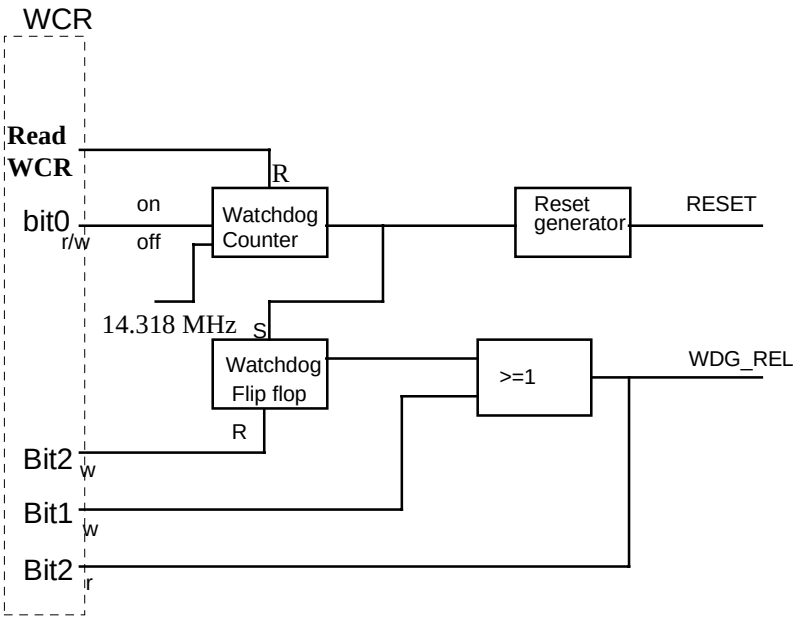
	15 4	3	2	1	0
WCR			WD_RES	WD_SET	WD_ON

I/O Watchdog Control Register reset: xxxxxxxxxxxxxx01b
power down/up: xxxxxxxxxxxxx001b

$160_{R/W}$ WD_ON Watchdog Enable. When this bit is set, the watchdog function is enabled, otherwise it is disabled. To prevent a reset generated by the enabled watchdog circuit, it must be re-triggered by reading the WCR. This bit is readable. This bit is set to 1 by a System Reset.

WD_SET When set to 1, this bit sets the Watchdog output line directly. This bit is not readable. This bit is reset to 0 by a System Reset.

WD_RES When set to 1, this bit resets the watchdog flip flop. The watchdog flip flop is not reset by a system Reset. The watchdog flip flop is reset by a power down/up cycle. This bit is readable. Reading this bit gives the current state of the WDG_REL line. Software can determine whether the last System Reset was caused by the watchdog by reading this bit. If a 1 is read, the last Reset was caused by the watchdog.



3.11.3 LED Output

The LED Output can be turned on and off via the LED Control Register LEDCR. After reset, the LED is turned on by hardware and turned off when running the first instructions of the system BIOS.. The LED can be used for any user-defined purpose.

	7	6	5	4	3	2	1	0
LEDCR	RES							LED_ON

I/O LED Control Register reset: xxxxxxx1

168_W LED_ON LED on/off. When this bit is set the LED is turned on. This is the state immediately after a hardware reset. When reset, the LED is turned off. The BIOS resets this bit within its first instructions in order to indicate that the BIOS has begun to run.

RES Reserved for future use.

3.11.4 NMI Timer

The VP7 features a timer which can trigger NMIs periodically. The timer is programmable in 7 steps from 0.25 ms up to 16 ms. The usage of the NMI timer together with appropriate software available from your distributor, Windows 3.11, Windows 95 and Windows NT offer "Real Time Functions".

	7	6	5	4	3	2	1	0
NMITCR	RES					TSEL2	T_SEL1	T_SEL0

I/O NMI Timer Control Register reset: 11111000

$161w T_SEL[ ] Enable and disable the NMI-timer and selects the NMI-timer period

T_SEL2..T_SEL0	**NMI period**
000	NMI-timer disabled
001	0.256 ms
010	0.512 ms
001	1.024 ms
100	2.048 ms
101	4.096 ms
110	8.192 ms
111	16.384 ms

RES Reserved for future use.

☞ **After a NMI has occurred, the external NMI ticker circuitry must first be reset by an IO write (don't care value) to a shadow port of port 061h at address 861h, with the lock register LOCKR unlocked. Only this cycle will pass the PCI to ISA bridge and will reset the ticker. After this, the IOCH bit of PORT061 has to be cleared by setting and clearing the ENIOC bit.**

The two registers shown below are standard PC registers important for NMI handling.

	7	6	5	4	3	2	1	0
PORT061		IOCH			ENIOC			

I/O Port at $061, PC/AT compatible

061_{R/W}$ IOCH IOCHCK state. This bit reflects the latched state of the IOCHCK line of the ISA bus. If the IOCHCK line is asserted, this bit will be set.

ENIOC Enable IOCHCK. This bit enables the IOCHCK line. If this bit is cleared and the NMI is enabled via the RTC, an active IOCHCK line issues an NMI.

	7	6	5	4	3	2	1	0
RTCADD	NMIM							

I/O RTC Address Register

070_{W}$ NMIM NMI Mask bit. When this bit is set the NMI is disabled. When cleared, the NMI function is enabled and the IOCHCK line can trigger an NMI. Note that RTCADD is a write-only register. BIOS calls (also via DOS call) and application software accessing the CMOS RAM may change the NMIM bit.

3.11.5 Reset Button

The lever switch on the front panel has two functions. Pushing the lever to the upwards will issue a reset, while pushing downwards will trigger a NMI.

☞ The reset signal is active for all subsystems of the VP7.

3.11.6 Speaker

A standard PC compatible speaker is onboard. An external standard PC compatible speaker may be connected between the appropriate IO connector at the back side and +5V.
The register shown below is a standard PC register used for speaker programming.

	7	6	5	4	3	2	1	0
PORT061			TIM2_OUT				SPK_DAT	SPK_GAT

I/O Port at $061, PC/AT compatible

061_{R/W}$ TIM2_OUT$_{R}$ Timer channel 2 out. Toggles with the frequency defined by timer 2 when SPK_GAT is set.

SPK_DAT Speaker data. When set, the speaker is fed with a frequency defined by timer 2. SPK_GAT must be set before.

SPK_GAT Speaker gate. Enable timer 2 gate to speaker.

Appendix

Update Information

The VP7 is delivered with a software CDROM. It contains SCSI, Ethernet and VGA/LCD drivers for the most popular operating systems including Windows 95, Windows NT, OS/2 etc. For other drivers or updates use the contact addresses from the table below.

Device	Internet
SCSI(Symbios)	www.lsilogic.com
Ethernet (AMD)	www.amd.com
VGA/LCD(C&T)	www.assiliant.com
VMEbus Controller	www.tundra.com
System BIOS	www.sbs.com

The CDROM contains a utility program for system BIOS updates. The VP7 is equipped with an in-system programmable FLASH ROM device.

- Additional Software Tools
  Some applications do not allow battery backup of the CMOS RAM. Customization of system BIOS for these applications is available on request.

SBS Technologies provides a full set of DLLs (MSDOS, Windows 3.11, Windows 95, Windows NT) for their PC boards. Please contact your distributor or SBS Technologies.

- Setup
  To enter system BIOS Setup, press <**DEL**> after power on or reset.

- Reset
  To restore default BIOS Setup, press **<INS>** after power on or reset.

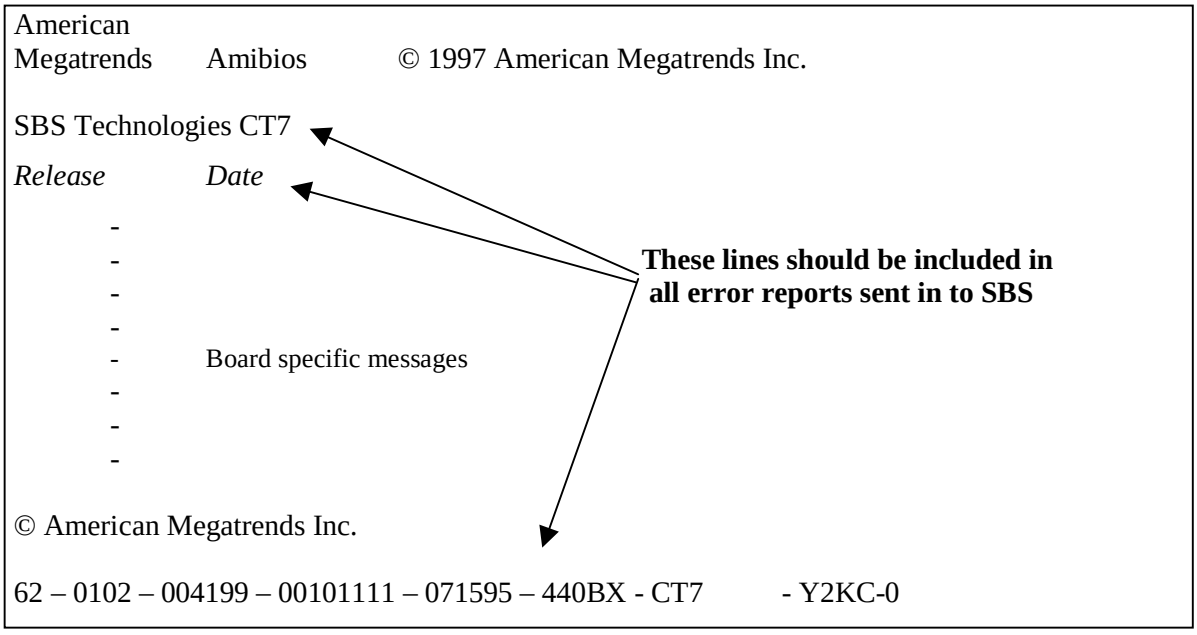
☞ When the system is reset or turned off while in BIOS Setup, all Setup information may be lost and the ROM defaults will be restored.

For further information please read the “Cx7/Vx7 AMI BIOS User’s Manual”.

Error Report Form

When you are returning a product for repair, it is very important to include a written report which details the nature of the problem in order to expedite the repair.
Please always use the Error Report Form attached a the end of this maual or include the following information:

- RMA Number
- Product & Serial Number
- Part Number
- Version
- Contact: Name & Phone Number
- Detailed Description of the Problem/Defect



Example /coding of the ID line:

processor, flash ROM size	major & minor BIOS revisions	supplier ID	BIOS features	AMIBIOS core copyright date	chip set	project ID	year 2000 compliant
62 -	0102 -	004199 -	00101111 -	071595 -	440GX -	CT7/CE7 -	Y2KC-0

You can stop the video output for proper reading the three information lines as described: Simply press the “0 / Enter “ key during the start-up sequence. This key is located on the numeric keypad of your keyboard

Error Report Form (Europe)

SBS Technologies GmbH & Co.KG	Company Name
Memminger Str. 14	Department
86159 Augsburg	Contact Person
	Mailing Address
Phone Number **+49 821 5034-170**	Phone Number
Fax Number **+49 821 5034-119**	Fax Number
	Email Address

Part. N. **VP7** Version: V _ . _ Date _ _ _ _ Serial N. _ _ _ _ _ _ _ _

Error Description:		
Hardware Environment:		
Operating System/Software:		
Warranty repair: ❑ YES ❑ NO		(Please see section 'Warranty')

Error Report Form (US + Rest of World)

SBS Technologies, Inc.	Company Name
6301 Chapel Hill Road	Department
Raleigh, NC 27607-5115	Contact Person
	Mailing Address
Phone Number **+1 919 851-1101**	Phone Number
Fax Number **+1 919 851-2844**	Fax Number
	Email Address

Part. N. **VP7** Version: V _ . _ Date _ _ _ _ Serial N. _ _ _ _ _ _ _ _

Error Description:		
Hardware Environment:		
Operating System/Software:		
Warranty repair: ❑ YES ❑ NO		(Please see section 'Warranty')