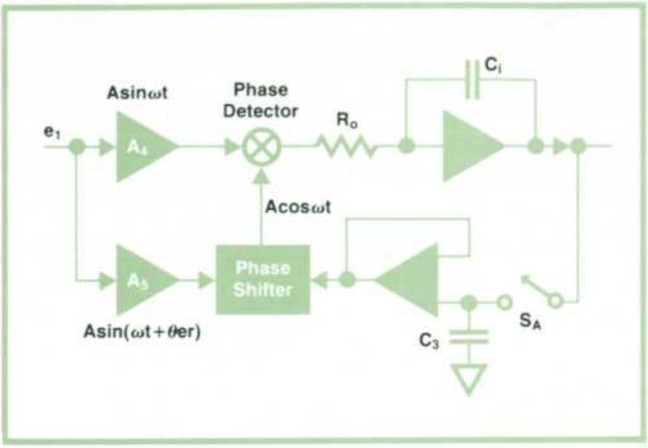

Fig. 7. *Circuit diagram for auto phase adjustment. Closing S_A creates a first-order feedback loop that stores on capacitor C_3 a voltage proportional to the differential phase shift of amplifiers A_4 and A_5.*

4261A uses a ROM-centered design. It has two 4K-bit ROMs, one for sequence control and the other a decoder. With this design, it was easy to add the self-test functions. The ROMs are n-channel MOS ROMs manufactured by HP.

Full Autoranging

The 4261A has two autoranging modes. One is a fixed measurement circuit mode in which the operator selects either the series or the parallel equivalent circuit, and the other is full autoranging including circuit mode changing. Measurement circuit mode changes are done by switching S_C in Fig. 3. In the full autoranging mode, the instrument selects an appropriate range from the eight available ranges according to the value of the component being tested. In this mode, the function switch need only be set to L, C, or R to make the measurement.

Self-Test

The 4261A has self-test functions that enable it to check most performance areas. No additional equipment or circuitry is required for making the self-check. The user need only set two slide switches. Two tests are provided. One tests the logic systems and the other mainly checks the analog circuits. Slide switches located on the sequence control board are set to the appropriate positions to put the 4261A into its self-test mode.

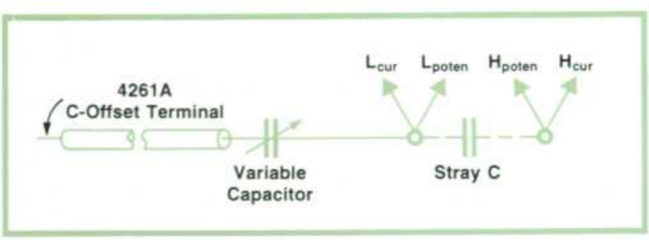

Fig. 8. *To cancel stray capacitance between the unknown terminals, a capacitance offset signal, available at a rear-panel connector, provides a capacitance offset of 0 to 100 pF when fed into the low-current terminal through a variable capacitor. The capacitor is adjusted for a zero display with no unknown connected.*

Minimizing Errors

The five-terminal connection configuration minimizes the measurement error caused by residual impedance of the test leads. It is especially useful for the measurement of low impedances (below 1Ω). However, some care is required in making the test lead connections when measuring capacitors from 100 to 1000 μF at 1 kHz. Here, an error is caused by the mutual inductance of the Hp, Hc cable or the Lp, Lc cable. If the mutual inductance of each cable is M/2 henries, then:

$$C\ \text{measured} = \frac{C_x}{1 - \omega^2 M C_x}$$

To minimize this error, it is necessary to use short test leads or to twist the Hp and Lp cables together. Similarly in high-impedance measurements, it is possible to minimize the stray capacitance between the high and low terminals by shielding with the GUARD terminal. Compensation for high-impedance measurement errors can also be made by using an offset voltage equal to the voltage across the DUT but opposite in polarity; this is done with the 4261A in the connection configuration shown in Fig. 8. The variable capacitor is adjusted for a zero display.

Accessories

Several accessories are available for the 4261A. The 16061A Test Fixture is a direct-connection type for

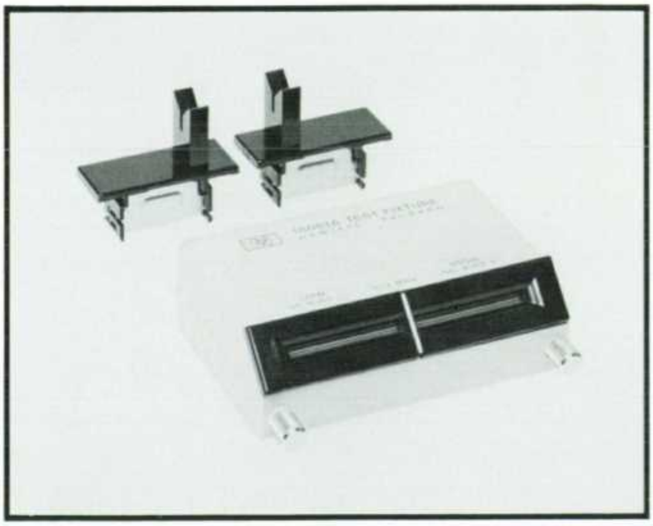

Fig. 9. *Model 16061A Test Fixture for general-purpose use.*

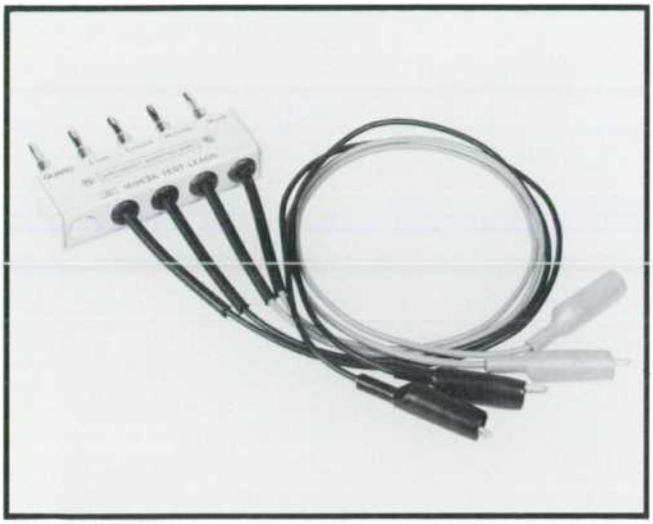

Fig. 10. *Model 16062A Test Leads for low-impedance devices.*

general-purpose use. The 16061A Test Fixture (Fig. 9) has inserts for both parallel and axial lead components. The 16062A Test Leads (Fig. 10) are for comparatively low-impedance DUTs (four-terminal connections). The 16063A Test Leads (Fig. 11) are for comparatively high-impedance DUTs (three-terminal connections).

Acknowledgments

The authors wish to express appreciation to the many people who participated in the development of the Model 4261A. The team members included Kohichi Maeda, who directed the project, Hiroshi Sakayori, who designed the process amplifier section, Kenzo Ishiguro, who designed the display and decoder section, Seiji Mochizuki, who did the power supply design, Toshio Manabe and Yoshimasa Shibata, who contributed to the mechanical design, and Kazu Shibata and Yoshio Satoh, who handled the industrial design. Hitoshi Noguchi provided many useful suggestions for the project. Akira Yamaguchi designed part of the logic section in the early stages of the project.

Fig. 11. *Model 16063A Test Leads for high-impedance devices.*

References

1. T. Sugiyama and K. Yamaguchi, "Pulsewidth Modulation DC Potentiometer," IEEE Transactions, Vol. IM-19, No. 4, November 1970.
2. K. Maeda, "An Automatic Precision, 1-MHz Digital LCR Meter," Hewlett-Packard Journal, March 1974.

Satoru Hashimoto

Satoru Hashimoto received his BSEE from Tokyo Metropolitan University in 1971, and soon afterwards joined Yokogawa-Hewlett-Packard. He worked on the design of the logic section of the 4271A 1-MHz Digital LCR Meter, then joined the 4261A Digital LCR Meter project. He developed the counter and the sequence control section circuitry for the 4261A. In his spare time Satoru enjoys mountain climbing and photography.

Toshio Tamamura

Toshio Tamamura received his BSEE degree in 1971 from the University of Electro-Communications in Tokyo. He has been with Yokogawa-Hewlett-Packard as a development engineer since that time. He was a principal contributor to the design of the 4271A 1-MHz Digital LCR Meter and the 4261A Digital LCR Meter; he developed the analog section circuitry for the 4261A. He's married and the father of a small son. In his spare time Toshio likes to play tennis.

SPECIFICATIONS
HP Model 4261A LCR Meter

Common Specifications

PARAMETERS MEASURED: C-D, L-D, R
DISPLAY: 3½ digit, max. display 1900
CIRCUIT MODES: auto, parallel and series
MEASUREMENT CIRCUIT: five-terminal method
RANGE MODE: auto or range hold
MEASUREMENT FREQUENCIES: 120 Hz ±3% and 1 kHz ±3%
TRIGGER: internal, manual, or external

C-D Measurement

Range	120 Hz 1 kHz	1000 pF 100.0 pF	10.00 nF 1000 pF	100.0 nF 10.00 nF	1000 nF 100.0 nF	10.00 µF 1000 nF	100.0 µF 10.00 µF	1000 µF 100.0 µF	10.00 mF 1000 µF
Test Signal Level	Parallel	1V or 50 mV							
	Series				10 µA	100 µA	1 mA	10 mA	70 mA
(Note 1)	Auto	Same as parallel mode				Same as series mode			
C Accuracy	Parallel	0.2% + 1 count + 0.2 pF					(Test signal = 1V)		
		0.5% + 3 counts	0.3% + 2 counts				(Test signal = 50 mV)		
	Series				0.3% + 2 counts			0.5% + 2 counts	1% + 2 counts (Note 3)
(Note 2)	Auto	Same as parallel mode				Same as series mode			
D Accuracy	Parallel	0.2% + (2 + 200/Cx) counts					(Test Signal = 1V)		
			0.3% + (2 + 1000/Cx) counts				(Test signal = 50 mV)		
	Series				0.3% + (2 + Cx/500) counts				1% + (5 + Cx/500) counts
(Note 2)	Auto	Same as parallel mode				Same as series mode			

1. Typical data. Varies with value of D and number of counts.
2. ±(% of reading + counts + α). Cx is capacitance readout in counts.
3. (5% + 2 counts) at 1 kHz.
Accuracy applies over a temperature range of 23°C ±5°C. Error doubles for 0-55°C.

L-D Measurement

Range	120 Hz 1 kHz	1000 µH 100.0 µH	10.00 mH 1000 µH	100.0 mH 10.00 mH	1000 mH 100.0 mH	10.00 H 1000 mH	100.0 H 10.00 H	1000 H 100.0 H
Test Signal Level	Parallel				1V			
	Series	70 mA	10 mA	1 mA	100 µA	10 µA		
(Note 1)	Auto	Same as series mode				Same as parallel mode		
L Accuracy	Parallel				0.3% + 2 counts		1% + 2 counts	
	Series	0.2% + 2 counts + 0.2 µH						
(Note 2)	Auto	Same as series mode				Same as parallel mode		
D Accuracy	Parallel				0.3% + (3 + Lx/500) counts		1% + (3 + Lx/500) counts	
	Series	0.2% + (3 + 200/Lx) counts						
(Note 2)	Auto	Same as series mode				Same as parallel mode		

1. Typical data. Varies with value of D and number of counts.
2. ±(% of reading + counts + α). Lx is inductance readout in counts.
Accuracy applies over a temperature range of 23°C ±5°C. Error doubles for 0-55°C.

R Measurement

Range	120 Hz or 1 kHz	1000 mΩ	10.00Ω	100.0Ω	1000Ω	10.00 kΩ	100.0 kΩ	1000 kΩ	10.00 MΩ
Test Signal	Parallel				1V				
	Series	70 mA	10 mA	1 mA	100 µA	10 µA			
(Note 1)	Auto	Same as series mode				Same as parallel mode			
R Accuracy	Parallel				0.3% + 2 counts				
	Series	0.2% + 2 counts							
(Note 2)	Auto	Same as series mode				Same as parallel mode			

1. Typical data. Varies with number of counts.
2. ±(% of reading + counts).
Accuracy applies over a temperature range of 23°C ±5°C. Error doubles for 0-55°C.

DC Bias

INTERNAL SOURCE: 1.5V, 2.2V, 6V (selectable on front panel). Accuracy ±5%.
EXTERNAL SOURCE: Provision for external dc bias voltage of +30V maximum at binding posts on rear panel.

General

OPERATING TEMPERATURE AND HUMIDITY: 0° C to 55°C, to 95% RH at 40°C.
VOLTAGE REQUIREMENTS; 100/120/220/240 ± 10% 48-66 Hz
POWER CONSUMPTION: ≤25 W with any option.
DIMENSIONS: 213 W × 134 H × 422 D mm
WEIGHT: Approximately 6 kg

Reference Data

MEASURING TIME: the period between start of a measurement and completion of the measurement is equal to measuring time when RANGE HOLD is set to ON plus time required for autoranging. The following are typical times for a measurement of approximately 1000 counts on low loss components when RANGE HOLD is set to ON.
1 kHz: C/L, 220-260 ms; R, 120-160 ms
120 Hz: C/L, 900 ms; R, 700 ms
TIME REQUIRED FOR AUTORANGING (RANGE HOLD OFF):
1 kHz: 180 × n ms
120 Hz: 670 × n ms
where n is the number of ranges stepped by the autorange circuit.
READING RATE: the period between the start of a measurement and the start of the next measurement is equal to the measuring time plus 30 milliseconds (typical) hold time.
PRICE IN U.S.A.: $1740.
MANUFACTURING DIVISION: YOKOGAWA HEWLETT-PACKARD, LTD.
9-1, Takakura-cho
Hachioji-shi
Tokyo 192 Japan

Hewlett-Packard Company, 1501 Page Mill Road, Palo Alto, California 94304

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