ALLEN-BRADLEY

PLC-5/250
Programmable Controller

System Overview

Important User Information

Because of the variety of uses for the products described in this publication, those responsible for the application and use of this control equipment must satisfy themselves that all necessary steps have been taken to assure that each application and use meets all performance and safety requirements, including any applicable laws, regulations, codes, and standards.

The illustrations, charts, sample programs, and layout examples shown in this guide are intended solely for purposes of example. Since there are many variables and requirements associated with any particular installation, Allen-Bradley does not assume responsibility or liability (to include intellectual property liability) for actual use based on the examples shown in this publication.

Allen-Bradley publication SGI-1.1, Safety Guidelines for the Application, Installation, and Maintenance of Solid State Control (available from your local Allen-Bradley office), describes some important differences between solid-state equipment and electromechanical devices that should be taken into consideration when applying products such as those described in this publication.

Throughout this manual, we use notes to make you aware of safety considerations:

ATTENTION: Identifies information about practices or circumstances that can lead to personal injury or death, property damage or economic loss.

Attention statements help you to:

- identify a hazard
- avoid the hazard
- recognize the consequences

Important: Identifies information that is critical for successful application and understanding of the product.

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Chapter 1

Introducing PLC-5/250 Programmable Controllers

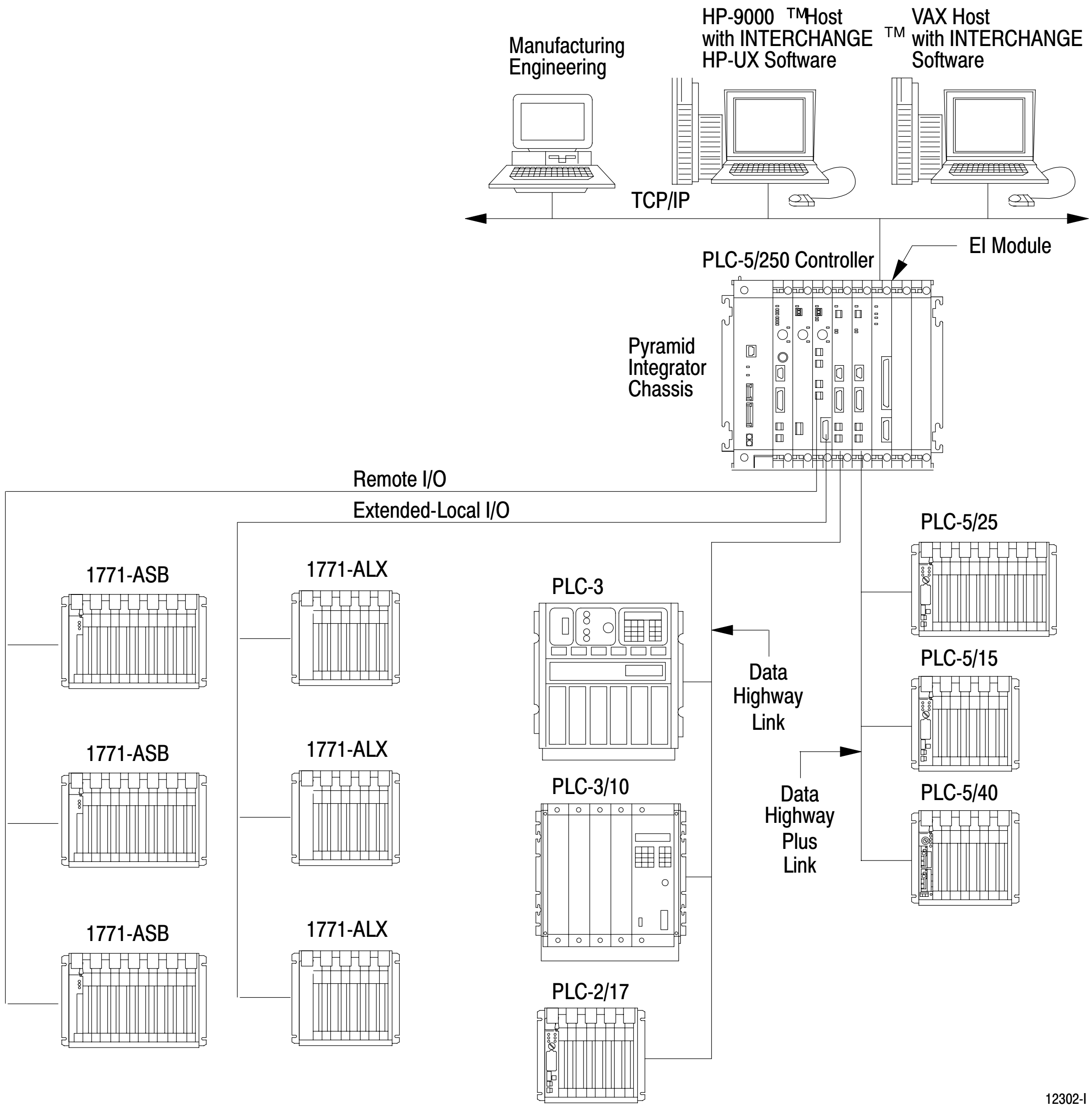
PLC-5/250 Programmable Controllers

The Allen-Bradley PLC-5/250™ programmable controller is an advanced, multi-processor programmable controller that offers modular processor power. It is the largest member of the PLC-5® processor family. Combined with other Pyramid Integrator™ modules, the PLC-5/250 processor becomes a key component in an integrated, expandable control system. The PLC-5/250 processor provides:

- Integrated supervisory control of other controllers and I/O
- Advanced parallel processing
- Multi-tasking capabilities
- Communication with:
  - 1771 I/O (remote and extended-local I/O)
  - Data Highway (DH) and Data Highway Plus™ (DH+)
  - OSI (MAP)
  - DECnet™/OSI
  - Ethernet®

Figure 1.1 shows an example of an integrated control system using a PLC-5/250 processor.

Figure 1.1
Example PLC-5/250 Integrated Control System



Benefits

High performance for increased process speeds and productivity. The PLC-5/250 processor is the most powerful of the PLC-5 family of programmable controllers. Extensive memory, I/O capacity, communication capability, and multiple processors make the PLC-5/250 processor the most versatile programmable controller available.
The PLC-5/250 processor provides fast, reliable gathering and processing of control information. Use the PLC-5/250 for the smooth and quick flow of information between plant floor and management computers.

Distributed systems on Data Highway Plus networks. The PLC-5/250 processor supports a network of multiple DH+ links and acts as a system coordinator for distributed systems. The PLC-5/250 processor, together with smaller PLC-5 systems, provides a single integrated control system.

Centralized control and reporting for SCADA systems. The PLC-5/250 processor acts as a high-speed data concentrator and provides an interface between remote terminal units and supervisory computer systems. Simultaneous master/remote-station configurations allow for comprehensive control of remote locations

Leveraged investment in PLC-5 family. As part of the PLC-5 family of processors, the PLC-5/250 processor communicates with both local and remote I/O. The PLC-5/250 processor uses an enhanced PLC-5 instruction set, sequential function chart programming, and multiple processor capability. Your investment in training and in spares is protected.

Cost savings through product-line compatibility and expandability. Configure a system to meet your needs, and leave plenty of room for expansion. The modular nature of the PLC-5/250 processor and Pyramid Integrator systems lets you select modules that meet the needs of your application. You can easily add modules to fit changing system requirements.

Features

Figure 1.2 shows the modules in one example of a PLC-5/250 processor system.

Figure 1.2
PLC-5/250 Processor Components

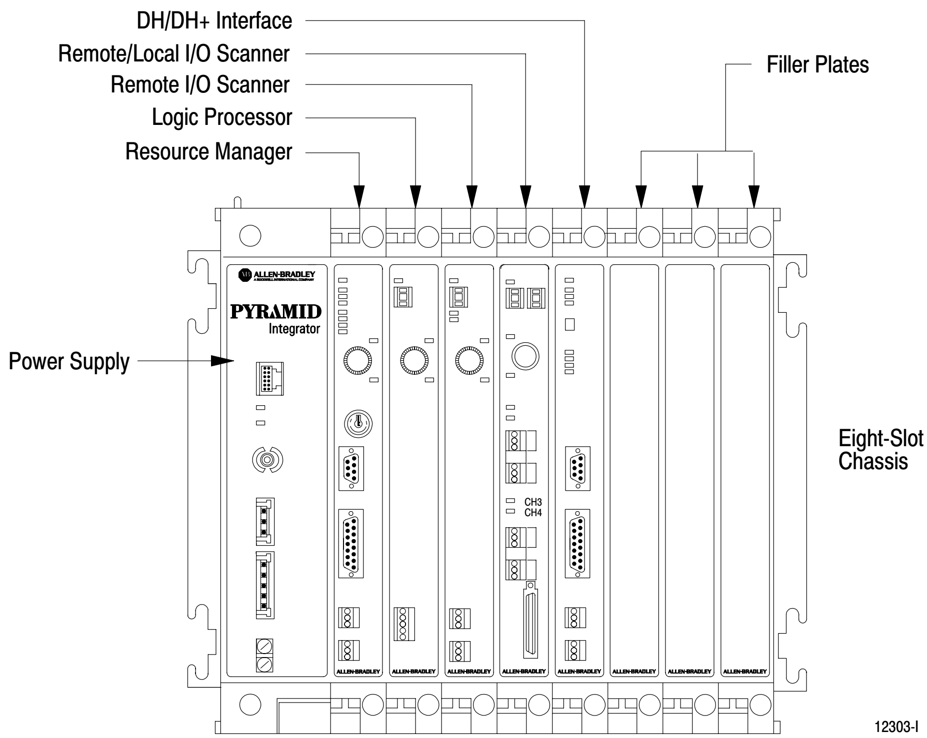


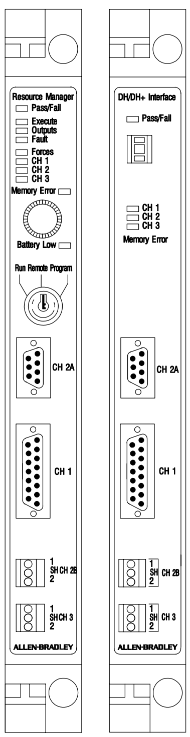
Table 1.A describes the components of the above PLC-5/250 processor system.

Table 1.A
PLC-5/250 System Components

Component	Number Per Chassis	Function	Catalog Number
Chassis		Houses the modules	5110-A4 (4 slot), 5110-A8 (8 slot)
Power Supply	1	Supplies power	5120-P1
Resource Manager	1	Arbitrates bus communication Provides 2 DH/DH+ ports and 1 serial port Provides shared data table	5130-RM1, -RM2
Data Highway / Data Highway Plus Interface	1–4	Provides additional communication channels (2 DH/DH+ ports and 1 serial)	5130-KA
Logic Processor	1–4	Executes control logic Provides local data table	5250-LP1, -LP2, -LP3, -LP4

Component	Number Per Chassis	Function	Catalog Number
Remote I/O Scanner	1–4	Interfaces with remote I/O adapters	5150-RS2
Remote/Local I/O Scanner	1–4	Interfaces with remote and extended-local I/O adapters	5150-RS5

Resource Manager (5130-RM1, -RM2) and the Data Highway / Data Highway Plus Interface (5130-KA)



RM KA

The resource manager (RM) arbitrates bus communication across the backplane and provides for DH/DH+ and serial communications. The RM also provides a shared data table. You need one RM in each PLC-5/250 configuration; you can have only one RM per chassis.

The Data Highway / Data Highway Plus Interface (KA) provides the same communication channels as the RM. Use KAs for additional DH/DH+ and serial communication channels.

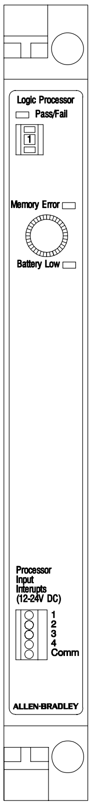
Connect a programming terminal. You can connect an Allen-Bradley programming terminal (1784-T47, 6160-T53, -T60, -T70) or an IBM® PC AT® or compatible to the RM or KA to develop programs.

Connect an RS-232, RS-422, or RS-423 device. Through one channel on the RM and KA, you can connect an RS-232, RS-422, or RS-423 device to the PLC-5/250 system. Use this channel for a printer, modem, programming terminal, or other serial device. You can also use this channel to configure master/remote-station communications.

Protect your programs. You can define up to eight privilege classes, each with a different set of abilities. Use these privilege classes to restrict access to program and data files, RM channels, or DH and DH+ stations.

Route DH+ messages. A station on one DH+ link can communicate with stations on other DH+ links. The RM or KA can receive a message at one DH+ port and route that message to another DH+ port on the same or another RM or KA.

Logic Processor (5250-LP1, -LP2, -LP3, -LP4)



LP

The logic processor (LP) executes ladder logic and sequential function charts (SFCs). The LP has a local data table. You can have up to four LPs per PLC-5/250 system.

Perform concurrent processing with multiple LPs. Multiple LPs let you segment your application and assign specific functions or areas to each LP. Coordinate multiple LPs through a master SFC to perform concurrent multi-tasking.

Execute compiled instruction code. Compiled code executes faster than interpreted code.

Edit the processor program online or offline. When you edit online (such as during the startup and maintenance phases of your process), there is no change in processor scan time; your process stays under control.

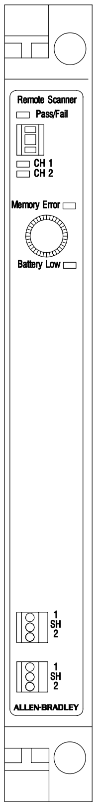
Use ladder logic to develop control programs. The PLC-5/250 processor uses an enhanced PLC-5 instruction set. You can convert your PLC-5 programs to run on PLC-5/250 processors.

Use SFCs to structure your programming. SFCs let you organize your program as a sequence of individual steps separated by transitions. SFCs provide an alternate programming mode for customers who want higher-level language support.

Interrupt the processor based on time intervals. You can execute up to eight interrupt routines based on time intervals. When a time interval expires, the processor immediately runs the selectable timed interrupt (STI) program. When the interrupt routine is completed, program execution resumes where it left off.

Interrupt the processor based on events. The LP has four +12 –12V dc inputs for event-driven interrupts. When one of these inputs goes high, the processor immediately stops executing the main program and executes the processor input interrupt (PII) routine you specify. When the interrupt routine is completed, the LP resumes executing the main program.

Perform independent tasks in the background as the processor executes the main program. Each LP can have up to 32 independent background programs (IBPs), four of which can be active at one time. Use these IBPs to run such tasks as computations and data manipulations or fault recording.



RS2

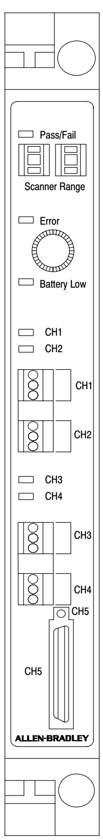
Remote I/O Scanner (5150-RS2)

The remote scanner (RS2) communicates with 1771 I/O. The RS2 stores I/O image tables so that the other modules in the PLC-5/250 processor can access that data. You can have up to four RS2s per chassis.

Select scanner or adapter mode. Each RS2 has two communication channels. Select each channel individually to operate in either scanner mode or adapter (direct-communication) mode. In scanner mode, the channel scans and controls its own remote I/O link. In adapter mode, the channel communicates with a supervisory processor.

Have as many as 32 I/O adapters per channel. When an RS2 channel is set for scanner mode, it can operate with a maximum of 32 adapters on the I/O link.

Scan 1024 I/O with unique I/O addressing. You can have a maximum of 1024 I/O per RS2 (total for the two I/O links) distributed across a maximum of eight racks and still have a unique address for each I/O module.



RS5

Remote/Local I/O Scanner (5150-RS5)

The remote/local scanner (RS5) communicates with both remote and extended-local I/O. You can have up to four RS5s per chassis.

Select remote scanner or adapter mode. Each RS5 has four remote communication channels. Select each channel individually to operate in either scanner mode or adapter (direct communication) mode. In scanner mode, the channel scans and controls its own remote I/O link. In adapter mode, the channel communicates with a supervisory processor.

Increase the speed of data transfer by using the extended-local I/O channel. Each RS5 has one extended-local communication channel. Extended-local I/O functions similarly to remote I/O, but it has faster I/O throughput.

Scan 4096 I/O with unique I/O addressing. You can have a maximum of 4096 I/O per RS5 (total for the four remote I/O links) distributed across a maximum of 32 racks and still have a unique address for each I/O module. There can only be a maximum of four logical scanners (4096 I/O) in a system.

Chapter 2

System Components

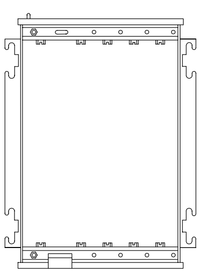
Chapter Objectives

This chapter introduces the components that you can use in a PLC-5/250 processor system:

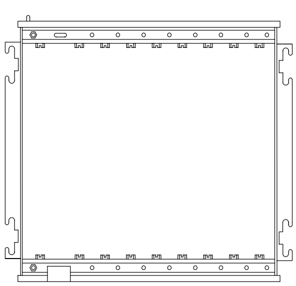
- Chassis
- Power Supply
- Resource Manager
- Data Highway / Data Highway Plus Interface
- Logic Processor
- I/O Scanner
- Other Pyramid Integrator Modules
- Programming Terminal
- Cables

Pyramid Integrator Chassis

The Pyramid Integrator chassis provides the backplane over which the processor modules communicate as well as a common housing for the modules.



4-slot chassis



8-slot chassis

Table 2.A
Selecting a Pyramid Integrator Chassis

This chassis:	Provides:
5110-A4	4 slots
5110-A8	8 slots

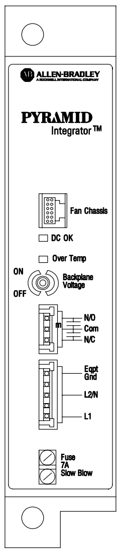
Movable mounting brackets let you mount the chassis in either a panel-mount or rack-mount configuration.

ATTENTION: When you install or remove a module from the chassis, you must shut off dc power to the chassis using the front-panel power switch on the power supply.

Power Supply

The power supply (5120-P1) provides power for the modules in the Pyramid Integrator chassis. The power supply provides +5V dc at 4 to 35 A, +12V dc at 0 to 3 A, and -12V dc at 0 to 1 A for module power.

The power supply fits in a dedicated double-wide slot (not one of the module slots) at the left end of the Pyramid Integrator chassis.



Resource Manager

The resource manager (5130-RM1, -RM2) arbitrates communication between the modules on the backplane and provides communication to external plant-floor devices. In addition, it is a programming interface for the PLC-5/250 processor. The RM also handles system power-up, system power-down, and system configuration. It plays a major role in system fault handling and recording.

All PLC-5/250 processor systems must have one resource manager. Place the RM in the leftmost slot of the chassis, next to the power supply. The resource manager is the only slot-dependent module (not including the power supply).

The RM contains system memory and user-defined global memory that is accessible by other Pyramid Integrator modules. Use the global memory for data that must be shared by multiple LPs.

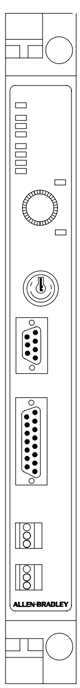
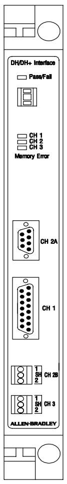


**Table 2.B
Selecting RMs**

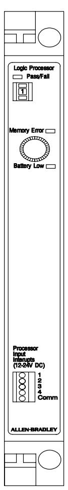
This RM:	Has this memory:
5130-RM1	192K words
5130-RM2	384K words

Data Highway/Data Highway Plus Communication Interface



Use the Data Highway / Data Highway Plus Interface (5130-KA) for additional DH/DH+ and serial communication capability. The KA has the same communication channels as the RM. You can have up to four KAs in a Pyramid Integrator chassis. The KA does not provide a data table.

Logic Processor



The logic processor (5250-LP1, -LP2, -LP3, -LP4) executes control logic. Input data can come from other Pyramid Integrator modules in the local chassis and from devices connected to the RM or KA via a DH or DH+ link.

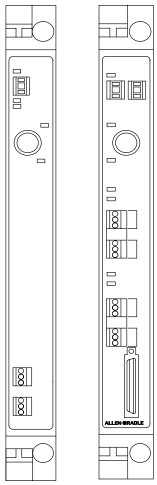
You can have up to four LPs in one Pyramid Integrator chassis. Each LP executes its own ladder-logic program.

The LP has memory for storing ladder-logic programs and data tables. The PLC-5/250 processor stores and executes compiled instruction code, which executes faster than interpreted code.

Table 2.C
Selecting LPs

Logic Processor Memory Size	PLC-3® Equivalent Program Size (Worst Case)	PLC-3 Equivalent Program Size (Typical)	Cat. No.	Maximum Data Table Size	Comments
256K words	42K words	84K words	5250-LP1	256K words	Actual equivalent will vary, depending on program structure, instruction mix, and other factors.
512K words	85K words	170K words	5250-LP2	512K words	
1024K words	170K words	340K words	5250-LP3	1024K words	
2048K words	341K words	682K words	5250-LP4	1024K words (not 2048)	

I/O Scanners



The I/O scanners (5150-RS2, -RS5) interface with 1771 remote I/O adapters and other adapters that are compatible with the Allen-Bradley remote I/O link. The I/O scanners store I/O image tables that the logic processor can read from and write to; and they perform I/O scans independent of and asynchronous to the program scan.

In addition, the remote/local I/O scanner (5150-RS5) has a local I/O channel that links to a 1771-ALX adapter residing in a 1771 I/O chassis.

The RS2 and RS5 both contain I/O image files that store input and output data. Scanner memory also contains block-transfer data, block-transfer control information, and internal storage data.

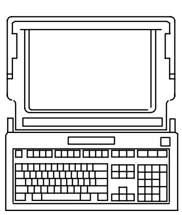
Other Pyramid Integrator Modules

The PLC-5/250 processor system is one possible configuration for a Pyramid Integrator system. There are other modules available for a Pyramid Integrator system:

- OSI Interface
- MicroVAX Information Processors
- Ethernet Interface
- CVIM™ Modules

For more information about these modules, see the Pyramid Integrator System System Overview, publication 5000-2.3.

Programming Terminal



Connect a programming terminal to the RM or a KA. Use the programming terminal to program and monitor this PLC-5/250 processor as well any processor on any DH+ link in your system.

These terminals have been tested as programming devices for the PLC-5/250 processor using the DOS version of 6200 PLC-5/250 Programming Software, release 4.1 and later.

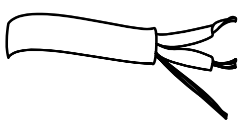
Programming Terminal	Operating Systems
• 1784-T47 • 6160-T53 • 6160-T60 • 6160-T70	MS-DOS 3.2, 3.3, 4.x, 5, or 6

These computers and terminals have been tested with the VAX/VMS version of 6200 Series PLC-5/250 Programming Software, release 4.1 and later.

Computer	Programming Terminal	Operating System
• VAX® • MicroVAX® • VAXstation™ • MicroVAX Information Processor	DEC VT200 series and higher	• VAX/VMS version 5.4 and later • Optional INTERCHANGE™ (5730-DTLS, 5830-VS) version 3.1 and later • Optional 6001NET (6001-A1DB, -G1DB) version 2.5 and later

Cables

When planning your system, be aware of maximum cable lengths for DH+ and I/O links.   Also, consider which cable you will need to connect the processor to a programming terminal.



Connecting to DH+ or Remote I/O Links

Select your cable lengths for DH+ or remote I/O link from Table 2.D.

Table 2.D
Maximum Cable Length per Communication Rate

To connect a PLC-5 processor to:	At transmission rate:	Use this maximum cable length:
DH+ link	57.6 kbps 115.2 kbps	10,000 ft 5,000 ft
Remote I/O link	57.6 kbps 115.2 kpbs 230 kbps	10, 000 ft 5,000 ft 2,500 ft

Connecting to Resource Manager Channel 1 (Serial)

See Table 2.E for information about the maximum cable lengths used with channel 1 on the RM.

Table 2.E
Cable Lengths per Communication Rate for RM Channel 1

RS Port	Transmission Rate	Maximum Cable Length
232C	110 - 19.2 k bps	50 ft
422	19.2 k bps	200 ft
423	9600 bps	400 ft

Connecting a Processor to a DOS Programming Terminal

You can connect your DOS programming terminal to a PLC-5/250 processor by:

- direct connection to the DH+ link (RM or KA channel 2A)
- remote connection (DH+ to DH to DH+, still through RM channel 2A)
- remote DH+ connection (RM or KA channel 2B or 3)
- serial connections (RM or KA channel 1)

The cable that you use to connect a processor to a programming terminal depends on the communication device you use. Table 2.F lists the cables that you need for different configurations.

Table 2.F
Cables for Connecting a DOS Programming Terminal

If you have this device:	With this device:	Use this cable:
T53, T60, IBM PC XT/AT (or compatible)	1784-KT	1784-CP 1784-CP2 1784-CP3 1784-CP5 1784-CP6/A
IBM PS/2™(MCA)	1784-KT2	
6121, 6122	1784-KTK1	
6123, 6124	1784-KT2	
T53, T60, 6121, IBM PC/AT (or compatible), IBM PS/2	1785-KE	1784-CAK
6123, 6124, IBM PC/XT	1785-KE	1784-CXK
6120, 6122	1785-KE	1784-CYK
Notebook Computer with PCMCIA Slot[1]	1784-PCMK	1784-PCM5

[1] For a list of notebook computers that are currently certified for use with the PCMK card and 6200 Series Programming Software, contact your local Allen-Bradley office or distributor.

You can also use a 1770-KF2/B communication interface to connect to a PLC-5/250 processor. You build your own cables to connect your programming terminal via the COM1 or COM2 serial ports to the 1770-KF2/B. For the cable pin assignments, see the Pyramid Integrator Installation Manual, publication 5000-6.2.10.

Connecting a Processor to a VAX

You can connect your VAX to a PLC-5/250 processor by:

- serial to DH+ connection (RM or KA channel 1)
- PI MicroVAX using INTERCHANGE connection
- VAX processor on Ethernet using INTERCHANGE connection

The hardware that you use to connect a processor to a VAX depends on the communication connection that you use. Table 2.G lists the hardware that you need for different configurations.

Table 2.G
Hardware for Connecting to a VAX

If you:	Use these devices:
Have a serial to DH+ link	Optional terminal server: DECserver Module 100 or 200 1785-KE or 1785-KF2/B
Are using INTERCHANGE 5730-DTLS	PI MicroVAX Information Processor
Are using INTERCHANGE 5830-VS	Ethernet Interface

Chapter 3

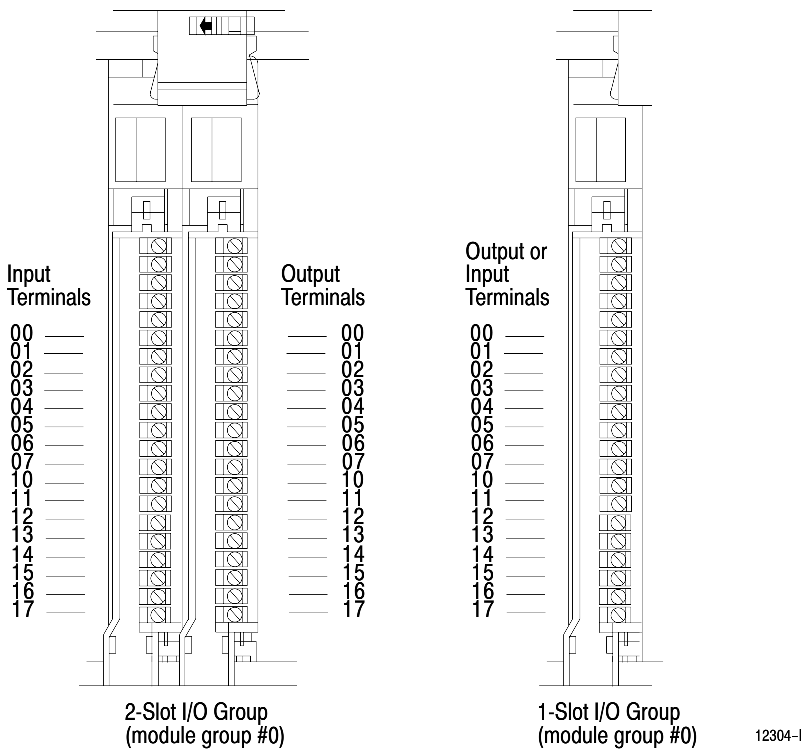
I/O Addressing

Chapter Objectives

This chapter covers I/O addressing modes, rack designation, and group designation.

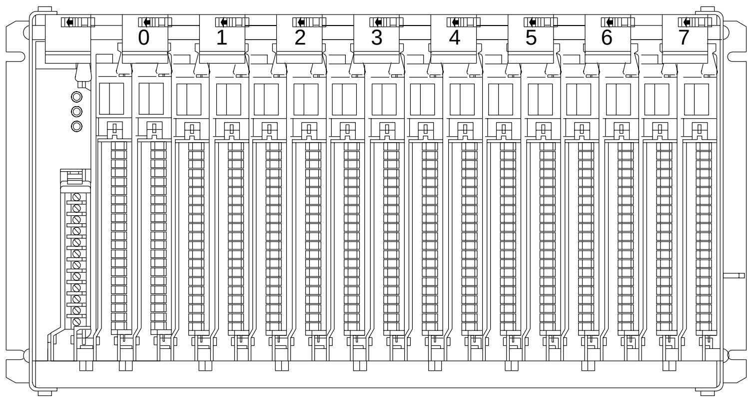
Each I/O scanner has at least two channels for links to remote I/O chassis. The I/O in these chassis can be in 2-slot, 1-slot, and 1/2-slot I/O groups. One **I/O group** corresponds to 16 input bits and 16 output bits of the I/O image table (Figure 3.1). An I/O group can contain up to 16 inputs and 16 outputs.

Figure 3.1
Example of an I/O Group



An **I/O rack** consists of up to 8 I/O groups. A rack is an addressing unit that corresponds to up to 8 input words and 8 output words in the I/O image table. Depending on the I/O chassis size and the I/O group size, an I/O rack can occupy a fraction of a chassis, a full chassis, or multiple chassis. Figure 3.2 shows one I/O rack in one full chassis.

Figure 3.2
Example of One I/O Rack (8 I/O Groups)



You can divide a remote I/O rack number between multiple I/O chassis. Also, with 1-slot addressing or 1/2-slot addressing, an I/O chassis can contain more than one I/O rack.

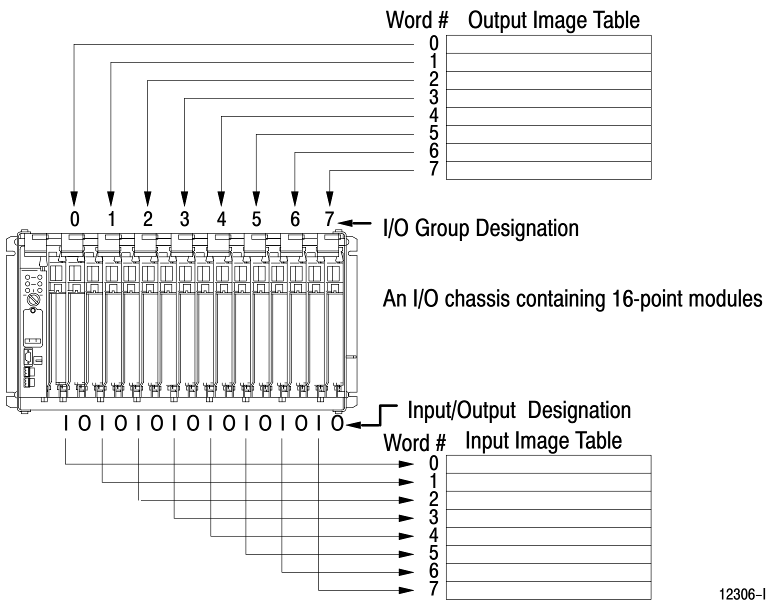
2-Slot Addressing

When you use **2-slot addressing**, the I/O scanner addresses two I/O module slots as one I/O group. Each physical 2-slot I/O group corresponds to one word (16 bits) in the input image table and one word (16 bits) in the output image table. The type (unidirectional or bi-directional) and density of a module that you install determines the number of bits that are used in each word.

Use either 8-point or 16-point I/O modules with 2-slot addressing. Because each 16-point module uses a full word in the image table, the only type of module that you can install in a 2-slot I/O group with a 16-point input module is an 8- or 16-point output module and vice versa. You cannot use 32-point I/O modules if you select 2-slot addressing.

Figure 3.3 shows how to place input and output modules when you use 2-slot addressing.

Figure 3.3
Placing Input and Output Modules When You Use 2-Slot Addressing



1-Slot Addressing

When you use **1-slot addressing**, the I/O scanner addresses one I/O module slot as one I/O group. Each physical slot in the chassis corresponds to an input (16 bits) and output (16 bits) image-table word. The type (unidirectional or bi-directional) and density of a module that you install determines the number of bits used in these words.

If you use an 8-point I/O module, the I/O scanner only uses 8 bits of the I/O image table words for that slot. If you use a 16-point I/O module, the I/O scanner uses 16 bits of the I/O image-table words for that slot.

If you use a 32-point I/O module, the I/O scanner needs 32 input and/or 32 output bits. Only 16 input bits and 16 output bits are available for each 1-slot I/O group. To address a 32-point module, the I/O scanner uses the address of the unused input or output word associated with the adjacent I/O slot within an even/odd pair of slots (under the same retention tab).

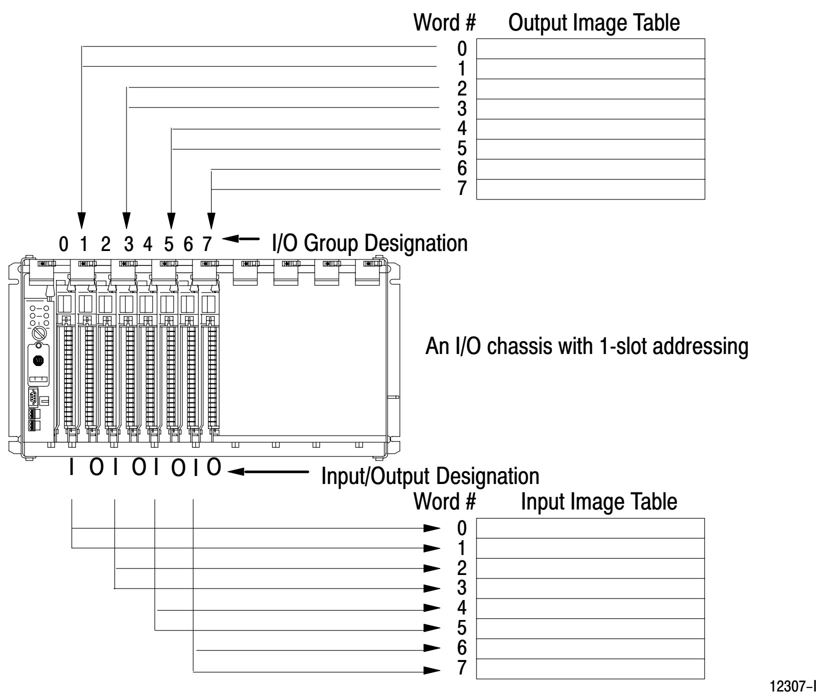
To use 32-point I/O modules with 1-slot addressing, you must install as a pair:

- a 32-point input module and an 8-, 16-, or 32-point output module
- a 32-point output module and an 8-, 16-, or 32-point input module

in two adjacent slots of the I/O chassis (under the same retention tab). If you cannot pair the modules in this way, one of the two slots of the pair must be empty. If I/O chassis slot 0 holds a 32-point input module, for example, I/O chassis slot 1 can hold an 8-, 16-, or 32-point output module—or the slot must be empty.

Figure 3.4 shows an example of how to place 32-point input and output modules when you use 1-slot addressing.

Figure 3.4
Placing Input and Output Modules When You Use 1-Slot Addressing



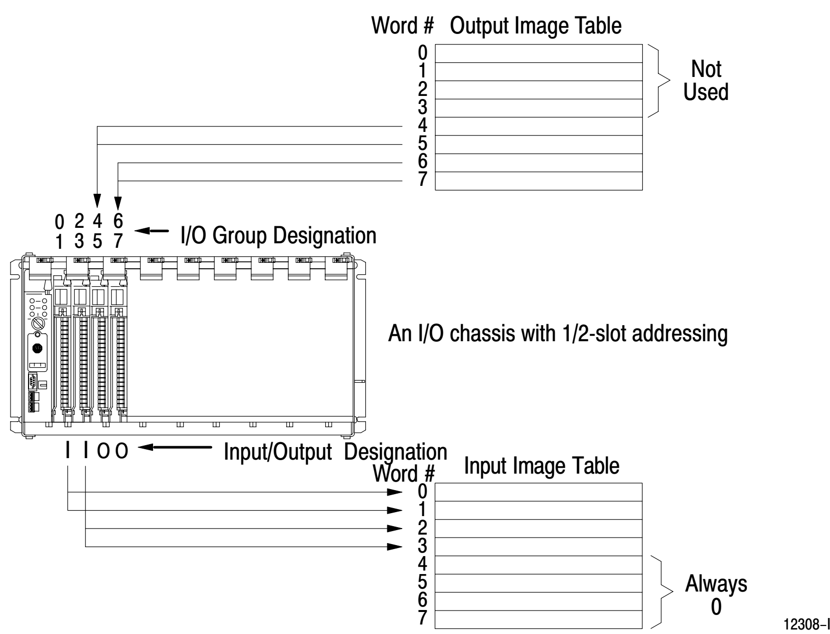
1/2-Slot Addressing

When you select **1/2-slot addressing,** the I/O scanner addresses one-half of an I/O module slot as one I/O group. Each physical slot in the chassis corresponds to two input and two output image-table words. The type (unidirectional or bi-directional) and density of the module that you install determines the number of bits that are used in each word.

If you use 8-point or 16-point modules, the I/O scanner uses 8 or 16 bits of the I/O image-table words available for that slot. You can mix 8-point, 16-point, and 32-point modules (input, output, or bi-directional) in any order in the I/O chassis.

Figure 3.5 shows an example of how to place 32-point input and output modules when you use 1/2-slot addressing.

Figure 3.5
Placing Input and Output Modules When You Use 1/2-Slot Addressing



Rack Numbers

The number of racks in an I/O chassis depends on the chassis size and the addressing mode. Table 3.A summarizes the relationship between chassis size, addressing mode, and the number of I/O racks in a chassis.

Table 3.A
How Chassis Size and Backplane Addressing Determine the Quantity of Logical Racks

If you are using this chassis size:	With 2-slot addressing, number of rack(s):	With 1-slot addressing, number of rack(s):	With 1/2-slot addressing, number of rack(s):
4-slot	1/4 rack	1/2 rack	1 rack
8-slot	1/2 rack	1 rack	2 racks
12-slot	3/4 rack	1 1/2 rack	3 racks
16-slot	1 rack	2 racks	4 racks

Each RS2 can support up to 8 logical I/O racks; each RS5 can support up to 32. You can assign a remote I/O rack to:

- a fraction of a chassis
- a single chassis
- multiple chassis

Duplicate I/O Addressing

When you need more than 1024 I/O total on the two I/O links to an RS2, you cannot configure the system with a unique address for each I/O module. You can configure one I/O chassis for all 8 I/O groups of an I/O rack on one I/O link, and duplicate those addresses in another I/O chassis on the other I/O link (complementary I/O).

Place input modules in an I/O group on one I/O link, and place output modules in the I/O group with duplicate addresses on the other I/O link. The inputs and outputs each use only half of the I/O image for the I/O group. The inputs and the outputs compliment each other. This complimentary I/O addressing allows you to address a maximum of 1024 inputs and 1024 outputs with a single RS2.

You could also configure two output modules with duplicate addresses. The outputs would be controlled by the same output image bits. The outputs of one module could control a machine, and the outputs of the other modules could control an annunciator panel to indicate the state of the machine.

Chapter 4

Connecting to Serial, Data Highway, and Data Highway Plus Links

Chapter Objectives

This chapter describes and explains how you use the front-panel connectors on the resource manager (RM) and the Data Highway / Data Highway Plus Interface (KA). These modules provide access to serial, Data Highway (DH), and Data Highway Plus (DH+) links.

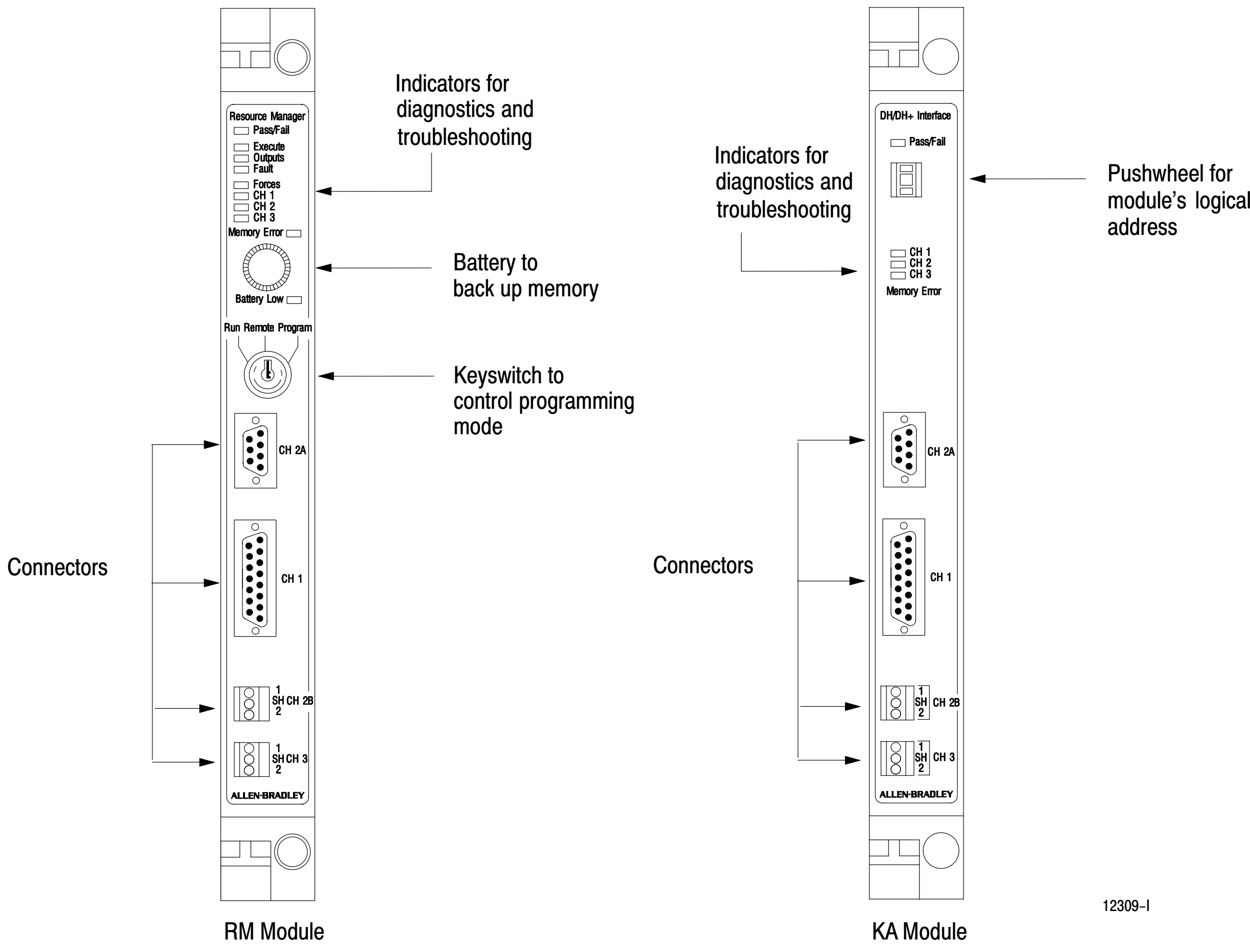
The RM and KA provide communication with plant-floor devices, such as programming terminals. Use hardware switches to select the communication protocol for one channel per module; use programming software to select the communication protocol for the other channels.

This chapter also describes how to route messages through DH+ channels on the RM and KA to other programmable controllers on other DH+ links.

Connecting Devices to an RM or KA

Every PLC-5/250 processor must have an RM. You can add a KA to provide additional communication channels. Figure 4.1 shows the front panel of an RM and a KA.

Figure 4.1
Resource Manager and DH/DH+ Interface Front Panels



Channel/ Connector	Physical Description	Functional Description	Communication Modes
1	25-pin D-shell	This port provides asynchronous serial communication. Select RS-232, RS-422, or RS-423 electrical characteristics.	ASCII DF1 Master Slave
2A	9-pin D-shell	This port is for connecting a programming terminal. This connector has parallel connections with the channel 2B connector. If a programming terminal is connected to this port, channel 2B must be configured for a DH+ link.	DH link DH+ link
2B	3-pin	This port supports DH and DH+ links. This connector has parallel connections with the channel 2A connector. If a programming terminal is connected to this port, channel 2A be configured for a DH+ link.	DH link DH+ link
3	3-pin	This port supports DH and DH+ links.	DH link DH+ link

Table 4.A through Table 4.F list the characteristics that you can configure through the software.

Table 4.A
Characteristics for Channel 1 Communications

Characteristic	Description	Values	Default
Protocol	Protocol used for CH1 communication	ASCII, DF1, master, slave, or inactive	Inactive
Message timeout period	Time resource manager waits for an answer to a message before sending an error message to the user program	0-255 sec	5 sec
Diagnostic counter file	File created and maintained by the resource manager that stores diagnostic results	0-999	None
PLC-2® / privilege station address	Specifics data table files for PLC-2 stations on the link and privilege classes assigned to any processor	Addresses: 0-376 octal Privilege classes: 1-8	None

Table 4.B
Characteristics for ASCII Protocol (Channel 1)

Use the ASCII protocol if you want to attach an ASCII device, such as a modem, plant-floor display device, or printer.

Characteristic	Description	Values	Default
Communication rate	Number of bits transferred per second	110, 300, 600, 1200, 2400, 4800, 9600, or 19200 bps	9600
Parity	Type of parity used	None, even, or odd	None
Stop bits	Number of stop bits	1, 1.5, or 2	1.5
Modem	Type of modem control	Half duplex or full duplex	Full duplex
Line length	Maximum length of a line of characters	0 to 255 characters	80
Pad characters	Null characters sent after each combination of carriage-return and line-feed characters	0 to 255	0
Expand tabs	Transmit an equivalent number of spaces for each programmed tab character	Expanded or not expanded	Not expanded
Form feed	Transmit 7 line-feed characters for each form-feed character	Expanded or not expanded	Not expanded
XON/XOFF	Respond to XON and XOFF characters	Enabled or disabled	enabled
Bits per character	Number of bits in each character	7 or 8	8
Echo	PLC-5/250 echo	Active or inactive	Active
Delete mode	Action for the processor to take when it receives an ASCII delete character from an ASCII read or read line instruction	CRT/TTY or printer	CRT
RTS to XMIT delay	Time between sending an RTS signal and start of transmission	0 to 255 increments of 25 ms	0
Termination character 1	First termination character for incoming message	Hexadecimal number	0D
Termination character 2	Second termination character for incoming message	Hexadecimal number	0A
Write append character 1	Append this character to the end of an outgoing message	Hexadecimal number	0D
Write append character 2	Append this character to the end of an outgoing message	Hexadecimal number	0A

Table 4.C
Characteristics for DF1 Protocol (Channel 1)

Use the DF1 protocol if you want peer-to-peer communications on a serial, point-to-point link.

Characteristic	Description	Values	Default
Station number	Station number of this port on the link	000 to 376 octal	003
Communication rate	Number of bits transferred per second	110, 300, 600, 1200, 4800, 9600, or 19200 bps	9600
Parity	Type of parity used	None or even	None
Error detection	Method of error detection used	BCC or CRC	CRC
ACK timeout	Time the processor waits for an ACK before considering a fault to exist	10 ms to 65 sec	100 ms
NAKs receive/retries	Number of retries if an ACK is not received	0-255	3
ENQs send	Number of times the device asks a station to re-send its last ACK or NAK	0-255	3
Privilege class	Privilege class assigned to the channel	1-8	1

Table 4.D
Characteristics for Slave Protocol (Channel 1)

Use the slave protocol if you want the processor to act as a slave on a serial link.

Characteristic	Description	Values	Default
Station number	Station number of this port on the link	000-376 octal	003
Communication rate	Number of bits transferred per second	110, 300, 600, 1200, 4800, 9600, or 19200 bps	9600
Parity	Type of parity used	None or even	None
Error detection	Method of error detection used	BCC or CRC	CRC
ACK timeout	Time the processor waits for an ACK before considering a fault to exist	10 ms to 65 sec	100 ms
Modem	Type of modem control	Half duplex or full duplex	Full
RTS to XMIT delay	Time between sending an RTS signal and start of transmission	0-255 increments of 25ms each	0
Retries	Number of retries if an ACK is not received	0-255	3
Privilege class	Privilege class assigned to the channel	1-8	1

Table 4.E
Characteristics for Master Protocol (Channel 1)

Use the master protocol if you want the processor to act as a master on a serial link.

Characteristic	Description	Values	Default
Station number	Station number of this port on the link	0-376 octal	003
Communication rate	Number of bits transferred per second	110, 300, 600, 1200, 2400, 4800, 9600, or 19200 bps	9600
Parity	Type of parity used	None or even	None
Error detection	Method of error detection used	BCC or CRC	CRC
ACK timeout	Time the processor waits for an ACK before considering a fault to exist	10 ms to 65 sec	100 ms
Modem	Type of modem control	Half duplex or full duplex	Half
RTS to XMIT delay	Time between sending an RTS signal and the start of transmission	0-255 increments of 25 ms each	0
Privilege class	Privilege class assigned to the channel	1-8	1
Priority MSG reply wait	Time the master will wait for a reply to a priority message it sends	0-255 ms	10
Polling mode	How the master polls the remote stations	Standard (poll remote stations in sequence defined by poll configuration) or message based (only master initiates communication; sends message waits for reply; stops after last reply.)	Standard
Master message transmit (if standard polling mode)	When messages from the master are transmitted	In poll sequence (the master is included in the normal poll configuration and sends its messages in its turn as defined by that file) or between station polls (after each station is polled, the master sends all of its messages)	In poll sequence
Node table file (if standard polling mode)	Number of file that stores addresses of active remote stations	File number 0-999	None
Normal poll configuration (if standard polling mode)	Defines the sequence of station polling; includes list of station addresses (may include any address multiple times) and whether to handle only one message from each station per poll or all messages.	For each station: address 000-376 octal; multiple or single message polling	None
Priority poll configuration	Lists stations to be given priority polling. Master polls priority stations, then some stations in normal poll configuration, then priority stations, etc. Group size specifies how many stations in normal poll configuration are polled between each poll of priority stations	For each station: address 000-376 octal; multiple or single message polling; group size 0-999 Priority poll configuration may contain up to 10 stations. Sum of priority poll stations and normal poll stations must be no more than 250.	None

Table 4.F
Characteristics for Channels 2A, 2B, and 3 Communications

Characteristic	Description	Values	Default
Protocol	Communication protocol used	DH or DH+	DH+
Message timeout	Time the resource manager waits for an answer to a message before sending an error message to the user program	0-255 sec	5 sec
Diagnostic counter file	Number of the file used to store diagnostic results	0-999	None
PLC-2/privilege station addresses	Specifies data table files for PLC-2 stations on the link and privilege classes assigned to any processor	For each station: station address 000-375 octal; privilege class 1-8	None
Station number (DH and DH+ links)	Station number of this port on the DH or DH+ link	0-376 octal	003
Communication rate (DH+ link only)	Number of bits transferred per second	57.6 or 115.2 kbps	57.6 kbps
Node table file (DH+ link only)	Number of the file that contains the names of other active stations on the network	0-999 (must be integer file)	None
Token pass file (DH+ link only)	Number of the file that holds a status word from each station on the network	0-999 (must be integer file)	None
Privilege class (DH and DH+ links)	Privilege class assigned to the channel	1-8	1

Configuring Communication

You must configure one channel on the RM and each KA with the switches and jumpers on the module. The other channels you configure through programming software. You can't use the software to change characteristics that are configured with switches and jumpers.
Table 4.G lists the parameters that you can configure with the hardware.

Table 4.G
Switches and Jumpers on RM and KA Modules

Characteristics	Values	Factory Setting
Channel/Protocol	Channel 3 DH Channel 2A/2B DH Channel 3 DH+ Channel 2A/2B DH+ Channel 1 Master Channel 1 Slave Channel 1 DF1 Switch Banks Inactive	Channel 2A/2B DH+
Parity	None or Even	None
Error Detection Method	BCC or CRC	CRC
Communication Rate	Channel 1 selected: 110, 300, 600, 1200, 2400, 4800, 9600, or 19200 bps Channel 2A/2B or Channel 3 selected: 57.6 or 115.2 kbps	57.6 kbps
Station Address (of Resource Manager)	000-376 octal	None
CH1 Interface	RS-232-C, RS-422 or RS-423	RS-232-C, RS-422 or RS-423
Termination Resistor for DH or DH+ Link	In or Out	Out

Routing Data Highway Plus Messages

Use DH+ routing to view applications and other information at stations on remote links and to program processors on remote links. You can also use routing to send MSG instructions to stations on remote links.
DH+ routing:

- provides a central point for programming and monitoring (although you don't need a programming terminal to use DH+ routing)
- eliminates the need for a separate drop on each link for a programming terminal
- allows a larger number of stations to communicate in a network while allowing short medium access time on small links

Figure 4.2 shows an example of basic DH+ routing. In this configuration, routing transfers data between two links only. A port on the RM accepts a message from the programming terminal; the RM routes that message out a channel on the KA to the PLC-5 processor.

Figure 4.2
Basic DH+ Routing

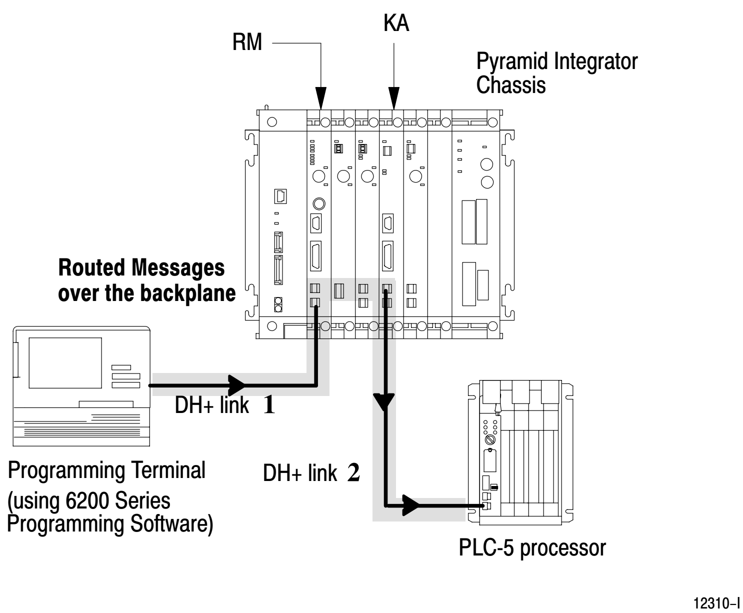
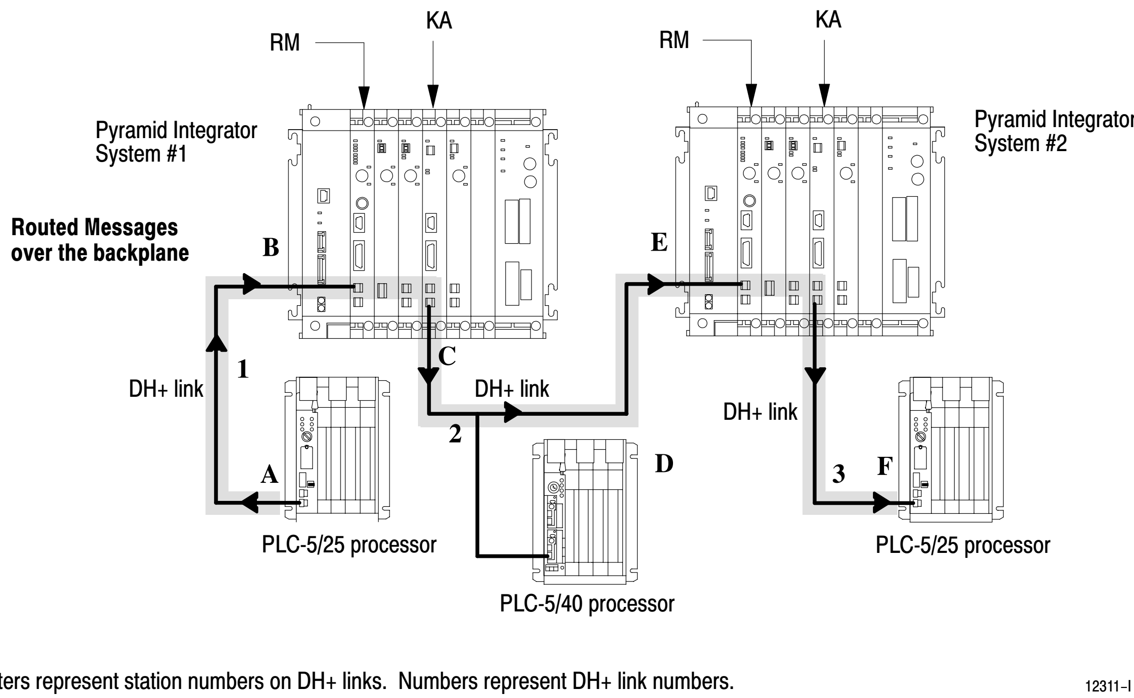


Figure 4.3 shows a more complex routing configuration. In this configuration, the PLC-5 processor (station A on link 1) can send messages to the stations identified as B, C, D, E, and F over the DH+ links identified as 1, 2, and 3. The RM and KA route messages to designated links.

Figure 4.3
Advanced DH+ Routing



Chapter 5

Connecting to I/O Links

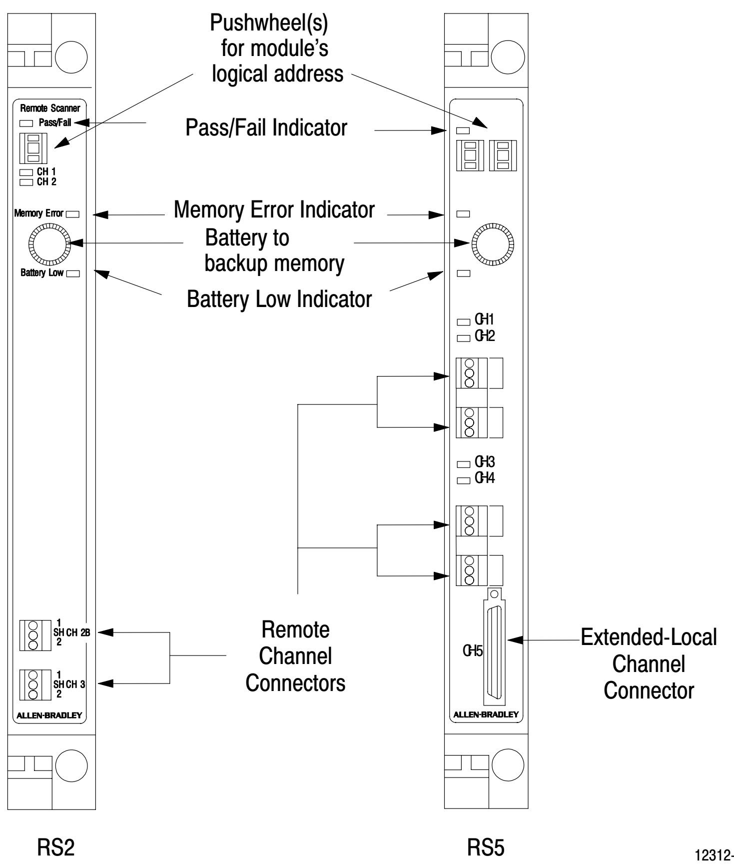
Chapter Objectives

This chapter describes and explains how you use the front panel connectors on the I/O scanner modules. The remote scanners (RSs) provide communication with remote I/O. Each RS2 has two channels that you can configure for remote-scanner or -adapter (direct communication) mode; each RS5 has four channels that you can configure for remote-scanner or -adapter (direct communication) mode as well as one extended-local channel.

Connecting Devices to a Remote Scanner

A PLC-5/250 processor can have up to four RS2 or RS5 modules. Figure 5.1 shows the front panels of the RS2 and RS5.

Figure 5.1
I/O Scanner Front Panel



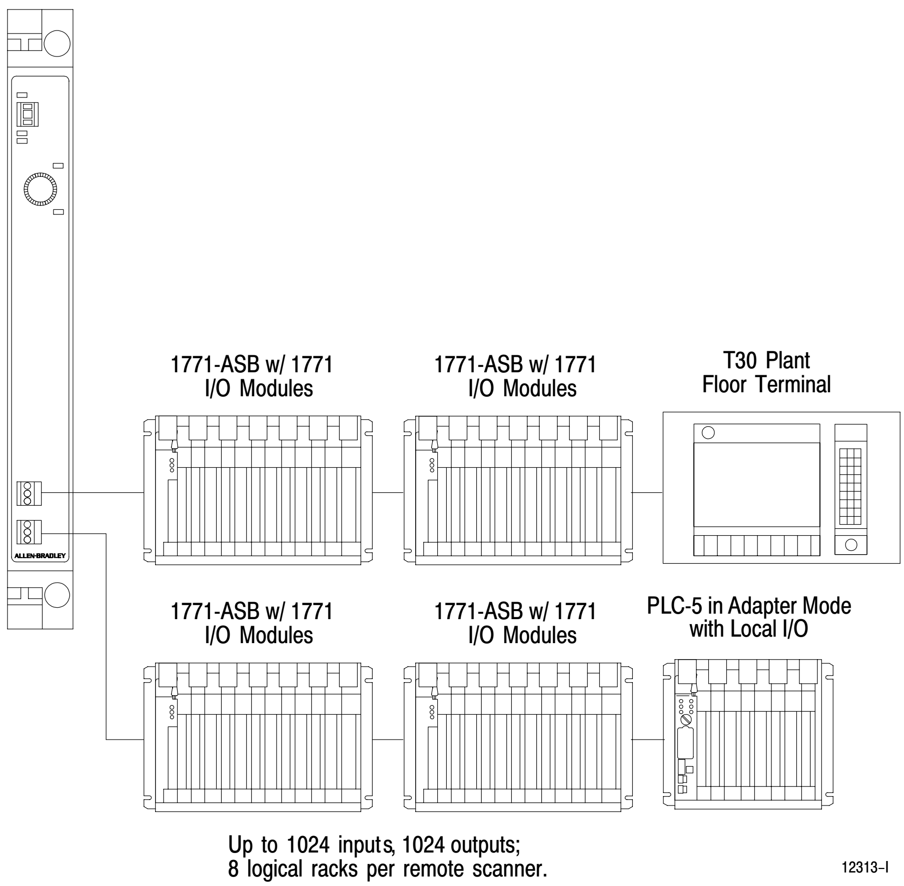
Remote I/O Link

You can use each remote channel of an RS for scanner mode or adapter (direct communication) mode.

Scanner Mode

You can configure either one or all remote channels on each RS to be in scanner mode. In scanner mode, an RS channel scans and controls its remote I/O link. The scanner-mode processor also acts as a supervisory processor to other processors in adapter mode. Figure 5.2 shows an example of an RS2 in a system set for scanner mode.

Figure 5.2
Example of an RS2 in Scanner Mode



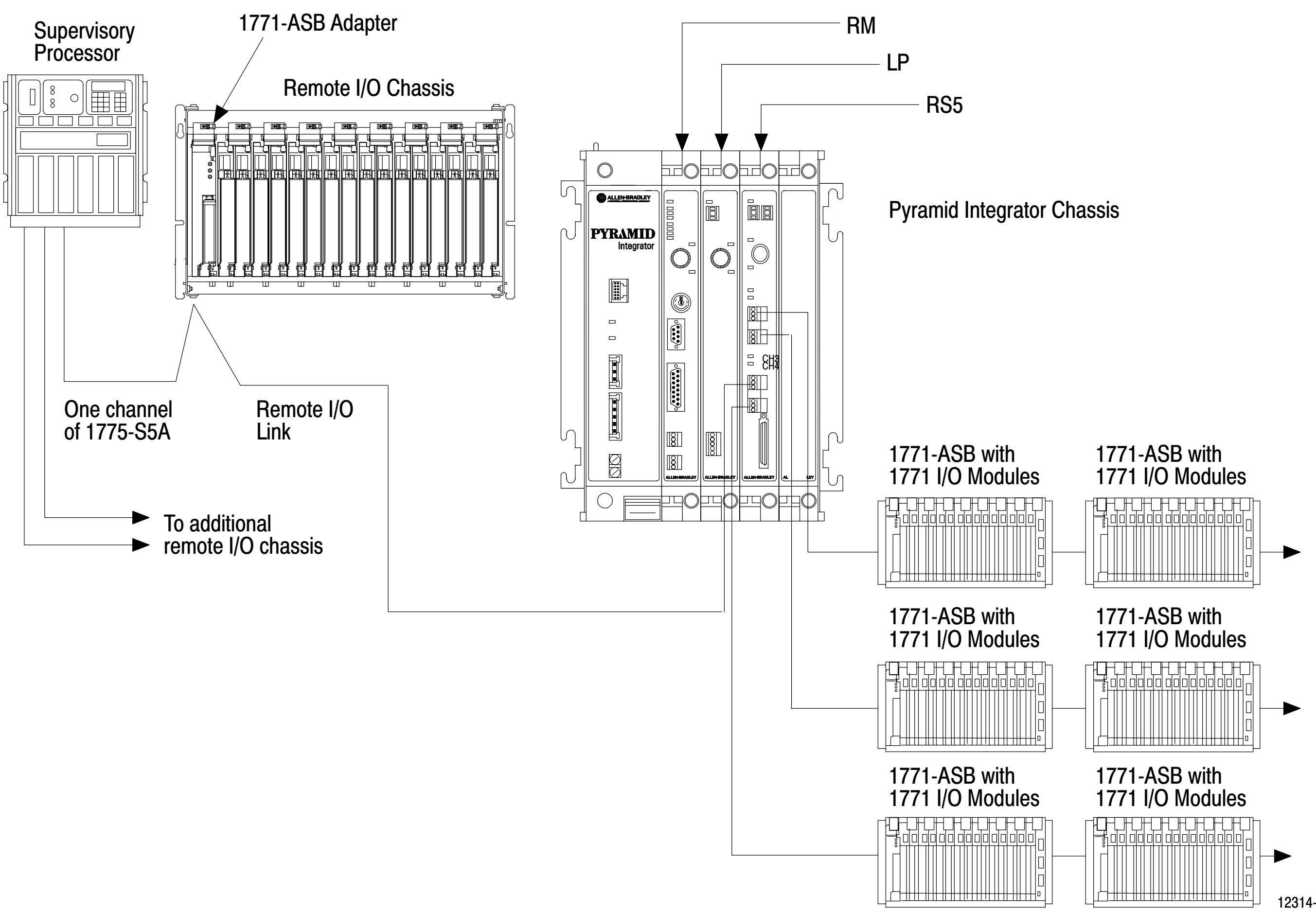
Adapter Mode

You can configure either one or both channels on each RS module to be in direct communication with a supervisory processor. In this configuration, the RS channel acts like a 1771-ASB adapter module to the supervisory processor on the remote I/O link. Possible supervisory processors are:

- PLC-3 processors
- PLC-5 processors
- PLC-5/250 processors

When an RS channel is configured for adapter mode, the PLC-5/250 processor and its supervisory processor exchange data in real time. Figure 5.3 shows an example of an RS5 in a system set for adapter mode.

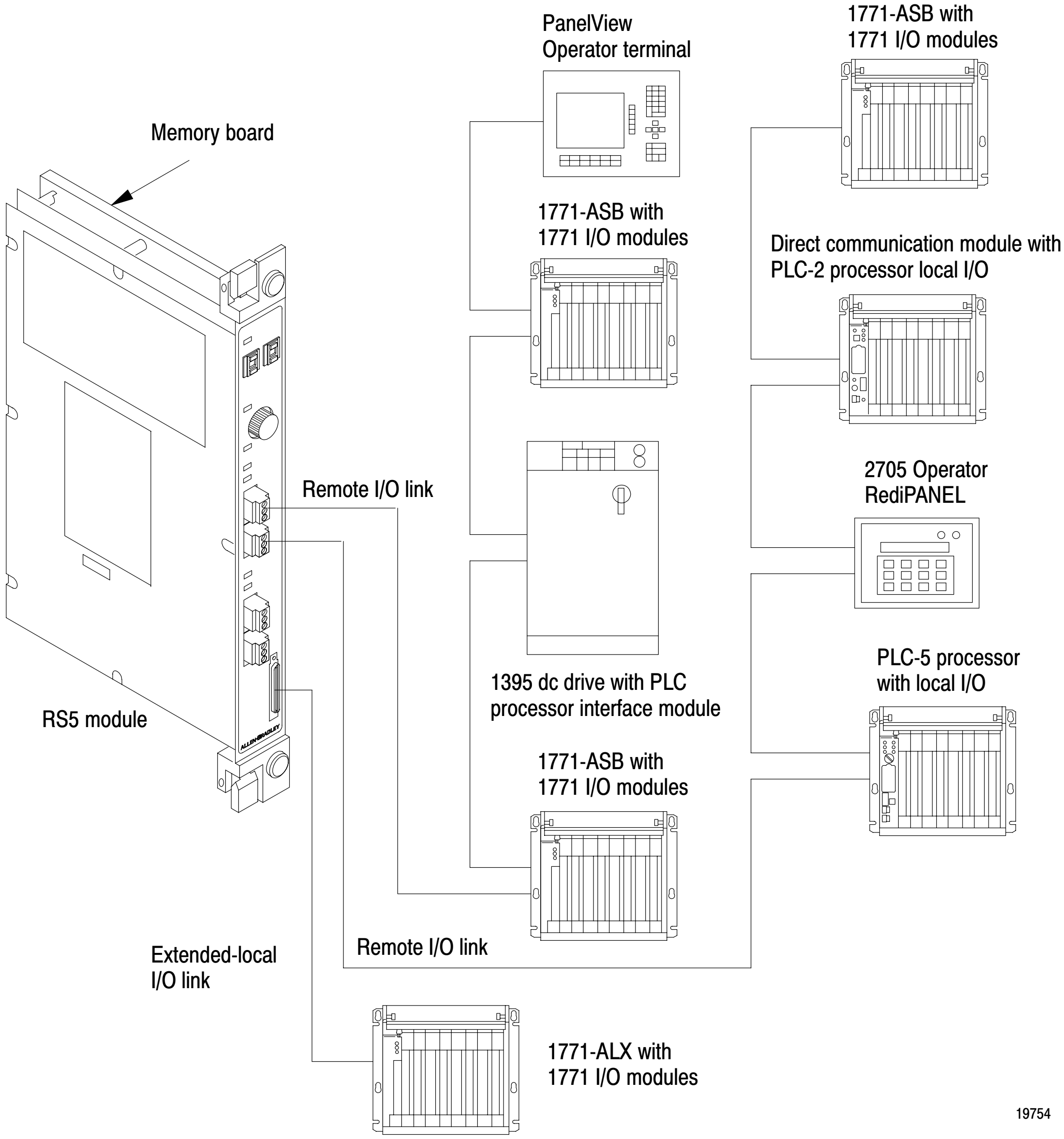
Figure 5.3
Example of an RS5 in Adapter Mode



Extended-Local I/O Link

The extended-local I/O channel on the RS5 functions similarly to the remote I/O channel, except that extended-local I/O is faster when transferring discrete and block-transfer data.

Figure 5.4
RS5 Remote and Extended-Local I/O Links



Chapter 6

Programming PLC-5/250 Processors

Chapter Objectives

This chapter explains how to:

- address data
- monitor processor status
- use the programming software
- consider special programming situations
- protect your programs

Addressing Data

PLC-5/250 processors address data in a logical format that specifies:

```
modulenumber datatype filenumber : wordnumber / bitnumber
```

Table 6.A lists the types of formats you can use to address data table files:

Table 6.A
Available Formats for Addressing Data

Type of Format	Description	Example
Logical address	An alphanumeric coded format with punctuation to specify the data location	`1N7:0`
I/O image address	Logical address format, but relates physical locations in the I/O chassis to memory addresses in the I/O image file	`I:001/10`
Indirect address	Logical address format, but lets you change address values in the base address with your ladder program	`1N[1N8:6]:0`
Indexed address	Index prefix (#) followed by a logical address format, but adds an index value from processor status file to the base address	`#2N7:0`
Symbolic address	ASCII character name that relates the address (of a file, word, or bit) to what it represents in the application. When you enter ladder logic, use the symbols you defined rather than typing the actual address	`Mixer_1`

Table 6.B lists valid data table file-type specifications.

Table 6.B
PLC-5 Processor Data Table Memory Map

Data Section Type	Description	Stored in these Modules
AS	Adapter status	RS
B	Binary	RM, LP
BR	Block transfer read control structure	RS
BTD	Block-transfer data	RS
BW	Block transfer write control structure	RS
C	Counter	RM, LP
F	Floating point	RM, LP
I	Input image	RS
IS	Internal storage	RS
L	Long integer	RM, LP
MSG	Message control	RM
N	Integer	RM, LP
O	Output image	RS
PD	PID control	RM, LP
R	Control	RM, LP
S	Status	RM, LP
SD	Shared data	RM with CVIM
ST	String	RM, LP
T	Timer	RM, LP

PLC-5/250 Processor Status

Each module in the PLC-5/250 processor system stores status information. This status information is available through different configuration screens in the software and status files in the modules. Table 6.C lists the type of status information each module stores and where you can access the information.

Table 6.C
Processor Status

This module:	Stores this status information:	Which you access through:
RM/KA	System status Channel status	RM/KA configuration screens
LP	Main program execution Processor input interrupt (PII) execution Selectable timed interrupt (STI) execution Independent background program (IBP) execution	LP configuration screens
RS	RS channel configuration modes I/O adapter list	RS configuration screens

Programming Software

Use the 6200 Series PLC-5/250 Programming Software to configure your processor as well as to develop, edit, monitor, document, and troubleshoot your programs.

Product Offering

Table 6.D shows the 6200 software packages that are available for programming PLC-5/250 processors.

Table 6.D
6200 Series Software Products for PLC-5/250 Processors

Operating System	Catalog Number	Online Capability	Offline Capability	Upload/Download Capability
DOS	6201–PLC5 (3-1/2 inch disks)	YES	NO	DH+
	6211–PLC5 (5-1/4 inch disks)			
	6203–PLC5 (3-1/2 inch disks)	YES	YES	
	6213–PLC5 (5-1/4 inch disks)			
VMS	6223–52VDM (magnetic tape)	YES	YES	Serial to DH+
	6233–52VDM (TK50)	YES	YES	INTERCHANGE
	6233–52VTM (bundled with INTERCHANGE)	YES	YES	INTERCHANGE and Ethernet Interface

NOTES:
Online means that your programming terminal is connected to the processor and you create or edit a program directly in processor memory.

Offline means that program development and storage is internal to the programming terminal.

Connection to a PLC-5/250 processor is not required.

Software Functionality

The software is a menu-driven interface for programming and monitoring your processor. The major features of the software are:

Ladder-logic editor/monitor
Use the ladder editor to develop and monitor a ladder-logic program (Figure 6.1). You can search for and replace instructions and operands. You can cut, copy, and paste groups of rungs along with the associated instructions, addresses, and data values. The ladder editor also includes a feature for testing your edits.

Figure 6.1
Ladder Logic and Program Documentation

```
|    I:000 I:000 I:000 I:000                                             O:000 |
+-+++-] [---] [---] [-+-]/[-++-------------------------------------------( )--+
| |||   10    11    16|   12||                                              13 |
| |||I:002            |     ||                                                 |
| ||+-]/[-------------+     ||                                                 |
| ||    10                  ||                                                 |
| ||I:003 I:000             ||                                                 |
| |+-]/[---] [--------------+|                                                 |
| |    11    10              |                                                 |
| |I:003                     |                                                 |
| +-]/[----------------------+                                                 |
|     12                                                                       |
| I:001                                                                  O:005 |
+--]/[-------------------------------------------------------------------(  )--+
|    14                                                                     10 |
|                                                     +TON---------------+      |
+----------------------------------------------------+TIMER ON DELAY    +-(EN)-+
|                                                    |Timer         T4:0|      |

Press a function key for desired editing function.
FILE:1>
Rem Prog    Forces:Disabled  Edits:None                5/250  Addr 20 LIMIT
Select    Cut    Copy    Paste                   Copy    Paste
                                                To Disk Fr Disk
  F1      F2      F3      F4                      F7      F8
```

Database editor
The database editor contains all your comments and symbols. Use the database editor to edit or delete comments and symbols. You can also search for and replace character strings.

Program documentation
Specify symbols, address comments, instruction comments, and rung comments to document your programs.

Sequential function chart editor/monitor
Use the sequential function chart (SFC) editor to develop and monitor an SFC. The SFC editor provides multiple display modes, searching and replacing, and “zoom” to move between the ladder editor and the SFC editor.

The SFC editor lets you enter only correct step and transition pairs. Figure 6.2 shows a sample SFC.

Figure 6.2
Sequential Function Chart

```
  START
+---+---+
+===+===+
| 1::000|
+===+===+
   -+-
  1::000
    |
+---+---+
| 1::001|
+---+---+
   -+-
  1::000
    |
+---+---+
| 1::002|
+---+---+

Press a function key.
EDIT (0,0) >
Rem Prog   SFC Frc:ENABLED                              5/250  Addr 20  LIMIT
Sel Brn Sim Brn Append  Insert  Modify  Delete   Undel   Label  Config/  Macro
   *       *    Stp/Trn Stp/Trn Stp/Trn Stp/Trn Stp/Trn  /GoTo   Build     *
  F1      F2      F3      F4      F5      F6      F7      F8      F9      F10
```

Reports

The programming software can generate and print reports. These reports are: ladder-program listing, ladder cross-reference, SFC listing, SFC cross-reference, memory map, processor status, I/O status, data table, force status, symbol table, unused addresses, memory usage, program directory, and privilege class.

Configuration for your application

You can configure the software so that it best fits your application. Choose display colors on color monitors, define directory paths for files, and select display options for the ladder editor and SFC editor.

The programming software also provides the following functions:

- **Hot keys**—`[Alt]` keys for short cuts to software functions
- **File management**—create, delete, rename, and merge program files
- **Memory map**—display processor memory usage
- **Data monitor**—display the contents of data files
- **Save and restore**—save processor memory files to disk; restore processor memory files from disk
- **I/O configuration**—configure intelligent I/O modules
- **Processor mode change**—when the keyswitch is in `Remote` position, change mode to Program, Test, or Run via software
- **Histogram**—display information about specific data locations over time
- **Forcing**—force I/O on and off
- **Import and export**—convert database files and processor memory files to ASCII for use with your own word processor and from ASCII to the 6200 format for use with the current processor memory file

Programming Considerations

Table 6.E lists some features to consider when you design your system.

Table 6.E
Programming Considerations

Programming Consideration	Comment
I/O update	You can configure LPs for synchronous or asynchronous I/O update. In synchronous I/O mode, the LP reads the input image files of the RSs once per program scan and stores a copy in LP memory. Output data are updated asynchronously. In asynchronous I/O update, changes in inputs are read by the LP directly from the RS as requested by the ladder program. The LP doesn't store a copy of I/O image; it uses the I/O image files from the RS.
Selectable timed interrupt (STI)	Use selectable timed interrupts (STIs) when time-driven events interrupt the logic processor. You specify the time between interrupts for a specific STI as multiples of 10ms. You can configure up to 8 STIs per logic processor. To enable an STI, store the STI program file descriptor (STEP file) and interrupt time on the configuration screen for the associated LP module.
Processor input interrupt (PII)	Use processor input interrupts (PIIs) in high-speed processing applications, where, based on input the processor receives, the processor interrupts the active program to run the specified PII program file. For each PII, specify the filter constant in μs (the time that an input must be true before the LP runs the PII). You can configure up to 4 PIIs per logic processor. To enable a PII, store the PII program file descriptor (STEP file) and filter constant on the configuration screen for the associated LP module.
Independent background program (IBP)	Use independent background programs (IBPs) to run ladder programs independent of the main ladder program. Use IBPs for such tasks as time-consuming computations and data manipulations, or fault recording and fault reporting. You can enable an IBP through the IBP instruction in ladder logic or you can configure an IBP through the LP configuration screens. You can have up to 4 IBP tasks per logic processor with up to 32 IBP programs (IBP files) per task.
Time periodic communication (TPC)	Use time periodic communications (TPCs) to send message (MSG) instructions based on time intervals, independent of program scan. You can configure up to 8 TPCs per each RM and KA. You enable TPCs through the RM/KA configuration screens. When you configure a TPC, you specify the MSG control structure and the time interval.
Fault routine	You can use a fault routine to specify how a system responds to a major fault. You can have as many fault routines as you want; but the logic processor will only run the fault routine that is specified in the system configuration. To enable a fault routine, store the program file descriptor (IBP file) on the configuration screen for the associated system.
Power-up routine	You can use a power-up routine to provide protection from powering up in run mode when the processor recovers from a power loss. Use the power-up routine to set initial data conditions or to direct program execution to begin at either a start-up or re-start initial step in the SFC. You can have as many power-up routines as you want; but the logic processor will only run the power-up routine that is specified in the system configuration. To enable a power-up routine, store the program file descriptor (IBP file) on the configuration screen for the associated system.
Scanner mode	In scanner mode, the RS channel performs single transfers with each adapter on the associated I/O link. The same RS channel also performs block-transfers with any block transfer module in the chassis with the adapters.
Adapter mode (direct communication mode)	An RS channel in adapter mode can scan its remote I/O and communicate with a supervisory processor. In adapter mode, the RS remote channel: • acts as a 1771–ASB module to the supervisory processor • transfers I/O data and status data using discrete and block transfers

Protecting Your Programs

You can define up to 8 privilege classes (class 1–8), each with a different set of abilities and passwords. Use privileges to restrict access. You can assign:

- read and write privileges to individual program files and data files
- privilege class to a channel
- privilege class to a station

Table 6.F describes the abilities that you can define for each privilege.

Table 6.F
Abilities Available per Privilege Class

This ability:	Lets you:
Privilege Modification	Change class privileges (This ability cannot be deleted from privilege class 1)
Data Table File Create/Delete	Create or delete data table files
Program File Create/Delete	Create or delete program files
ASCII Extended Address	Use ASCII extended addresses (e.g. 3.2.8.256.23)
Logical Write	Restore a processor memory file with a logical address
Physical Write	Restore a processor memory file with a physical address
Physical Read	Save a processor memory file with a physical address
Public Status Write	Write to system memory, even though all users have read access to this area
Private Status Write	Write to system memory when read access is also limited
Symbol Create/Delete	Enter or change a symbol for a device in the symbol table (Note: a program name is a symbol)
Input Image Write	Enter or change input data (I:n)
Output Image Write	Enter or change output data (O:n)
Internal Storage Write	Enter or change internal storage data (IS:n)
BT Data Write	Enter or change block transfer data (BTD:n)
BT Control Write	Enter or change the control word of a block transfer
Adapter Status Write	Enter or change I/O adapter status data (AS:n)
Shared Data Write	Enter or change shared data (SD:n)
Mode Change	Change processor mode through the programming software when the keyswitch on the RM is in Remote
Configuration	Change system parameters through the programming software
Program Edit	Edit a ladder program file
I/O Force	Enable or disable forces in the system, force individual transitions on or off, or to clear all system forces
SFC Force	Enable or disable SFC forces, force individual transitions on or off, or to clear all SFC forces
Clear Fault	Clear major or minor faults through the programming software
Clear Memory	Clear processor memory
Save/Restore	Save, restore, or merge a processor memory file
SFC Edit	Edit an SFC

Instruction Set Quick Reference

The following table shows an example of each of the available PLC-5/250 instructions and provides a brief description of each example.

Table 7.A
Available PLC-5/250 Instructions

Category	Instruction		Description
Relay Instructions	I:012] [07	Examine On XIC	Examine bit I:012/07, which corresponds to terminal 7 of an input module in I/O rack 1, I/O group 2. If this bit is on (1), the rung element is true.
	I:012]/[07	Examine Off XIO	Examine bit I:012/07, which corresponds to terminal 7 of an input module in I/O rack 1, I/O group 2. If this bit is off (0), the rung element is true.
	O:013 ( ) 01	Output Energize OTE	If the rung is true, turn on (1) bit O:013/01, which corresponds to terminal 1 of an output module in I/O rack 1, I/O group 3. (If the rung is false, turn off (0) bit O:013/01.)
	O:013 (L) 01	Output Latch OTL	If the rung is true, turn on (1) bit O:013/01, which corresponds to terminal 1 of an output module in I/O rack 1, I/O group 3. This bit remains on until an OTU instruction or other logic turns off the bit.
	O:013 (U) 01	Output Unlatch OTU	If the rung is true, turn off (0) bit O:013/01, which corresponds to terminal 1 of an output module in I/O rack 1, I/O group 3. This bit remains off until an OTL instruction or other logic turns on the bit.
	012 (IIN)	Immediate Input IIN	If the rung is true, update the 16 input image bits in I/O rack 1, I/O group 2 before the next synchronous input image update. The PLC-5/250 does not have an immediate output (IOT) instruction because the processor immediately updates the output image table when a corresponding instruction is scanned.

Category	Instruction		Description
Timer and Counter Instructions	TON TIMER ON DELAY Timer 1T4:1 Time Base 1.0 Preset 180 Accum 0	Timer On Delay TON	If the input conditions go true, logic processor 1 increments its timer 1 of file 4 in 1-second intervals as long as the rung conditions remain true. When the rung goes false, the accumulated value goes to 0. When the accumulated value is equal to the preset value (180), the timer stops and sets the timer done bit.
	TOF TIMER OFF DELAY Timer 1T4:1 Time Base 1.0 Preset 180 Accum 0	Timer Off Delay TOF	If the input conditions are false, logic processor 1 increments its timer 1 of file 4 in 1-second intervals as long as the rung conditions remain false. When the rung goes true, the accumulated value goes to 0. When the accumulated value is equal to the preset value (180), the timer stops and resets the timer done bit.
	RTO RETENTIVE TIMER ON Timer 1T4:10 Time Base 1.0 Preset 10 Accum 0	Retentive Timer On RTO	If the input conditions go true, logic processor 1 increments its timer 10 of file 4 in 1-second intervals as long as the rung remains true. When the rung goes false, the timer stops but retains the accumulated value. If the rung goes true again, the timer continues. When the accumulated value is equal to the preset (10), the timer stops and sets the timer done bit.
	GTN GLOBAL TIMER ON Timer 1T4:10 Time Base 1.0 Preset 10 Accum 0	Global Timer On GTN	If the input conditions go true, logic processor 1 increments its timer 10 of file 4 in 1-second intervals. Once enabled, the GTN instruction continues to time an operation until the accumulated value equals the preset (10), the GTN instruction is turned off by a global timer off (GTF) instruction, or the GTN instruction is reset by a reset (RES) instruction.
	GTF GLOBAL TIMER OFF Timer 1T4:10 Time Base 1.0 Preset 10 Accum 0	Global Timer Off GTF	If the input conditions go true, logic processor 1 stops incrementing its timer 10 of file 4, but retains the accumulated value.
	CTU COUNT UP Counter 1C4:0 Preset 4 Accum 0	Count Up CTU	Logic processor 1 increments counter 0 of file 4 by 1 each time the rung goes from false to true. When the accumulated value is greater than or equal to the preset value (4), the counter sets the counter done bit.
	CTD COUNT DOWN Counter 1C5:1 Preset 10 Accum 35	Count Down CTD	Logic processor 1 decrements counter1 of file 5 by 1 each time the rung goes from false to true. When the accumulated value is less than the preset (10), the counter resets the counter done bit.
	1T4:1 ——(RES)——	Timer and Counter Reset RES	If the input conditions are true, logic processor 1 resets its timer1 of file 4. This instruction resets timers and counters, as well as control words and MSG instructions.

Category	Instruction		Description
Compare Instructions	CMP COMPARE Expression 1N7:5 < 1N7:10	Compare CMP	If the compare expression is true, this rung element is true. The CMP instruction can perform these operations: equal (=), less than (<), less than or equal (<=), greater than (>), greater than or equal (>=), not equal (<>), AND, logical AND (LAND), OR, logical OR (LOR), logical exclusive OR (LXOR), NOT, logical NOT, add (+), subtract (–), multiply (*), divide (|), modulo divide (MOD), negate (–), exponential (**), shift left (<<), shift right (>>). The CMP instruction can perform these conversion operations: floating point (FLT), integer (INT), radians (RAD), degrees (DEG), to BCD (TOD), from BCD (FRD), A-B floating point (ABF), IEEE floating point (IEF). The CMP instruction can perform these manipulation operations: absolute value (ABS), sign detector (SGN), square root (SQR), round (RND), truncate (TRN), minimum (MIN), maximum (MAX), pi (PI), log base 10 (LOG), inverse natural log (EXP), random number generator (RAN), random number seed (RAS). The CMP instruction can perform these trigonometric functions: sine (SIN), cosine (COS), tangent (TAN), inverse tangent (ATN), inverse tangent to a line (ATN2).
	EQU EQUAL Source A 1N7:5 Source B 1N7:10	Equal to EQU	If the value in Source A (1N7:5) is equal to the value in Source B (1N7:10), the rung element is true.
	GEQ GRTR THAN OR EQUAL Source A 1N7:5 Source B 1N7:10	Greater than or Equal GEQ	If the value in Source A (1N7:5) is greater than or equal to the value in Source B (1N7:10), the rung element is true.
	GRT GREATER THAN Source A 1N7:5 Source B 1N7:10	Greater than GRT	If the value in Source A (1N7:5) is greater than the value in Source B (1N7:10), the rung element is true.
	LEQ LESS THAN OR EQUAL Source A 1N7:5 Source B 1N7:10	Less than or Equal LEQ	If the value in Source A (1N7:5) is less than or equal to the value in Source B (1N7:10), the rung element is true.
	LES LESS THAN Source A 1N7:5 Source B 1N7:10	Less than LES	If the value in Source A (1N7:5) is less than the value in Source B (1N7:10), the rung element is true.

Category	Instruction		Description

	LIM
	LIMIT TEST (CIRC)
	Low limit 1N7:10
	Test 1N7:15
	High limit 1N7:20
		Limit Test
		LIM
			If 1N7:10 is less than or equal to 1N7:20, then
			If the Test value (1N7:15) is greater than or equal to the Low Limit (1N7:10) and less than or equal to the High Limit (1N7:20), the rung element is true.
			If 1N7:10 is greater than 1N7:20, then
			If the Test value (1N7:15) is equal to or outside the limits, the rung element is true. If the Test value (1N7:15) is between or not equal to either limit, the rung element is false.

	MEQ MASKED EQUAL Source 1N7:5 Mask 1N7:6 Compare 1N7:10	Mask Compare Equal MEQ	The processor takes the value in the Source (1N7:5) and passes that value through the Mask (1N7:6). Then the processor compares the result to the Compare value (1N7:10). If the result and the comparison value are equal, the rung element is true.
	NEQ NOT EQUAL Source A 1N7:5 Source B 1N7:10	Not Equal NEQ	If the value in Source A (1N7:5) is not equal to the value in Source B (1N7:10), the rung element is true.
Compute Instructions	CPT COMPUTE Dest 1N7:3 Expression N7:4 – (N7:6 * N7:10)	Compute CPT	If the input conditions go true, evaluate the Expression and store the result in the Destination (1N7:3). The CPT instruction can perform these operations: AND, OR, exclusive OR (XOR), NOT, add (+), subtract (–), multiply (*), divide (|), modulo divide (MOD), negate (–), exponential (**), shift right (>>), shift left (<<). The CPT instruction can perform these conversion operations: floating point (FLT), integer (INT), radians (RAD), degrees (DEG), to BCD (TOD), from BCD (FRD), A-B floating point (ABF), IEEE floating point (IEF). The CPT instruction can perform these manipulation operations: absolute value (ABS), sign detector (SGN), square root (SQR), round (RND), truncate (TRN), minimum (MIN), maximum (MAX), pi (PI), log base 10 (LOG), inverse natural log (EXP), random number generator (RAN), random number seed (RAS). The CPT instruction can perform these trigonometric functions: sine (SIN), cosine (COS), tangent (TAN), inverse tangent (ATN), inverse tangent to a line (ATN2).
	ADD ADD Source A 1N7:3 Source B 1N7:4 Dest 1N7:12	Addition ADD	When the input conditions are true, add the value in Source A (1N7:3) to the value in Source B (1N7:4) and store the result in the Destination (1N7:12).

Category	Instruction		Description
	CLR CLR Dest 1N7:3	Clear CLR	When the input conditions are true, clear the Destination (1N7:3), which means set the value to zero.
	DIV DIVIDE Source A 1N7:3 Source B 1N7:4 Dest 1N7:12	Division DIV	When the input conditions are true, divide the value in Source A (1N7:3) by the value in Source B (1N7:4) and store the result in the Destination (1N7:12).
	MUL MULTIPLY Source A 1N7:3 Source B 1N7:4 Dest 1N7:12	Multiply MUL	When the input conditions are true, multiply the value in Source A (1N7:3) by the value in Source B (1N7:4) and store the result in the Destination (1N7:12).
	NEG NEGATE Source 1N7:3 Dest 1N7:12	Negate NEG	When the input conditions are true, take the opposite sign of the Source (1N7:3) and store the result in the Destination (1N7:12). This instructions turns positive values into negative values and negative values into positive values.
	SQR SQUARE ROOT Source 1N7:3 Dest 1N7:12	Square Root SQR	When the input conditions are true, take the square root of the Source (N7:3) and store the result in the Destination (N7:12).
	SUB SUBTRACT Source A 1N7:3 Source B 1N7:4 Dest 1N7:12	Subtract SUB	When the input conditions are true, subtract the value in Source B (1N7:4) from the value in Source A (1N7:3) and store the result in the Destination (1N7:12).

Category	Instruction		Description
Logical Instructions	AND BITWISE AND Source A 1N9:3 Source B 1N10:3 Dest 1N2:3	AND	When the input conditions are true, the processor evaluates an AND operation between Source A (1N9:3) and Source B (1N10:3) (bit-for-bit) and stores the result in the Destination (1N2:3). The truth table for an AND operation is: Source A Source B Result 0 0 0 1 0 0 0 1 0 1 1 1
	NOT NOT Source 1N9:3 Dest 1N10:4	NOT Operation	When the input conditions are true, the processor performs a NOT operation (takes the opposite of) on the Source (1N9:3) (bit-for-bit) and stores the result in the Destination (1N10:4). The truth table for a NOT operation is: Source Destination 0 1 1 0
	OR BITWISE INCLUS OR Source A 1N9:3 Source B 1N10:4 Dest 1N2:3	OR	When the input conditions are true, the processor evaluates an OR operation between Source A (1N9:3) and Source B (1N10:4) (bit-for-bit) and stores the result in the Destination (1N2:3). The truth table for an OR operation is: Source A Source B Result 0 0 0 1 0 1 0 1 1 1 1 1
	XOR BITWISE EXCLUS OR Source A 1N9:3 Source B 1N10:4 Dest 1N2:3	Exclusive OR XOR	When the input conditions are true, the processor evaluates an EXCLUSIVE OR operation between Source A (1N9:3) and Source B (1N10:4) (bit-for-bit) and stores the result in the Destination (1N2:3). The truth table for an XOR operation is: Source A Source B Result 0 0 0 1 0 1 0 1 1 1 1 0
Conversion Instructions	FRD FROM BCD Source 1N7:3 Dest 1N9:3	Convert from BCD FRD	When the input conditions are true, convert the value in the Source (1N7:3) from a BCD format to an integer format and store the result in the Destination (1N9:3).
	TOD TO BCD Source 1N9:3 Dest 1N7:3	Convert to BCD TOD	When the input conditions are true, convert the value in Source (1N9:3) from integer to a BCD format and store the result in the Destination (1N7:3).

Category	Instruction		Description
Bit Modify and Move Instructions	MOV MOVE Source 1N7:0 Dest 1N7:2	Move MOV	When the input conditions are true, move a copy of the value in Source (1N7:0) to the Destination (1N7:2). This overwrites the original value in the Destination.
	MVM MASKED MOVE Source 1N7:0 Mask 00000055 Dest 1N7:2	Masked Move MVM	When the input conditions are true, the processor passes the value in the Source (1N7:0) through the Mask (00000055) and stores the result in the Destination (1N7:2).
	RMW R–M–W Source 1N7:0 AND Mask 000000FF OR Mask 00000F0F Dest 1N7:1	Read-Modify-Write RMW	When the input conditions are true, the processor passes the value in the Source (1N7:0) through the AND Mask (000000FF) and then passes that result through the OR Mask (00000F0F) and stores the final result in the Destination (1N7:1).
File Instructions	FAL FILE ARITH/LOGICAL Control 1R6:1 Length 4 Position 0 Mode ALL Dest #1N28:0 Expression #1N27:3 –5	File Arithmetic and Logic FAL	When the input conditions are true, the processor reads 4 words of 1N27:3, and subtracts 5 (a constant) from each word. The results are stored in 1N28:0. The control file 1R6:1 controls the operation. The Mode determines whether the processor performs the expression on all words in the files (ALL) per program scan, one word in the files (INC) per false-to-true transition, or a specific number of words (NUM) per scan.
	FSC FILE SEARCH/COMPARE Control 1R9:0 Length 90 Position 0 Mode 10 Expression #1B4:0 <> #1B5:0	File Search and Compare FSC	When the input conditions are true, the processor performs the not-equal-to comparison on 90 words (10 per scan) between files 1B4:0 and 1B5:0. The Mode determines whether the processor performs the expression on all words in the files (ALL) per program scan, one word in the files (INC) per false-to-true, or a specific number of words (NUM) per scan.

Category	Instruction		Description
Diagnostic Instructions	DDT DIAGNOSTIC DETECT Source #I:030 Reference #1B3:0 Result #1N10:0 Cmp Control 1R6:0 Length 48 Position 0 Result Control 1R6:1 Length 10 Position 0	Diagnostic Detect DDT	When the input conditions are true, the processor compares the number of bits specified in the Cmp Control Length (48) of the Source file (I:030) with the bits in the Reference (1B3:0). The processor stores the results in the Result (1N10:0) and modifies the mismatched bit in the Reference file to match the Source file. Control structure 1R6:0 controls the compare and control structure 1R6:1 controls the file that contains the results. The file containing the results can hold up to 10 mismatches between the compared files.
	FBC FILE BIT COMPARE Source #I:031 Reference #1B3:1 Result #1N7:0 Cmp Control 1R6:4 Length 48 Position 0 Result Control 1R6:5 Length 10 Position 0	File Bit Compare FBC	When the input conditions are true, the processor compares the number of bits specified in the Cmp Control Length (48) of the Source file (I:031) with the bits in the Reference (1B3:1). The processor stores the results in the Result (1N7:0). Control structure 1R6:4 controls the compare and control structure 1R6:5 controls the file that contains the results. The file containing the results can hold up to 10 mismatches between the compared files.
Shift Instructions	BSL BIT SHIFT LEFT File #1B3:1 Control 1R6:53 Bit Address I:022/12 Length 58	Bit Shift Left BSL	If the input conditions go true, the BSL instruction shifts the number of bits specified by Length (58) in File (1B3:1), starting at bit 0, to the left by one bit position. The source bit (I:022/12) shifts into the first bit position, 1B3:1. The last bit shifts out of file 1B3:1 and into 1R6:53.UL.
	BSR BIT SHIFT RIGHT File #1B3:2 Control 1R6:54 Bit Address I:023/06 Length 38	Bit Shift Right BSR	If the input conditions go true, the BSR instruction shifts the number of bits specified by Length (38) in File (1B3:2), starting with the highest bit position, to the right by one bit position. The source bit (I:023/06) shifts into the highest bit position 1B3:/69. The lowest bit shifts out of file 1B3:2 and into 1R6:54.UL.
	FFL FIFO LOAD Source 1N60:1 FIFO #1N60:3 Control 1R6:51 Length 64 Position 0	FIFO Load FFL	When the input conditions go true, the processor loads 1N60:1 into the next available word in the stack, as pointed to by the position word of 1R6:51. Each time the rung goes from false to true, the processor loads another word in the stack #1N60:3.

Category	Instruction		Description
	FFU FIFO UNLOAD FIFO #1N60:3 Dest 1N60:2 Control 1R6:51 Length 64 Position 0	FIFO Unload FFU	When the input conditions go true, the processor unloads a word as pointed to by the position word of 1R6:51 from #1N60:3 into 1N60:2 and shifts all the data in the stack one position towards the first element. Each time the rung goes from false to true, the processor unloads another word.
	LFL LIFO LOAD Source 1N70:1 LIFO #1N70:3 Control 1R6:61 Length 64 Position 0	LIFO Load LFL	When the input conditions go true, the processor loads 1N70:1 into the next available word in the stack, as pointed to by 1R6:61. Each time the rung goes from false to true, the processor loads another word.
	LFU LIFO UNLOAD LIFO #1N70:3 Dest 1N70:2 Control 1R6:61 Length 64 Position 0	LIFO Unload LFU	When the input conditions go true, the processor unloads the last word from #1N70:3 and puts it into 1N70:2. Each time the rung goes from false to true, the processor unloads another word.
Sequencer Instructions	SQI SEQUENCER INPUT File #1N70:11 Mask 0000FFF0 Source #I:031 Control 1R6:21 Length 4 Position 0	Sequencer Input SQI	The SQI instruction compares the Source (#I:031) input image data through a Mask (0000FFF0) to Reference file #1N70:11 to see if they match. The operation is controlled by the information in the control structure 1R6:21. When the status of all unmasked bits matches the corresponding reference bits, the rung goes true.
	SQL SEQUENCER LOAD File #1N70:20 Source I:002 Control 1R6:22 Length 5 Position 0	Sequencer Load SQL	The SQL instruction loads data into the sequencer File (#1N70:20) by stepping through the number of words specified by Length (5) of the File (1N70:20), starting at the Position (0). The operation is controlled by the information in the control structure 1R6:22. When the rung goes from false to true, the SQL instruction increments to the next step in the sequencer file and loads the Source data into it for every scan that the rung remains true.
	SQO SEQUENCER OUTPUT File #1N70:1 Mask 00000F0F Dest O:014 Control 1R6:20 Length 4 Position 0	Sequencer Output SQO	When the rung goes from false to true, the SQO instruction increments to the next step in the sequencer File (#1N70:1). The data in the sequencer file is transferred through a Mask (00000F0F) to the Destination (O:014) for every scan that the rung remains true.

Category	Instruction		Description
Program Control Instructions	—(MCR)—	Master Control Reset MCR	If the input conditions are true, the program scans the rungs between MCR instruction rungs and processes the outputs normally. If the input conditions are false, all non-retentive outputs are reset within the MCR zone.
	10 —(JMP)—	Jump JMP	If the input conditions are true, the processor skips rungs by jumping to the rung identified by the label (10).
	10 —[LBL]—	Label LBL	When the processor reads a JMP instruction that corresponds to label 10, the processor jumps to the rung containing the label and starts executing.
	15 —(GSB)—	Jump JMP	If the input conditions are true, the processor skips to the subroutine identified by the label (15).
	—[BRK]—	Break BRK	When the input conditions go true, the BRK instruction aborts a loop in the current routine.
	WIL WHILE Label 10 Expression 1N7:0 < 1N9:0	WHILE Loop WIL	The processor executes the rungs at Label 10 repeatedly in one program scan, until the expression is true or a BRK instruction aborts the operation.
	FOR FOR Label 16 Index 1N72:57 Initial Value 1 Final Value 8 Step 3	FOR Loop FOR	The processor executes the rungs at Label 16 repeatedly in one program scan, until it reaches the Final Value (8) or until a BRK instruction aborts the operation. After each scan the processor increments the Initial Value (1) by the Step (3).
	JSR JUMP TO SUBROUTINE Program File 1STEP9 Input par 1N16:23 Input par 1N16:24 Input par 231 Return par 1N19:11 Return par 1N19:12	Jump to Subroutine JSR	If the input conditions are true, the processor starts running a subroutine Program File (1STEP9). The processor uses the Input Parameters (1N16:23, 1N16:24, 1231) in the subroutine and passes Return Parameters (1N19:11, 1N19:12) back to the main program, where the processor encountered the JSR instruction.
	SBR SUBROUTINE Input par 1N43:0 Input par 1N43:1 Input par 1N43:2	Subroutine SBR	The SBR instruction is the first instruction in a subroutine file. This instruction identifies Input Parameters (1N43:0, 1N43:1, 1N43:2) the processor receives from the corresponding JSR instruction. You do not need the SBR instruction if you do not pass input parameters to the subroutine.
	RET RETURN ( ) Return par 1N43:3 Return par 1N43:4	Return RET	The RET instruction ends the subroutine and stores the Return Parameters (1N43:3, 1N43:4) to the main program.

Category	Instruction		Description
	—[NOP]—	No Operation NOP	The NOP instruction is a marker that you can place in a ladder program. The processor ignores the NOP instruction; any other instructions on the same rung run normally.
	—(TND)—	Temporary End TND	The TND instruction stops the processor from scanning the rest of the current ladder file.
	—[AFI]—	Always False AFI	The AFI instruction disables the rung (i.e., the rung is always false).
	OSF ONE SHOT FALLING Output Bit O:126/15 Storage Bit O:010/12	One Shot Falling OSF	The OSF instruction triggers an event to occur one time. Use the OSF instruction whenever an event must start based on the change of state of a rung from true-to-false, not on the resulting rung status.
	OSR ONE SHOT RISING Storage Bit O:120/10 Output Bit O:010/12	One Shot Rising OSR	The OSR instruction triggers an event to occur one time. Use the OSR instruction whenever an event must start based on the change of state of a rung from false-to-true, not on the resulting rung status.
	—(EOT)—	End of Transition EOT	The EOT instruction should be the last instruction in an SFC transition file. If you do not use an EOT instruction, the processor always evaluates the transition as true.
Process Control Instructions	PID PID Control Block 1PD:0 Processor Variable 1BTD1:13 Tieback 1BTD1:14 Control Output 1BTD1:21	Proportional, Integral, and Derivative PID	If the input conditions are true, the processor performs PID calculations and controls a closed loop. The control block (1PD:0) contains the instruction information for the PID. The PID gets the process variable from 1BTD1:13 and sends the PID output to 1BTD1:21. The tieback stored in 1BTD1:14 handles the manual control station.
	TPO TPO Percent On 1PD0:0.OUT Timer 1T0:0 Time Base 0.01 Cycle Time 1000 Current 798 Output Bit 0:126/15	Time-Proportioning Output TPO	The TPO instruction sets and resets an output bit based on a cycle time and a “percent on” parameter. When the input instructions go true, the instruction sets the output bit, which remains set up to the specified percent on-time. At the end of the cycle, the instruction resets the output bit.

Category	Instruction		Description
Block Transfer Instructions	BTR BLOCK TRANSFER READ Rack 3 Group 0 Module 0 Control Block BR030 Data File 1BTD1:0 Length 0 Continuous NO BT Timeout 3	Block Transfer Read BTR	If the input conditions are true, the block transfer read is initiated for the I/O module located at rack 3, group 0, module 0. The Control Block (BR030) contains status for the transfer. The Data File contains the data that is read from the I/O module (1BTD1:0). The BT Length (0) identifies that all the words should be transferred. A non-continuous block transfer is queued and run only once per false-to-true transition; a continuous block transfer is repeatedly requeued. The BT Timeout (3) specifies the number of seconds the processor has to process the instruction.
	BTW BLOCK TRANSFER WRITE Rack 3 Group 0 Module 0 Control Block BW030 Data File 1BTD2:0 Length 0 Continuous NO BT Timeout 3	Block Transfer Write BTW	If the input conditions are true, the block transfer write is initiated for the I/O module located at rack 3, group 0, module 0. The Control Block (BW030) contains status for the transfer. The Data File contains the data to write (1BTD2:0). The BT Length (0) identifies that all the words should be transferred. A non-continuous block transfer is queued and run only once per false-to-true transition; a continuous block transfer is repeatedly requeued. The BT Timeout (3) specifies the number of seconds the processor has to process the instruction.
Message Instructions	MSG SEND/RECEIVE MESSAGE Control Block 0MSG0:0	Message MSG	If the input conditions are true, the data is transferred according to the instruction parameters you set when you entered the message instruction. The Control Block (0MSG0:0) contains status and instruction parameters.
Independent Background Instructions	IBP IBP Control Block 0MSG10:0 File 1IBP30 Task 4	Independent Background Program IBP	If the input conditions are true, the processor begins running the specified IBP file.
	ABT ABORT IBP IBP Control Block 0MSG10:0 ABT Control Block 0MSG7:0	Abort Independent Background Program ABT	If the input conditions are true, the processor stops running the specified IBP file.
Fault Instructions	(CMF)	Clear Minor Fault CMF	If the input conditions are true, the processor clears all current minor faults.
	GMF GET MINOR FAULT File #1N0:0	Get Minor Fault GMF	If the input instructions are true, the GMF instruction removes a minor fault record from the Minor Fault FIFO Buffer and places that record in the file address (#1N0:0).
	SMF SET MAJOR FLT Source #1N70:20	Set Major Fault SMF	If the input instructions are true, the processor initiates the specified major fault. The Source (#1N70:20) can be either an address that holds a major fault code or it can be the major fault code.

Category	Instruction		Description
Clock Instruction	CLK SET CLOCK File #1N7:0 Control 1R6:0	Set Clock CLK	If the input conditions go true, the processor uses the date and time stored in the File (#1N7:0). The Control (1R6:0) controls the Set Clock operation.
ASCII Instructions	AAL ASCII ALLOCATE Channel RM–1 Control 0MSG10:0	ASCII Allocate AAL	If input conditions go true, the processor allocates the Channel (RM–1) for ASCII operations. The Control (0MSG10:0) contains status information for this channel.
	ABL ASCII TEST FOR LINE Channel 1KA–1 Control 0MSG10:0 Characters	ASCII Test for Line ABL	If input conditions go true, the processor reports the number of characters in the buffer associated with the Channel (1KA–1), up to and including the end-of-line characters and puts this value into the position field. The processor stores the number of characters in 0MSG10:0.DLEN
	ACB ASCII CHARS IN BUFFER Channel 1KA–1 Control 0MSG10:0 Characters	ASCII Characters in Buffer ACB	If input conditions go true, the processor reports the total number of characters in the buffer associated with the Channel (1KA–1). The processor stores the number of characters in 0MSG10:0.DLEN.
	ACI ASCII STRING TO INTEGER Source 1ST38:90 Dest 1N7:123	Convert ASCII String to Integer ACI	If input conditions are true, convert the string in the Source (1ST38:90) to an integer and store the result in the Destination (1N7:123).
	ACN STRING CONCATENATE Source A 1ST37:42 Source B 1ST38:91 Dest 1ST52:76	ASCII String Concatenate ACN	If input conditions are true, concatenate the string in Source B (1ST38:91) to the end of Source A (1ST37:42) and store the result in the Destination (1ST52:76).
	ADL ASCII DEALLOCATE Channel RM–1 Control 0MSG10:0	ASCII Deallocate ADL	If input conditions go true, the processor deallocates the Channel (RM–1) for ASCII operations. The Control (0MSG10:0) contains status information for this channel.
	AEX STRING EXTRACT Source 1ST38:40 Index 42 Number 10 Dest 1ST52:75	ASCII String Extract AEX	If input conditions are true, extract the Number (10) of characters starting at the Index (42) character of the Source (1ST38:40) and store the result in the Destination (1ST52:75).

Category	Instruction		Description
	AIC INTEGER TO STRING Source 876 Dest 1ST38:42	Convert Integer to ASCII String AIC	If input conditions are true, convert the Source (876) to a string and store the result in the Destination (1ST38:42).
	ARD ASCII READ Channel 1KA–1 Dest 1ST52:76 Control 0MSG0:28 String Length 50 Characters Read	ASCII Read ARD	If input conditions are true, read the String Length (50) from the buffer associated with the Channel (1KA–1) and move them to the Destination (1ST52:76). The processor stores the Characters Read field in 0MSG10:0.DLEN.
	ARL ASCII READ LINE Channel 1KA–1 Dest 1ST50:72 Control 0MSG0:28 String Length 18 Characters Read	ASCII Read Line ARL	If input conditions are true, read the String Length (180) or until end-of-line from the buffer associated with the Channel (1KA–1) and move them to the Destination (1ST50:72). The processor stores Characters Read field in 0MSG10:0.DLEN.
	ASC STRING SEARCH Source 1ST38:40 Index 35 Search 1ST52:80 Result 1N7:12	ASCII String Search ASC	If input conditions are true, search 1ST52:80 starting at the Index (35) character, for the string found in the Source (1ST38:40). The processor stores the position-matching character in the Result (1N7:12).
	ASR ASCII STRING COMPARE Source A 1ST37:42 Source B 1ST38:90	ASCII String Compare ASR	If the string in Source A (1ST37:42) is identical to the string in Source B (1ST38:90), set the output conditions.
	AWA ASCII WRITE APPEND Channel 1KA–1 Source 1ST52:76 Control 0MSG10:0 String Length 50 Characters Sent	ASCII Write Append AWA	If input conditions are true, read the String Length (50) from the Source (1ST52:76) and write those characters to the display device connected to the Channel (1KA–1); then write a carriage return.
	AWT ASCII WRITE Channel 1KA–1 Source 1ST37:40 Control 0MSG10:0 String Length 40 Character Sent	ASCII Write AWT	If input conditions are true, read the String Length (40) from the Source (1ST37:40) to the display device connected to the Channel (1KA–1).

Chapter 8

Specifications

Specifications

This section briefly lists specifications for PLC-5/250 system components.

Environmental

Temperature
- 0 to 60° C (operating)

Humidity
- 5 to 95% (noncondensing)

Chassis

Four or eight slots
Rack or panel mount

Power Supply

Input Voltage
- 85 - 132V ac
- 170 - 264V ac

Input Frequency
- 47 - 63 Hz

Connectors
- Fan status
- ac input line
- Interlock relay

Weight
- 9 lbs, 14.5 oz or 4.50 kg

Logic Processor

Memory
- 256K words
- 512K words
- 1024K words
- 2048K words

I/O Capacity
- 4096 inputs/outputs

Weight
- 3 lbs, 13.5 oz or 1.74 kg

Resource Manager

Memory
- 128K words or 384K words

Communication Channels
- 2 Data Highway or Data Highway Plus
- 1 RS-232C, RS-422, RS-423

Weight
- 4 lbs, 4 oz or 1.92 kg

Data Highway/Data Highway Plus Interface

Memory
- None

Communication Channels
- 2 Data Highway or Data Highway Plus
- 1 RS-232C, RS-422, RS-423

Weight
- 3 lbs, 11 oz or 1.67 kg

Remote I/O Scanner (RS2)

I/O Channels
- 2 channels remote
- Scanned independently
- 1024 discrete inputs/outputs

Scan Rate
- 5 ms per adapter

Communication Rate
- 57.6 k bps
- 115.2 k bps
- 230 k bps

Number of Devices Supported
- Up tp 32 devices per I/O channel

Weight
- 3 lbs, 11 oz or 1.67 kg

Remote/Local I/O Scanner (RS5)

I/O Channels
- 4 channels remote / 1 channel local
- Scanned independently
- 4096 discrete inputs/outputs

Scan Rate
- 4 ms per adapter

Communication Rate
- 57.6 k bps
- 115.2 k bps
- 230 k bps

Number of Devices Supported
- Up tp 32 devices per I/O channel

Weight
- 2 lbs, 15.6 oz or 1.35 kg

Power Requirements for a PLC-5/250 Chassis

Table 8.A lists backplane current loads for the power supply.

Table 8.A
Power Requirements for PLC-5/250 Systems

Module	A +5V DC Current	B +12V DC Current	C −12V DC Current
4-slot chassis (5110-A4)	2.0 A	0	0
8-slot chassis (5110-A8)	2.0 A	0	0
Resource Manager with 128K word memory (5130-RM1)	2.9 A	0.07 A	0.05 A
Resource Manager with 384K word memory (5130-RM2)	2.2 A	0.07 A	0.05 A
Logic Processor with 256K word memory (5250-LP1)	1.82 A	0.02 A	0
Logic Processor with 512K word memory (5250-LP2)	2.06 A	0.02 A	0
Logic Processor with 1024K word memory (5250-LP3)	2.5 A	0.02 A	0
Logic Processor with 2048K word memory (5250-LP4)	1.9 A	0.02 A	0
Remote I/O Scanner with memory (5150-RS2)	2.18 A	0.0139 A	0
Remote I/O Scanner with memory (5150-RS5)	4.85 A	0.02 A	0
Data Highway/Data Highway Plus Interface module (5130-KA)	2.9 A	0.07 A	0.05 A
Total			
Available power in a 60°C ambient environment without a fan chassis is 170 watts; with a fan chassis, it is 225 watts. If all total chassis current drains are less than these figures, select the standard power supply (5120-P1). You must install a fan assembly if the chassis contains a MicoVAX Information Processor or if the power supply load is over 170 watts. If any total chassis current drain exceeds these figures, reconfigure your system using more than 1 PI chassis.	35 A	3 A	1 A

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