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U S E R ' S M A N U A L

DUAL 8X1 MULTIPLEXER M-MODULE

MODEL M220

(FORMERLY HP E2272A)

Document Part No: 11029554

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INTRODUCTION

This manual describes the operation and use of the C&H Model M220 Dual 8x1 Multiplexer M-Module (Part Number 11029550). This module was formerly manufactured by HP (Agilent) as Model E2272A. C&H obtained the manufacturing rights from Agilent and now manufacturers it as C&H Model M220. This mezzanine module is designed to interface within any M/MA-Module carrier adhering to the ANSI/VITA 12-1996 M-Module specification. These carriers are available in many formats such as Ethernet, VME, VXI, PXI, cPCI, and the PC.

Contained within this manual are the physical and electrical specifications, installation and startup procedures, functional description, and configuration and programming guidelines to adequately use the product.

This manual is based on a low level register access, and is written in such a manner to provide understanding to the user based on this type of access. If a driver is provided, please refer to the driver documentation for instruction using the higher level interface provided by the driver.

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1.0 GENERAL DESCRIPTION

The M220 provides two separate 8 to 1, two-wire multiplexers or you can move a jumper to connect the common channels of each multiplexer together and create a single 16 to 1, two-wire multiplexer on a single wide M-Module adhering to the ANSI/VITA 12-1996 specification for M-Modules. The M220 may be installed on any carrier board supporting the M-Module specification. Carriers are available that allow the M220 to be used in Ethernet, VXI, VME, PCI, cPCI and other system architectures.

1.1 PURPOSE OF EQUIPMENT

The M220 can connect multiple instruments to multiple points in your test system. This provides flexible interconnection between test points, instrumentation, factory automation and test fixtures.

> **CAUTION:** This module uses latching relays that retain their last programmed state whenever power is removed (closed relays will remain closed until opened via your test program).

> **CAUTION:** This module DOES NOT have provisions for on-board current limiting components (if input current can exceed 2A DC or 2A AC, you must install external current limiting circuitry)

1.2 SPECIFICATIONS OF EQUIPMENT

1.2.1 Key Features

- 16 Latching Relays
- Connector Type: 44-pin D-Sub
- Interrupts when requested relay movements have completed
- Latching relays retain last programmed state
- FIFO register structure allows fast system operation
- Single-width M-Module provide high-density and maximum flexibility of configuration

1.2.2 Specifications

The M220 incorporates the standard 40-pin, 20x2 row connector interfaces to the carrier board for power and data/control, but does not have the 24-pin optional connector for carrying user-connections back onto the carrier board.

The user input/output is provided through a standard 44-pin D-subminiature female receptacle. A mating connector kit can be ordered separately as AM111 (C&H Part Number 11029700-0001). CONEC part number 302A10889X (or equivalent) is used on the assembly. The connector pin-outs are shown in Appendix A.

Table I. Specifications

MAXIMUM RATINGS

Parameter	Condition	Rating	Units
Voltage	Clean room Environment (any terminal to any other terminal)	200 125 175	VDC VACrms VAC peak
	Non-Clean room Environment (any terminal to any other terminal)	60 48 68	VDC VACrms VAC peak
Current (non-inductive)	Per Switch, DC Per Switch, AC Per Module, DC Per Module, AC	2 2 8 8	A A peak A A peak
Power	Per Switch, DC Per Switch, AC 16 to 1, Per Module, DC 16 to 1, Per Module, AC 8 to 1, Per Module, DC 8 to 1, Per Module, AC	50 50 50 50 100 100	W VA W VA W VA
Thermal Offset		< 3 typ	µV

RESISTANCE

Parameter	Condition	Rating	Units
Closed Channel	Initial, Hi or Lo End of Life, Hi or Lo	< 0.2 typ < 2	Ω Ω
Insulation	Between any two points ≤40°C, ≤65% relative humidity ≤25°C, ≤40% relative humidity	 10^8 typ 10^8 typ	 Ω Ω

RELAYS

Parameter	Condition	Rating	Units
Relay Life	at rated load	10^5	operations
Time to open/close	register programming	8	ms
Insulation	Between any two points ≤40°C, ≤65% relative humidity ≤25°C, ≤40% relative humidity	 10^8 typ 10^8 typ	 Ω Ω

AC CHARACTERISTICS

Parameter	Condition	Rating	Units
Typical Bandwidth	-3dB	> 10	MHz
Crosstalk (channel-to-channel)	<100 KHz <1 MHz <10 MHz	-64 typ -44 typ -24 typ	dB dB dB
Closed Channel Capacitance	8 to 1, Channel-Channel 8 to 1, Hi-Lo 8 to 1, Channel-Chassis 16 to 1, Channel-Channel 16 to 1, Hi-Lo 16 to 1, Channel-Chassis	< 20 typ < 40 typ < 75 typ < 25 typ < 70 typ < 140 typ	pF pF pF pF pF pF

1.2.3 Mechanical

The mechanical dimensions of the module are in conformance with ANSI/VITA 12-1996 for single-wide M-Module modules. The nominal dimensions are 5.687" (144.5 mm) long × 2.082" (52.9 mm) wide.

1.2.4 Bus Compliance

The module complies with the ANSI/VITA 12-1996 Specification for single-wide M-Modules and the MA-Module trigger signal extension. The module also supports the optional IDENT and VXI-IDENT functions.

Module Type:	M-Module
Addressing:	A08
Data:	D16
Interrupts:	supported
DMA:	not supported
Triggers:	not supported
Identification:	IDENT
Manufacturer ID:	$0FFF_{16}$ (See note below)
Model Number:	0688_{16}
VXI Model Number:	$025D_{16}$

Note: C&H obtained the manufacturing rights from Hewlett Packard (Agilent) for this module. The ID's have been retained as Hewlett Packard to provide compatibility with existing SW drivers.

1.2.5 Applicable Documents

ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification, Approved May 20, 1997, American National Standards Institute and VMEbus International Trade Association, 7825 E. Gelding Dr. Suite 104, Scottsdale, AZ 85260-3415, http://www.vita.com

2.0 INSTALLATION

2.1 UNPACKING AND INSPECTION

Verify that there has been no damage to the shipping container. If damage exists then the container should be retained, as it will provide evidence of carrier caused problems. Such problems should be reported to the shipping courier immediately, as well as to C&H. If there is no damage to the shipping container, carefully remove the module from its box and anti static bag and inspect for any signs of physical damage. If damage exists, report immediately to C&H.

2.2 HANDLING PRECAUTIONS

The module contains components that are sensitive to electrostatic discharge. When handling the module for any reason, do so at a static-controlled workstation, whenever possible. At a minimum, avoid work areas that are potential static sources, such as carpeted areas. Avoid unnecessary contact with the components on the module.

2.3 INSTALLATION OF M/MA MODULES

All M-Modules must be installed into the carrier before the carrier is installed into the host system. To install a module, firmly press the connector on the M/MA-Module together with the connector on the carrier as shown in Figure 1. Secure the module through the holes in the bottom shield using the original screws.

CAUTION: M/MA-Module connectors are NOT keyed. Use extra caution to avoid misalignment. Applying power to a misaligned module can damage the M/MA-Module and carrier.

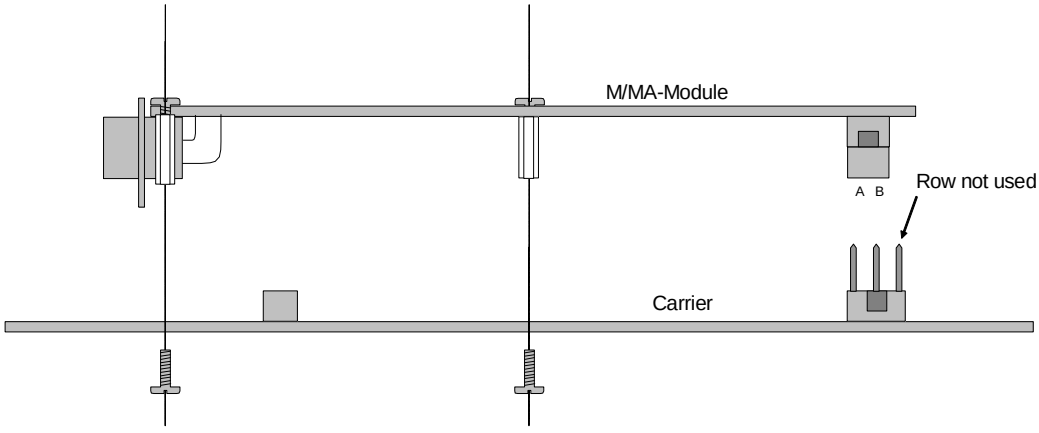


Figure 1. M-MODULE Installation

2.4 PREPARATION FOR RESHIPMENT

If the module is to be shipped separately it should be enclosed in a suitable water and vapor proof anti-static bag. Heat seal or tape the bag to insure a moisture-proof closure. When sealing the bag, keep trapped air volume to a minimum. The shipping container should be a rigid box of sufficient size and strength to protect the equipment from damage. If the module was received separately from a C&H system, then the original module shipping container and packing material may be re-used if it is still in good condition.

3.0 FUNCTIONAL DESCRIPTION

3.1 OVERVIEW

A simplified functional block diagram is shown in Figure 2.

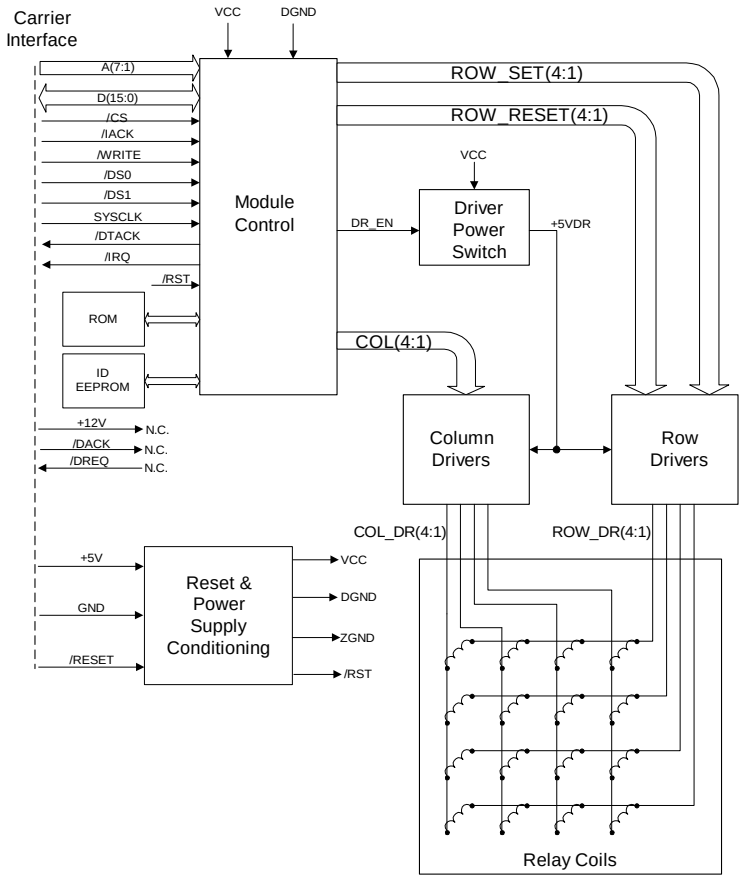


Figure 2. M220 Functional Block Diagram

3.1.1 M-Module Interface

The M-Module Interface allows communication between the M220 and the carrier module. The interface is an asynchronous 16-bit data bus with interrupt capabilities. The interface adheres to the ANSI/VITA 12-1996 Standard for The Mezzanine Concept M-Module Specification for MA modules.

3.1.2 Module Control

This block contains all of the logic for the module including all registers, interrupt control and carrier interface.

3.1.3 ID EEPROM

The EEPROM holds sixty-four 16-bit words of M-Module ID data and VXI M-Module data. Refer Section 3.2.3 for more details.

3.1.4 Row and Column Drivers

The module uses a matrix drive scheme (rows and columns) in which a maximum of four of the relays (one row) can be operated at any one time. An on-board timer (part of Module Control block) ensures the relay coils have been driven long enough for the contacts to move and settle.

The Row Driver block translates the ROW_SET(4:1) and ROW_RESET(4:1) command lines from the Module Control block into bipolar and tri-state capable buffered drive signals. The ROW_DR(4:1) signals provide either current source from the +5VDR supply (relay set), current sink to ground (relay reset), or tri-stated output (both current-source and current-sink off). Each output is tri-stated whenever that particular row is not being driven.

The Column Driver block translates the COL(4:1) command lines from Module Control into the bipolar buffered drive signals, COL_DR(4:1). The COL_DR(4:1) signals provide either current source from the +5VDR supply (relay reset) or current sink to ground (relay set).

3.1.5 Driver Power Switch

This block removes all power from the Row and Column Driver circuitry except when needed to move relays. This FET switch is open at power-up to prevent any relay contact movement until register writes cause drive-power to be applied.

3.1.7 Relay Coils

This block contains the 16 relay coils arranged as a 4x4 matrix. To close a relay, a ROW_DR line sources current while a COL_DR line sinks current to ground. To open a relay, a COL_DR line sources current while a ROW_DR line sinks current to ground. Refer to Figure 3 for switching schematic.

3.1.8 Reset and Power Conditioning

This block filters +5V power to produce VCC power (+5V) for logic and isolates the various grounds used by the module. This block also processes the /RESET signal from the Carrier Interface and monitors power to produce the /RST reset signal for the module.

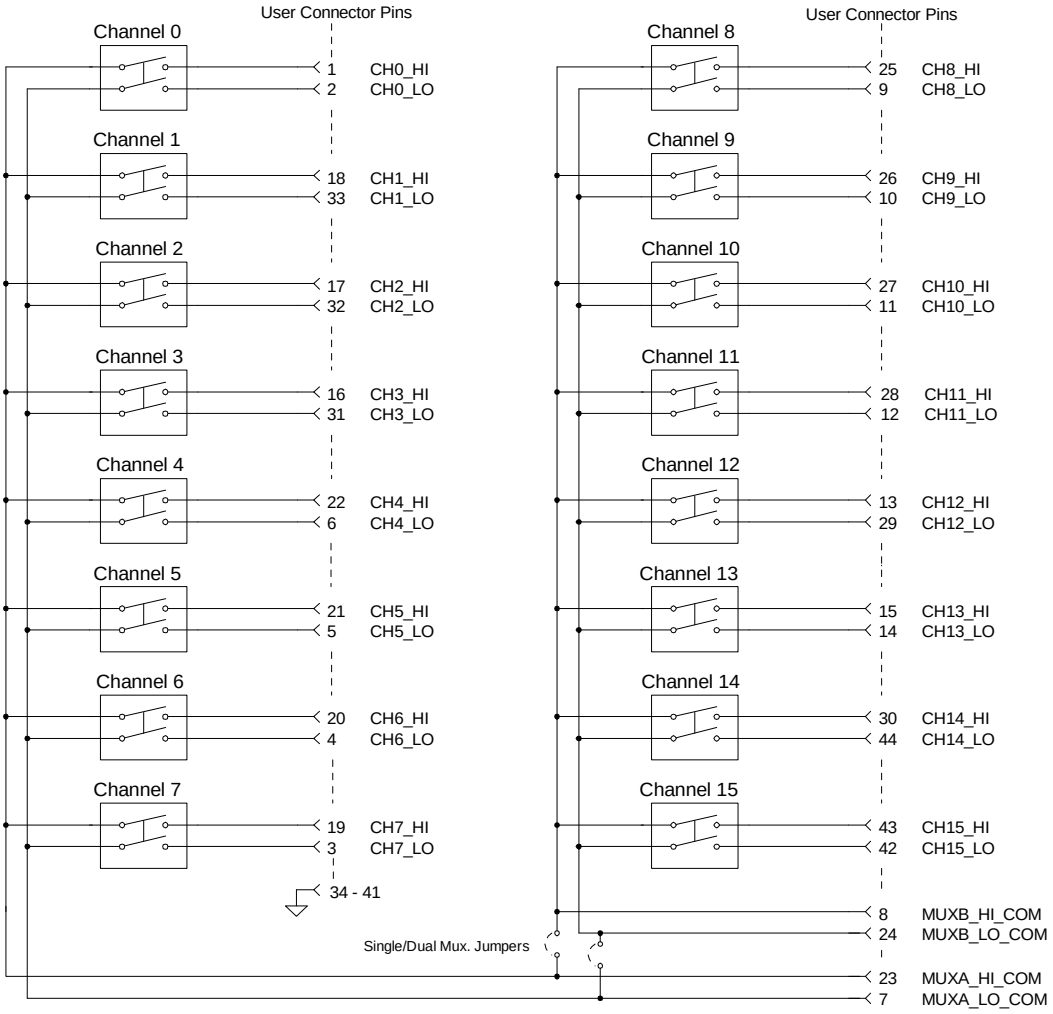


Figure 3. M220 Switching Schematic

3.2 IDENTIFICATION AND CONFIGURATION REGISTERS

3.2.1 Setting Multiplexer Size

Figure 4 shows the two jumper positions for the M220. When in position A (jumper **not** connecting one row of pins), the module is configured as a dual 8-to-1 multiplexer. When in position B (jumper connecting all pins), the module is configured as a single 16-to-1 multiplexer. The M220 leaves the factory with the jumper placed in position A (dual 8-to-1 multiplexer). If you need to change this jumper position, it must be done **before** installing the M-Module onto the carrier.

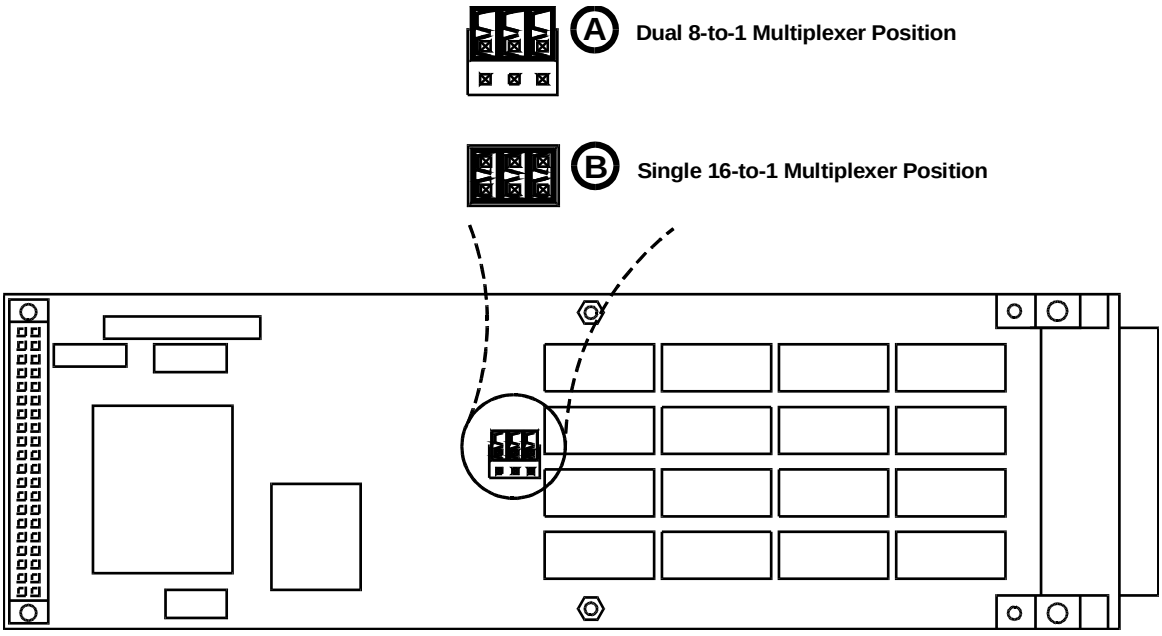


Figure 4. Jumper Positions

3.2.2 I/O Registers

There are a variety of registers used to configure and control the M219 module. These registers are located in the IOSpace. The address map of the registers is shown in Table II. Details of the registers are provided in Figure 5.

Table II. I/O Address Map/Command Summary

	Register Name	**Register Type**	**FIFO-able Register (Y/N)**
00h	Status Register	Read Only	N
02h	Control Register	Read/Write	N
04h-0Eh	Reserved	NA	N
10h	Row 0 Set Register	Read/Write	Y
12h	Row 0 Reset Register	Read/Write	Y
14h	Row 1 Set Register	Read/Write	Y
16h	Row 1 Reset Register	Read/Write	Y
18h	Row 2 Set Register	Read/Write	Y
1Ah	Row 2 Reset Register	Read/Write	Y
1Ch	Row 3 Set Register	Read/Write	Y
1Eh	Row 3 Reset Register	Read/Write	Y
20h - 7Eh	Unused	NA	N
80h – FEh	ID EEPROM	Read/Write	N

Reg. 00

Status

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Read-only															
Read	Reserved											INIT	MPS	FIFOE	FIFOF	INT

INIT ⇨ Init Status (1 = initialized since last power up, 0 = not initialized since last power up)
MPS ⇨ Multiplexer Size (0 = 16 to 1 multiplexer, 1 = dual 8 to 1 multiplexer, see note)
FIFOE ⇨ FIFO Empty Status (1 = FIFO currently empty, up to 8 writes available and not busy)
FIFOF ⇨ FIFO Full Status (1 = FIFO currently full, additional writes are lost)
INT ⇨ Interrupt Status (if enabled; 1 = interrupt line asserted, 0 = interrupt line not asserted)

Note: The multiplexer size is controlled by the jumper discussed in Section 3.2.1. This bits indicates the configuration of the jumper.

Reg. 02

Control

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Reserved										TM		DPE	STE	INTE	RST
Read	Reserved										TM		DPE	STE	INTE	RST

TM ⇨ Timer Mode (proper operation is guaranteed only for the time = 8ms)
0 0 8ms
0 1 2ms
1 0 4ms
1 1 64ms
DPE ⇨ Driver Power Enable (1 = enables power to relay drivers, 0 = removes power)
STE ⇨ Self-Test Enable (1 = disable power to all row & column drivers and allows testing the operation of the FIFO without causing relay movement, 0 = allows row & column drivers to be powered (if driver power is enabled). Be sure the FIFO is empty before returning this bit to 0.
INTE ⇨ Interrupt Enable (1 = enables interrupts, 0 = disables interrupts)
RST ⇨ Reset (1 = initiates a soft reset, 0 = releases module from reset condition)

Figure 5. I/O Registers

Reg. 10

Row 0 Set Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Unused												R0C3	R0C2	R0C1	R0C0
Read	Unused												R0C3	R0C2	R0C1	R0C0

Reg. 12

Row 0 Reset Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Unused												R0C3	R0C2	R0C1	R0C0
Read	Unused												R0C3	R0C2	R0C1	R0C0

Reg. 14

Row 1 Set Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Unused												R1C3	R1C2	R1C1	R1C0
Read	Unused												R1C3	R1C2	R1C1	R1C0

Reg. 16

Row 1 Reset Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Unused												R1C3	R1C2	R1C1	R1C0
Read	Unused												R1C3	R1C2	R1C1	R1C0

Reg. 18

Row 2 Set Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Unused												R2C3	R2C2	R2C1	R2C0
Read	Unused												R2C3	R2C2	R2C1	R2C0

Reg. 1A

Row 2 Reset Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Unused												R2C3	R2C2	R2C1	R2C0
Read	Unused												R2C3	R2C2	R2C1	R2C0

Reg. 1C

Row 3 Set Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Unused												R3C3	R3C2	R3C1	R3C0
Read	Unused												R3C3	R3C2	R3C1	R3C0

Reg. 1E

Row 1 Reset Register

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Unused												R3C3	R3C2	R3C1	R3C0
Read	Unused												R3C3	R3C2	R3C1	R3C0

RxCy ⇨ Row x, Column y (1 = close relay, 0 = open relay)

Note: The Switch M-Modules use a row and column relay drive scheme. To close a particular relay, write a logic "1" to the corresponding column in a Row n Set register. To open a relay, write a logic "0" in the corresponding column in a Row n Reset register. For example, to close the Channel 04 relay on the module (Row 1, Column 0 in relay drive scheme) place a logic "1" in bit 00 of the Row 1 Set register. To open this relay, place a logic "0" in bit 00 of the Row 1 Reset register. Table V shows the correlation of the matrix drive rows and columns to Switch M-Module channels.

Figure 5. I/O Registers (continued)

3.2.3 Module Identification

The M220 supports the identification function called IDENT. This IDENT function provides information about the module and is stored in a sixteen-word deep (32 byte) serial PROM. Access is accomplished with read/write operations on the last address in IOSpace (hex FE) and the data is read one bit at a time. The PROM is compatible with a standard IC 9603 type PROM. For specific timing information refer to the 9603 or compatible PROM data sheet. Data should not be written to the PROM.

The module also supports the VXI-IDENT function. This function is not part of the approved ANSI/VITA 12-1996 standard. This extension to the M-module IDENT function increases the size of the PROM to 64 words and includes VXI compatible ID and Device Type Registers. Details are shown in Table III.

Table III. M/MA Module PROM IDENT Words

Word	Description	Value (hex)
0	Sync Code	5346
1	Module Number	0688
2	Revision Number [1]	0002
3	Module Characteristics [2]	0868
4-7	Reserved	0000
8-15	M-Module Specific	0000
16	VXI Sync Code	ACBA
17	VXI ID	0FFF [3]
18	VXI Device Type [3]	F25D (M220)
19-31	Reserved	0000
32-63	M-Module Specific	0000

Notes:

1) A Revision Number greater than 1 indicates that the module was manufactured by C&H Technologies.
2) The Module Characteristics bit definitions are:

Bit(s)	Description
15	0 = no burst access
14/13	unused
12	0 = does not need ±12V
11	1 = needs +5V
10	0 = no trigger outputs
9	0 = no trigger inputs
8/7	00 = no DMA requestor
6/5	11 = interrupt type
4/3	01 = 16-bit data
2/1	00 = 8-bit address
0	0 = no memory access

3) The VXI ID of 0xFFF is the identification value for Hewlett-Packard. C&H has left the ID equal to this value to allow operation with existing E2272A software drivers. The revision number (see note 1) can be used to identify the module as manufactured by C&H.
4) The VXI Device Type word contains the following information:

Bit(s)	Description
15-12	F_{16} = 256 bytes of required memory
11-0	$25D_{16}$ = C&H specified VXI model code for M220

4.0 OPERATION

The M220 is a register-based instrument that is controlled through a series of I/O registers described in Section 3.2.2. The exact method of accessing and addressing the I/O registers is dependent on the M-Module carrier used to interface the module to your data acquisition or test system. Refer to the carrier's documentation for information on the address mapping of an M-Module's I/O registers and to your system software documentation for details on data access.

Typically a high level driver is available to aid in control of the module. Refer to the software driver documentation for instructions on using the driver.

4.1 FIFO STRUCTURE

The FIFO (First-In-First-Out) structure allows multiple writes to the module to be stacked-up. This helps reduce interrupt overhead by allowing an interrupt only after the completion of the last relay operation in a sequence of up to eight operations. Eight was chosen because it allows at least one ***open*** and one ***close*** to each of the four relay rows, allowing a complete change of all relay states.

If the M-Module is enabled to interrupt, it asserts the INT line on the M-Module interface to the Carrier when the last commanded relay operation in the FIFO has completed. For example, if relays in only one row were instructed to move, the module asserts an interrupt after that one row has been driven. If four rows were instructed to move (four writes to the FIFO--see note below), then the module asserts an interrupt only after the completion of the fourth operation.

Note: The module asserts an interrupt after the relay drive time is complete (relay drive timer) and no other operations have been stored in FIFO. The above example assumes the four writes are stored in FIFO one after the other with very little time between the writes. If, in the above example, the amount of time between writes is greater than the relay drive time (8 ms), the module would actually interrupt four times--one interrupt after driving each relay.

4.2 RELAY SET/RESET

When the FIFO is empty (no relay operations pending) bits 03, 02, 01, and 00 in the above registers indicate the state of the corresponding relay. Logic "1" means the relay in Row n Column n is closed or soon will be (depending on the FIFO Empty Status bit's state). Logic "0" means the corresponding relay is open. Following are some general notes on relay operation:

1. Writing to a Row n Set register closes the relays only in the bit positions set to logic "1." Writing logic "0" to **a Row n Set** register has no effect on relay position. Writing to a Row n Reset register opens relays only for the bit positions set to logic "0." Writing logic "1" to **a Row n Reset** register has no effect on relay position.
2. Reading either the **Row n Set** or **Row n Reset** register addresses returns identical data because they are actually mapped to the same register. When you write to one of these registers (and FIFO is not full), the data is stored in the register and stored in FIFO.

3. The Row n Set/Reset readback registers return the programmed relay state only if you use the module correctly. Since the driver power can be disabled (the power-on state), the **Row n Set** and **Row n Reset** registers can be written to and read from without moving any relay contacts.
4. When the module loses power, any closed relays remain closed (latching relays). When power is restored, the relays remain closed but the Row n Set and Row n Reset registers have lost their relay state information. This relay information is lost whenever power is cycled or the carrier asserts /RESET. You must initialize the module after a power-up or /RESET to achieve correlation between the Row n Set/Reset readback registers and the actual relay positions. To initialize the module:
   a. Enable driver power.
   b. Write all four column bits to zero in each **Row n Reset** register.

You can check for initialization by reading the Init Status bit. If the module has not been initialized since the last power-up or /RESET, the Init Status bit will be logic "0". The Init Status bit is set to logic "1" whenever the module has been successfully initialized.

1. To guarantee break-before-make relay operation, write to the Row n Reset registers before writing to the Row n Set registers.
2. It is important to use the FIFO status bits when writing to the Row n Set/Reset registers, especially when writing in bursts (such as when resetting the module's relays). Writing to a Row n Set/Reset register when the FIFO is full results in the loss of data since the FIFO has no room to hold it. You should always check the FIFO FULL status to ensure that FIFO is not full before writing to a Row n Set/Reset register.

4.3 MATRIX DRIVE TO CHANNEL MAPPINGS

Table IV correlates the matrix drive rows and columns to channel numbers on the M220.

Table IV. Matrix Drive

	Matrix Drive	Column 0	Column 1	Column 2	Column 3
Multiplexer A	**Row 0**	Channel 0	Channel 1	Channel 2	Channel 3
	Row 1	Channel 4	Channel 5	Channel 6	Channel 7
Multiplexer B	**Row 2**	Channel 8	Channel 9	Channel 10	Channel 11
	Row 3	Channel 12	Channel 13	Channel 14	Channel 15

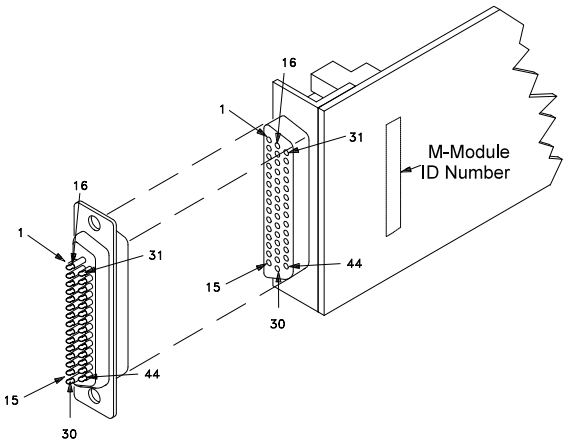
4.4 INTERRUPTS

Module interrupts are enabled by setting the INTE bit in the Control register; however, routing of the m-module interrupt request to your system is dependent on the m-module carrier and the system interface. Refer to user manuals for those devices for details.

If the M-Module is enabled to interrupt, it asserts the INT line on the M-Module interface to the Carrier when the last commanded relay operation in the FIFO has completed. For example, if relays in only one row were instructed to move, the module asserts an interrupt after that one row has been driven. If four rows were instructed to move (four writes to the FIFO--see note below), then the module asserts an interrupt only after the completion of the fourth operation.

Note: The module asserts an interrupt after the relay drive time is complete (relay drive timer) and no other operations have been stored in FIFO. The above example assumes the four writes are stored in FIFO one after the other with very little time between the writes. If, in the above example, the amount of time between writes is greater than the relay drive time (8 ms), the module would actually interrupt four times--one interrupt after driving each relay.

APPENDIX A: CONNECTORS



MAXIMUM VOLTAGE/CURRENT. The maximum voltage that may be applied to any connector on the M220 is 200 VDC, 125 VAC rms, or 175 VAC peak--these limits apply only if the product is installed in a humidity-controlled (<60% RH) environment where airborne contaminants and transients are controlled, and there is NOT a relay connection made to power mains. If these conditions CANNOT be maintained, then the maximum voltage is 60 VDC, 48 VAC-rms or 68 VAC-peak.

The maximum current (non-inductive) that may be applied to the M220 is:

Per Switch: 2 ADC, 2 AAC peak
Per Module: 8 ADC, 8 AAC peak

Pin #	Use	Pin #	Use	Pin#	Use
1	CH0_HI	16	CH3_HI	31	CH3_LO
2	CH0_LO	17	CH2_HI	32	CH2_LO
3	CH7_LO	18	CH1_HI	33	CH1_LO
4	CH6_LO	19	CH7_HI	34	GND
5	CH5_LO	20	CH6_HI	35	GND
6	CH4_LO	21	CH5_HI	36	GND
7	MUXA_LO_COM	22	CH4_HI	37	GND
8	MUXB_HI_COM	23	MUXA_HI_COM	38	GND
9	CH8_LO	24	MUXB_LO_COM	39	GND
10	CH9_LO	25	CH8_HI	40	GND
11	CH10_LO	26	CH9_HI	41	GND
12	CH11_LO	27	CH10_HI	42	CH15_LO
13	CH12_HI	28	CH11_HI	43	CH15_HI
14	CH13_LO	29	CH12_LO	44	CH14_LO
15	CH13_HI	30	CH14_HI		

Figure A-1. Front Panel I/O Signals

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