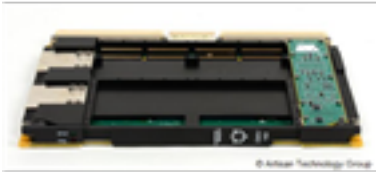
Curtiss-Wright DMV-182-2606

Single-Board Computer



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PRODUCT DATASHEET

SVME/DMV-182

Single / Dual PowerPC™ 7455/57 Single Board Computer

- Single or dual PowerPC™ 7455/7457 (AltiVec Technology™-enhanced) CPUs, each with:
  - 64 Kbytes L1 cache
  - 256/512 Kbytes internal L2 cache
  - Altivec™ technology-enabled
  - 19.2 GFLOPS peak processing power at 1.2 GHz core frequency
- 2 MB external L3 cache per processor
- 512 MB or 1 GB of DDR SDRAM with ECC
- 128 MB of contiguous direct-mapped Flash
- Hardware Flash write protection jumper
- Protected Access Boot System (PABS)
- 32 KB or 128 KB AutoStore nvSRAM, with hardware write protection
- Two Ethernet interfaces, one 10/100/1000BaseTX, one 10/100BaseTX
- Two 64-bit PMCs on independent PCI buses
  - one 100 MHz PCI-X, one 66 MHz PCI
- Two asynchronous RS-232 serial ports
- Up to 4 HDLC/SDLC-capable synch/asynch RS-232/422/485 serial channels with DMA support
- Up to 14 TTL discretes software-configurable as input or output, with interrupt capability as inputs
- Up to 16 RS-422/485 differential discretes, with interrupt capability on inputs
- Option for either 8- or 16-bit SCSI interface
- Two USB 2.0 ports
- Four general-purpose 32-bit user timers
- Option for up to 2 MIL-STD-1553 channels
- Four general-purpose PCI/SDRAM DMA controllers
- Six 32-bit OS timers, 3 per processor
- Two avionics-style watchdog timers
- Real-Time Clock
- Four on-board temperature sensors

- Tundra Universe II™
  VME64 interface Support for VME64x geographic addressing
- Basecard uses +5V-only, backplane 3.3V, 5V, and +/-12V are routed to the PMC sites
- Single .8" slot in all configurations
- Optimized conduction cooling with TherMax™ thermal frame and direct processor shunts
- Comprehensive Ethernet-capable Foundation Firmware with
  - debug monitor with system exerciser functions
  - embedded non-volatile memory programmer (NVMP)
  - power-up BIT (PBIT) and run-time BIT libraries for Initiated and Continuous BIT
- VxWorks/Tornado BSP & Driver Suite
- INTEGRITY BSP from Green Hills Software
- Linux SDK from TimeSys
- IXLibs-AV Altivec™-optimized DSP library
- Available in a range of ruggedization levels, both air- and conduction-cooled

Overview

Using single or dual Motorola MPC7455/7457 PowerPC™ processors with AltiVec™ technology and up to 1 GB of state-of-the-art DDR SDRAM, the 182 represents the new functionality and performance benchmark for rugged Single Board Computers. With two 64-bit PMC sites, one supporting 100 MHz PCI-X, and an unparalleled complement of I/O capability such as Gigabit Ethernet, SCSI, up to six serial ports, and two USB 2.0 ports, the 182 satisfies the most demanding requirements of embedded computing applications. Available in a full range of environmental build grades, the 182 is targeted to the sophisticated data- and digital signal-processing needs of tactical aircraft, armored vehicles and harsh environment naval systems.

For retrofit and technology insertion applications, the SVME/DMV-182 offers a superset of the I/O features of earlier generations of our PowerPC SBCs and optional pin-out modes for backplane compatibility as well. As a member of our continuously evolving stream of PowerPC SBCs including the SVME/DMV-178, SVME/DMV-179 and SVME/DMV-181, the SVME/DMV-182 supports the life-cycle model of successive technology insertions throughout a platform's lifetime.

Powerful Core Architecture

Figure 1 illustrates the core processing architecture of the 182. Two powerful 7455/57 processors connect via the MPX bus to the advanced GT-64360 Discovery™ II system controller. The Discovery™ II system controller bridges the MPX bus of the two processors to the DDR SDRAM bus, two 64-bit PCI busses, and a high-performance device bus on which the Flash EPROM and non-PCI peripherals are found. The powerful crossbar fabric internal to the Discovery™ II device allows for concurrent data transfers to take place on the various busses of the 182. Examples of data transfers that can occur concurrently on the 182 include:

- processor accesses to Flash concurrent with PCI-SDRAM transfers on either PCI bus
- processor accesses to one PCI bus concurrent with PCI-SDRAM transfers on the other PCI bus
- processor accesses to on-chip peripherals (Ethernet and serial ports) concurrent with PCI-SDRAM transfers on either PCI bus

The 182 provides hardware-enforced cache coherency with respect to accesses to SDRAM from PCI and bus-mastering peripherals, freeing driver software developers from the complexity of managing cache coherency in software. For applications requiring the highest-possible PCI-SDRAM performance, hardware-enforced cache coherency can be disabled.

A high-performance EPLD bridges the Discovery device bus to the Flash array and to a peripheral bus that interfaces to the Core Functions FPGA, RTC, and nvSRAM.

The Core Functions FPGA is a Virtex™-II V1000 device that implements a number of important 182 features including serial ports, interrupt control, system timers, watchdog timers, TTL discrete I/O and differential discrete I/O registers. To increase the serviceability of the 182 over the long life cycles of the military/aerospace programs for which it is designed, the Core Functions FPGA is In-System Programmable (ISP) and can be reprogrammed in the field.

PCI bus 1 is a 64-bit, 100 MHz-capable PCI-X bus that is dedicated to PMC site 1. Offering a peak PCI transfer rate of 800 MB/sec, PMC site 1 has the necessary bandwidth to support high performance PMC modules such as Fibre Channel NICs, graphics controllers, fabric interfaces, and custom high-speed devices. PCI bus 2 is a 64-bit, 66 MHz-capable PCI bus serving PMC site 2, the Core Functions FPGA, and a PCI to PCI bridge which connects to the low-speed PCI peripherals.

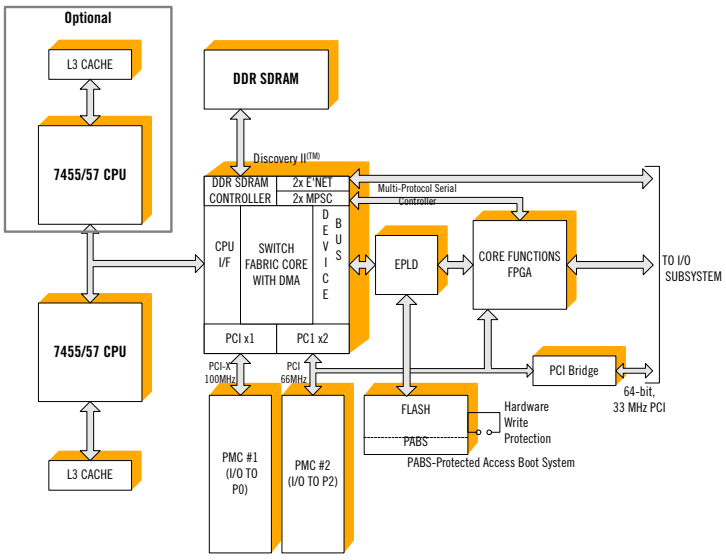


Figure 1: SVME/DMV-181 Block Diagram (See Table 3 for I/O routing options)

Discovery II Controller Delivers Full Potential of PowerPC MPX Bus

The 182's Discovery II is the first system controller to support the PowerPC's advanced MPX bus interface in a dual processor configuration, providing the following performance features:

- split transactions, illustrated in Figure 2, allows faster accesses such as to DDR SDRAM to complete in advance of an access to a slower device such as Flash or a PCI peripheral that was initiated first
- data intervention, explained further below, allows a cached copy of data found in the cache of one processor to be transferred directly to the second processor
- address streaming; no dead cycles between consecutive address tenures driven by the same device
- data streaming, no dead cycles between consecutive data phases driven by the same device

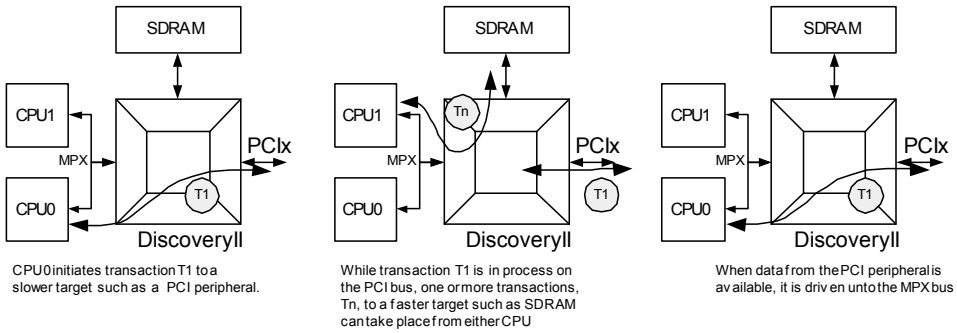


Figure 2: Support for the split transaction feature of the PowerPC's MPX bus allows the Discovery II system controller to provide data from high-speed targets such as SDRAM between the address and data phases of a transaction targeting a lower-speed peripheral.

Data intervention

If a processor using the MPX bus protocol performs a read of data that exists modified in another processor's cache, the modified data can be directly forwarded to the requesting processor. Systems based on the 60x bus, in comparison, would require that the cached data be pushed back to memory, the requesting cycle retried, and the data finally obtained from memory.

Data Intervention allows the latency for data that exists in another processor's cache to be reduced from 20 clock cycles or more to as low as 5 or 6 cycles. See Figure 3.

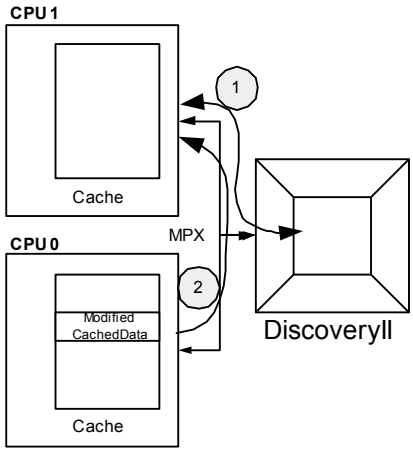


Figure 3: When a processor sees a cache-line read operation on the MPX bus (1) for data which is in it's cache in a modified state, it will intervene and provide the data directly to the requesting processor (2). This is known as Data Intervention.

Flexible I/O with Interface Personality Modules (IPMs)

Figure 4 illustrates the 182's feature-rich I/O subsystem. I/O features inherent to the 182 basecard include VME, two RS-232, two Ethernet, and two USB 2.0 ports, card fail status out, card reset input, and ALT-BOOT input.

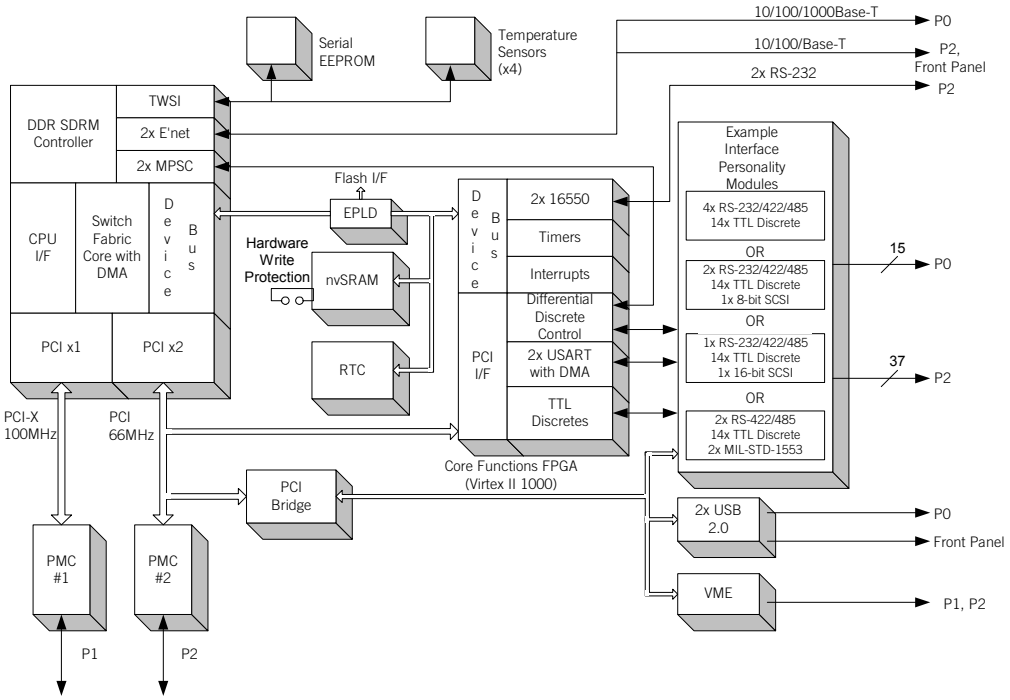


Figure 4: 182 I/O Subsystem Architecture

Designed for Harsh Environments

To cost-effectively address a diverse range of military/aerospace applications, the 182 is available in a range of ruggedization levels, both air- and conduction-cooled. All versions are functionally identical, with air-cooled versions (SVME) available in ruggedization levels 0 and 100, and conduction-cooled versions (DMV) in levels 100 and 200. Air-cooled level 200 is available on a special order basis. Our standard ruggedization guidelines define the environmental tolerance of each ruggedization level (see Ruggedization Guidelines datasheet for more information).

I/O can be expanded by the addition of Interface Personality Modules (IPMs) that work in conjunction with the Core Functions FPGA. The IPM is a connectorized subassembly that can either simply provide physical-level transceivers for controller devices implemented in the Core Functions FPGA as in the case of serial ports, or can host PCI peripherals such as a SCSI interface device. The combination of the large FPGA on the 182 basecard and the IPM for physical-level tailoring provides the 182 with a flexible means to incorporate product improvements and custom requirements.

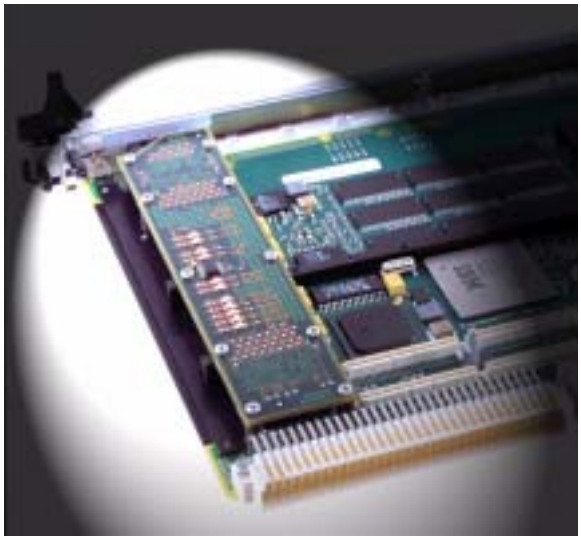


Figure 5: Interface Personality Module (IPM) Adds Flexibility

Enhanced Thermal Management for Conduction Cooled Applications

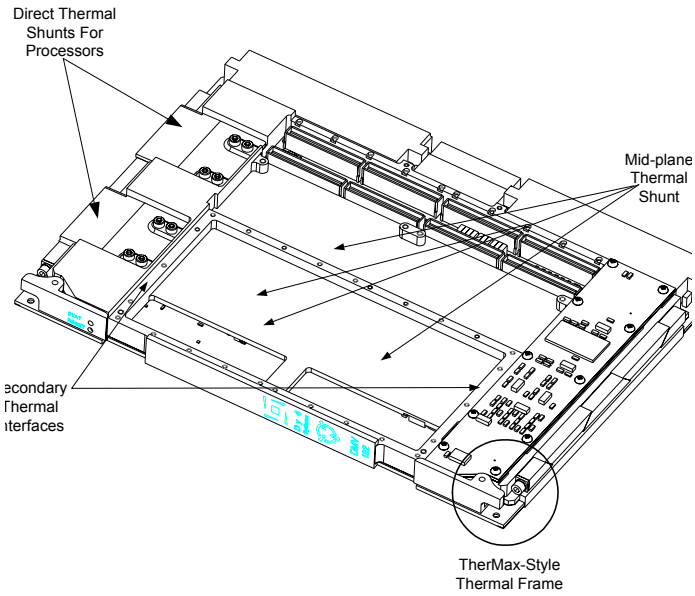
For those demanding application environments that require conduction-cooling, the 182 uses a combination of thermal management layers within the Printed Wiring Board (PWB) and an aluminum thermal frame that provides a cooling path for the PMC sites and for high-power components such as the processors, caches, and bridge device.

The 182 thermal frame employs a number of innovative design techniques to keep the temperature rise of the electronic components to a minimum, thus increasing the long-term reliability of the product:

- direct processor thermal shunts
- provision of both primary and secondary thermal interfaces on PMC sites
- mid-plane thermal shunts for PMC sites
- TherMax design approach
- full-width thermal interface to back-side slot wall

Mid-plane thermal shunts for PMCs

To optimize the conduction-cooling of high-performance, high power PMC modules such as graphics or networking PMCs, the 182 thermal frame incorporates mid-plane thermal shunts for the PMC sites. High power PMCs can include a mating cooling surface on the PMC module to contact the mid-plane thermal shunt. By taking advantage of the thermal shunt, suitably designed PMC modules can significantly lower the heat rise from the 182 card edge to the PMC components. The mid-plane thermal shunt does not impinge on the VITA 20- allowed component height.



TherMax-style thermal frame

A TherMax™ thermal frame provides an unbroken metallic path from the PMC sites and shunted components to the back-side cooling surface of the card therefore minimizing the temperature rise to these devices. In comparison, a typical thermal frame simply sits on top of the PWB and forces heat to flow through the PWB which has a high thermal resistance compared to aluminum.

Figure 6: 182 Thermal Frame

Direct processor thermal shunts

The direct processor thermal shunts provide a direct thermal path from the processor die to the top-side slot wall of the enclosure. This provides the best possible cooling path for the two processors, and also diverts heat flow from the back-side slot wall interface, which reduces the temperature rise across the card-to-slot wall interface. For a given level of processor power dissipation, having the direct processor shunts results in lower processor temperatures therefore increasing the board's reliability and/or allowing higher frequency processors to be used. The processor shunts are compatible with the standard slot geometry and do not impact the design of the enclosure.

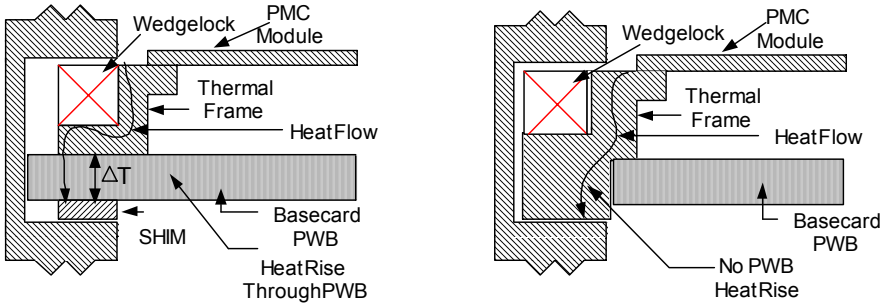


Figure 7: A TherMax thermal frame eliminates the PWB heat rise inherent in a standard thermal frame

Full-width thermal interface to back-side slot wall

To minimize the temperature rise from the mating slot wall of conduction-cooled enclosures to the back-side thermal interface region of the 182, the 182 thermal frame maximizes the thermal interface area by extending the frame to the full width of the card, as illustrated in Figure 9. This deviation from the IEEE 1101.2 standard, which calls for the thermal frame to be notched for compatibility with card guides in standard air-cooled chassis, has the benefit of lower card operating temperatures and increased long-term reliability. During test and integration activities where it may be desirable to install a conduction-cooled 182 into an air-cooled card-cage, this can normally be accomplished simply by removing the card guides.

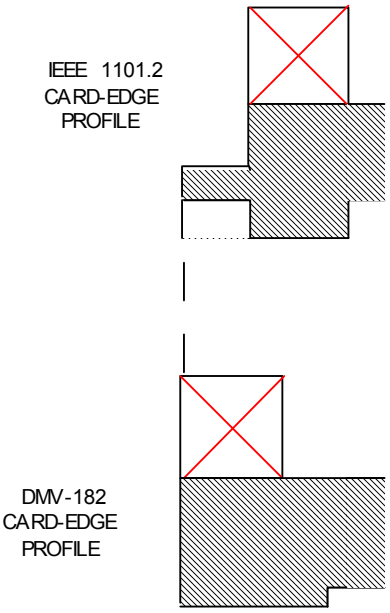


Figure 8: DMV-182 Card-Edge Profile is Optimized to Provide a Full-width Thermal Interface to the Back-side Slot Wall

Advanced 7455/57 PowerPC™ CPU

The 182 is equipped with two high performance PowerPC 7455/57 CPUs, advanced fourth generation members of Motorola®'s broad family of PowerPC family of 32/64-bit RISC microprocessors. Developed for a wide range of embedded computing applications, the 7455/57 provides industry-leading performance per watt. The 182's processors run at speeds of up to 1.2 GHz on-chip and offer estimated CPU benchmarks as shown in Table 1.

The 7455/57 processor incorporates Motorola's powerful AltiVec Technology, which enhances the PowerPC architecture through the addition of a 128-bit vector execution unit. The vector unit provides for highly parallel operations, allowing for the simultaneous execution of up to 16 integer operations or 8 floating point operations per clock cycle. For two processors each operating at 1.2 GHz, this translates to a peak theoretical computational rate of over 19.2 GFLOPS.

Table 1: Device Manufacturer's Estimated Processor Performance (Per Device)

Processor	7457 @ 1 GHz	7457 @ 1.2 GHz
Dhrystone 2.1 MIPS	2,308 (1)	2,770 (1)

(1) Motorola 7457 Fact Sheet, MPC7457FS/D Rev. 0

Multiprocessor Support Features

The 182 provides a number of important features to allow the applications software running on the two processors to communicate efficiently and to share the hardware resources of the board. These consist of the following:

- SMP-style shared memory, providing each processor with a uniform view of the board memory map, including Flash and SDRAM
- doorbell interrupt registers
- semaphore registers
- powerful interrupt mapping logic

Doorbell interrupt registers

Implemented within the Discovery™ II system controller, the 182 has a doorbell interrupt register for each processor. The doorbell interrupt registers allow for processor-to-processor interrupts, PCI-to-processor interrupts, or for a processor to interrupt itself.

Semaphore registers

Implemented within the Discovery™ II system controller, the 182 has a total of 8 high-speed hardware semaphore registers that can be used as locks for resources being shared between the two processors and/or a PCI device. Having dedicated hardware semaphores can avoid having the processor access SDRAM for semaphore operations, creating additional contention for that critical resource.

Powerful interrupt mapping logic

Through a combination of the Discovery™ II system controller and logic implemented in the Core Functions FPGA, the 182 allows the hardware to adapt to the needs of the software by providing a means to route all interrupts sources (PMCs, VME, PCI, peripherals, etc.) to either or both processors. This feature speeds interrupt response time by routing the interrupt directly to the intended processor.

Memory Subsystems

Two MB of L3 Cache Per Processor

The 182 provides 2 MB of L3 cache per processor, with parity error detection. Running at 200 MHz, the L3 cache bus is capable of a peak data transfer rate of 1.6 GB/sec. To provide more deterministic code execution times for repetitive algorithms, the 7455/57 processor can configure the L3 cache memory to be treated as high-performance direct-mapped SRAM. This provides software a straightforward way to load and maintain key code segments and associated data sets in high-speed memory.

Up To 1 GB of Dual Data Rate (DDR) SDRAM

The main memory of the 182 consists of either 512 MB or 1 GB of high performance Dual Data Rate (DDR) SDRAM. To preserve data integrity, the SDRAM is provided with Error Checking and Correcting (ECC) circuitry that detects and corrects all single-bit data errors, detects all double bit errors, and detects all three and four bit errors within the same nibble. With ECC enabled, the instantaneous peak data transfer rate to the DDR SDRAM is 1.6 GB/sec.

The DDR SDRAM is accessible from the processor and from both PCI busses. Via the Universe II™ PCI-to-VME interface, the DDR SDRAM is also accessible from the VMEbus.

128 MB of Flash Memory

The 182 provides 128 MB of contiguous, directly-accessible, high-speed Flash memory using 70 nsec. AMD Am29PDL128G devices. The Flash devices are specified for a minimum of 1,000,000 program-erase cycles and a data retention time of 20 years.

Read performance of the Flash array is optimized in order to minimize system boot up time for applications such as avionics mission computers where fast restarts after power interruptions are critical, and execution directly from Flash without first cross loading to SDRAM is advantageous. Optimizations include Flash decoding logic being implemented within a high-speed EPLD device, and a form of interleaving whereby multiple Flash devices are addressed in parallel and data is read out in turn using sequenced Output Enables.

For absolute security against inadvertent Flash programming or corruption, a hardware jumper is provided to disable the Write Enable line to the Flash devices. Cards are configured for shipment with Flash reprogramming enabled in hardware.

Flash memory is reprogrammable on-board using our Non-Volatile Memory Programmer utility embedded into the standard Foundation Firmware.

Protected Access Boot System (PABS)

PABS provides a backup boot capability in the event that the foundation firmware in the main Flash becomes corrupted. This can occur because of an error during reprogramming or an incorrect image being loaded. PABS provides users with a convenient mechanism to recover from corruption of the main Flash without removing the card from the system in which it is installed. When a P0 backplane pin is asserted the 182 will boot from PABS, and run a utility that will allow user's to reinstall our Foundation Firmware and from there the application code.

256 KB High-Speed SRAM

Incorporated into the Discovery™ II system controller, the 182 provides 256KB of high-speed SRAM directly on the processors' MPX bus. While useful as a general-purpose high-performance memory area that offloads traffic to SDRAM, the high-speed SRAM is particularly beneficial for holding descriptors for Discovery™ II peripheral devices, allowing DMA units to simultaneous access data from SDRAM while descriptors are accessed from the SRAM.

32 KB of AutoStore nvSRAM

A Simtek 14C88-3 AutoStore nvSRAM provides fast, non-volatile storage of mission state data that must not be lost when power is removed. During normal operation, application software reads and writes the AutoStore nvSRAM just like standard SRAM, with no special programming algorithm required. Upon detecting a power loss on the +5 V rail, an AutoStore cycle is performed and all 32 KB are automatically transferred from the on-chip SRAM to the on-chip EEPROM using energy stored in an on-board capacitor. At the next power-up a recall cycle is performed to transfer the EEPROM contents back to the SRAM, where the application code can now

utilize the stored data to continue normal operation. The number of recall cycles is unlimited: the maximum number of store cycles is 1,000,000 and the data retention period is 100 years.

For security against inadvertent writes to nvSRAM, a hardware jumper is provided to disable the Write Enable line to the device. Cards are configured for shipment with nvSRAM reprogramming enabled in hardware.

A planned enhancement to the 182 will increase the amount of nvSRAM provided as standard to 128 KB. Contact your local representative for schedule details.

Serial EEPROM

The 182 provides 512 bytes of Serial EEPROM for storing configuration data used by card initialization firmware.

Ethernet & SCSI

Two Ethernet™ Interfaces

The 182 is equipped with two Ethernet interfaces, both implemented within the Discovery™ II system controller device. Ethernet 1 is 10/100BASE-T capable and routed to both the front panel and P2 connectors. Ethernet 2 is 10/100/1000BASE-T capable and is routed to the P0 connector.

The Discovery™ II Ethernet controllers integrate a number of features designed to minimize processor loading due to Ethernet traffic. These include dedicated DMA engines, support for jumbo packets up to 9KB, efficient buffer management schemes, checksum calculation for IP, TCP, and UDP, and interrupt coalescence.

Optional 8/16-Bit SCSI-2 Interface

The 182 optionally provides a single-ended, 8- or 16-bit Ultra SCSI (SCSI-2) interface, based on the LSI Logic 53C875 SCSI controller. The 53C875 is a highly autonomous device and transfers data to and from PCI via an internal SCSI DMA controller and an associated DMA FIFO, minimizing the loading of the main PowerPC processors by SCSI traffic. As a PCI master the 53C875 is capable of zero wait-state data bursts at 132 MB/sec, conserving both PCI bus and main memory bandwidth.

In 16-bit mode the device supports peak transfer rates of 40 MB/sec synchronous and 14 MB/sec asynchronous. In 8-bit mode peak transfer rates on the SCSI bus are 20 MB/sec in synchronous mode and 7 MB/sec asynchronous.

See Table 3, I/O Options, for information on I/O options that include SCSI.

Serial Ports & USB

Two RS-232 Serial Ports

Serial channels 1 and 2 are RS-232 serial ports implemented with a 16550- based controller built into the Core Functions FPGA. A base clock of 36.864 MHz allows for all standard asynchronous baud rates from 50 baud to 115.2 Kbaud. The baud rate of each port can be set independently. The DSR signal on serial channel 1 is used as a cable detect signal to force the card to boot into the General Purpose Monitor.

On air-cooled cards the two RS-232 channels are accessible on the front panel in addition to being available on the rear-panel on both air- and conduction-cooled cards.

Option for Up to Four RS-232/422/485 Serial Ports

Up to a total of four asynchronous- and synchronous-capable RS-232/422/485 ports are available on the 182.

Serial channels 3 and 4 are implemented with the Discovery™ II's Multi-Protocol Serial Controllers (MPSC). These powerful serial controllers handle standard asynchronous and synchronous HDLC/SDLC modes, and in addition provide a transparent mode. In synchronous mode a full range of data encoding schemes are supported (NRZ, NRZI Mark, NRZI Space, FM0, FM1, Manchester, and Differential Manchester). Based on an input clock of 100 MHz, all standard asynchronous baud rates up to 115.2Kbaud are provided as well as synchronous bit rates up to 5 Mbits/sec for NRZ clock mode, 2.5 Mbits/sec for clock-encoded modes (FM0, FM1, etc.). The Discovery™ II MPSC ports are equipped with dedicated DMA controllers to offload the processors from handling serial data traffic to and from the controllers.

The choice of physical level (RS-232 or RS-422/485) for the MPSC serial channels is software selectable on a per-channel basis via a control register within the Core Functions FPGA.

Serial channels 5 and 6 are implemented with a IP-based Synchronous Serial Controller (SSC) built into the Core Functions FPGA. An input clock of 36.864 MHz provides for asynchronous communication at baud rates from 1200 to 115.2 Kbaud, and synchronous HDLC/SDLC data rates up to 2.0 Mbps. To support high data rate applications without excessive loading of the processors, dedicated serial DMA controllers are provided, implemented within the Core Functions FPGA.

The choice of physical level (RS-232 or RS-422/485) for the SSC serial channels is software selectable on a per-channel basis via a control register within the Core Functions FPGA.

See Differential Discrete I/O below for information on how the 182 provides the capability to control each of the RS-422/485 drivers and receivers as differential-mode discrete signals for use as serial control signals or general purpose I/O.

See Table 3, I/O Options, for information on which serial I/O channels are available for the different I/O options.

Up to 16 Bits of Differential Discrete Digital I/O

The 182 provides the capability to control each of the RS-422/485 drivers and receivers as differential-mode discrete signals via registers in the Core Functions FPGA. This allows flexibility in how the drivers and receivers are used. The choice of whether the drivers and receivers are attached to serial ports or used as discrete differential I/O is software selectable on a per-serial channel basis. When configured as discrete differential I/O, the drivers and receivers can be used as serial-line control signals (RTS, CD, etc.) in conjunction with another serial channel, or used as general-purpose differential-mode control signals unrelated to serial I/O requirements. Differential discrete inputs can generate an interrupt upon a change of state, with programmable edge direction. Note that if the serial channel physical levels are set to RS-232, then discrete digital I/O at RS-232 levels is obtained.

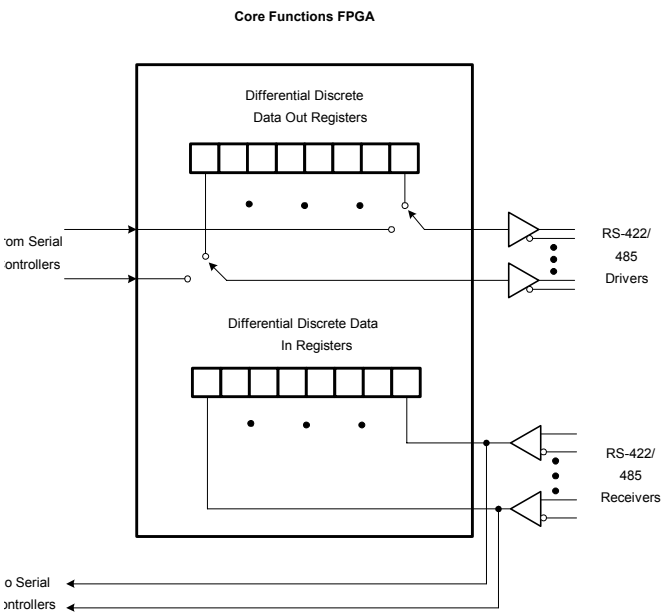


Figure 9: Option for Discrete Control of RS-422/485 Drivers and Receivers

Two USB 2.0 Ports

The 182 incorporates an NEC uPD720100 which provides two USB 2.0-capable ports in a 32-bit, 33 MHz PCI 2.2-compatible device. Each port can handle high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation. When operating at low-speed or full-speed, each port is managed by independent OHCI-compliant controllers internal to the device. One EHCI-compliant controller manages any ports operating in high-speed mode. One USB port is accessible on the front panel connector only, the other is accessible on the P0 connector only. Each port provides a fused +5V output to power low-power USB devices such as keyboards.

14 Bits of LVTTL Discrete Digital I/O

The 182 optionally provides 14 bits of LVTTL-compatible discrete digital I/O. Each bit is individually programmable to be an input or output. In addition, each bit is capable of generating an interrupt upon a change of state, with the edge direction (high-to-low, low-to-high) also being programmable. Each bit has a 10K pull-up resistor to 5V. Output drive current is 24 mA.

Timers & RTC

Real-Time Clock (RTC)

A Maxim/Dallas Semiconductor DS1501 real-time clock chip provides the RTC function. It contains registers for century, year, month, day, hours, minutes, and seconds. The RTC is capable of generating alarm interrupts.

The RTC draws its power from the standard +5 V input during normal operation. In the event of loss of +5 V power, the RTC will automatically switch over to draw current from the +5V STDBY line.

Extensive Timing Resources

The 182 provides a large number of timing resources to facilitate precise timing and control of system events. The list of available timers is given in Table 2.

Avionics Watchdog Timers

The 182 provides two watchdog timers, one for each processor. Each watchdog timer is a presettable downcounter with a resolution of 1 usec. Time periods from 1 usec to 16 seconds can be programmed. Initialization software can select whether a watchdog exception event causes an interrupt or a card reset. Once enabled to cause a reset, the watchdog cannot be disabled. A watchdog time-out log bit tells start-up code whether the last card reset was due to a watchdog exception.

The watchdog timer can be used in two ways. Used as a standard watchdog timer, a single time period is programmed which defines a maximum interval between writes to the watchdog register. For increased system integrity, the watchdog can optionally be configured to operate in "Avionics" mode whereby a minimum interval between writes to the watchdog register is also enforced. I.e., writing to the watchdog register either too soon or too late causes an exception event.

Table 2: 182 Timing Resources

Timer Facility	Implementation	Type	Size	Tick Rate/ Period	Maximum Duration
PowerPC	CPU	Free running counter	64 bit	25.0 Mhz/40.0 nsec.	23,398 years
Time Base Register					
PowerPC	CPU	Presettable, readable downcounter	32 bit	25.0 Mhz/40.0 nsec.	171.8 sec.
Decrementer					
General Purpose #0-3	Discovery II	Presettable, readable downcounter with autoreload or stop options	32 bit	100.0 Mhz/10 nsec.	42.95 sec.
RTC Alarm Interrupt	Real-time clock	alarm interrupt	-	specific day, hour, minute, and second	-
Watchdog Timers (one per CPU)	Core Functions FPGA	Presettable, readable downcounter with interrupt or reset on terminal count	24 bit	1 Mhz/1 usec.	16.77 sec
System Timers #1-6	Core Functions FPGA	Presettable, readable, downcounters with interrupt on terminal count	32 bit	50 MHz/20 usec.	85.9 sec.

Four General Purpose DMA Controllers

Four DMA controllers provided by the Discovery™ II bridge chip are available for general purpose use. The four general purpose DMA controllers can be used for transferring blocks of data between the SDRAM, Flash memory, device bus peripherals, and the PCI busses without loading down the PowerPC CPU. The General Purpose DMA controllers are capable of sustaining burst transfers using the full 64-bit width of the PCI bus. Advanced features include DMA chaining and the ability to schedule DMA transfers via a general-purpose timer.

For transferring large blocks of data over the VMEbus, it is recommended that the DMA controllers internal to the Universe II device be used rather than the two general purpose DMA controllers. This is because the Universe II DMA controllers are capable of supporting maximum-size MBLT block sizes on the VMEbus.

Option for Up to Two MIL-STD-1553 Channels

The 182 provides up to two MIL-STD-1553 channels implemented with DDC 65864 PCI micro-ACE TE devices offering the following key features:

- support for 1553A, 1553B Notice 2, and STANAG 3838 protocols
- BC, RT, MT modes independently selectable for each channel
- choice of transformer-coupled (standard) or direct-coupled outputs (on a special order basis)
- MIL-STD-1760 amplitude compliant
- 64K words of RAM per channel, with parity
- PCI interface is 33 MHz, 32-bit and supports burst writes with a FIFO for up to a complete 1553 message
- Transmit Inhibit input for each channel
- Bus Controller features
  - > highly autonomous bus controller with built-in message sequence control engine for multi-frame message scheduling, branching, and asynchronous message insertion
  - > programmable inter-message gap size
  - > single frame or auto-repeat modes
  - > automatic retries
  - > time-tag can be transmitted with Synchronize With Data mode code
  - > External Trigger input for each channel

- Remote Terminal features
  - > programmable illegalization of RT commands
  - > Busy bit programmable on a subaddress basis
  - > 16-bit time-tag option with options of 2, 4, 8, 16, 32, or 64 usec/LSB based on internal clock
  - > external time-tag clock input
  - > time-tag can be set via Synchronize With Data mode code
  - > external Subsystem Flag input
- Monitoring Terminal features
  - > selective message monitor mode, used for selecting monitoring based on RT address, Transmit/Receive bit, and Subaddress
  - > simultaneous RT and monitor modes

The RT address for each channel can be set by software. Also, for each channel a backplane configuration input is provided that can independently select an option whereby the RT address can be set by using a subset of the TTL discrete digital I/O lines.

To meet the MIL-STD-1760 First Response requirement of an RT response within 150 msec, one of the 1553 channels initializes as an RT with the Busy status word bit set. This requires that the 1553 channel be configured to set the RT address in hardware.

Our driver software for the 182's 1553 channels provides a flexible, easy to use, and robust applications programming interface (API). The driver supports BC, RT, and MT modes of operation, and offers a high degree of compatibility to the proven software driver provided for our popular PMC-601 1553 module. Source code is provided for user reference.

The 1553 driver for the 182 is sold separately from the hardware and the 182 Board Support Packages, part number DSW-602-000-CD. See separate datasheet for details.

Figure 10: Interface Personality Module with MIL-STD-1553

VME Interface

The 64-bit PCI architecture of the 182 combined with the Universe II's 64-bit PCI interface and extensive decoupling FIFOs allow for high-speed, bandwidth efficient data transfers between the VMEbus and on-board memory and PCI targets. VME data can be transferred at the full sustained rate of 50+ MB/sec supported by the Universe II while only consuming only a fraction of the local PCI bus bandwidth of 264 MB/sec.

Other key features of the 182's VME interface include:

- Full system controller capability including our own/Tundra Auto-ID option
- Programmable DMA controller with linked list support
- Wide range of VMEbus address and data transfer modes;
  - > A32/A24/A16 master and slave, (not A64 or A40)
  - > D64/D32/D16/D08 master and slave, (no MD32)
  - > MBLT, BLT, ADOH, RMW, LOCK, and location monitors
- Four mailbox registers and four location monitors for inter-board communications and synchronization
- Nine programmable PCI-to-VME windows and eight programmable VME-to-PCI windows
- Extensive support for Built-in-Test

The 182 also provides support for five geographical addressing bits as defined by the ANSI/VITA 1.1-1997 (VME64 extensions) specification.

PMC Sites

The functionality of the 182 SBC can be substantially expanded via its two PCI Mezzanine Card (PMC) sites. The two PMC sites interface to other system elements via 64-pins of back panel I/O per site. The placement of the PMC sites is such that a single, double width PMC module can also be fitted.

PMC site 1 (closer to top of card) is served by its own dedicated 64-bit, 100 MHz-capable PCI-X bus providing a peak bandwidth to memory of 800 MB/sec. High-performance PMC modules such as networking modules or graphics modules can operate at 100 MHz independent of the speed at which the PMC module in PMC site 2 operates. PMC site 2 (closer to bottom of card) is served by a 64-bit, 66 MHz PCI bus providing a peak bandwidth to memory of 533 MB/sec.

I/O routing is done in accordance with ANSI/VITA 35-2000 specification, such that PMC site 1's I/O is routed to the P0 connector, while that of PMC site #2 is routed to A and C rows of the P2 connector. Front panel I/O is supported as a standard feature on air-cooled cards and, on a special order basis, for conduction-cooled cards.

The 182 conforms fully to the IEEE 1386/1386.1 requirement for a component keep-out area at the front of the PMC site for connectors or high components.

Each PMC site uses 3.3V signaling, is 5V tolerant, and is keyed as a universal PMC site meaning that no keys are installed. The Vio voltage to each PMC is selectable via push-on jumpers.

Routing for High-Speed PMC I/O Signals

The 182's routing for PMC I/O signals to the rear-panel connectors is carefully implemented to support high-bandwidth signals.

PMC site #1, which routes to the P0 connector in accordance with ANSI/VITA 35-2000, has the following routing provisions:

- 27 differential pairs with a nominal impedance of 50 ohms
- pair-to-pair skew is controlled within various pair groupings as required to support multiple TMDS and LVDS digital video channels as implemented on our PMC-70x graphics modules
- select pairs constrain in-pair skew to 0.012" (nominal) to support two Fibre Channel interfaces as implemented on the PMC-643 Fibre Channel PMC

PMC site #2, which routes to the A & C rows of P2, has the following routing provisions:

- all 64 signals are routed as differential pairs with a nominal impedance of 50 ohms capable of supporting four full StarFabric links as implemented on the StarLink PMC module
- pair-to-pair skew is controlled within various pair groupings as required to support multiple TMDS and LVDS digital video channels as implemented on the PMC-70x graphics modules
- select pairs constrain in-pair skew to 0.012" (nominal) to support two Fibre Channel interfaces as implemented on the PMC-643 Fibre Channel PMC

Contact your representative for further information on the routing provisions for high-speed PMC I/O.

PMC Power Routing

The PMC sites are provided with 3.3V, +12V, and -12V power from the VMEbus backplane. No 3.3V power is provided to the PMC sites by the regulators on the 182 basecard itself.

Support for Processor PMCs

The 182 is capable of hosting Processor PMCs in non-Monarch mode as described in the VITA 32-2003 draft standard (the Monarch# signal is left floating). The 182 does not support the optional second PCI agent, the optional EREADY signal, or the optional RESETOUT# signal.

Conduction-Cooled PMC Modules

To support the industry drive to open standards on conduction-cooled cards, the PMC site mechanical interfaces follow the VITA 20-2001 Conduction Cooled PCI Mezzanine Card standard. To optimize the thermal transfer from PMC modules to the base card the standard 182 thermal frame incorporates both the Primary and Secondary thermal interfaces as defined by VITA 20-2001.

The combination of the secondary thermal interfaces, the mid-plane thermal shunt, and our own unique TherMax™ thermal frame design provides optimum cooling for conduction-cooled PMC modules, allowing for higher power PMCs and/or increased long-term reliability through lower component temperatures.

Utility Features

Status Indicators and Controls

The 182 SBC provides run/fail status by asserting a backplane signal and illuminating a red front panel LED in the event the diagnostics detect a card failure. There is also a software controlled green LED that the application can use to indicate status.

A card reset signal is available on the backplane connectors and on the front panel connector on air-cooled cards. The front panel and P0 break-out cables for the 182 include a push button switch that interfaces to this signal to allow the card to be reset without doing a full system reset.

COP and JTAG Test and Debug Interfaces

For software debug purposes the Control and Observation Port (COP) of the 7455/7457 processors are accessible via solder pads on the top side of the board in the PMC front panel keep out area. A wire link option allows one processor or the other to be accessed via the COP interface.

To support acceptance testing the 182 provides a JTAG scan chain that can be made accessible on Reserved pins on the P1 connector. An on-board jumper enables JTAG to the P1. The JTAG test chain coverage includes the processors, L3 cache devices, Discovery™ II system controller, VMEbus interface chip, FPGA, and EPLD. PMC modules are automatically added to the JTAG chain when present.

Temperature Sensors

The 182 provides four Maxim 6634 temperature sensors located at the approximate corners of the board. Software can read the temperature sensors at any time through their I2C interface connected via the Discovery™ II system controller, or receive an independent interrupt for each sensor when a software programmable over- or under- temperature condition occurs. The temperature sensors are accurate to +/-2.5C from -40C to 125C.

I/O Options

See Table 3 for a definition of the various I/O modes available for the 182.

Table 3: SVME/DMV-182 I/O Options

Mode	Front Panel (air-cooled only)	P0 Connector	P2 Connector
#00	Upper 9-pin connector: • Serial 1, RS-232 • Serial 2, RS-232 • card reset input Lower 9-pin connector • E'net 1 • USB 1	PMC site #1 I/O E'net 2 (GBE) USB 2 cardfail status out card reset input ALT-BOOT input	PMC Site #2 I/O (rows A&C) E'net 1 (10/100) Serial 1, RS-232 Serial 2, RS-232
#01	Same	PMC site #1 I/O E'net 2 (GBE) 14 TTL discrete I/O USB 2 cardfail status out card reset input ALT_BOOT input	PMC site #2 I/O (rows A&C) E'net 1 (10/100) 8-bit SCSI Serial 1, RS-232 Serial 2, RS-232 Serial 3, RS-232/422/485 Serial 4, RS-232/422/485
#04	Same	Same	PMC site #2 I/O (rows A&C) E'net 1 (10/100) 16-bit SCSI Serial 1, RS-232 Serial 2, RS-232 Serial 3, RS-232/422/485
#06	Same	Same	PMC site #2 I/O (rows A&C) E'net 1 (10/100) Serial 1, RS-232 Serial 2, RS-232 Serial 3, RS-232/422/485 Serial 4, RS-232/422/485 Serial 5, RS-232/422/485 Serial 6, RS-232/422/485
#08	Same	Same	PMC site #2 I/O (rows A&C) E'net 1 (10/100) Serial 1, RS-232 Serial 2, RS-232 Serial 3, RS-232/422/485 Serial 4, RS-232/422/485 MIL-STD-1553 #1
#09	Same	Same	PMC site #2 I/O (rows A&C) E'net 1 (10/100) Serial 1, RS-232 Serial 2, RS-232 Serial 3, RS-232/422/485 Serial 4, RS-232/422/485 MIL-STD-1553 #1 MIL-STD-1553 #2

Software Support

Foundation Firmware and BIT

The 182 SBC is equipped with a comprehensive on-board firmware package called Foundation Firmware that includes:

- General Purpose Monitor (GPM) - provides monitoring, diagnostic, and board exerciser functions to facilitate system startup and integration activities (see General Purpose Monitor data sheet for more information)
- Built-in-Test (BIT) - a library of Card Level Diagnostic (CLD) routines is provided to support Power-up BIT (PBIT), Initiated BIT (IBIT) and Continuous BIT (CBIT) (see Card Level Diagnostics data sheet for more information)
- Non Volatile Memory Programmer (NVMP) - provides for in-circuit and closed chassis reprogramming of Flash memory over serial port or Ethernet (see Non-Volatile Memory Programmer data sheet for more information)

Our BIT firmware is designed to provide 95% fault coverage for testable functionality and supports tests in Power-up BIT (PBIT), Initiated BIT (IBIT), and Continuous BIT (CBIT) modes. PBIT consists of a reduced set of tests that provide confidence that the hardware is operating correctly while minimizing power-up time.

The IBIT capability allows users to initiate testing with a more comprehensive suite of tests to provide more robust testing in an off-line mode. CBIT allows applications to test hardware components in the background while the mission software operates as a higher priority task. The selection of tests for PBIT, IBIT, and CBIT is user configurable.

Operating System Software

The 182 is supported by the following real-time operating systems:

- VxWorks® (Tornado™) from Wind River Systems (part number is DSW-182-002-CD, see separate VxWorks BSP and Driver Suite datasheet for details)
- INTEGRITY from Green Hills Software (part number is DSW-182-404-CD, see separate datasheet for details).
- Linux SDK from TimeSys Corporation

Contact your local representative for updates on support for other operating systems.

IXLibs-AV DSP Library

Our IXLibs-AV DSP library allows customers to fully exploit the performance potential of the 182's AltiVec-equipped 7455/7457 processors. IXLibs-AV provides a comprehensive set of AltiVec-optimized C-callable functions written primarily in assembly language, yielding a significant performance advantage over equivalent functions written only in a high-level language. This object-format library integrates easily with standard software development tools and supports real and complex array, vector, and scalar signal processing functions.

Part number is DSW-DEV-IXLIBAV-OO.

Integration Support

We provide all the supporting items necessary to ensure a smooth system integration process. These include:

- Comprehensive hardware, firmware, and software documentation package, in hard copy and on CD-ROM
- Break-out cables for the front and rear-panel I/O to convert the 182-specific pin-outs to industry standard connectors for use in laboratory development environments. See Table 4.

Professional technical support from our in-house team of Technical Support Specialists to ensure timely resolution of any support issues

Table 4: SVME/DMV-182 Cable Set

Cable Number	Connects To	Description
CBL-182-FPL-000	front panel in all pin-out modes	Two-part front panel cable set for SVME-182. One cable provides two 9-pin D connectors for RS-232 ports and a push-button switch for card reset; second cable provides standard RJ-45 10/100BaseT Ethernet jack and one USB type A receptacle.
CBL-182-P0-000	P0 in all pin-out modes	P0 break-out cable for SVME/DMV-182 in all pin-out modes. Provides RJ-45 Jack for 10/100/1000BaseT Ethernet interface, 25-pin female D connector for TTL discretes, USB type A receptable for USB port 2, and PMC I/O on our standard 78-way connector. Also includes reset switch
CBL-182-P2-000	P2 in pin-out mode 0 (no IPM)	P2 break-out cable for SVME/DMV-182 in pin-out mode 0. Provides two 9-pin D connectors for RS-232 ports and our standard 78-way connector for PMC I/O. (Note - no Ethernet connector.)
CBL-SBC-P2-000	P2 in pin-out mode 1	P2 break-out cable with separate branches and connectors for 8-bit SCSI interface (using 68-way 16-bit SCSI connector), 2 EIA-232 ports, EIA-422/485 ports 3 and 4, and PMC I/O on our standard 78-way connector. (Note - no Ethernet branch.)
CBL-SBC-P2-002	P2 in pin-out mode 4	P2 break-out cable with separate branches and connectors for 16-bit SCSI interface (using 68-way 16-bit SCSI connector), 2 EIA-232 ports, EIA-422/485 port 3, and PMC I/O on our standard 78-way connector. (Note - no Ethernet branch.)
CBL-SBC-P2-003	P2 in pin-out mode 6	P2 breakout cable with separate branches and connectors for 2 EIA-232 ports, 4 EIA-422/485 ports, and PMC I/O on our standard 78-way connector. (Note - no Ethernet branch.)
CBL-182-P2-009	P2 in pin-out mode 8 and 9	P2 break-out for SVME-182 in mode 8 (single 1553) and mode 9 (dual 1553). Provides separate branches and connectors for the transformer-coupled '1553 signals, '1553 configuration inputs, two RS-232 ports, two RS-232/422/485 ports, and PMC I/O on our standard 78-way connector. Connectors for '1553 signals are 3-lug Twinax bulkhead jack connectors (Trompeter part number BJ79-47)

Specifications

Power Inputs

The 182 basecard uses only +5V and optionally +5V STDBY for the real-time clock. On-board regulators provide all necessary internal voltages. Backplane +5 V, ±12 V, and 3.3V is routed to the PMC sites.

Power Consumption

Power consumption increases as operating temperature rises. Table 5 figures are for the highest rated operating temperature while executing a test application generating CPU processing loads and data traffic representative of a typical customer application.

Table 5: Power Consumption

Ruggedization Level	Reference Configuration	Typical	Maximum
Level 0 air-cooled	SVME-182-0600	TBD	TBD
Level 100 air-cooled	SVME-182-1600	TBD	TBD
Level 100 conduction-cooled	DMV-182-1600	40W	TBD
Level 200 conduction-cooled	DMV-182-2600	45W	TBD

Mechanical Format

Conduction-cooled modules conform to the dimensions defined in IEEE 1101.2-1992, Standard for Mechanical Core Specifications for Conduction-Cooled Eurocards.

Air-cooled modules conform to the dimensions defined in ANSI/VITA 1-1994, American National Standard for VME64. Front panel hardware on air-cooled modules includes: injector/extractor handles, EMC strip, alignment pin, and keying provisions in accordance with ANSI/VITA 1.1, American National Standards for VME64 Extensions (and IEEE 1101.10).

For air-cooled applications where the enclosure is not compatible with the IEEE 1101.10-style front panels, original-style non-injector equipped front panel kits can be purchased separately and fitted to the card by the customer.

Table 6: SVME/DMV-182 Specifications

Power Requirements	Maximum	Typical
+5 V (+5.0%, -2.5%)	See Table 5	See Table 5
+12 V	0 A	Not used by the base card, only routed to the PMC sites.
-12 V	0 A	Not used by the base card, only routed to the PMC sites.
3.3 V	0 A	Not used by the base card, only routed to the PMC sites.
+5 V STDBY: - with +5 V present - without +5 V	 <tbd uA <tbd uA	 <tdb uA <tbd uA

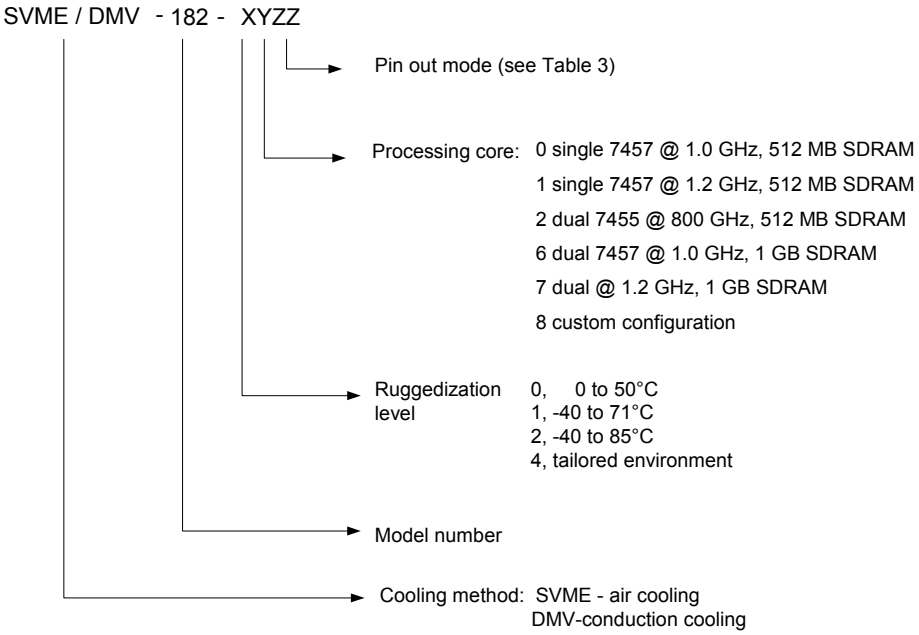
Dimensions & Weight	Dimensions	Weight
SVME card	per ANSI/VITA 1-1994	<500 g (<1.21 lbs.)
DMV card	per IEEE 1101.2**	<800 g (<1.77 lbs)
** Except for the card-edge profile as shown in Figure 8		

Ruggedization Levels	
SVME card	Available in levels 0, 100 (Required airflow is TBD cfm at sea level)
DMV card	Available in levels 100 and 200
Unless otherwise noted environmental tolerance is as defined in the Ruggedization Guidelines datasheet.	

Part Numbers

Table 7: Part Numbers

Check with your local representative for availability of specific part numbers.



Contact Information

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