User's Manual

PTIMBAT400-PB / PBAT66-PB

Rev. 2.0 - Valid for BusView version 2.6x & firmware revision 5.6x

PTIMBAT400-PB	PCI Bus 400 MHz Timing Analyzer & Anomaly Trigger
PBAT66-PB	PCI Bus Anomaly Trigger

Piggyback Modules for the PBT-415

CE

VMETRO

The Bus Analyzer Specialist

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USA:

VMETRO, Inc.
1880 Dairy Ashford, #535
HOUSTON, TX 77077, USA
Tel: (281) 584-0728
Fax: (281) 584-9034

Europe, Asia:

VMETRO asa
Brynsveien 5
0667 OSLO, Norway
Tel: +47 22 10 60 90
Fax: +47 22 10 62 02

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1. PRODUCT OVERVIEW

1.1 Product Highlights

The PTIMBAT400-PB and the PBAT66-PB, are piggyback modules for use with the PBT-415 (PCI Bus Analyzer & Exerciser). The PTIMBAT400-PB is a piggyback module combining the functionality of the PBAT66-PB and a 400MHz Timing Analyzer into one piggyback module.

The PBAT66 features a comprehensive PCI Bus Anomaly Trigger, which automatically screens the PCI bus for violations of the bus protocol, like illegal signal sequences, timing, setup times on address/data lines, etc.

The 400MHz Timing Analyzer provides a powerful, full-featured 64-channel 400 MHz timing analyzer for the PCI bus, for high-resolution analysis of the bus timing. When installed on a PBT-415, the timing analyzer comes in addition to the analyzing and exercising capabilities of the PBT-415, i.e. as a completely independent analyzer. This means that the PBT-415 can run its PCI transfer or clock analysis in parallel with the PTIMBAT400-PB 400 MHz PCI timing analysis.

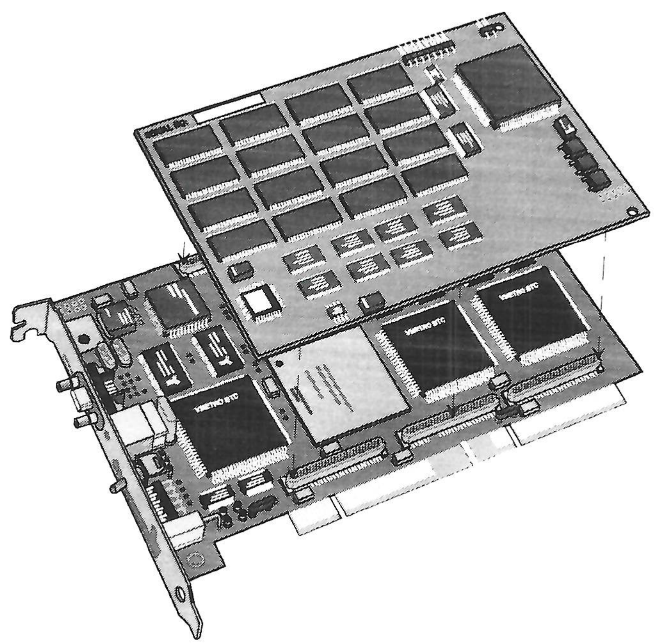


Figure 1.1 The PBT-415 with the PBAT66-PB or PTIMBAT400-PB

1.1.1 Anomaly Trigger (PBAT66-PB)

- Detects anomalies in all types of 32 bits PCI cycles in 33MHz and 66MHz systems (PCI bus specification 2.1).
- Recognizes 38 classes of PCI bus violations, resulting in 68 violations in total. Hardwired trigger logic eliminates the need to specify trigger words.
- Is a passive detector which does not drive any lines and does not affect in any way the operation of the PCI bus system.
- Can be used to cross-trigger the PBT-415, or an external instrument (e.g. an oscilloscope) with any anomaly trigger output signal, for detailed investigation of the signal timing that caused the violation.

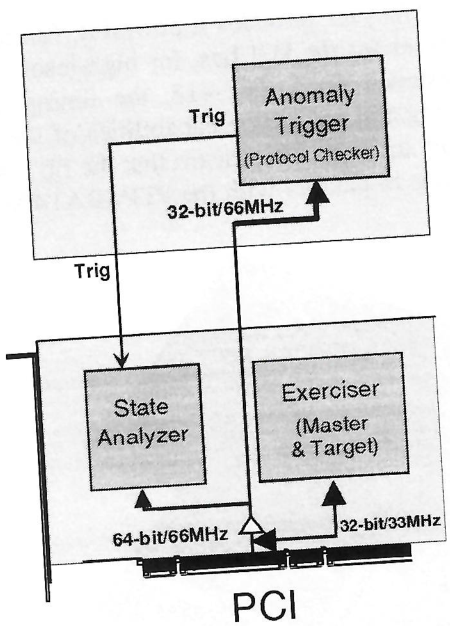


Figure 1.2 PBAT66-PB - PBT-415 cross-triggering

1.1.2 400 MHz Timing Analyzer & Anomaly Trigger (PTIMBAT400-PB)

400MHz Timing Analyzer

- Features 64 channel 32 bits PCI bus timing analysis at 400 MHz in both 33MHz and 66MHz PCI systems.
- Has 4 external inputs.
- Can be triggered from the PBAT66, the PBT-415, and the external input Ext[0]. Used with the PBT-415, simultaneous transfer and clock analysis can be performed.

- Has 4Mx64 channel trace buffer.

Anomaly Trigger

- Detects anomalies in all types of 32 bits PCI cycles in 33MHz and 66MHz systems (PCI bus specification 2.1).
- Recognizes 38 classes of PCI bus violations, resulting in 68 violations in total. Hardwired trigger logic eliminates the need to specify trigger words.
- Is a passive detector which does not drive any lines and does not affect in any way the operation of the PCI bus system.
- Can be used to cross-trigger the 400MHz Timing Analyzer, the PBT-415, or an external instrument (e.g. an oscilloscope) with any anomaly trigger output signal, for detailed investigation of the signal timing that caused the violation.

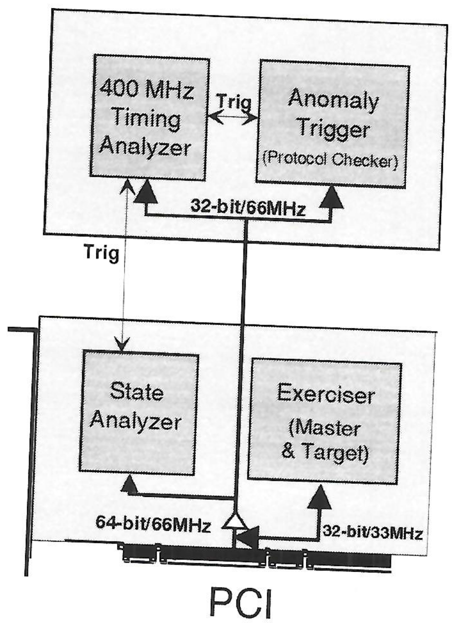


Figure 1.3 PTIMBAT400-PB - PBT-415 cross-triggering

2. INSTALLATION

2.1 Static Electricity - Precautions

Before unpacking the PBAT66-PB or the PTIMBAT400-PB from its shipping container, make sure that this takes place in an environment with controlled static electricity. The following recommendations should be followed:

- Make sure your body is discharged to the static voltage level on the floor, table and system chassis by wearing a conductive wrist-chain connected to a common reference point.
- If a conductive wrist-chain is not available, touch the surface where the board is to be put (like table, chassis etc.) before unpacking the board.
- Leave the board only on surfaces with controlled static characteristics, i.e. specially designed anti-static table covers.

If handing the board over to another person, touch this persons hand, wrist etc. to discharge any static potential.

Note! Never put the board on top of the conductive plastic bag in which the board is shipped. The external surface of the bag is highly conductive and may cause rapid static discharge causing damage. (The internal surface of the bag is insulating.) A safe place to leave the board is on the pink coating found inside the shipping container.

2.2 Mounting

The PBAT66-PB and the PTIMBAT400-PB piggyback modules are designed to be mounted on a PBT-415.

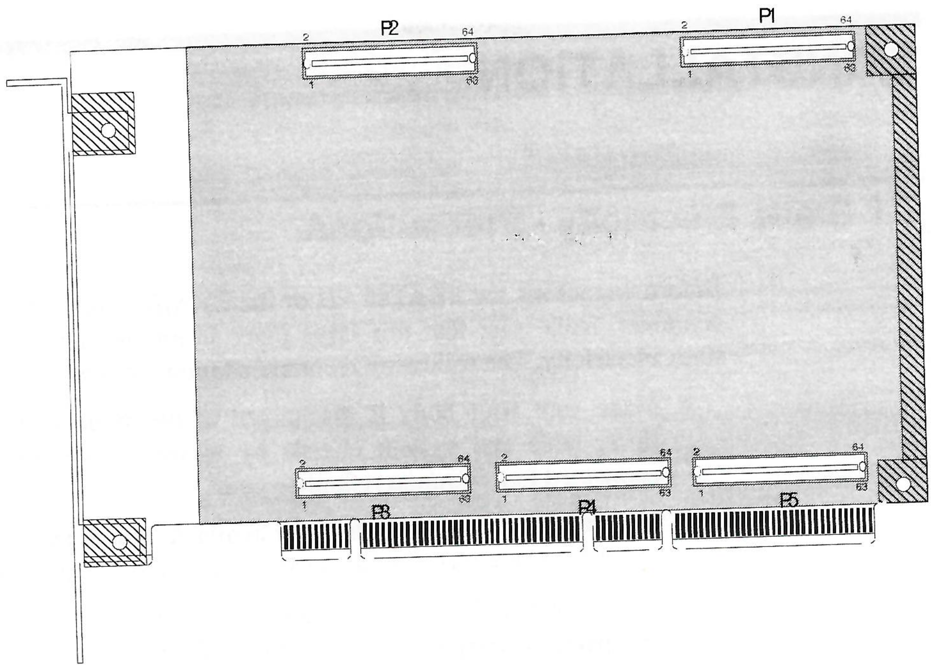


Figure 2.1 Connector layout of the PBT-415

2.2.1 Inspection

Make sure that the PTIMBAT400-PB/PBAT66-PB you have received is according to your purchase order with respect to model.

With the PTIMBAT400-PB you should find the following accessories :

- External power cable (401-315-EPC)
- The PTIMBAT400-PB cooling module.

No accessories are supplied with the PBAT66-PB.

2.2.2 PTIMBAT400-PB Cooling Module

In order to keep the PTIMBAT400-PB at its normal operating temperature within the computer case, an additional fan must be installed. Cooling is not necessary for the PBAT66-PB. This fan works in conjunction with the computers standard fan to increase the airflow around the PTIMBAT400-PB.

The PTIMBAT400-PB cooling module consists of:

- Fan.
- Power split cable, for powering the fan from the power supply in the PC.
- Plastic rivets, for mounting of the PTIMBAT400-PB on the PBT-415.

Warning!

It is mandatory that the PTIMBAT400-PB analyzer has forced air cooling. However, some systems, will have insufficient room to install the fan-cooling module. If this is the case, ensure that the target system itself provides PCI card cooling before use. Failure to provide sufficient cooling will result in board malfunction.

If the PTIMBAT400-PB piggyback card is removed from the analyzer, the fan-cooling module is not required

2.2.3 Fan Specifications

DC Volts	Voltage Range	Current	Power	Air Flow
13	8-15	300mA	3.9W	3.5CFM/~100 l/min

Table 2.1 Fan Specifications

The PTIMBAT400-PB cooling module is powered by the computers standard power supply, ensure that the addition of the cooling module doesn't exceed the power supplies maximum output current. Power for the fan is drawn from the +12Volt line located on a standard floppy/hard drive power cable.

2.2.4 Installation Procedure - Fan

Place the PBT-415 on a surface with controlled static environment, according to Section 2.1.

Mounting the fan:

- Insert the cooling module's power-split cable (supplied) before installation to the Analyzer.

The power split cable (supplied) enables the cooling-module to share a computer power connection with another device (e.g. a disk). The cable, when stretched out, has three connectors installed. The connectors mounted on each end are power outputs and the connector in the center functions as the power input.

To install the cable, insert one power output into the reciprocal located on the back of the analyzer-cooling module. Finally, connect power, from the computer's power supply, to the cables input connector. The remaining power output is available to power another computer component, as shown in Figure 2.3 and Figure 2.2.

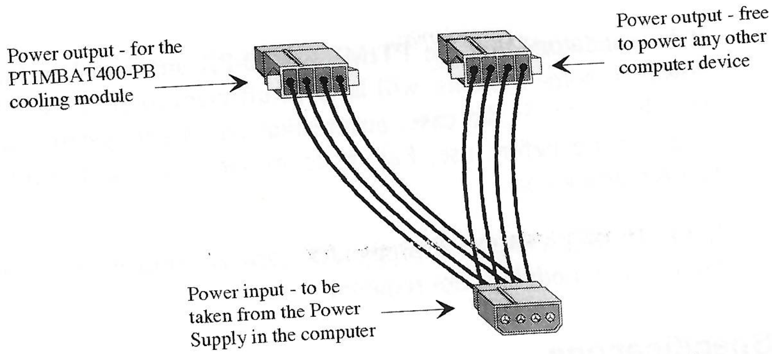


Figure 2.2 The power cable of the PTIMBAT400-PB cooling module

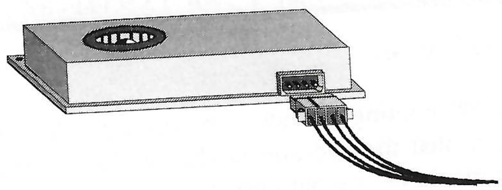


Figure 2.3 Powering the cooling module

- Place the fan under the analyzer board and align the mounting holes, as shown in Figure 2.4.
- Insert the snap rivets into the mounting holes and push the rivet head with the thumb to lock.

Note! The snap rivets can be removed and re-installed. To release, push the rivet-expanding pin until level with legs, then remove rivet head.

Warning! Once the cooling module is installed on to the Analyzer, do not attempt to remove or refit the power cable. Attempting to do so places stress on the analyzer circuit board, possibly causing damage. If power cable removal is necessary, the cooling module must first be removed from the Analyzer.

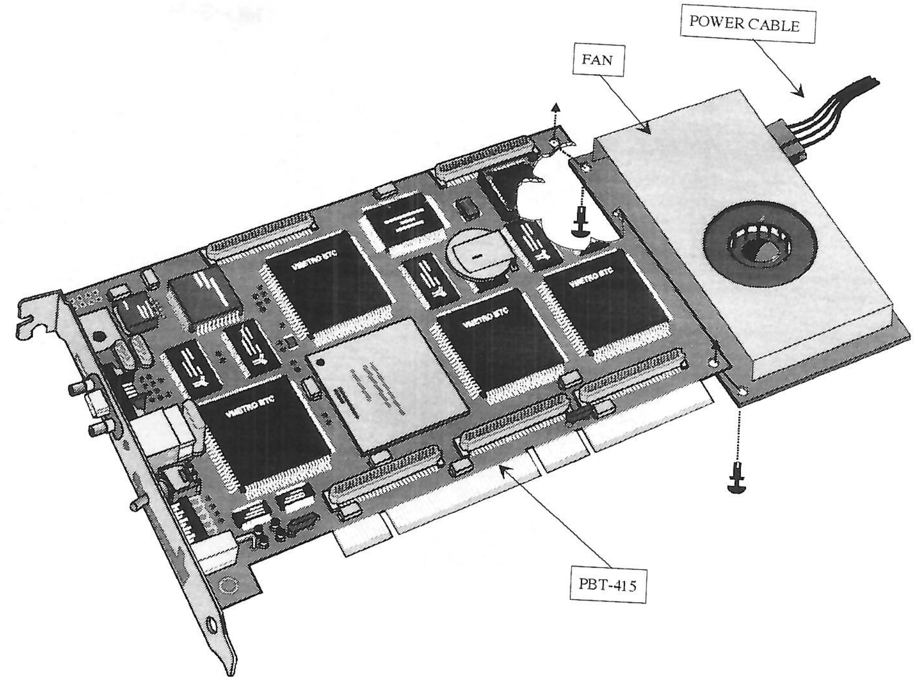


Figure 2.4 Mounting the cooling module on the PBT-415

2.2.5 Installation Procedure - PTIMBAT400-PB / PBAT66-PB

As can be seen in Figure 2.1, the PBT-415 have 5 piggyback connectors. All of the 5 connectors are used when mounting a piggyback, i.e. it should not be possible to mount it the wrong way!

Warning! Make sure that the table surface under the PBT-415 is smooth, and apply pressure with your hands gently around all the piggyback connectors while the board is lying flat on the table. Make sure that all the connectors are firmly seated (i.e. there shall be no gap between the white connector housings on the PBT-415 and the piggyback). See Figure 2.5.

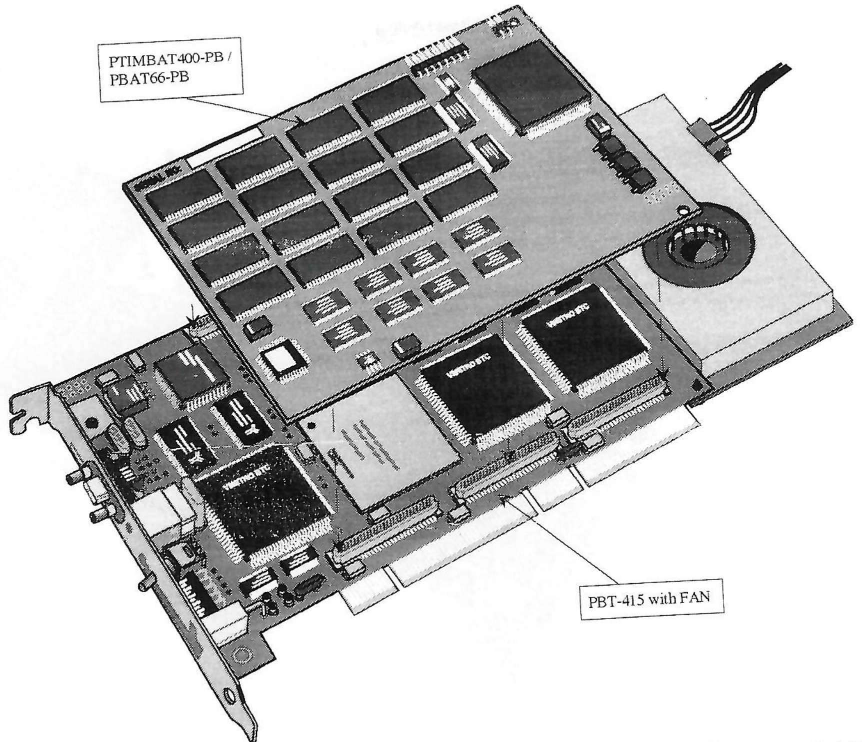


Figure 2.5 Mounting the PTIMBAT400-PB/PBAT66-PB on the PBT-415. Note that the fan is only necessary when mounting the PTIMBAT400-PB.

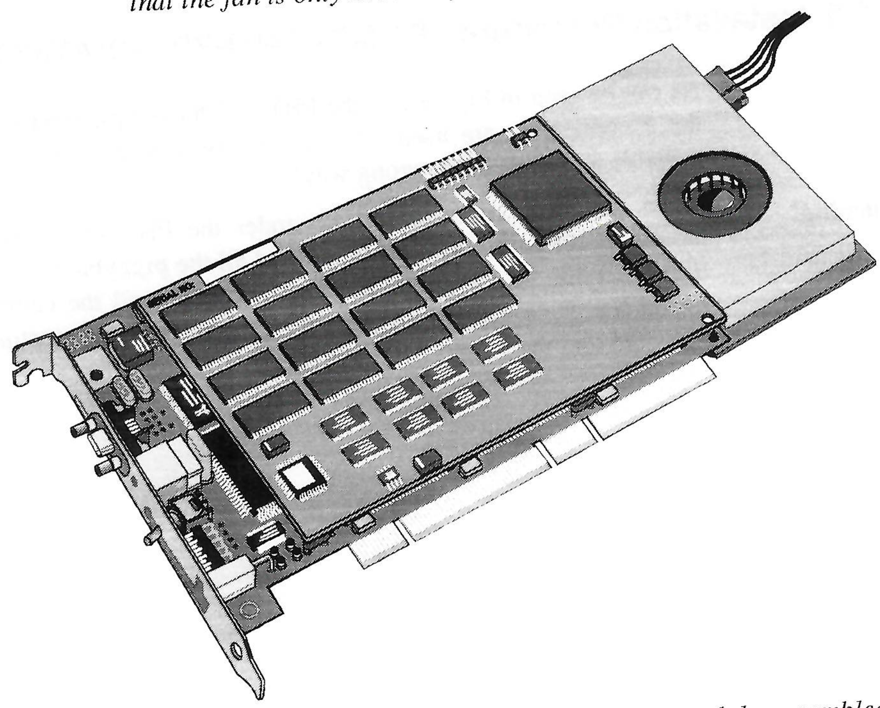


Figure 2.6 The PBT-415, the fan, and the piggyback module assembled and ready for use

2.3 Power Consumption

When capturing data using the Timing Analyzer, the PTIMBAT400-PB consumes approximately 3.6A (≈ 18W) when sampling. The PBT-415 consumes approximately 3.5A (≈ 18W) when sampling in CLOCK mode.

Table 2.2 summarizes the power consumption for the PTIMBAT400-PB and the PBT-415 at 5.0V:

Sampling Mode	PBAT66	PTIMBAT400	PBT-415	Total
Idle		2.7A	2.4A	5.1A
PTIMBAT 400MHz and PBT-415 in CLOCK mode (33MHz).		3.6A	3.5A	7.1A
Idle	0.5A		2.4A	2.9A
PBAT66 and PBT-415 in CLOCK mode (33MHz).	0.5A		3.5A	4.0A

Table 2.2 PBT-415 and PTIMBAT400-PB Power Consumption at 5.0V

Some PCs are equipped with power supplies without sufficient spare power to run with the PTIMBAT400-PB.

Due to the relatively high power consumption of the PTIMBAT400-PB, one External Power Cable (401-315-EPC) is included with each shipped PTIMBAT400-PB. This allows the user to power the PBT-415/PTIMBAT400-PB boards from an external power supply.

2.4 External Power Supply - PTIMBAT400-PB

Connect the External Power Cable (401-315-EPC) to a 5V power supply with at least 10A capacity.

Important! **The +5V and GND terminals on the cable must be connected to the corresponding terminals on the power supply.**

Before connecting the power cable to the PBT-415/PTIMBAT400-PB, adjust the power supply idle voltage to 5.20V. This will compensate for the voltage drop over the power cable when connecting to the PBT-415/PTIMBAT400-PB.

Move the two blue heavy duty power jumpers installed on the PBT-415 in position Z1 and Z2 (factory setting) to position Z3 and Z4. By moving the two jumpers the PBT-415/PTIMBAT400-PB can be powered from the external power supply.

Power jumper locations are shown in Figure 2.7. Please note that power jumpers Z1 and Z2 are located under the PTIMBAT400-PB.

Warning! Always move the Z1/Z2 jumpers as a pair, i.e. never leave one jumper in Z1 or Z2, and one jumper in Z3 or Z4, since this will give connection to both the back plane 5V and the external voltage source.

Warning! When working with external power, the PBT-415/PTIMBAT400-PB should be powered up before the rest of the PCI system, and powered down after the rest of the PCI system.

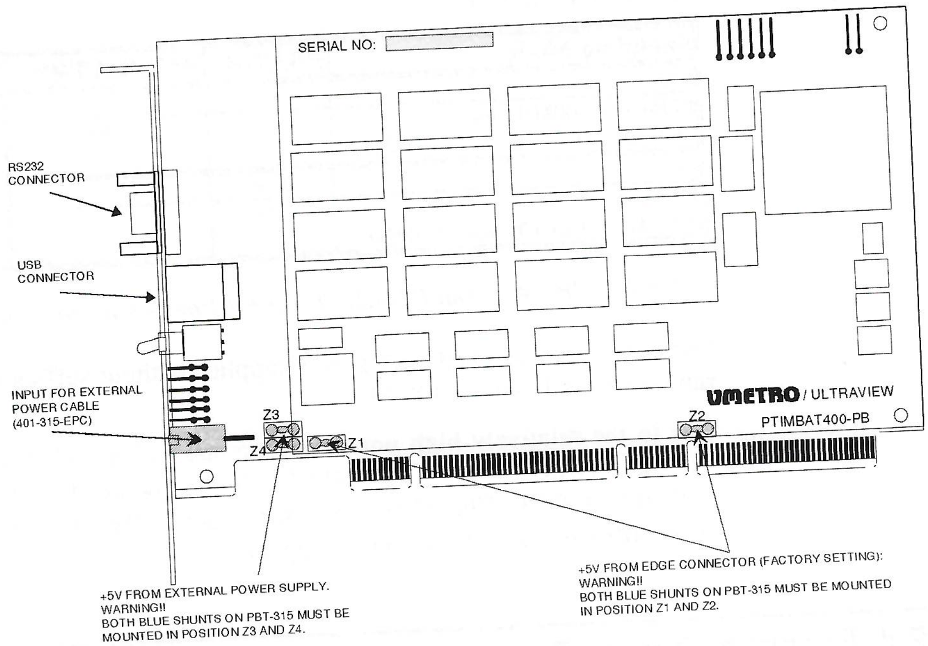


Figure 2.7 The PBT-415 with the PTIMBAT400-PB

3. FUNCTIONAL DESCRIPTION - ANOMALY TRIGGER

3.1 Main Blocks

The PBAT66 is a parallel trigger module which recognizes violations of the PCI bus specification in real time. If one of a specified set of violations is detected, a trigger signal is generated. This signal may be used to trigger the 400MHz Timing Analyzer part of a PTIMBAT400-PB and/or the PBT-415 PCI bus analyzer.

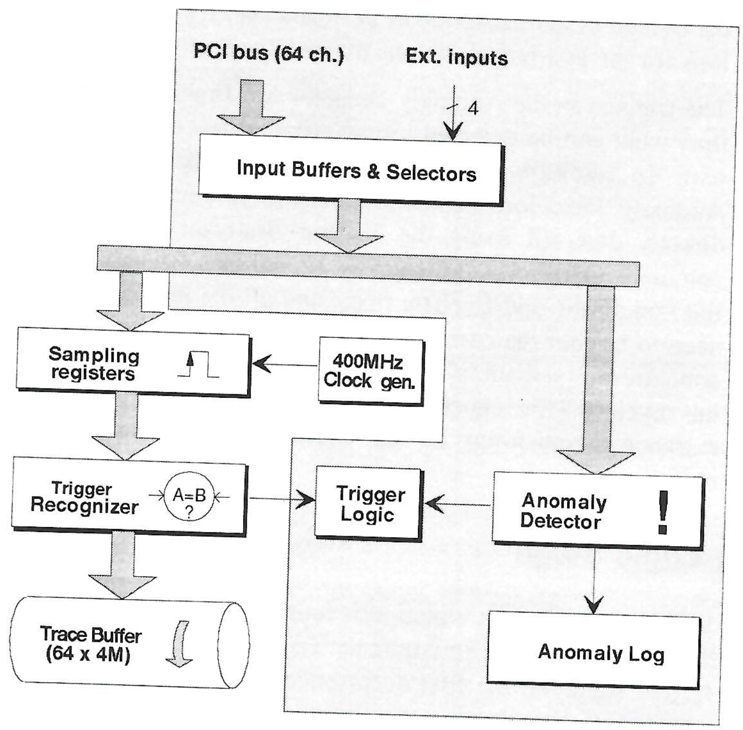


Figure 3.1 The PBAT66 part of the PTIMBAT400-PB is outlined in gray

As shown in the block diagram in Figure 3.1, the PBAT66 part consists of three main stages:

- Anomaly Detector stage
- Trigger Logic stage
- Anomaly Log stage

3.1.1 Anomaly Detector Stage

The Anomaly Detector stage looks for errors by watching every bus cycle during operation. It has a set of rule-based trigger elements that continuously and simultaneously screen the PCI bus lines to detect 38 classes of PCI bus timing and protocol violations, 68 violations in all.

The Anomaly Detector helps uncover design, manufacturing and field-failure-induced flaws in portions of the bus interface circuitry of both PCI masters and targets. It will also uncover a wide variety of hardware problems originating in other parts of a PCI board that indirectly causes illegal bus activity. It does this by watching the boards in use in the actual system configuration. This way it can help determine why a board from a particular manufacturer does not function properly in a system from another manufacturer, etc.

The Anomaly Detector may be programmed to ignore "innocent" PCI bus violations, i.e. violations that occur sporadically and generally do not restrict the overall system function or performance. Using this feature, it allows you to look for the PCI bus violations that really cause the problems.

The triggers in the Anomaly Detector can find faults of much shorter duration than what can be detected by the triggering circuitry of the Timing Analyzer part. In addition, the edge-sequence-rule-based triggering nature of the Anomaly Detector, makes it possible to recognize events that cannot be directly detected using the Timing Analyzer part alone. For example, the Anomaly Detector automatically recognizes "instability", (i.e. changes on a line) on all the address/data lines, and all the main control signals, without the need to be told the correct state of these lines beforehand. This is essential for concurrently screening for all address and data stability violations in all PCI bus cycles. This capability further enables the Anomaly Detector to find extraneous transitions on bus signals due to meta-stability, bus ringing and noise.

3.1.2 Trigger Logic Stage

Whenever a PCI bus violation is found, a fast trigger output is generated within 2 to 4 PCI clocks. The Anomaly Trigger may be programmed to generate this trigger signal on the first occurrence, or on every occurrence of the violation. The trigger signals give the engineer a direct lead to timing errors and other problems on the PCI bus.

If the piggyback is a PTIMBAT400-PB, the trigger signal can be used to trigger the 400MHz Timing Analyzer part. On both the PBAT66-PB and the PTIMBAT400-PB the trigger output signal can also be used to trigger the PBT-415, or be incorporated in event definitions. Either this trigger signal or the PBT-415 Trigger Output can trigger external test equipment, such as an oscilloscope, for immediate inspection of the problem.

The difficult part of debugging is to determine on which conditions to trigger. Often the symptoms of failure give no clue as to their cause. The 38 parallel triggers of the Anomaly Trigger continuously screen the bus for illegal activity, and can often establish an immediate trigger on extremely obscure bugs. The combination of the Anomaly Trigger with a Timing Analyzer is a very powerful troubleshooting aid, eliminating the trial and error approach often required to devise a suitable triggering strategy.

The possibility of triggering the PBT-415 PCI Bus Analyzer as result of a PCI bus violation significantly enhances the versatility of the PBT-415.

3.1.3 Anomaly Log Stage

The Anomaly Log stage keeps record of which PCI bus violations have occurred. Whenever a PCI bus violation is found, a corresponding flag is set in the Anomaly Log. The set of flags may later be examined to see which errors did occur. This way it is possible to survey a PCI bus system for bus violations, even without using the trigger signals to generate other actions in the analyzer.

3.2 Possibilities and Limitations

3.2.1 Classes of Errors Detected by the PBAT66

The PBAT66 screens the PCI bus traffic for the following 38 classes of PCI bus specification violations, and also detects Target abort, Master abort, and PCI bus RST# asserted.

Violation[0]: **C/BE#[3::0]** unstable .

Violation[1::4]: **AD[31::0]** unstable.

Violation[5]: **PAR#** unstable.

Violation[6]: Master Ctrl unstable - **FRAME#, IRDY#, LOCK#**.

Violation[7]: Target Ctrl unstable - **DEVSEL#, TRDY#, STOP#**.

Violation[8]: Misc. signals unstable - **PERR#, SDONE** or **SBO#**.

Violation[9]: Illegal **FRAME#** re-assertion.

Violation[10]: Illegal **FRAME#** or **IRDY#** change.

Violation[11]: **FRAME#** off before **IRDY#**.

Violation[12]: **FRAME#** off in DAC.

Violation[13]: Illegal **FRAME#** to **IRDY#**.

Violation[14]: Illegal **IRDY#** assertion.

Violation[15]: Illegal **LOCK#** assertion.

Violation[16]: First **LOCK#** not Read.

Violation[17]: Target protocol error.

Violation[18]: Illegal **TRDY#** assertion.

Violation[19]: Illegal target change.

Violation[20]: Illegal **DEVSEL#** off.

Violation[21]: Illegal **DEVSEL#** on/off.

Violation[22]: Abnormal **STOP#**.

Violation[23]: Illegal **STOP#** to **FRAME#** off.

Violation[24]: Illegal **A1**, **A0** & **BE[3..0]**.

Violation[25]: Illegal command response.

Violation[26]: Illegal **A1**, **A0** Memory commands.

Violation[27]: Illegal Linear Address Incrementing Mode.

Violation[28]: Illegal Configuration 0 cycle.

Violation[29]: **BE[3::0]#** change in Data.

Violation[30]: **PERR#** only on Data Transfer.

Violation[31]: Too many clocks in cycle.

Violation[32]: Missing Master-Abort.

Violation[33]: Illegal Master-Abort.

Violation[34]: Illegal Back-To-Back.

Violation[35]: Clock < 28.5ns.

Violation[36]: Data Phase Parity Error

Violation[37]: Address Phase Parity Error.
Master Abort.
Target Abort.
RST# asserted.

3.2.2 Debugging Features - Anomaly Trigger

The following are examples of problems the PBAT66 module can help uncover:

- Improper design of PCI bus interface circuitry.
- Bus noise, including cross-talk, ringing and ground-bounce, leading to setup time violations.
- Two masters "fighting on the bus".
- Two targets responding to the same address.
- Invalid signal sequences and combinations.

3.2.3 Verification of Detected violations

The PBAT66 cannot be used as a complete "Definitive Bus Compliance Validator", since it does not check for all possible bus specification violations. While the PBAT66, when properly used, is believed to be free of any deficiencies which could indicate false errors, an error indication by the PBAT66 should never, by itself, be used to implicate a vendor. All errors reported by the PBAT66 should be verified by actually inspecting the bus activity causing the error. Only on the basis of such subsequent confirmation of the existence of errors should any vendor be presumed to be at fault.

4. FUNCTIONAL DESCRIPTION - TIMING ANALYZER

4.1 Main Blocks

The Timing Analyzer has a 64 channel sampling stage, a 3 input trigger recognizer, and a trace buffer for PCI bus signals. Some of the 64 input lines, and the 4 reserved PCI lines, may be replaced by external input lines, as explained in Section 8.3.

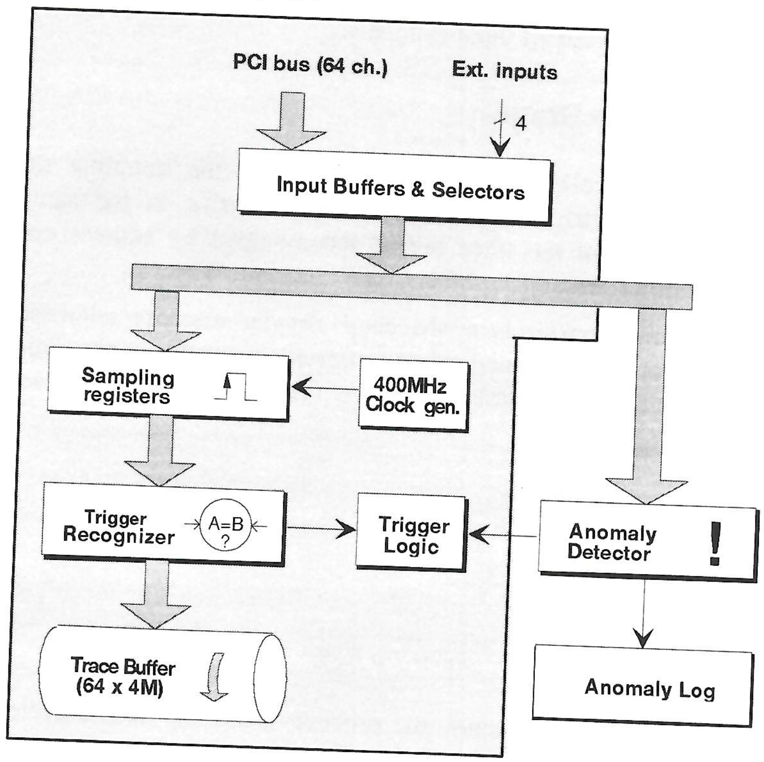


Figure 4.1 The 400MHz Timing Analyzer part of the PTIMBAT400-PB is outlined in gray

As shown in the block diagram in Figure 4.1, the Timing Analyzer part consists of three main stages, through which samples are passing through during the acquisition process:

- Sampling stage
- Trigger Recognition stage
- Sample Storage stage

4.1.1 Sampling Stage

2.5ns resolution

The sampling stage contains sampling registers and clock generation circuitry providing asynchronous sampling of the target bus at a fixed rate of 400 MHz. This gives 2.5ns resolution for high speed timing analysis of the signal behavior in the target system.

4.1.2 Trigger Recognition Stage

3 triggers

The timing analyzer offers 3 trigger possibilities, i.e. it can be cross-triggered from the PBAT66 or the PBT-415, or it can be triggered from the external input Ext[0].

Cross-triggering from the PBT-415 gives the Timing Analyzer full triggering possibilities for all input channels.

4.1.3 Sample Storage Stage

After the collected samples have passed the sampling stage and the word recognition/triggering stage, they will arrive in the sample storage stage, consisting of the trace buffer accompanied by address counters and trigger position counters.

Trace buffer

The trace buffer is a 4M deep circular memory addressed by an address counter which is incremented after each stored sample. This buffer is written to continuously until a trigger is found, overwriting previous samples when full.

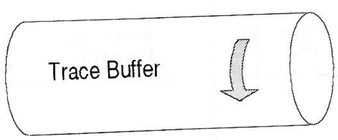


Figure 4.2 The circular trace buffer

Trigger position

When a trigger occurs, the process of storing further cycles depends on the selected *trigger position*. If the trigger position is set to "End of Trace", 512K of additional samples will be stored before the sampling stops, for a trigger position of 87.5%. This is an intentional approximation to "End", to ensure that the trace always contains some samples after the trigger point. Opposite, if the trigger position is set to "Start of Trace"", 3.5M of the 4M trace buffer will be filled with new cycles before the acquisition process stops, leaving up to 512K ahead of the trigger point, for an actual trigger position of 12.5%. In between, there are possibilities to select trigger positions as 25, 50 and 75%.

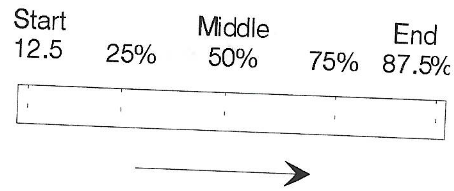


Figure 4.3 Five trigger positions in the trace buffer can be selected

Note that the trigger may occur before the trace buffer has been filled completely ahead of its specified trigger position. In such cases the trace buffer will be only partly filled before the trigger. (Imagine if the second sample collected was the trigger, and the trigger position was 50%, then 2M-1 cells in the first part of the trace buffer will be empty.)

See Section 8.3.7 for more information about setting the trigger position.

5. USER INTERFACE STRUCTURE

5.1 Functional Units

With a PBAT66-PB or a PTIMBAT400-PB mounted on a PBT-415, the product may, in its maximum configuration, consist of up to two analyzers and one anomaly trigger as shown in Table 5.1:

	PBT-415	PBT-415+ PBAT66-PB	PBT-415+ PTIMBAT400-PB
PCI Bus Analyzer	x	x	x
400MHz Timing Analyzer			x
Anomaly Trigger		x	x

Table 5.1 The analyzer possibilities using the PBT-415 and its piggyback modules

5.2 Window Categories

The user interface for the 400 MHz Timing Analyzer part is based on two different windows, the Setup window and the Trace Display window. The user interface for the Anomaly Trigger (PBAT66) part is based on a third window, the PCI bus Violation window. The windows appear as MDI (Multiple Device Interface) windows in BusView, which are activated by clicking on them.

5.2.1 Setup Window

The Setup window is the "control panel" of the 400 MHz Timing Analyzer. In addition to the menu bar, this window contains two major elements, the **Event Pattern** window and the **Trigger Condition** window, used to define and display trigger conditions. These windows are described in detail in Sections 7.2 and 7.3.

5.2.2 Trace Display Window

The Trace Display window is where the contents of the trace buffer are displayed. The trace data may be displayed as an alphanumeric trace list or as waveforms. Multiple trace windows of either type may be created. The command bar in the Trace Display window is tailored to perform efficient navigation, searching and formatting of the trace data contents.

5.2.3 PCI bus Violation Window

The PCI bus Violation window is used to control the Anomaly Trigger (PBAT66) part. In this window the user can set up the operation of the Anomaly Trigger, as well as see what errors have been detected during a run. The Violation window is described in detail in Section 6.3.

5.2.4 Switching Between Windows

Switching between the different windows can be done in many ways:

- By clicking with the mouse in the desired window.
- By clicking with the mouse in the desired window field on the status line at the bottom of the BusView window, i.e. clicking in the field saying T400_PCI, makes the T400_PCI setup window appear in front.
- By using the **Ctrl-Tab** keys at the keyboard.
- By selecting Window/Select `Window` from the menu bar (or tool bar).

5.3 Cross-triggering

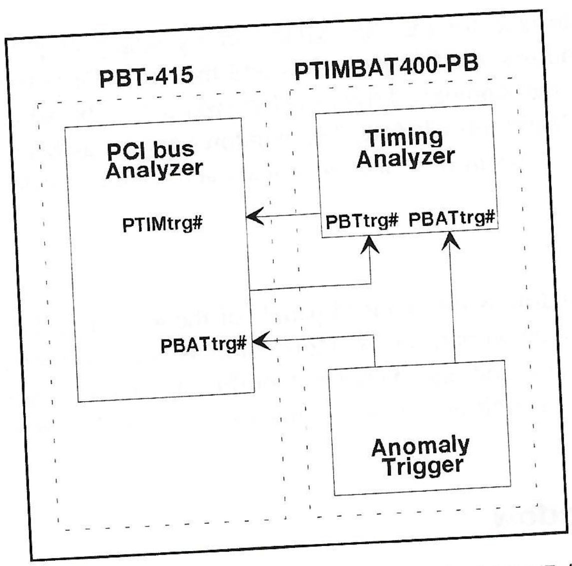


Figure 5.1 Cross triggering using the PTIMBAT400-PB

Piggyback Module	Cross-triggering Signals
PBAT-PB	PBATtrg#
PTIMBAT400-PB	PTIMtrg#, PBTtrg#, PBATtrg#

Table 5.2 The cross triggering signals for the piggyback modules

If the piggyback in use is a PBAT66-PB the only possible cross-triggering is using the Anomaly Trigger output signal PBATtrg# to trigger the analyzer on the PBT-415, see Table 5.2, and Figure 5.1.

In the case of a PTIMBAT400-PB, there are four different signals, making numerous cross-triggering possibilities of the different target modules, see Figure 5.1.

5.3.1 Triggering the PTIMBAT400-PB from the PBT-415

As an example of cross-triggering, let us assume that we want to use the trigger output signal from the PBT-415 PCI bus Analyzer to trigger the Timing Analyzer module on a PTIMBAT400-PB. In order to do this, select T400_PCI as target by clicking in the T400_PCI setup window.

To cause the PBTtrg# signal to trigger the PTIMBAT400-PB Timing Analyzer, double-click on the PBTtrg# signal field in one of the event patterns (T400_PCI0-3) in the Event Patterns window, and select "TRIG" in the dialog box that appears, as shown in Figure 5.2 .

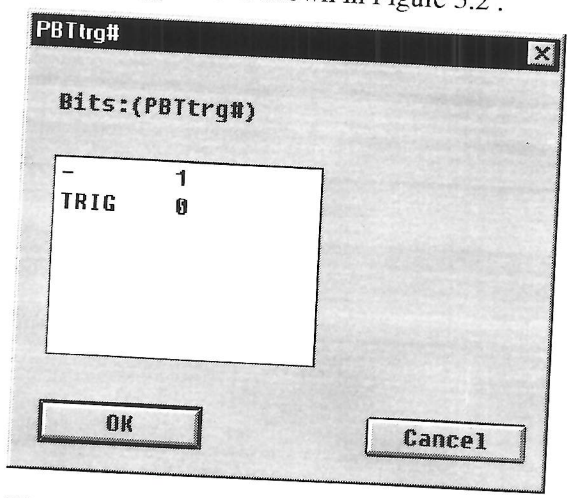


Figure 5.2 Cross-triggering from the PBT-415

Note! When using cross-triggering between two analyzers, both analyzers should be started simultaneously by using the command `Run Multiple` in the `Trace` menu. See Section 8.4.2.

5.3.2 Triggering Analyzers from PBAT66

A common use of cross-triggering is to use the Anomaly Trigger module on a PBAT66-PB, or PTIMBAT400-PB to trigger the PCI bus analyzer on the PBT-415, or, in the case of a PTIMBAT400-PB, the PTIMBAT400-PB Timing Analyzer and/or the PCI Bus Analyzer on the PBT-415. Let us assume that we want to use the PBAT66-PB to trigger the PCI bus Analyzer on the PBT-415. Similar to the example above we would then include the PBAT66-PB output trigger signal PBATtrg# in the event definition on the PCI bus Analyzer.

6. OPERATION - ANOMALY TRIGGER

6.1 Introduction

When a PBAT66-PB or PTIMBAT400-PB is properly installed and detected by the PBT-415 the menu bar of the Setup window will include both the `Pbat` menu item, and the `Pbat` tool bar button, as shown in Figure 6.1.

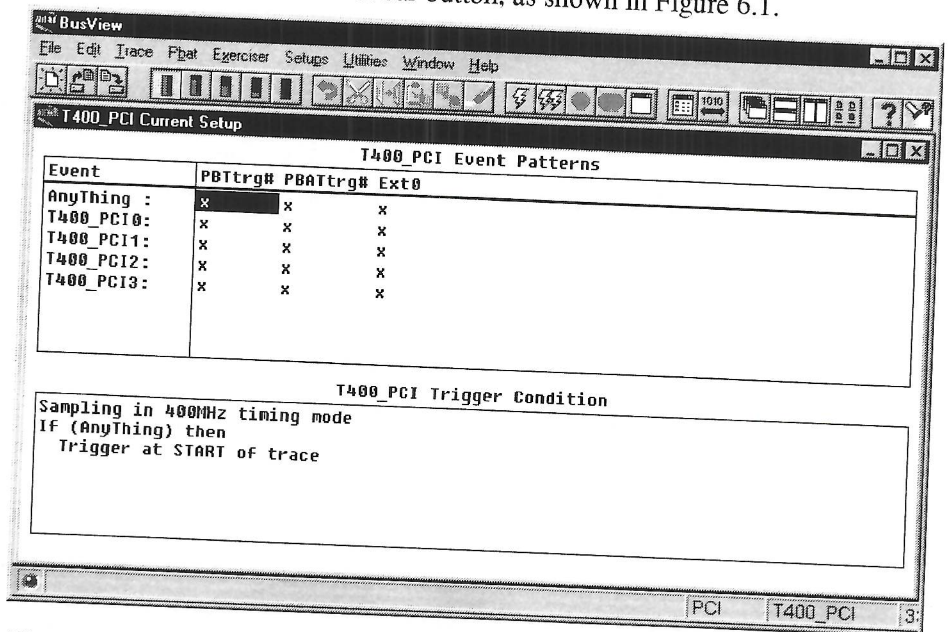


Figure 6.1 The Setup window with the Pbat menu item at the menu bar

6.2 Anomaly Trigger Output Signal

The PTIMBAT400-PB Anomaly Trigger generates the trigger signal PBATtrg#, that is automatically fed to the dedicated input channels of the PTIMBAT400-PB Timing Analyzer, and to the PBT-415. The trigger signal can be a part of the trigger on one or both of these analyzers, and it is also visible in the trace.

When the PBAT66-PB is used together with either of the analyzers (e.g. to identify which cycles caused a PCI bus violation), the Anomaly Trigger output signal should be inserted into the Event Patterns window. This is done by clicking on the signal you want the trigger output to be in front of, and then pressing INS to insert signals. Select the signal name PBATtrg#. See Section 8.3.6.

On both the PTIMBAT400-PB and the PBT-415 PCI Bus Analyzer the Anomaly Trigger signal is called PBATtrg#, and can have the values "x" (don't care), "-" (no violation), or "TRIG" (PCI bus violation).

6.3 PCI bus Violation Window

The operation of the PBAT66-PB is controlled from a dedicated command window. This window is activated by selecting the `Pbat` menu item (from the setup window), or by pressing the correct tool bar button, see Section 8.5. The PCI bus Violation window should appear, as shown in Figure 6.2.

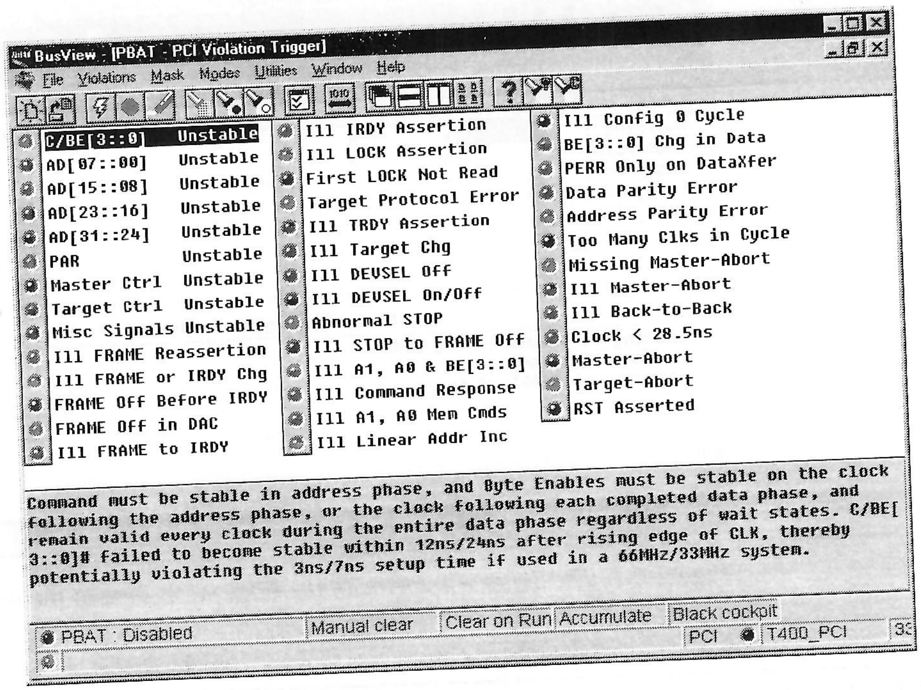


Figure 6.2 The PCI Bus Violation window

6.3.1 Selecting Specific Violations

The PCI bus Violation window allows the user to select any set of violations to investigate. Only those violations that have been selected will cause the PBAT66 to activate the trigger output signal.

Select

All the violations are selected by choosing `Mask/Select All`. None of the violations are selected by choosing `Mask/Select None`. Alternatively, press the corresponding button at the tool bar.

Explanations to violations

One violation at a time can be toggled on and off by double clicking at the violation check boxes. At the same time an explanation of the violation is displayed at the bottom of the PBAT66 window. See Figure 6.2.

Whenever the PBAT66 has detected a violation, a message will be posted in the lower left corner of the window, and the actual violation will be highlighted.

6.3.2 Enabling and Disabling the Anomaly Trigger

The user can enable and disable the function of the Anomaly Trigger by means of the commands `Enable` and `Disable` in the `Violations` menu.

When using the PBAT66 to trigger an analyzer, it is important to start the analyzers before giving the `Enable` command. Otherwise a violation may already have been detected, and a trigger signal be present when the PBAT66-PB is enabled. This will cause the analyzer to store trace data from the moment the PBAT66 is enabled, i.e. the violation that caused the trigger will not be visible in the trace. Alternatively the PBAT66 can be cleared on trace run by selecting the `Clear on trace run` check box in the PBAT `Modes` command dialog box. See Section 6.3.3 below.

6.3.3 PBAT66 Options

Clear Modes

The PBAT66-PB can operate in either Automatic Clear mode or Manual Clear mode. These modes are selected by selecting the `Automatic Clear` or `Manual Clear` options in the `Modes` command dialog box shown in Figure 6.3.

In Automatic Clear mode, the PBAT66 output trigger signal will automatically reset one PCI clock after a violation was detected. It is intended for triggering an oscilloscope, etc. No violations will be displayed. In Manual Clear mode, the trigger signal will remain active until reset by the operator.

The operator can manually reset the PBAT66 output trigger signal by using the `Clear` command in the `Violations` menu.

Lock Modes

The `Modes` command dialog box contains two Lock Mode options called `Lock On First` and `Accumulate`. In Lock On First mode, the PBAT66 will trigger only on the first violation, and ignore all later ones. In Accumulate mode, the PBAT66 will accumulate violations as they occur on the bus.

Black Cockpit

The `Black Cockpit` option presents the Violation window as a screen, only showing the violations that have actually occurred on the bus.

The `Show Explain Text` option enables/disables the text field below the violation window where the violations are explained.

The `Simulate LEDs` option makes the signal "lamps" on the status line look "three dimensional".

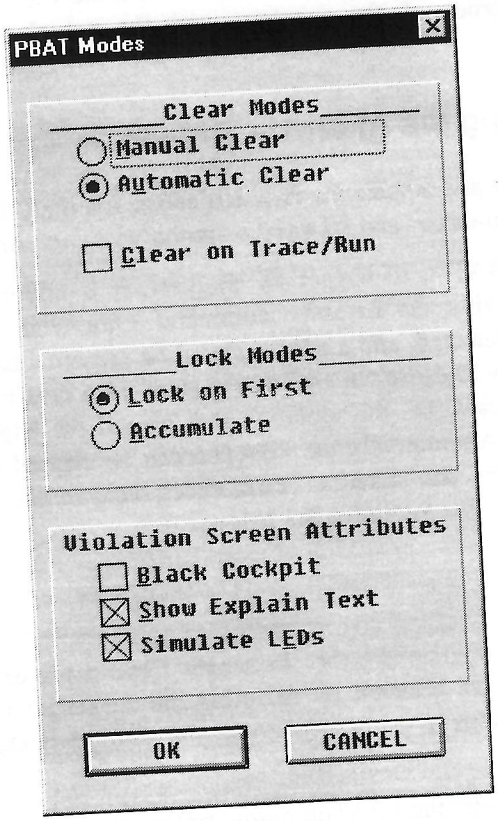


Figure 6.3 The PBAT Modes dialog box

6.4 Investigating Violations

As mentioned earlier, all PCI bus violations reported by the Anomaly Trigger should be verified by actually inspecting the bus activity causing the error before any of the vendors are presumed to be at fault.

6.4.1 Using the PTIMBAT400-PB

In the case of the PTIMBAT400-PB, the most convenient tool for investigation of the violations would be the onboard 400 MHz Timing Analyzer. The 400 MHz speed of this module, as well as its ability to be triggered directly from the Anomaly Trigger, makes it a convenient tool for investigating the signals relevant to the violation detected.

6.4.2 Using an Oscilloscope

As explained later in this section, even the 2.5 ns resolution of the 400MHz Timing Analyzer may not be enough under certain circumstances. In such cases, a faster timing analyzer (800-1000 MHz) may be used, but the best is to use a high-speed digital oscilloscope with storage capabilities and at least 600 MHz bandwidth.

An oscilloscope without storage capability can also be used if the violation repeats itself frequently enough to create a visible image on a standard oscilloscope screen. (Programming a special test loop may be a good idea). In such a case, the automatic clear mode in combination with the proper mask setting should be used to create a pulse each time the violation to be investigated is detected.

6.5 Trigger External Instruments on Violations

Trigger

An oscilloscope or external logic analyzer can be triggered by the Anomaly Trigger in different ways. One way is to use the Anomaly Trigger output signal available on the pin header on the PBAT66-PB or the PTIMBAT400-PB, see Section 8.3. A more convenient way is to use the front panel trigger output as follows:

Normally the front panel "Trig" output on the PBT-415 is the trigger output from the PCI bus analyzer of that board. The Anomaly Trigger output signal from a PBAT66-PB or PTIMBAT400-PB may, however, be automatically fed to the PBT-415 front panel by using the trigger output command in the `Utilities` menu, see Section 8.7.4.

2-4 PCI clocks delay

Note that the Anomaly Trigger output signal will not be asserted until 2-4 PCI clocks after the actual violation is detected on the bus.

6.6 Invisible Violations

During use of the Anomaly Trigger it may happen that a violation is detected, although an investigation of the PCI bus traffic shows nothing wrong with the bus signals. This can be quite frustrating, since the Anomaly Trigger obviously believes something is wrong, whereas when the signals are displayed by means of the Timing Analyzer, (or on an external oscilloscope or logic analyzer), everything looks normal. However, usually there is a subtle but real problem which warrants further investigation. The following are the main reasons for getting a PCI bus violation trigger, but being unable to see the violation.

6.6.1 Viewing the Wrong Bus Cycle

You may not be viewing the actual PCI bus cycle that generated the trigger. To prevent this possibility, always display the Anomaly Trigger output signal along with the relevant bus signals. In this way the erroneous bus signals will be easier to spot, as they will be very closely aligned in time with the high-tolow transition of the trigger. Generally the violation will be seen from 2 to 4 PCI clocks before the assertion of the Anomaly Trigger output signal.

6.6.2 Insufficient Bandwidth

The PTIMBAT400-PB Timing Analyzer part, with its 2.5 ns resolution, will normally be sufficient to catch the signal transitions that were causing the violation. Under certain circumstances, however, even the 400 MHz Timing Analyzer may not have sufficient bandwidth to see certain very brief violations which are detected by the Anomaly Trigger.

To investigate PCI bus violations not visible by means of the PTIMBAT400-PB Timing Analyzer, it is recommended to use a high speed oscilloscope. A fast logic analyzer may, however, also be used. In some cases an analyzer with a sampling speed of 800 to 1000 MHz may be required to consistently observe the error. Attention should also be paid to the analog bandwidth of the input buffers in the logic analyzer pods, as this bandwidth may not match the sampling rate of the logic analyzer itself. In this case a brief glitch may come and go before the slow rise time of the pod gives the buffered signal a chance to cross the logic threshold of the analyzer.

If the violation is still not visible, you should try to change the threshold of the logic analyzer. Certain glitches in PCI bus systems have amplitudes of no more than 2 volts. If the logic analyzer is tried with threshold at both 1.2 volts and 2.0 volts, the problem will normally be seen.

7. OPERATION - TIMING ANALYZER

7.1 Setup Window

The operation of the 400 MHz Timing Analyzer is controlled from the Setup window as shown in below Figure 7.1. The Setup window consists of four main elements:

- The menu bar
- The toolbar
- The "Event Patterns" window
- The "Trigger Condition" window

In addition, there is a status line at the bottom of the window that displays error messages, tool bar help messages, as well as sampling status.

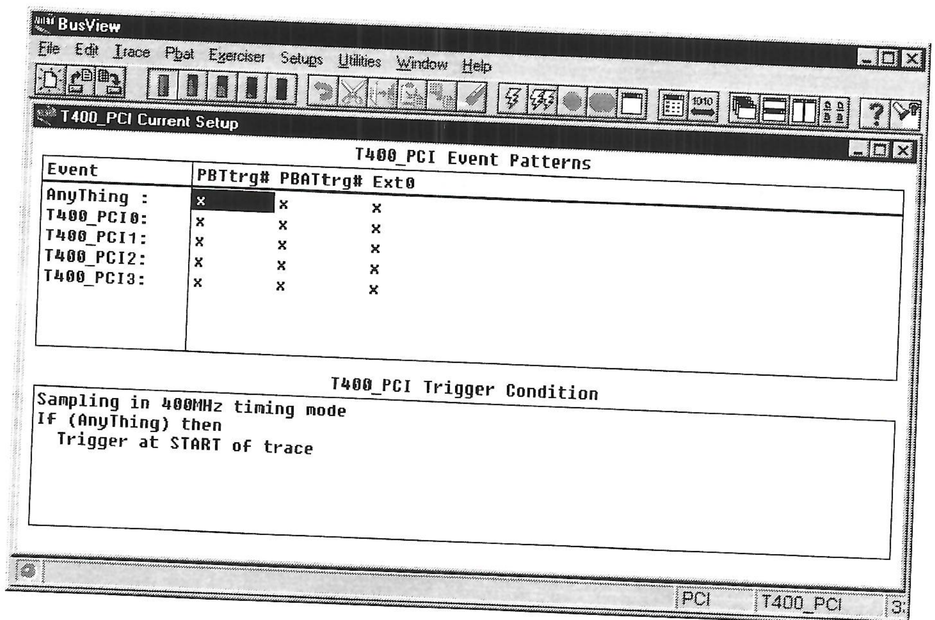


Figure 7.1 The Setup window

7.2 Event Patterns Window

The Event Patterns window defines the patterns to be loaded into the trigger recognizers of the Timing Analyzer. Only one of the event patterns can be used as trigger pattern.

T400_PCI0 to T400_PCI3
AnyThing

A list of four user alterable patterns is provided, labeled T400_PCI0 to T400_PCI3. In addition, there is an unalterable pattern called Anything, which is always set to "Don't Care" (X). In Figure 7.2, one of the user alterable patterns is renamed to "MyEvent", and one is deleted.

In the default setup, the three possible trigger signals are listed, as shown in Figure 7.2. Scroll bars enable vertical and horizontal scrolling.

T400_PCI Event Patterns

Event	PBATtrg#	PBTtrg#	Ext0
AnyThing :	x	x	x
T400_PCI0:	x	x	x
T400_PCI1:	x	x	x
MyEvent :»	TRIG	x	x

Figure 7.2 The Event Patterns window

7.3 Trigger Condition Window

The Trigger Condition window is a status-only window. The window presents the current selection of trigger position, and the name of the event currently chosen as the trigger pattern.

T400_PCI Trigger Condition

```
Sampling in 400MHz timing mode
If (AnyThing) then
  Trigger at START of trace
```

Figure 7.3 The Trigger Condition window

7.4 Trace Display Window

The Trace Display window is where the contents of the trace buffer are displayed. The trace data may be displayed as an alphanumeric trace list or as waveforms. Multiple trace windows of either type may be created. The command bar in the Trace Display window is tailored to perform efficient navigation, searching and formatting of the trace data contents.

The Trace Display window is automatically presented when the trace buffer is full during sampling. (Except when more than one analyzer (target) is started at the same time with the command `Run/Multiple`. In this case, a sampling status box will be shown.)

To enter a trace window type F2, use the menu command `Trace/Show` or the appropriate tool bar button (all from the setup window). See Section 8.4.5.

7.4.1 Waveforms

Waveforms are provided to show the logic level of individual signals graphically as a function of time. This is particularly useful to show timing relations between different signals for hardware analysis. Busses may be presented as "ladders", with the value of the bus at the cursor position shown in hex value within the window. The ladder will contain a "step" when the bus changes value. The individual signals in a bus can also be selected. The waveform window is shown in Figure 7.4.

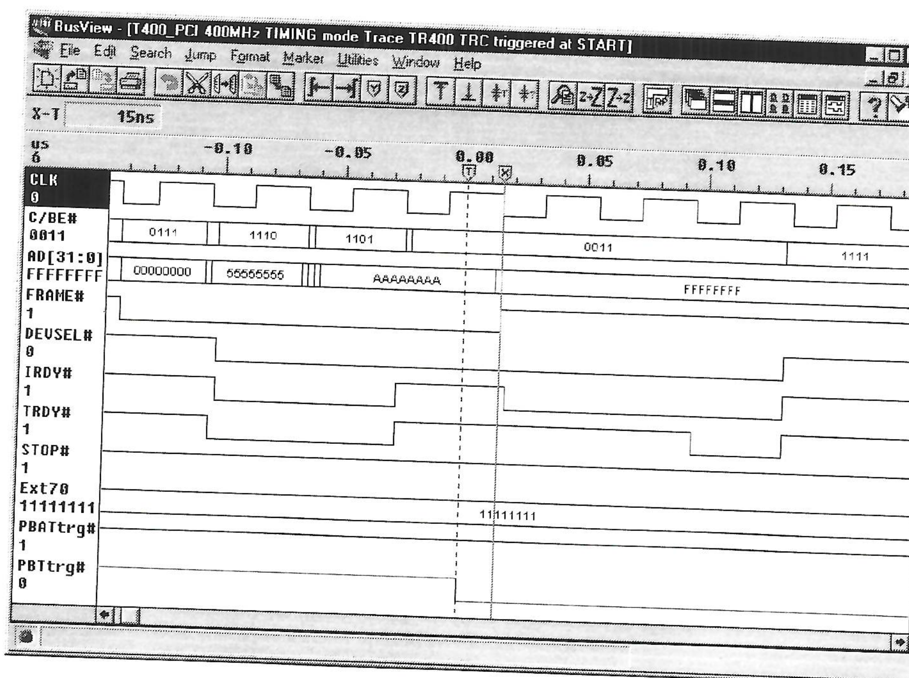


Figure 7.4 The waveform window for displaying trace data

7.4.1.1 Hex/Binary Value

The signal value at the cursor position is always shown directly under each visible signal/field name in the left column in the waveforms display. This allows for convenient recognition and location of cycles in the trace buffer.

7.4.1.2 Signal Selection

The analyzer will show a default selection of signals and signal groups in the waveform that is most relevant for the selected target bus. However, since most buses will contain more signals/groups than there is space for in the window, the user can see other signals by vertical scrolling. Similarly, the user can also insert signals/groups, as well as reorder the signals/groups by using the INS/DEL keys.

DEL Typing DEL when the cursor is placed in a signal allows you to delete the signal field column from the waveform window, see Section 8.3.2.

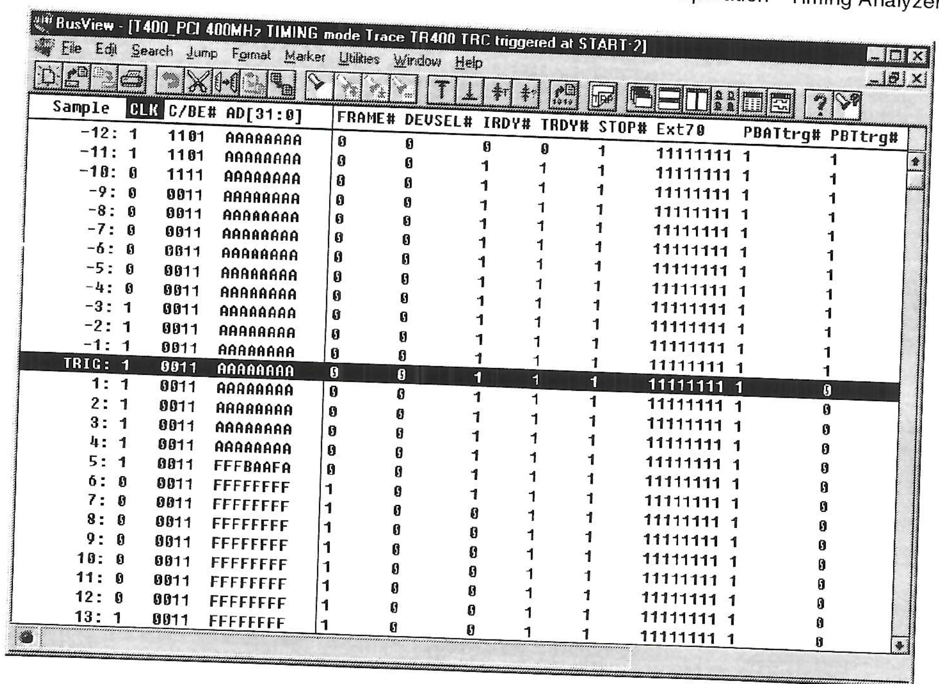
INS Typing INS when the cursor is placed in a signal field will cause the INSERT dialog box to appear. It allows you to insert a new signal group as a field column in the waveform window, see Section 8.3.6.

7.4.2 Zooming

The default scale setting is one sample per 5th pixel. This can be changed by using the command `Format/Scale` to allow a more or less detailed view of the signals in waveform mode. See Section 8.10.3.1.

7.4.3 Trace List

The trace list shows the samples collected in the trace buffer as a list of alphanumeric values, presented as mnemonics or binary/hex values for each signal group. See Figure 7.5.



Sample	CLK	C/BE#	AD[31:0]	FRAME#	DEVSEL#	IRDY#	TRDY#	STOP#	Ext70	PBATtrg#	PBTtrg#
-12:	1	1101	AAAAAAAA	0	0	0	0	1	11111111	1	1
-11:	1	1101	AAAAAAAA	0	0	1	1	1	11111111	1	1
-10:	0	1111	AAAAAAAA	0	0	1	1	1	11111111	1	1
-9:	0	0011	AAAAAAAA	0	0	1	1	1	11111111	1	1
-8:	0	0011	AAAAAAAA	0	0	1	1	1	11111111	1	1
-7:	0	0011	AAAAAAAA	0	0	1	1	1	11111111	1	1
-6:	0	0011	AAAAAAAA	0	0	1	1	1	11111111	1	1
-5:	0	0011	AAAAAAAA	0	0	1	1	1	11111111	1	1
-4:	0	0011	AAAAAAAA	0	0	1	1	1	11111111	1	1
-3:	1	0011	AAAAAAAA	0	0	1	1	1	11111111	1	1
-2:	1	0011	AAAAAAAA	0	0	1	1	1	11111111	1	1
-1:	1	0011	AAAAAAAA	0	0	1	1	1	11111111	1	1
TRIG:	1	0011	AAAAAAAA	0	0	1	1	1	11111111	1	0
1:	1	0011	AAAAAAAA	0	0	1	1	1	11111111	1	0
2:	1	0011	AAAAAAAA	0	0	1	1	1	11111111	1	0
3:	1	0011	AAAAAAAA	0	0	1	1	1	11111111	1	0
4:	1	0011	AAAAAAAA	0	0	1	1	1	11111111	1	0
5:	1	0011	FFFBAAFA	0	0	1	1	1	11111111	1	0
6:	0	0011	FFFFFFFF	1	0	1	1	1	11111111	1	0
7:	0	0011	FFFFFFFF	1	0	0	1	1	11111111	1	0
8:	0	0011	FFFFFFFF	1	0	0	1	1	11111111	1	0
9:	0	0011	FFFFFFFF	1	0	0	1	1	11111111	1	0
10:	0	0011	FFFFFFFF	1	0	0	1	1	11111111	1	0
11:	0	0011	FFFFFFFF	1	0	0	1	1	11111111	1	0
12:	0	0011	FFFFFFFF	1	0	0	1	1	11111111	1	0
13:	1	0011	FFFFFFFF	1	0	0	1	1	11111111	1	0

Figure 7.5 The trace data displayed in an alphanumeric trace list

7.4.3.1 Signal Selection, Alphanumeric Trace List

Any signal can be selected in the alphanumeric display by using the DEL and INS keys in the same way as described for the Waveform presentation in Section 7.4.1.2.

7.4.4 Add Window

A powerful feature of BusView is the ability to add extra trace windows, either as alphanumeric trace lists, or as waveform displays. The windows may be considered completely independent from each other in the sense that different parts of a trace may be shown in each window. Scrolling in one window takes place without affecting the others. Use the menu commands `Window/Alphanumeric List` and `Window/Waveform` to open new windows. See Section 8.8.5. and Section 8.8.6.

8. COMMANDS REFERENCE

8.1 Introduction

Commands are executed from the menu bar, the tool bar, the status line at the bottom of the window, or with accelerator keys.

8.2 File Menu

The `File` menu takes care of loading, saving, and printing of setups and traces.

8.2.1 New Setup


The "New Setup" tool bar button

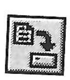
The `New Setup` command displays a list of possible new setups. Only the PCI and T400_PCI setups can be run with the PBT-415, but the user is free to create setups for VME, SCSI, VSB etc. as well. These setups can only run on the VBT-325 VME Bus Analyzer (with its piggybacks) also available from VMETRO.

8.2.2 Open


The "Open" tool bar button

The `Open` command enables a standard Windows "file open" dialog box, where the user may select the desired file.

8.2.3 Save, Save as


The "Save" tool bar button

The `Save` or `Save as` command saves the current setup or trace depending on which window is active. A dialog box where the user can type a file name and location appears. If a trace is being saved, there will also be a question of how many lines of the trace are going to be saved.

Binary/ASCII

Trace files can be saved both as binary files (with extension ".trc") and as ASCII files (with extension ".tra"). ASCII files can then be opened and edited in any other text editor.

8.2.4 Print

The "Print" tool bar button

The `Print` command is only available in the Trace Display window, and displays the dialog box in Figure 8.1. Type in the name of the trace file and how many lines to print.

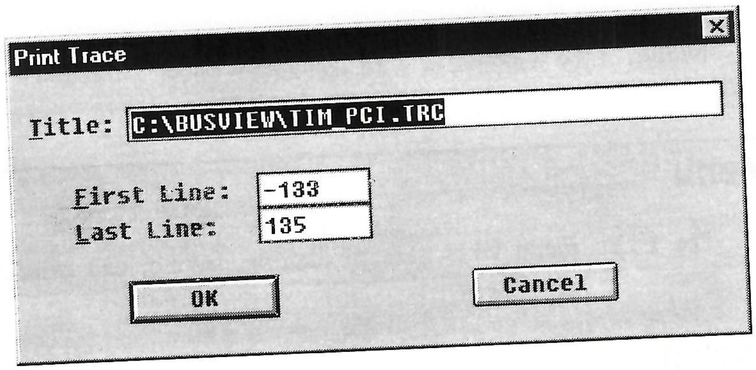


Figure 8.1 The Print Trace dialog box

8.2.5 Printer Setup

The `Printer Setup` command displays the dialog box in Figure 8.2. If the desired printer is not on the list, a new printer can be defined by pressing the "setup" button.

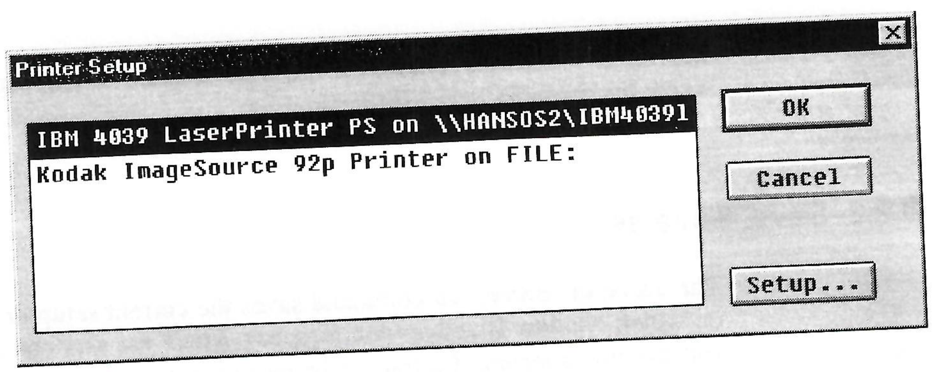


Figure 8.2 The Printer Setup dialog box

8.2.6 Save Settings on Exit

The `Save Settings on Exit` command makes BusView come up with the same windows and with the same settings as when you closed BusView last time.

8.2.7 Exit

The `Exit` command exits BusView.

8.3 Edit Menu

The `Edit` menu takes care of all kind of editing, both in the Event Patterns window, the Trigger Condition window, and the Trace Display window. The undo, cut, copy, paste, etc. functions are used in the same way as in any other Windows application the user may have used before.

8.3.1 Undo


The "Undo" tool bar button

The `Undo` command undoes the last executed `Edit`-command.

8.3.2 Cut


The "Cut" tool bar button

The `Cut` command allows the user to remove event patterns, signal fields, etc. Select the item to be deleted with the mouse, and choose `Edit/Cut`, press the `Cut` button at the tool bar, press the `DEL` key on the keyboard, or press the `Ctrl-x` keys.

8.3.3 Copy


The "Copy" tool bar button

The `Copy` command allows the user to copy event patterns, signal fields, etc. Select the item to be copied with the mouse, and choose `Edit/Copy`, press the `Copy` button at the tool bar, or press the `Ctrl-c` keys.

8.3.4 Paste


The "Paste" tool bar button

The `Paste` command allows the user paste event patterns, signal fields, etc., or whatever previously has been copied into the clipboard, into the appropriate window.

Event patterns

When pasting event patterns, place the cursor below the event pattern where the new pattern should be inserted, and select `Edit/Paste`, press the `Paste` button at the tool bar, press the `INS` key at the keyboard, or press the `Ctrl-v` keys.

Signal fields

When pasting signal fields, place the cursor on the signal field to the right of where the new one should be inserted, and select `Edit/Paste`, press the Paste button at the tool bar, press the INS key at the keyboard, or press the `Ctrl-v` keys.

8.3.5 Clear

The "Clear" tool bar button

The `Clear` command allows the user to clear event patterns, i.e. reset them to all "don't care" values. Select the event pattern to be cleared and select `Edit/Clear`, or press the `Clear` button at the tool bar. The `Cut` command can be used for clearing one signal field at a time in an event pattern.

8.3.6 Insert

The "Insert" tool bar button

The `Insert` command is used to insert new event patterns and signal fields into the Event Patterns window, and signal fields into the Trace Display window.

Event patterns

When inserting event patterns, place the cursor below the event pattern where the new pattern should be inserted, and select `Edit/Insert`, press the `Insert` button at the tool bar, or press the `INS` key at the keyboard. The dialog box in Figure 8.3 appears, where the user may type a name of the new event.

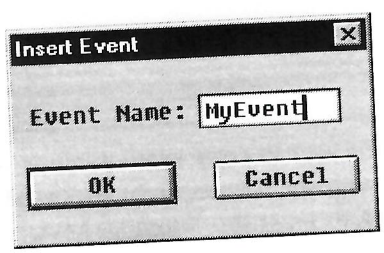


Figure 8.3 The Insert Event dialog box

Signal fields

When inserting signal fields, place the cursor on the signal field to the right of where the new one should be inserted, and select `Edit/Insert`, press the `Insert` button at the tool bar, or press the `INS` key at the keyboard. Figure 8.4 appears. Select the desired signal and press OK, or double click on it.

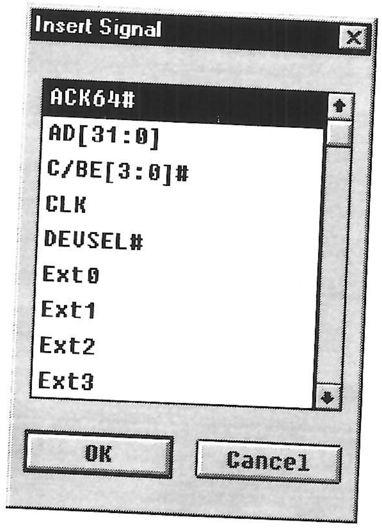


Figure 8.4 The Insert Signal dialog box

8.3.7 Trigger Position

The `Trigger Position` can be at five different places in the trace buffer:

- At Start of Trace (12.5%)

- At 25% of Trace

- At 50% of Trace

- At 75% of Trace

- At End of Trace (87.5%)

8.3.8 Sampling Options

Both the PBT-415 and the PTIMBAT400-PB are equipped with 4 external inputs. (Please refer to the PBT-415 User's Manual for a description of the external inputs on the PBT-415.) The external inputs on the PTIMBAT400-PB are located as shown in Figure 8.5. In addition to the 4 external inputs, there is also 3 GND pins, and the trigger output from the PBAT66-PB. This is the same PBAT66-PB trigger as can be inserted into the Event Patterns window of either the T400_PCI or the PCI Setup window, and used as a trigger there. See Section 6.2.

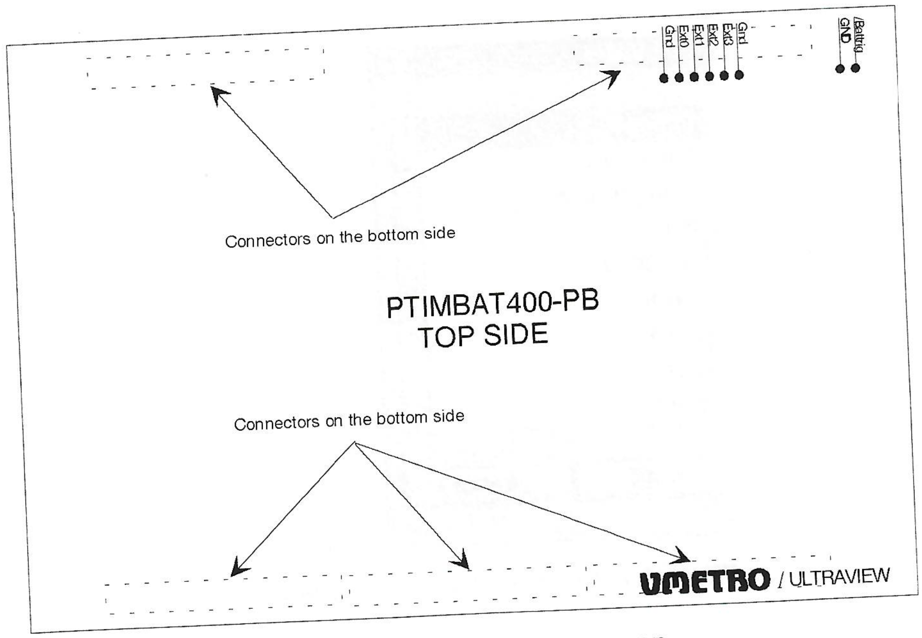


Figure 8.5 The external inputs on the PTIMBAT400-PB

The `Sampling Options` command opens the dialog box in Figure 8.6. From this dialog box it is possible to set up the sampling options as follows:

- When the first option is selected, the PTIMBAT400-PB has no external signals of its own, but uses the external signals on the PBT-415.
- When the second option is selected, there are actually 12 external inputs available. The external inputs on the front panel are used in the PCI setup, and the external inputs on the PTIMBAT400-PB are used in the T400_PCI setup. When using the `Run Multiple` command, a total of 12 external signals are sampled.
- When the third option is selected, the four external inputs are replaced by reserved signals on the PCI bus.