FibreXtreme®

# SL100X/SL240X Hardware Reference for Carrier and Rehostable CMC FPDP Cards

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CURTISS WRIGHT Controls, Inc.
Embedded Computing

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SL100/SL240 Dual-Port Memory FIFO U.S. Patent #6,259,648

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**FCC**

This product is intended for use in industrial, laboratory or military environments. This product uses and emits electromagnetic radiation, which may interfere with other radio and communication devices. The user may be in violation of FCC regulations if this device is used in other than the intended market environments.

**CE**

As a component part of another system, this product has no intrinsic function and is therefore not subject to the European Union CE EMC directive 89/336/EEC.

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# 1. INTRODUCTION

## 1.1 How to Use This Manual

### 1.1.1 Purpose

This manual describes the FibreXtreme SL100X/SL240X CMC FPDP card, and guides you through the process of unpacking, setting up, and using the card.

> **NOTE:** Both the FibreXtreme SL100X and SL240X hardware are referred to throughout this manual as SL240X. The software that supports both the SL100X and SL240X hardware are also referred to as SL240X, including the driver and API. Anything that is exclusive to the SL100X or the SL240X is described as such.

### 1.1.2 Scope

This manual contains the following information:

- An introduction to the FibreXtreme SL240X family of products.
- Applications and topologies for SL240X cards.
- Instructions for installing and configuring the cards.
- An operational overview of the product.
- General card specifications.
- Register set information.
- Configuration information.
- Summary of the protocol used by the SL240X cards.
- Ordering information for all products mentioned in this manual.
- A brief introduction to the Front Panel Data Port (FPDP) interface.
- Specifications for integrating the rehostable CMC FPDP card into an application.
- Definitions of words, phrases, and terms used in this manual.
- List of key words referenced in this manual.

The information in this manual is intended for information systems personnel, system coordinators, or highly skilled network users with at least a systems-level understanding of general computer processing, memory, and hardware operation.

### 1.1.3 Style Conventions

- Called functions are italicized. For example, *OpenConnect()*.
- Data types are italicized. For example, *int*.
- Function parameters are bolded. For example, **Action**.
- Path names are italicized. For example, *utility/sw/cfg*.
- File names are bolded. For example, **config.c**.
- Path file names are italicized and bolded. For example, ***utility/sw/cfg/config.c***.
- Hexadecimal values are written with a "0x" prefix. For example, 0x7e.
- For signals on hardware products, an 'Active Low' is represented by prefixing the signal name with a slash (/). For example, /SYNC.

- Code and monitor screen displays of input and output are boxed and indented on a separate line. Text that represents user input is bolded. Text that the computer displays on the screen is not bolded. For example:

```
c:\>ls
file1           file2               file3
```

- Large samples of code are Courier font, at least one size less than context, and are usually on a separate page or in an appendix.

## 1.2 Related Information

- *ANSI Z136.2-1988 American National Standard for the Safe Use of Optical Fiber Communication Systems Using Laser Diode and LED Sources.*
- *Draft Standard for a Common Mezzanine Card Family: CMC; IEEE P1386, Draft 2.0,* April 4, 1995.
- *Fibre Channel Association Product Information Bulletin Revision,* December 9, 1994.
- *Fibre Channel Physical and Signaling Interface (FC-PH), Revision 4.3,* June 1, 1994; Produced by the ANSI X3T9.3 standards group.
- *Fibre Channel Physical and Signaling Interface-2 (FC-PH-2), Revision 7.3,* January 5, 1996; Produced by the ANSI X3T11 standards group.
- *Fibre Channel Physical and Signaling Interface-3 (FC-PH-3), Revision 8.6,* April, 1996; Produced by the ANSI X3T11 standards group.
- *Front Panel Data Port Specifications, ANSI/VITA 17-1998, Revision 1.0;* February 11, 1999. Produced by the VITA Standards Organization.
- *Serial Front Panel Data Port (FPDP) ANSI/VITA 17.1– 2003 Specifications. Produced by the VITA Standards Organization.*
- *IEC 825-1984 Radiation Safety of Laser Products, Equipment Classification, Requirements, and User's Guide, 2 parts,* 1993.
- *FibreXtreme SL100/SL240 Hardware Reference Manual for PCI, PMC, and CPCI Cards,* (Doc. No. F-T-MR-S2PCIPMC), Curtiss-Wright Controls, Inc.
- *LinkXchange LX1500e Crossbar Switch Hardware Reference Manual,* (Doc. No. F-T-MR-LX1500E), Curtiss-Wright Controls, Inc.
- *LinkXchange LX2500 Crossbar Switch Hardware Reference Manual,* (Doc. No. F-T-MR-LX2500), Curtiss-Wright Controls, Inc.
- VITA - http://www.vita.com/
- Curtiss-Wright Controls, Inc. – http://cwcembedded.com/

## 1.3 Quality Assurance

Curtiss-Wright Controls policy is to provide our customers with the highest quality products and services. In addition to the physical product, the company provides documentation, sales and marketing support, hardware and software technical support, and timely product delivery. Our quality commitment begins with product concept, and continues after receipt of the purchased product.

Curtiss-Wright Controls' Quality System conforms to the ISO 9001 international standard for quality systems. ISO 9001 is the model for quality assurance in design, development, production, installation, and servicing. The ISO 9001 standard addresses all 20 clauses of the ISO quality system, and is the most comprehensive of the conformance standards.

Our Quality System addresses the following basic objectives:

- Achieve, maintain, and continually improve the quality of our products through established design, test, and production procedures.
- Improve the quality of our operations to meet the needs of our customers, suppliers, and other stakeholders.
- Provide our employees with the tools and overall work environment to fulfill, maintain, and improve product and service quality.
- Ensure our customer and other stakeholders that only the highest quality product or service will be delivered.

The British Standards Institution (BSI), the world's largest and most respected standardization authority, assessed Curtiss-Wright Controls' Quality System. BSI's Quality Assurance division certified we meet or exceed all applicable international standards, and issued Certificate of Registration, number FM 31468, on May 16, 1995. The scope of Curtiss-Wright Controls' registration is: "Design, manufacture and service of high technology hardware and software computer communications products." The registration is maintained under BSI QA's bi-annual quality audit program.

Customer feedback is integral to our quality and reliability program. We encourage customers to contact us with questions, suggestions, or comments regarding any of our products or services. We guarantee professional and quick responses to your questions, comments, or problems.

## 1.4 Technical Support

Technical documentation is provided with all of our products. This documentation describes the technology, its performance characteristics, and includes some typical applications. It also includes comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. We also publish and distribute technical briefs and application notes that cover a wide assortment of topics. Although we try to tailor the applications to real scenarios, not all possible circumstances are covered.

Although we have attempted to make this document comprehensive, you may have specific problems or issues this document does not satisfactorily cover. Our goal is to offer a combination of products and services that provide complete, easy-to-use solutions for your application.

If you have any technical or non-technical questions or comments, contact us. Hours of operation are from 8:00 a.m. to 5:00 p.m. Eastern Standard/Daylight Time.

- Phone: (937) 252-5601 or (800) 252-5601
- E-mail: support@systran.com
- Fax: (937) 252-1465
- World Wide Web address: www.cwcembedded.com

## 1.5 Ordering Process

To learn more about Curtiss-Wright Controls' products or to place an order, please use the following contact information. Hours of operation are from 8:00 a.m. to 5:00 p.m. Eastern Standard/Daylight Time.

- Phone: (937) 252-5601 or (800) 252-5601
- E-mail: info@systran.com
- World Wide Web address: www.cwcembedded.com

# 2. PRODUCT OVERVIEW

## 2.1 Overview

The FibreXtreme SL240X cards provide fast, low latency point-to-point or broadcast connections between sensors and processing devices. The FPDP versions include a 6U VME or PCI-based solution with standard FPDP connectors, and a rehostable Common Mezzanine Card (CMC).

The CMC card provides this interface through a simple unidirectional parallel port. This port can be connected to existing FPDP equipment or can be integrated into new products (CMC). All of these variations interoperate completely on the link interface, providing seamless integration between diverse platforms.

## 2.2 SL240X Features

SL240X provides reliable point-to-point or broadcast interconnects between systems, with minimal overhead and very low latency. The protocol involved for this transport is based on Fibre Channel, though it is not Fibre-Channel compliant. The major SL240X features are listed below:

- Uses proven 8B/10B encoding for data transmission.
- End-to-end throughput of 247 MBps with or without frame checksums (SL240X).
- End-to-end throughput of 105 MBps with or without frame checksums (SL100X).
- Minimizes implementation cost and enhances throughput by using a simple protocol.
- Provides built-in data synchronization with very little reduction in throughput.
- Integrated interrupt controller to report link failure, transaction completion, or buffer space request.
- Status LED that reports link stability.
- Loop operation with out-of-band arbitration or point-to-point operation.
- Provides a register set designed for easy programming and status retrieval.
- Four media options available—long-reach wavelength laser, long wavelength laser, short wavelength laser, and HSSDC2 copper.
- Watchdog timer for failover operation.
- 1 MB Receive FIFO.
- 2 KB Transmit FIFO.
- Rugged versions of some cards are available.

### 2.2.1 Media Options

There are four basic media options—a long wavelength laser (1300 nm), short wavelength laser (850 nm), and HSSDC2 copper. The long-reach wavelength laser is required for very long distances (10 km to 50 km). Long wavelength laser interconnections are recommended for intermediate distances (300 m to 10 km). The short wavelength version is useful for intrasystem connections, such as connecting between cards on the same backplane. It is also suited for short reach intersystem connections (< 300 m). HSSDC interconnections are recommended for very short distances of 30 meters or less.

All cards use a Duplex LC style connector or HSSDC2 receptacle, available from most major cable manufacturers. For details concerning this connector, contact Curtiss-Wright Controls, Inc. Technical Support.

## 2.3 SL240X Cards

This section contains photographs of the SL240X CMC and VME FPDP cards.

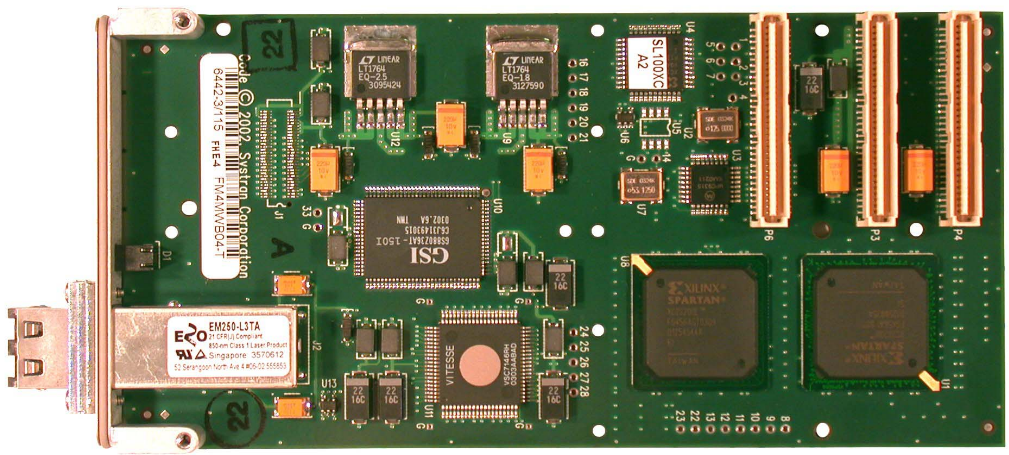


**Figure 2-1 SL240X Rehostable CMC Card**

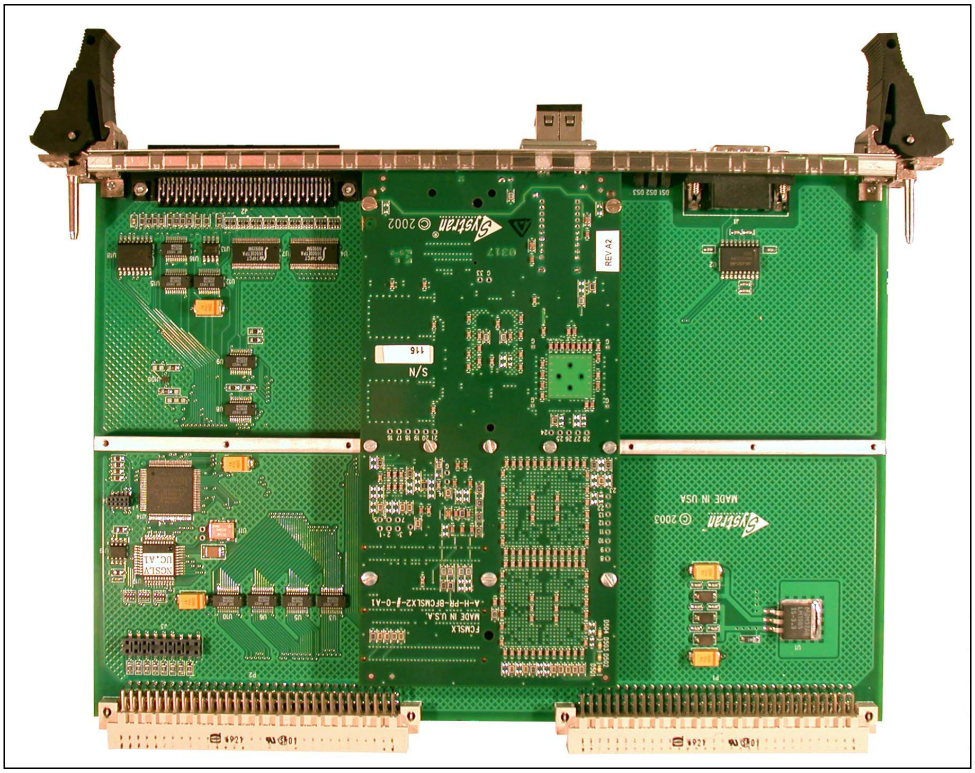

**Figure 2-2 NGSL VMER Card**

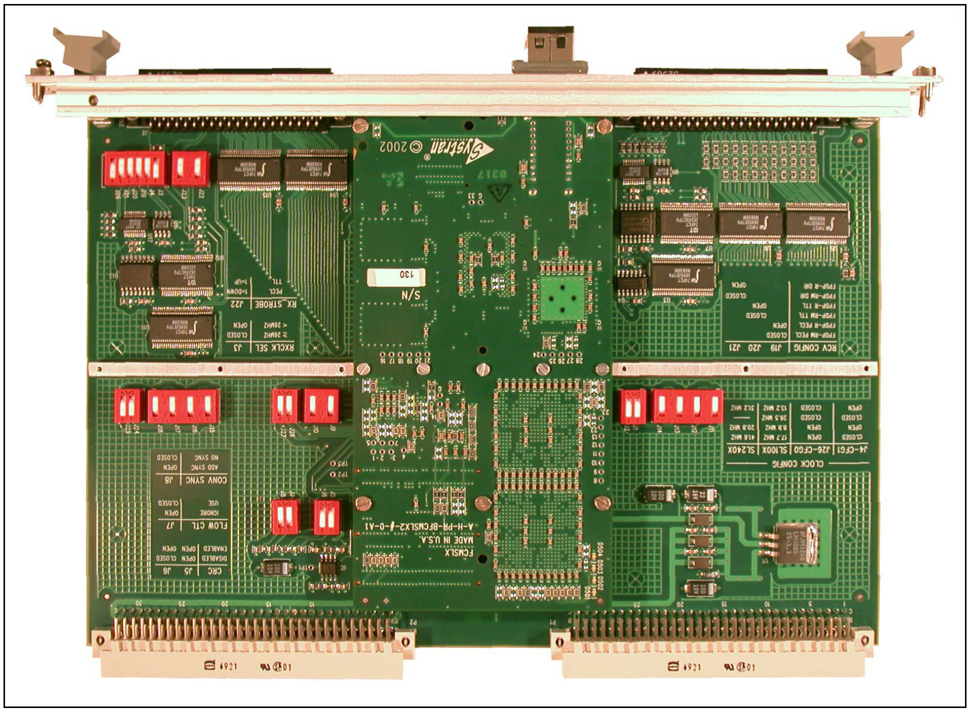

**Figure 2-3 FXSL VMER Card**



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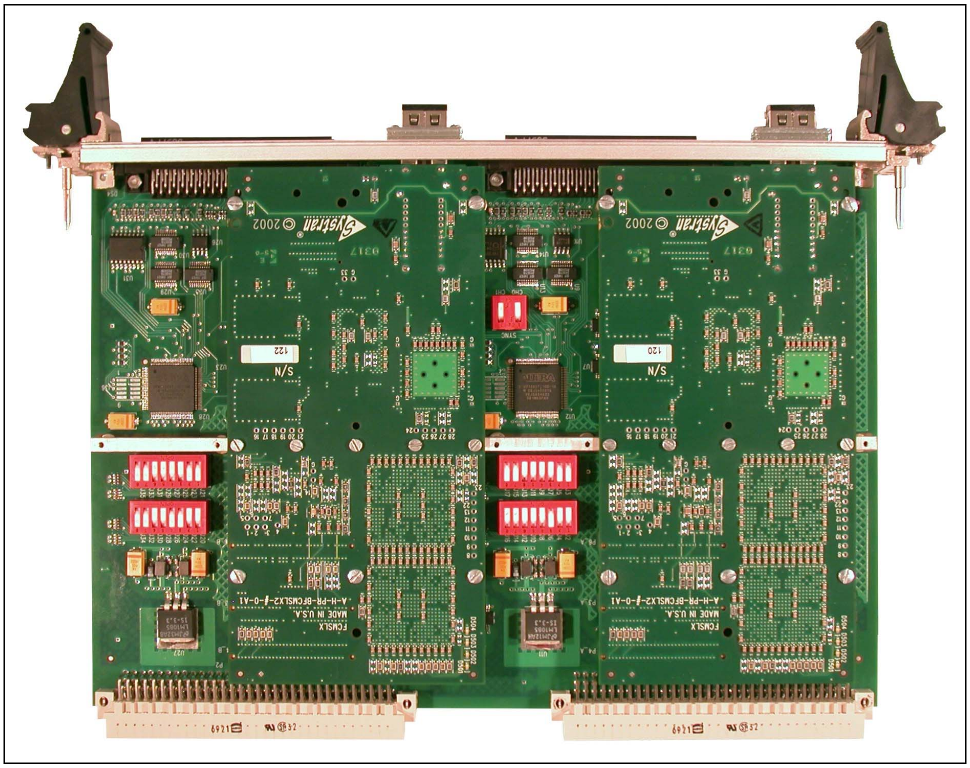

**Figure 2-4 DUAL VMER Card**

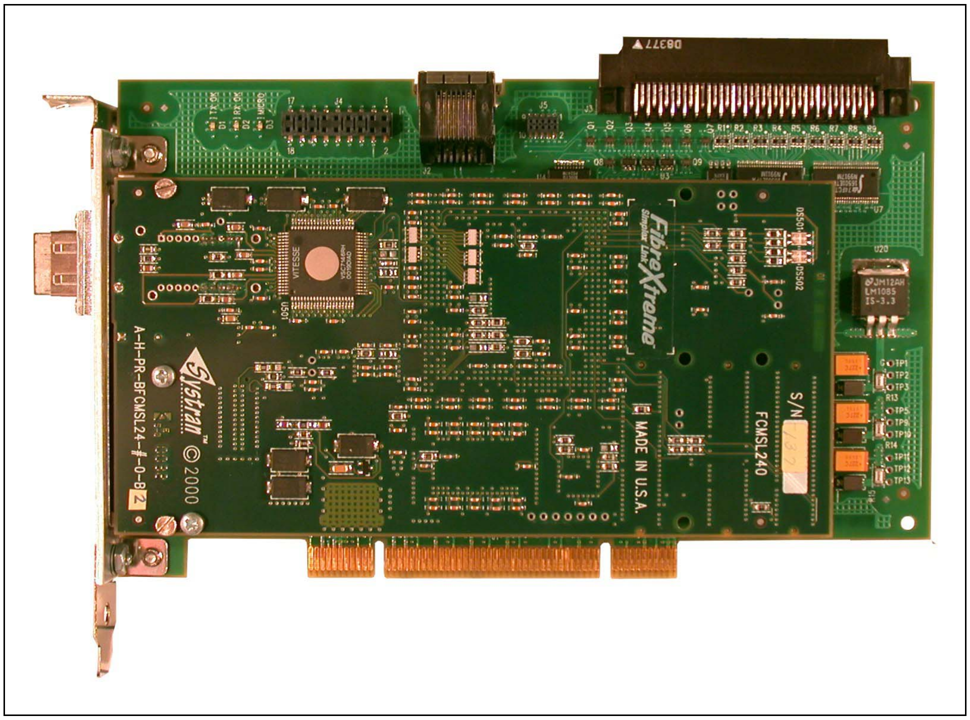

**Figure 2-5 PCI FibreXtreme Carrier Card**

## 2.3.1 FPDP Card Features

The major features of the various FPDP cards are listed below. See Table 2-1 for a summary of all FPDP card features.

**NOTE:** The FPDP bus speeds are derived from the reference clock (53.125 MHz or 125 MHz) divided by 2, 3, 4, or 6.

### NGSL VMER FPDP CARDS

Sample Application: Useful for applications where it is desired to change the FPDP port data direction via software control and a 6U VME form factor is required.

Features:

- 6U VME form factor
- One FPDP port configurable for input or output
- Accepts one SL100X/SL240X CMC card
- Configurable using a microcontroller interface via an RS-232 port
- Offers access to SL100X/SL240X CMC card's register set
- Supports the following FPDP transmitter bus speeds

**Table 2-1 NGSL VMER FPDP Transmitter Bus Speeds**

| Reference Clock Division Factor | SL100X (53.125 MHz) | SL240X (125 MHz) |
|---|---|---|
| 2 | 26.5625 MHz | 62.5000 MHz |
| 3 | 17.7083 MHz | 41.6667 MHz |
| 4 | 13.2813 MHz | 31.2500 MHz |
| 6 | 8.8542 MHz | 20.8333 MHz |

### FXSL VMER FPDP CARD

Sample Application: Useful for applications requiring bi-directional data flow on the link interface and two channels of FPDP data.

Features:

- 6U VME form factor
- Two FPDP ports (one input and one output)
- Accepts one SL100X/SL240X CMC card
- Does not offer access to SL100X/SL240X CMC card's register set
- Configurable using switches
- Supports the following FPDP transmitter bus speeds

**Table 2-2 FXSL VMER FPDP Transmitter Bus Speeds**

| Reference Clock Division Factor | SL100X (53.125 MHz) | SL240X (125 MHz) |
|---|---|---|
| 2 | 26.5625 MHz | 62.5000 MHz |
| 3 | 17.7083 MHz | 41.6667 MHz |
| 4 | 13.2813 MHz | 31.2500 MHz |
| 6 | 8.8542 MHz | 20.8333 MHz |

## DUAL VMER FPDP CARDS

Sample Application: Useful for applications requiring two channels of FPDP data but having a limited number of available VME slots.

Features:

- 6U VME form factor
- Two independent FPDP ports configurable for input or output (one FPDP port per CMC card)
- Accepts one or two SL100X/SL240X CMC cards
- Does not offer access to SL100X/SL240X CMC card's register set
- Configurable using switches
- Supports the following FPDP transmitter bus speeds

**Table 2-3 Dual VMER FPDP Transmitter Bus Speeds**

| Reference Clock Division Factor | SL100X (53.125 MHz) | SL240X (125 MHz) |
|---|---|---|
| 2 | 26.5625 MHz | 62.5000 MHz |
| 3 | 17.7083 MHz | 41.6667 MHz |
| 4 | 13.2813 MHz | 31.2500 MHz |
| 6 | 8.8542 MHz | 20.8333 MHz |

## PCI FIBREXTREME CARRIER CARD

Sample Application: Useful for applications where it is desired to change the FPDP port data direction via software control and a PCI form factor is required.

Features:

- PCI form factor
- One FPDP port configurable for input or output
- Accepts one SL100X/SL240X CMC card
- Configurable using a microcontroller interface via an RS-232 port
- Offers access to SL100X/SL240X CMC card's register set
- Supports the following FPDP transmitter bus speeds

**Table 2-4 PCI FibreXtreme Carrier FPDP Transmitter Bus Speeds**

| Reference Clock Division Factor | SL100X (53.125 MHz) | SL240X (125 MHz) |
|---|---|---|
| 2 | 26.5625 MHz | 62.5000 MHz |
| 3 | 17.7083 MHz | 41.6667 MHz |
| 4 | 13.2813 MHz | 31.2500 MHz |
| 6 | 8.8542 MHz | 20.8333 MHz |

**Table 2-5 Summary of FPDP Card Features**

| Features | Carrier Card | | | |
|---|---|---|---|---|
| | NGSL VMER | FXSL VMER | Dual VMER | PCI |
| Number of FPDP Ports | 1 | 2 | 2 | 1 |
| Number of CMC Cards | 1 | 1 | 2 | 1 |
| Configuration Method | Microcontroller | Switches | Switches | Microcontroller |
| Form Factor | 6UVME | 6UVME | 6UVME | PCI |
| CMC Cards Supported | | | | |
| SL100X | Yes | Yes | Yes | Yes |
| SL240X | Yes | No | Yes | Yes |
| Register Set Access | | | | |
| Carrier Card | Yes | No | No | Yes |
| CMC Card | Yes | No | No | Yes |
| FPDP Transmitter Bus Speeds Supported | | | | |
| SL100X | | | | |
| 26.5625 MHz | Yes | Yes | Yes | Yes |
| 17.7083 MHz | Yes | Yes | Yes | Yes |
| 13.2813 MHz | Yes | Yes | Yes | Yes |
| 8.8542 MHz | Yes | Yes | Yes | Yes |
| SL240X | | | | |
| 62.5000 MHz | Yes | Yes | Yes | Yes |
| 41.6667 MHz | Yes | Yes | Yes | Yes |
| 31.2500 MHz | Yes | Yes | Yes | Yes |
| 20.8333 MHz | Yes | Yes | Yes | Yes |

## 2.4 Applications

SL240X cards can be used in a variety of topologies for a variety of applications. The following sections detail typical topologies used and some applications. Many other applications are possible in these configurations.

### 2.4.1 LinkXchange LX2500 Crossbar Switch (LX2500)

Curtiss-Wright Controls' LX2500 Crossbar Switch provides the following features:

- Up to 32 non-blocking media-specific I/O ports.
- Up to 2.5 Gbps/port baud rate (port card dependent).
- Support for multiple point-to-point, loop, and broadcast communication links simultaneously.
- Automatic I/O Port fault isolation.
- Multiple media options.
- Out-of-band control through an RS-232 port.
- Can be connected to a modem and controlled from a remote location.

For more detailed information regarding LX2500 features and operation, contact Curtiss-Wright Controls and request a copy of the *LinkXchange LX2500 Crossbar Switch Hardware Reference Manual* or visit our web site.

## 2.4.2 Typical Digital Signal Processing (DSP) Imaging System

With the support for 1.0625 Gbps or 2.5 Gbps link transmission rates between interconnected subsystems, SL240X is ideal for use in many of today's high-throughput data transfer applications. One example is shown in Figure 2-6. This figure shows the SL100X's usable data throughput rate. However, the figure is also applicable to SL240X by changing the data throughput rate to 247 MBps.

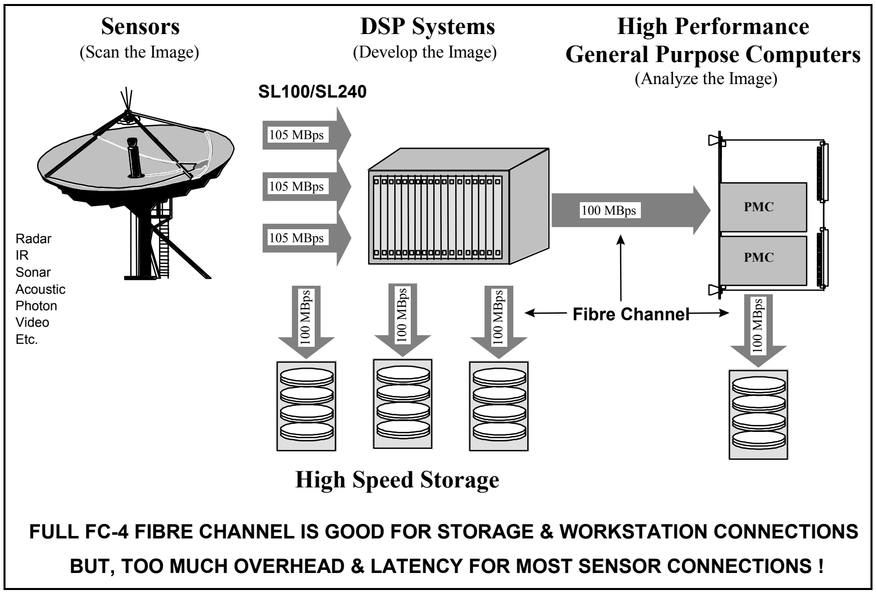


**Figure 2-6 Typical Applications of FibreXtreme SL240X in Advanced DSP Systems**

### 2.4.3 Extending FPDP

The maximum allowable length for FPDP cables ranges from 1 m to 5 m depending upon its configuration. The FibreXtreme SL240X system provides a communication link that extends the reach of FPDP while retaining simplicity, high bandwidth, and reliability. This concept is shown in Figure 2-7. The type of transceiver used determines the distance the FPDP cards can be separated. See section 2.2.1, Media Options, for details on transceivers. Using fiber optics provides electrical isolation.

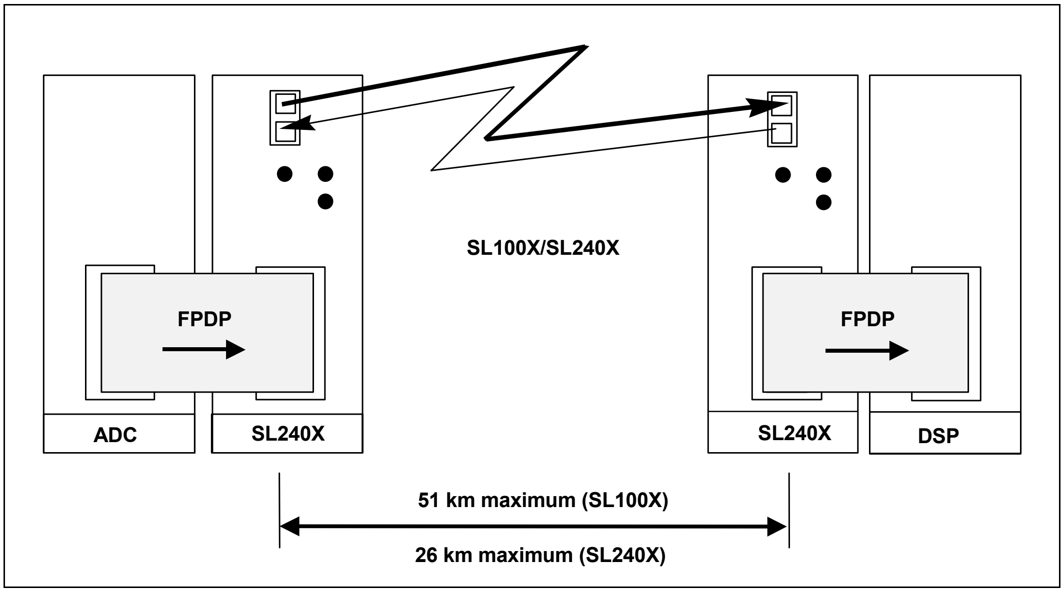


**Figure 2-7 FibreXtreme SL240X Extending FPDP**

## 2.5 Topologies

### 2.5.1 Typical Topologies

There are four typical topologies for the SL240X card. These topologies should cover most customer applications, though if another topology is desired contact Curtiss-Wright Controls Technical Support to see if it is possible. The topologies are:

- Point-to-point
- Chained
- Single Master Loop
- Multiple Master Loop

### 2.5.2 Point-to-point

The point-to-point topology is the native mode for the SL240X card. One user option available in this mode is if flow control is used. If flow control is used, the transmitter on each end will not transmit when the remote receiver is telling it to back off or the receive fiber is missing. In this mode, the maximum amount of data that can be transferred is 247 MBps per direction (in this case, both cards are receiving and transmitting 247 MBps at the same time). The maximum distance between the nodes is 26 km.

There are many applications for the point-to-point topology—as long as it involves only two nodes, this topology covers it. One advantage that point-to-point has over the other topologies is the ability to do simultaneous bi-directional traffic.

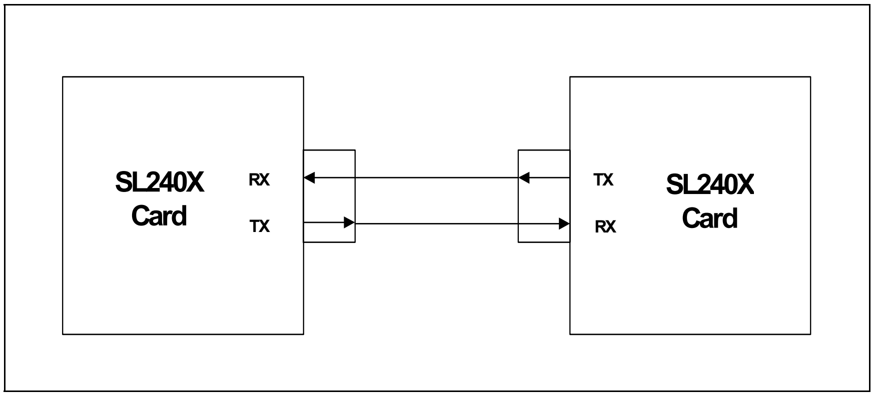


**Figure 2-8 Point-to-Point Topology**

## 2.5.3 Chained

This topology is a single transmitter on the end of a long string of receivers. No flow control is available in this topology, and the distance between the nodes is limited only by the transceivers used (10 km typical, 26 km maximum).

This topology is good for broadcasting data to multiple destinations where late data is of no use, such as video transmission applications.

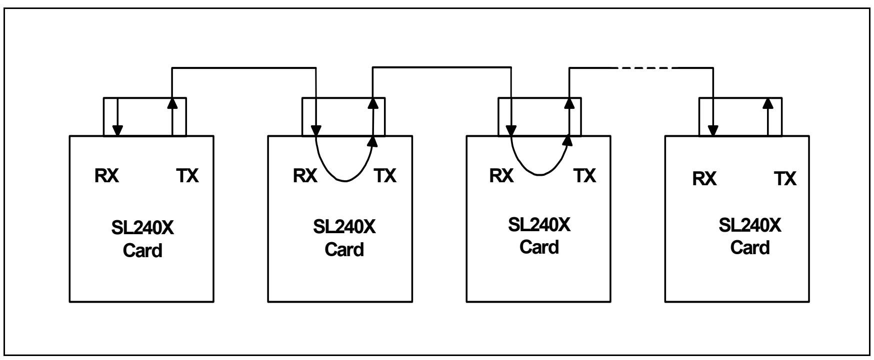


**Figure 2-9 Chained Topology**

## 2.5.4 Single Master Ring

This is one of the most useful topologies for the SL240X card. This topology allows a single transmitter to send data to a group of destinations with flow control from all of the destinations. Note that this flow control is a single flag to the master—either it can send or it cannot send data. This means that if one destination has a failure and stops removing data from its Receive FIFO, it should be switched out to avoid bringing down the loop. A Crossbar Switch suitable for this purpose, the LinkXchange LX2500 Crossbar Switch, is available from Curtiss-Wright Controls, Inc. Software controls mastership switching of the ring. There are rules associated with master switching listed in the "Programming Interface" section. The flow control used in this case is similar to a multi-drop FPDP bus, where any receiver can back the transmitter off.

This is the typical configuration for record-playback systems, where you have multiple signal processors and data storage elements present on the network and there is only one node (the data source or the recorder playing the data back) transmitting at a time.

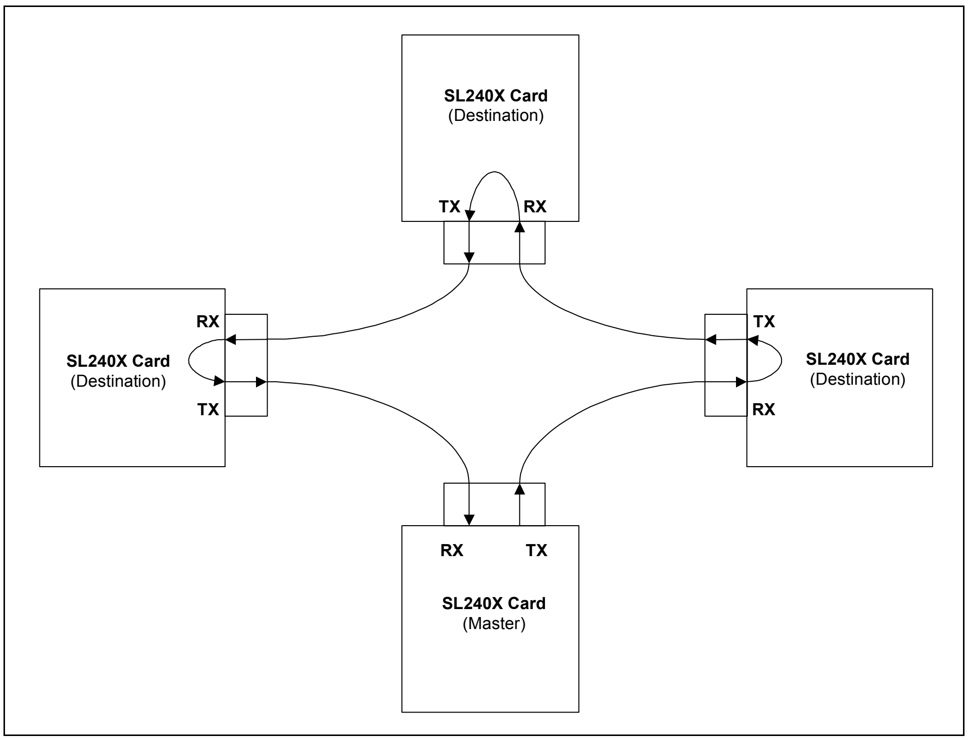


**Figure 2-10 Single Master Ring**

### 2.5.5 Multiple Master Ring

This is another form of ring topology, where there are multiple masters on the ring, and these masters have to receive data as well as transmit data to the next master. In the most complex case, each node is a master, which means that it receives data from the previous master and sends data to the next master. No flow control is allowed in this topology for rings above two nodes, and the data cannot be passed through masters unless control guarantees that there is at least one source-only node on the ring, and that no two masters will transmit at the same time. Single master rings should temporarily become multiple master rings when switching loop masters.

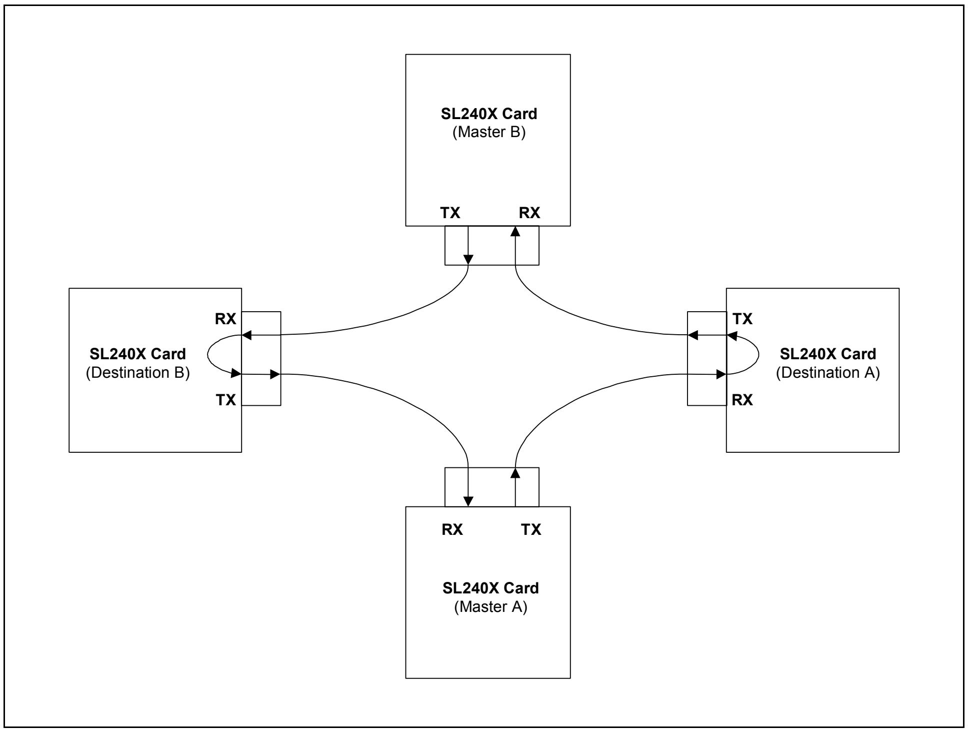


**Figure 2-11 Multiple Master Ring**

## 2.6 Status LEDs

### 2.6.1 "LINK UP" LED

All of the SL240X cards are equipped with a link status indicator LED. This LED is labeled "LINK UP"and is visible through the card's faceplate. When this LED is lit, it indicates a signal is present on the receiver. This LED gives no indication of the validity of the signal, only that a signal is present.

### 2.6.2 "MICRO," "RX OK," and "TX OK" LEDs

The NGSL VMER card has three status LEDs. The FXSL VMER card has two status LEDs. The Dual VMER card has four status LEDs. These LEDs viewed from the front end of the card are shown in Figures 2-11, 2-12 and 2-13. The PCI FibreXtreme Carrier card has three LEDs. These LEDs viewed from the component side of the card are shown in Figure 2-14.

The LED labeled "MICRO" is currently not used and will remain unlit.

When the LED labeled "RX OK" is lit, it indicates no errors have occurred on the FPDP receive interface or the link transmit interface. When this LED is not lit, the link interface is down and flow control is not ignored.

When the LED labeled "TX OK" is lit, it indicates no errors have occurred on the FPDP transmit interface or the link receive interface. When this LED is not lit, any one of the following errors have occurred:

- Receive FIFO overflow.
- The link interface is down.
- CRC error.
- 8B/10B decoding error.

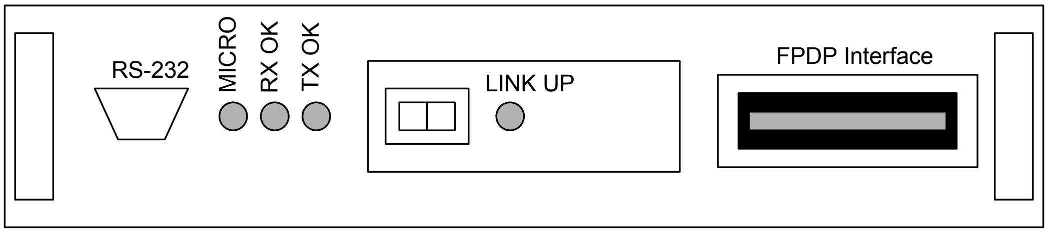


**Figure 2-12 Status LEDs on SL240X VME and Rehostable CMC Cards**

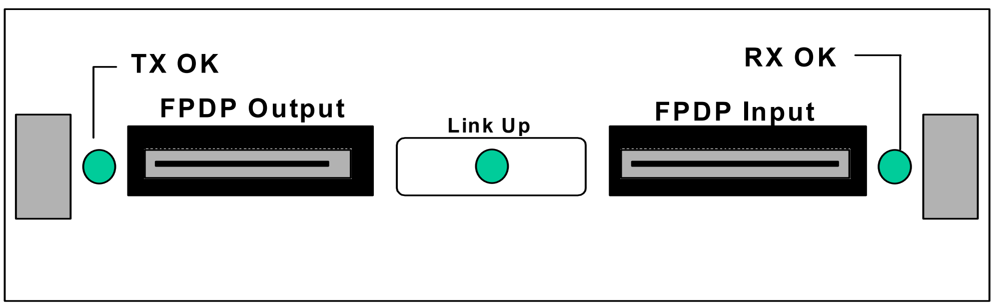


**Figure 2-13 Status LEDs on FXSL VMER and Rehostable CMC Card**

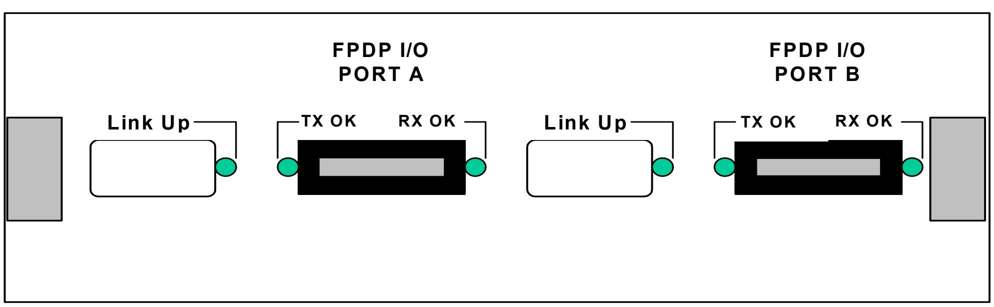


**Figure 2-14 Status LEDs on Dual VMER and Rehostable CMC Cards**

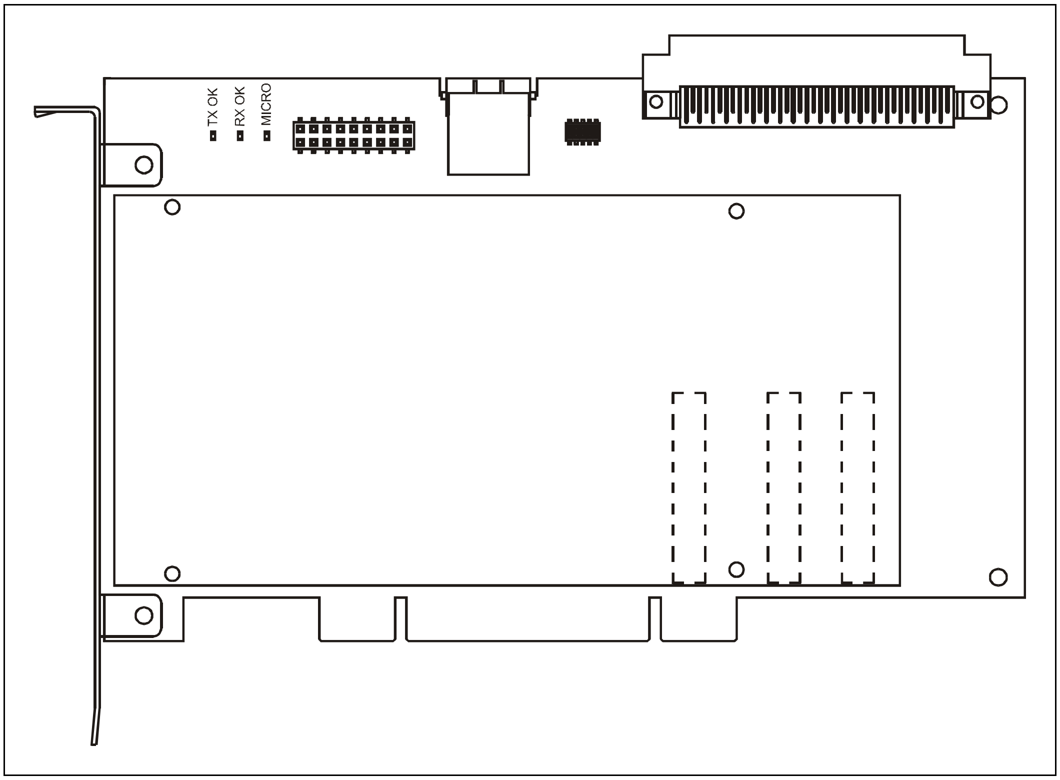


**Figure 2-15 Status LEDs on PCI FibreXtreme Carrier Card**

# 3. INSTALLATION

## 3.1 Installation Procedures

Each FibreXtreme VME FPDP card requires only one slot on the VME host backplane The PCI FibreXtreme Carrier card requires one PCI slot. A FibreXtreme SL240X rehostable CMC FPDP card requires only one slot on your custom-designed carrier.

To install the SL240X card, follow the steps below:

1. Unpack the card.
2. Inspect the card.
3. Install the card.
4. Configure the card.
5. Connect the cables.

## 3.2 Unpack the Card

**CAUTION:** Exercise care regarding the static environment. Use an anti-static mat connected to a wristband when handling or installing the SL240X card. Failure to do this may cause permanent damage to the components on the card.

Follow the steps below to unpack the card:

1. Put on a wristband attached to an anti-static mat.
2. Remove the card and anti-static bag from the carton.
3. Place the bag on the anti-static mat.
4. Open the anti-static bag and remove the card.
5. In the unlikely event you need to return your SL240X card, please keep the original shipping materials for this purpose.

Any optional equipment is shipped in separate cartons.

## 3.3 Inspect the Card

Each FibreXtreme FPDP card consists of a single card with a built-in link interface and FPDP interface. A FibreXtreme SL240X rehostable CMC FPDP card consists of a single card with a built-in link interface. If the card was damaged in shipping, notify Curtiss-Wright Controls or your supplier immediately.

# 3.4 Install the Card

**WARNING**: Before installing any peripheral component into a computer, ensure the system is powered off.

## 3.4.1 VME Card Installation

To install the VME card:

1. Insert the card into the VME backplane until it is firmly seated.
2. Install the screws to fasten the card in place.

## 3.4.2 PCI FibreXtreme Carrier Card Installation

To install the PCI FibreXtreme Carrier card, push the card into the mother card, as shown in Figure 3-1, steps 1 and 2, until it is firmly seated. Install the mounting screw as shown in step 3.

**NOTE:** The PCI FibreXtreme Carrier card only uses +5 volt power and ground from the PCI bus. As a result, it can be plugged into any PCI/PCI-X slot (3.3 or 5 volt) and will also have no impact on PCI/PCI-X bus throughput.

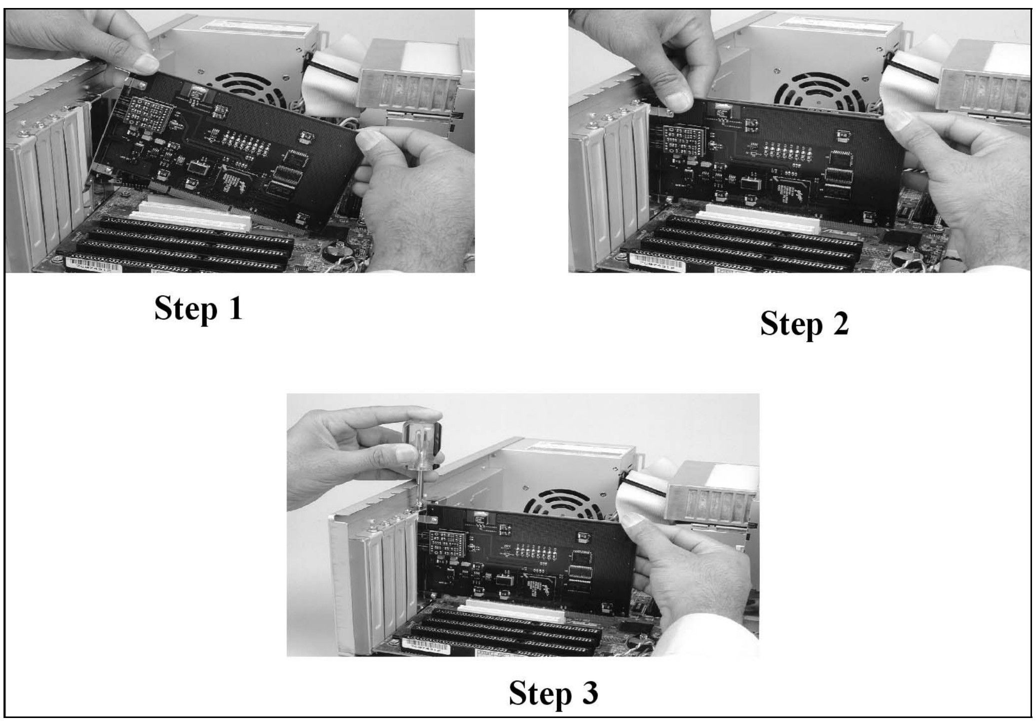


**Figure 3-1 SL240 PCI Card Installation**

## 3.4.3 Rehostable CMC Card Installation

Since the SL240X CMC FPDP card was designed to be rehostable, the installation procedures depend upon the user's design.



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# 3.5 Configure the Cards

See Appendix C, CARRIER/CMC Configuration, for configuration instructions.

# 3.6 Connect the Cables

## 3.6.1 FPDP Cables

The FPDP cables are ribbon cables with 80-pin Robinson-Nugent RN PAK-50 latching, high-density socket connectors at each end. Robinson-Nugent's part number for the ribbon cable connector is: P50E-080S-TG. Curtiss-Wright Controls uses the Robinson-Nugent P50E-080P1-SR1-TG connector on the SL240X VME FPDP card.

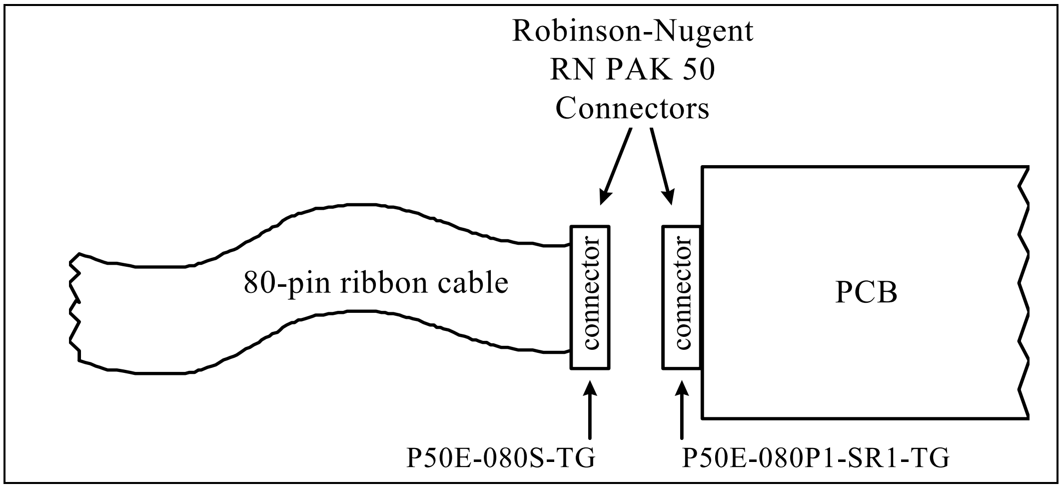


**Figure 3-2 FPDP Connectors**

**NOTE:** Curtiss-Wright Controls, Inc. does not provide the FPDP cables. Please use the Robinson-Nugent connector (part number: P50E-080S-TG) to make your own cable set or contact the appropriate cable vendor to acquire the cable set you desire.

## 3.6.2 Fiber-optic Cables

The two factors to consider when connecting the cables are the topology and the transmission media used. There are several different topologies the cards can be connected in, depending on your application. See section 2.5 for more detailed examples of topologies.

**Fiber-optic Cable Precautions**

**CAUTION:** Fiber-optic cables are made of glass and may break if crushed or bent in a loop with less than a 2-inch radius.

Look at the cable ends closely before inserting them into the connector. If debris is inserted into the transmitter/receiver connector, it may not be possible to clean the connector out and could result in damage to the transmitter or receiver lens. Hair, dirt, and dust can interfere with the light signal transmission.

Use an alcohol-base wipe to clean the cable ends.

For short wavelength laser modules, either a 50 µm or 62.5 µm core diameter cable should be used. A 62.5 µm cable can be used for distances up to 300 m. 50 µm cable allows distances up to 500 m. For distances greater than 500 m (up to 10 km), long wavelength laser modules with 9 µm core cable should be used.

The optional fiber-optic cables may be shipped in a separate carton. Remove the rubber boots on the fiber-optic transmitters and receivers as well as the ones on the fiber-optic cables. These rubber boots should be replaced when cables are not in use or in the event the node must be returned to the factory. Attach the fiber-optic cables to the connectors on the SL240X card.

Figure 3-3 and Figure 3-4 depict the types of fiber-optic connectors needed for the SL240X card.

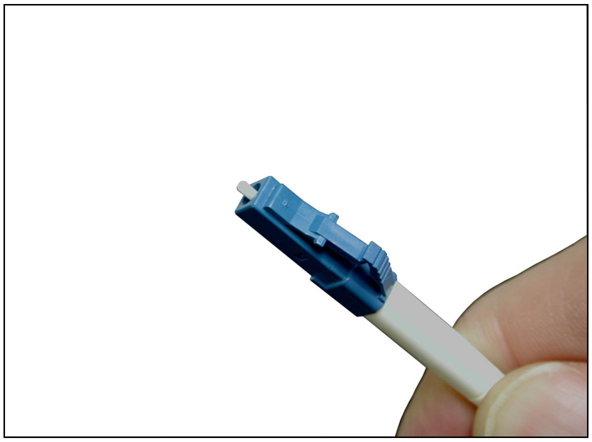

**Figure 3-3 Fiber-optic Simplex LC Connector**

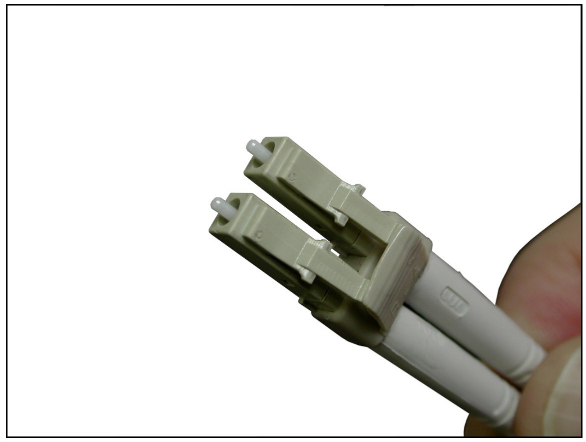

**Figure 3-4 Fiber-optic Duplex LC Connector**

### 3.6.3 Copper Cables

The copper media **i**nterface on the SL100X/SL240X cards support shielded cable, terminated with HSSDC2 style connectors, shown in Figure 3-5. Figure 3-6 displays the HSSDC2 SFP receptacle used on the SL100X/SL240X cards. This figure indicates the HSSDC2 contact pin locations and Table 3-1 contains the pin assignments.

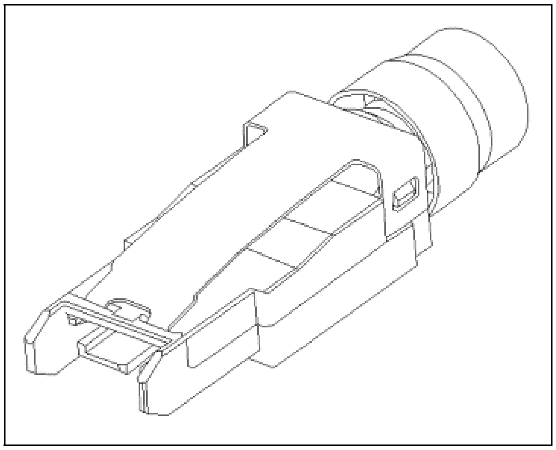

**Figure 3-5 HSSDC2 Copper Connector**

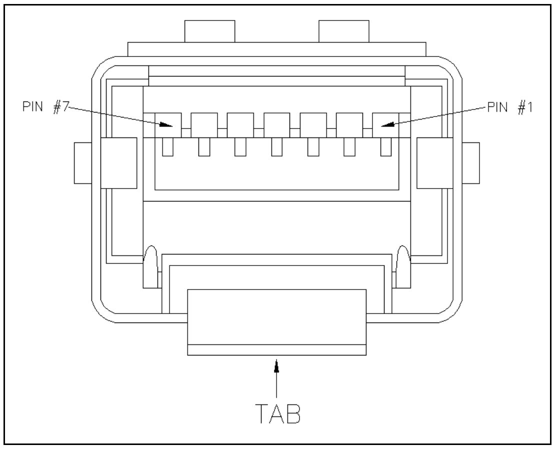


**Figure 3-6 HSSDC2 Receptacle Contact Pin Locations**

**Table 3-1 HSSDC2 Receptacle Pin Assignments for SL100**

| Pin Number | Pin Description |
|---|---|
| 1 | Ground |
| 2 | Receive - |
| 3 | Receive + |
| 4 | Ground |

| Pin Number | Pin Description |
|---|---|
| 5 | Transmit + |
| 6 | Transmit - |
| 7 | Ground |

**Table 3-2 HSSDC2 Receptacle Pin Assignments for SL240**

| Pin Number | Pin Description |
|---|---|
| 1 | Ground |
| 2 | Receive + |
| 3 | Receive - |
| 4 | Ground |
| 5 | Transmit - |
| 6 | Transmit + |
| 7 | Ground |

To insure data integrity, take care when selecting the appropriate HSSDC2 cable assembly for the SL100X/SL240X application. Application data rate and the presence of equalization circuits determine length boundaries for HSSDC2 cable assemblies. Application operating at 2.5 Gbps must use equalized 100 Ohm HSSDC2 cables for cable lengths greater than 5 meters. However, applications operating at 1.0625 Gbps must use equalized 150 Ohm HSSDC2 cables when cable lengths exceed 15 meters.

**NOTE:** The HSSDC2 cables are not interchangeable due to different keying.

## 3.7 Troubleshooting

If the system does not boot correctly, power down the machine, reseat the card, double-check cable connections, and turn the system back on. If problems persist, contact Curtiss-Wright Controls Technical Support at **(800) 252-5601** or **support@systran.com** for assistance.

Please be prepared to supply the following information:

Machine: ______________________________
OS Name: ______________________________
OS Version: ______________________________
Card Type: ______________________________
Card Serial #: ______________________________
Software Part #: ______________________________
Software S/N: ______________________________
Problem Reproducibility: _________________________
Problem Description: _________________________

# 4. OPERATION

## 4.1 Overview

SL100X/SL240X cards move data with very low latency between a host interface and a 1.0625 Gbps or a 2.5 Gbps link, respectively. The host interfaces available is an FPDP-like proprietary interface. The advantage of the FPDP-like interface is that it requires very simplistic hardware to interface.

**CAUTION**: Do **not** break the link between two SL100X/SL100X cards. The unpredictable results may affect your system. While the FPGA can recover from link break scenarios, the corresponding link and data errors caused by disruption of the link must be adequately addressed by the host interface.

**NOTE:** It is not possible for the SL100X and SL240X cards to communicate/operate with each other on the link because the link speeds are not compatible.

## 4.2 Theory of operation

The operation of SL240X cards is simple—take data from the host bus interface and transmit it across a link, or take data from the link and pass it to the host bus interface. The link protocol involved is kept minimal to reduce the latency and improve throughput, while still providing a set of useful features for users to customize their applications. The hardware is designed to offer many different features for advanced applications, while maintaining a simple interface to the most commonly used features.

**NOTE:** For further explanation of terms used in the following sections, consult the FPDP Primer located in Appendix F.

### 4.2.1 Receive Operation

The SL240X card has several options for receiving data. The most basic option is no loop operation with data receive enabled. In this case, data is:

1. Received from the link.
2. Decoded by the card.
3. Placed in the Receive FIFO.

At this point, the operation depends on the host interface. If it is an FPDP based card, and /SUSPEND is not asserted, the card asserts /DVALID and proceeds to transmit the data on the FPDP interface. If /SUSPEND or /NRDY is asserted, then the data waits in the Receive FIFO until these signals go away.

FPDP signals are embedded into the control words of a frame. The FPDP signals transported across are: /NRDY, /DIR, /SYNC, PIO1 and PIO2. A /SUSPEND signal is synthesized by the transmit state machine in response to how full the Receive FIFO is – this is not the /SUSPEND from an FPDP port.

All FPDP signals, with the exclusion of /SYNC, are passed around the Receive FIFO and are not synchronized with the data stream.

### 4.2.2 Transmit Operation

The transmit operation first has to collect data in the Transmit FIFO for transmission. FPDP cards collect any data words accompanied by /DVALID on the FPDP interface. Once a data word is in the FIFO, transmission can begin. The framing state machine first checks that there is no data in the Retransmit FIFO and that the remote node is not telling this node to back off. If it is clear to send, after it transmits the next SOF it begins filling the data frame as full as possible (up to 2048 bytes). The data is then encoded and sent out across the link. If there is data in the Retransmit FIFO or the card is being backed off from the destination, then the card waits until both conditions are clear before it starts transmission. Note that SYNC and SWDV can also be transmitted by the link logic and these two types of synchronization primitives are handled by the Transmit FIFO and transmit control logic in a similar method as standard data. Specifically, they are written to the link logic through the same interface, passed through the same internal link logic path, and are used in the assembly of link frames in a similar fashion, although the maximum frame size does differ for these types of associated Serial FPDP frames.

All FPDP signals, with the exclusion of /SYNC, are passed around the Transmit FIFO and are not synchronized with the data stream. For PCI variations of this card, the FPDP signals can be written to a register and then transmitted across the link.

### 4.2.3 Loop Operation

In the Loop Operation discussion below, SL100X/SL240X is used generically to refer to any Curtiss-Wright Controls SL100X/SL240X card. Anything that applies to only a specific SL100X/SL240X product will be noted as such.

Loop operation with the SL100X/SL240X acts like a virtual FPDP bus where one source (the loop master) can transmit to any number of receive nodes. The link protocol is the same for this operation, except any node in the loop may assert a suspend request embedded in this data stream. This implies if one node on the loop is not ready to receive data, the source is backed off for all nodes. This is the same way that multi-drop FPDP busses function.

The fundamental difference between a loop master and a receiving node is the loop master does not have its loop retransmission enabled. So, to the loop master, it appears as if it is still in a point-to-point connection with a single node. Receiving nodes, on the other hand, have knowledge that they are in a loop configuration and must be configured as such. Note that the loop master receives all the data it transmits, so data can either be checked for errors or ignored when it is received. This checking (beyond verification of CRC and 8B/10B decoding validity) is not done in the SL100X/SL240X and must be implemented by the system designer.

The receivers on the loop can choose to collect the data or ignore it off the loop. If the Receive FIFO is enabled (the node is collecting data), a suspend request may be asserted by this node as the data passes through. If it is not configured to receive the data, it simply passes the data through the Retransmit FIFO without modifying the suspend request.

Serial FPDP supports the DIR, NRDY, PIO1, and PIO2 FPDP signals. These signals do not propagate through the Transmit FIFO or the Receive FIFO and thus cannot be directly associated with the corresponding data. To guarantee a pulse on these signals is propagated to the remote Serial FPDP receiver, the pulse width from the host-bus interface must be equal to or greater than the maximum Serial FPDP frame length (512 words of data with an overhead of nine ordered sets). The use of these signals is host-specific and will now be explained for each SL100X/SL240X product.

For SL100X/SL240X CMC cards, the values of PIO1 and PIO2 are retransmitted according to their received link values and the values of DIR and NRDY are used as follows: if the receive interface is enabled, the values transmitted are the received link values logically ORed with the FPDP host-interface values; otherwise, the values are retransmitted according to their received link values. NRDY received from the link translates to /NRDY output from the FPDP receiver (FPDP-RM or FPDP-R) port. Thus, reception of NRDY from the link interface may be used to back off the FPDP transmitter, depending of the usage of /NRDY used by the respective FPDP transmit master.

Curtiss-Wright Controls' SL100X/SL240X CMC cards, when functioning as a FPDP transmit master, will stop the transmission of FPDP data when /NRDY is asserted by the FPDP receiver. The receipt of a suspend request will indirectly back off the FPDP transmitter, as the link logic no longer transmits link data, the link Transmit FIFO will back up, which will eventually back off the FPDP transmitter via the assertion of the /SUSPEND signal. The values of these four signals (PIO1, PIO2, DIR, and NRDY) sent to and received from the link are placed on the FPDP bus and also in the register set, if applicable. If placed in the register set, they can be accessed by a microcontroller via the optional microcontroller interface on the CMC carrier. The use of DIR and NRDY is consistent with the use of flow control (retransmission of a STOP request) for loop operation. See the ANSI/VITA 17.1 Serial FPDP specification for additional details.

Note that NRDY as a Serial FPDP signal has no direct impact on the operation of the link logic. Rather, NRDY is simply passed through the link logic and its function is dependent on the respective host interface. The Serial FPDP flow control (implemented via suspend requests which are also known as STOP ordered sets) is used by the link logic and does not directly affect the interface between the link logic and host interface.

**NOTE:** One node on the loop MUST be in non-loop operation in order for loop operation to work correctly. One node needs to remove the data from the loop. When switching masters on the loop, both the previous master and the next master should be in non-loop operation before the previous master switches into loop mode.

## 4.3 Data Synchronization

There is a data synchronization primitive, called SYNC, which is sent across the link under user control. This primitive is used to synchronize with the data stream. On the FPDP card, this signal is the /SYNC line on the FPDP interface.

Unless a non-intelligent device is used, such as a sensor, which cannot insert a periodic SYNC, SYNC should always be used to segment data transfers. It has little impact on system performance and will provide a mechanism to synchronize the send and receive operations via the link. This synchronization process is especially useful at application start-up, after error conditions, and is also useful to verify the error-free flow of data during normal operation.

## 4.4 Configuration Options

There are many different configuration options available which affect the operation of the SL240X card. Most of these options are configured in the Link Control register (described in Appendix B).

### 4.4.1 Flow Control

Flow control allows a Serial FPDP receiver to throttle the data stream from a Serial FPDP transmitter. If this option is turned off, the card continues to send data even when the receiver signals for it to stop or when the link is down.

In almost every application, flow control should be enabled. Even if the application must sustain maximum link throughput, it is better to drop the data at the sending source should the system experience a temporary overload condition. Some exotic conditions could apply where flow control is not desirable, but they require very careful system planning and should be confirmed with Curtiss-Wright Controls prior to architectural finalization. One possible exception is for applications that cannot use a duplex fiber-optic link, which means status information (link up and state of flow control) is not available from the remote node. In this circumstance, disable flow control to allow the transmitter to function without the receiver connected normally.

### 4.4.2 Loop Enable

The loop enable option allows the SL240X card to transmit the Serial FPDP received data stream again. Turning on the loop enable implies that this node is designated as a receiver in the current configuration.

### 4.4.3 Receiver/Transmitter Enable

The transmitter and receiver enable bits in the Link Control register turn off the transmit and receive Serial FPDP data streams, respectively. Neither affects the loop operation, so data is still retransmitted if the loop operation is enabled. This makes these options useful for record/playback systems where you wish to merely retransmit the data received without processing it. The receive enable is useful for disabling the Receive FIFO for the master in loop operation so that the data sent is not received.

### 4.4.4 CRC Generation/Checking

The CRC Generation/Checking option allows the SL240X card to detect data transmission errors. The card is not capable of correcting the errors—error correction is left to application level design.

A single bit controls both generation and checking. CRC should be used in almost all applications. It offers excellent coverage of data errors and has very little impact on link throughput for maximum frame sizes. The option of disabling CRC is only retained for compatibility with older third-part devices. Both nodes on the link (or all nodes in a loop configuration) should be set to a common CRC mode or the resulting mismatch will cause data errors and/or link errors.

### 4.4.5 Stop on Link Error or /SYNC

There are two DMA stop conditions available to the user—stop on link error and stop on /SYNC. The stop on link error stops the DMA engine from removing data from the Receive FIFO when there is a link error, such as the link going down. The stop on /SYNC option allows you to stop data from being received from the Receive FIFO when a /SYNC without /DVALID is received on the output.

### 4.4.6 Receive FIFO Threshold Interrupt

SL240X cards can be configured to interrupt the host when the FIFO passes a certain threshold, allowing for efficient PIO transactions out of the Receive FIFO. This is particularly important on data storage systems, where you do not want to remove data from the FIFO until you have a full block of data to transmit. One of four different thresholds (not empty, ¼ full, ½ full, ¾ full) can be selected through the control registers.

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# APPENDIX A

# SPECIFICATIONS

## TABLE OF CONTENTS

## A.1 Overview

This section shows the general card specifications of the FibreXtreme SL100X/SL240X VME and rehostable CMC FPDP cards and FPDP connector pin assignments.

**NOTE:** "Peak" current requirements represent a measured maximum for a typical card. Measurements were taken while the card was transmitting and receiving large buffers of data. "Average" current requirements represent a measured maximum for a card that is powered on but is not transmitting or receiving any data.

## A.2 NGSL VMER FPDP Card Specifications

Hardware Compatibility:.............................. ANSI/IEEE Std. 1014-1987
Physical Dimensions:.................................. 6.30 x 9.17 inches (160 x 233 mm)
Weight:........................................................ ≈ 0.5 lb.
Electrical Requirements:
SL100X ....................................................... +5 VDC, 1.8 Amps Peak, 1.6 Amps Average
SL240X ....................................................... +5 VDC, 2.2 Amps Peak, 2.0 Amps Average
Operating Temperature Range:..................... 0º to +50ºC
Mean Time Between Failure (MTBF)*:
SL100X, Short wavelength laser: ................ 199,174 hours (22.7 years)
SL100X, Long wavelength laser:................. 199,015 hours (22.7 years)
SL100X, Long-reach wavelength laser:........ 158,709 hours (18.1 years)
SL240X, Short wavelength laser: ................ 199,174 hours (22.7 years)
SL240X, Long wavelength laser:................. 199,015 hours (22.7 years)
SL240X, Long-reach wavelength laser:........ 156,844 hours (17.9 years)
VME Carrier without CMC card: ............... 402,589 hours (46.0 years)
Storage Temperature Range:........................ -40º to +85ºC
Maximum FPDP Node Separation: ............. 1 to 5 m (application dependent)

## A.3 FXSL VMER FPDP Card Specifications

Hardware Compatibility:.............................. ANSI/IEEE Std. 1014-1987
Physical Dimensions:.................................. 6.30 x 9.17 inches (160 x 233 mm)
Weight:........................................................ ≈ 0.5 lb.
Electrical Requirements:
SL100X ....................................................... +5 VDC, 1.7 Amps Peak, 1.5 Amps Average
SL240X ....................................................... +5 VDC, 2.1 Amps Peak, 1.8 Amps Average
Operating Temperature Range:..................... 0º to +50ºC
Mean Time Between Failure (MTBF)*:
SL100X, Short wavelength laser: ................ 178,635 hours (20.4 years)
SL100X, Long wavelength laser:................. 178,507 hours (20.4 years)
SL100X, Long-reach wavelength laser:........ 145,389 hours (16.6 years)
SL240X, Short wavelength laser: ................ 178,635 hours (20.4 years)
SL240X, Long wavelength laser:................. 178,507 hours (20.4 years)
SL240X, Long-reach wavelength laser:........ 143,822 hours (16.4 years)
VME Carrier without CMC card: ............... 326,669 hours (37.3 years)

Storage Temperature Range:......................... -40º to +85ºC
Maximum FPDP Node Separation: ............. 1 to 5 m (application dependent)

## A.4 Dual VMER FPDP Card Specifications

Hardware Compatibility:.............................. ANSI/IEEE Std. 1014-1987
Physical Dimensions:................................... 6.30 x 9.17 inches (160 x 233 mm)
Weight:......................................................... ≈ 0.5 lb.
Electrical Requirements:
SL100X ........................................................ +5 VDC, 3.1 Amps Peak, 2.9 Amps Average
SL240X ........................................................ +5 VDC, 4.1 Amps Peak, 3.9 Amps Average
Operating Temperature Range:..................... 0º to +50ºC
Mean Time Between Failure (MTBF)*:
SL100X, Short wavelength laser: ................ 111,943 hours (12.8 years)
SL100X, Long wavelength laser:................. 111,842 hours (12.8 years)
SL100X, Long-reach wavelength laser:........ 87,007 hours ( 9.9 years)
SL240X, Short wavelength laser: ................ 111,943 hours (12.8 years)
SL240X, Long wavelength laser:................. 111,842 hours (12.8 years)
SL240X, Long-reach wavelength laser:........ 85,887 hours ( 9.8 years)
VME Carrier without CMC cards:................ 259,100 hours (29.6 years)
Storage Temperature Range:......................... -40º to +85ºC
Maximum FPDP Node Separation: ............. 1 to 5 m (application dependent)

## A.5 Rehostable CMC FPDP Card Specifications

Hardware Compatibility:.............................. CMC IEEE P1386
Physical Dimensions:................................... 2.91 x 5.87 inches (74 x 149 mm)
Weight:......................................................... ≈ 0.25 lb.
Component Density:..................................... 90% (max)
Power Dissipation:
SL100X ........................................................ 4.6 W Peak, 3.9 W Average*
SL240X ........................................................ 5.6 W Peak, 4.6 W Average*
Electrical Requirements:
SL100X ........................................................ +3.3 VDC, 1.4 Amps Peak, 1.2 Amps Average
SL240X ........................................................ +3.3 VDC, 1.7 Amps Peak, 1.4 Amps Average
Operating Temperature Range:..................... 0° to +50° C
Mean Time Between Failure (MTBF)*:
SL100X, Short wavelength laser: ................ 394,195 hours (45.0 years)
SL100X, Long wavelength laser:................. 393,574 hours (44.9 years)
SL100X, Long-reach wavelength laser:........ 261,992 hours (29.9 years)
SL240X, Short wavelength laser: ................ 394,195 hours (45.0 years)
SL240X, Long wavelength laser:................. 393,574 hours (44.9 years)
SL240X, Long-reach wavelength laser:........ 256,949 hours (29.3 years)
Storage Temperature Range:......................... -40° to +85° C

*SL100X/SL240X CMC cards do not require 5 VDC. However, Curtiss-Wright Controls recommends supplying 5 VDC to P4 and P6 connectors.

# A.6 PCI FibreXtreme Carrier Card Specifications

Physical Dimensions: .................................... 174.6 x 106.7 mm
Weight: .......................................................... ≈ 0.40 lbs
Operating Voltage: ........................................ 4.75 V to 5.25 V
Electrical Requirements:
SL100X ...................................................... +5 VDC, TBD Amps Peak, TBD Amps Average
SL240X ...................................................... +5 VDC, TBD Amps Peak, TBD Amps Average
Operating Temperature Range: ..................... +0° to +50°C
Mean Time Between Failure (MTBF)*:
SL100X, Short wavelength laser: ................ 197,309 hours (22.5 years)
SL100X, Long wavelength laser: ................. 197,153 hours (22.5 years)
SL100X, Long-reach wavelength laser: ........ 157,523 hours (18.0 years)
SL240X, Short wavelength laser: ................ 197,309 hours (22.5 years)
SL240X, Long wavelength laser: ................. 197,153 hours (22.5 years)
SL240X, Long-reach wavelength laser: ........ 155,685 hours (17.8 years)
PCI FibreXtreme Carrier without CMC card: .................................... 395,042 hours (45.1 years)
Storage Temperature Range: ......................... -40° to +85°C
Maximum FPDP Node Separation: .............. 1 to 5 m (application dependent)

*The MTBF numbers are based on calculations using MIL-HDBK-217F, Appendix A; and Bellcore 332, Issue 6, for a ground-benign environment.

# A.7 Ruggedized CMC Environmental Specifications

The SL100X/SL240X products are offered at three different ruggedization levels. These levels are Standard, Rugged Level 1, and Rugged Level 2. Standard level operation specifications are defined in Sections A.1 of Appendix A. The specifications for Rugged Level 1 and Rugged Level 2 are defined in the following sections.

Current SL100X/SL240X standard and ruggedized products are listed in Appendix E.

## A.7.1 Rugged Level 1

Temperature Range:

Operating .................................... -10° to +70° C

Storage ........................................ -40° to +85°C

Humidity Range:

Operating .................................... 0% to 95% (noncondensing)

Storage ........................................ 0% to 95% (noncondensing)

Altitude:

Operating .................................... 25,000 ft steady; rapid decompression to 40,000 ft

Storage ........................................ 25,000 ft

Vibration:

Sine............................................... 10 g peak<br>10 Hz to 2 kHz

Random ....................................... .04 $g^2$/Hz<br>10 Hz to 2 kHz<br>-6 dB/octave<br>1 kHz to 2 kHz

Shock.................................................. 20 g peak<br>½ sine wave<br>11 ms duration

Airflow ................................................ 300 LFM

Conformal Coating............................. Acrylic HumiSeal 1B31*

* Ruggedized cards are coated with HumiSeal 1B31 acrylic conformal coating. This coating is qualified to MIL-I-46058C, Type AR. More detailed information on the coating can be found at the HumiSeal website http://www.humiseal.com/.

### A.7.2 Rugged Level 2

Temperature Range:

| | |
|---|---|
| Operating | -40° to +85° C |
| Storage | -40° to +85°C |

Humidity Range:

| | |
|---|---|
| Operating | 0% to 95% (noncondensing) |
| Storage | 0% to 95% (noncondensing) |

Altitude:

| | |
|---|---|
| Operating | 25,000 ft steady; rapid decompression to 40,000 ft |
| Storage | 25,000 ft |

Vibration:

| | |
|---|---|
| Sine | 10 g peak<br>10 Hz to 2 kHz |
| Random | .1 $g^2$/Hz<br>10 Hz to 2 kHz<br>-6 dB/octave<br>1 kHz to 2 kHz |

| | |
|---|---|
| Shock | 30 g peak<br>½ sine wave<br>11 ms duration |
| Airflow | 300 LFM** |
| Conformal Coating | Acrylic HumiSeal 1B31* |
| FPDP Ribbon Cable | The 80-pin FPDP ribbon cable must **not** exceed 12 inches for Rugged Level 2 environments |

* Ruggedized cards are coated with HumiSeal 1B31 acrylic conformal coating. This coating is qualified to MIL-I-46058C, Type AR. More detailed information on the coating can be found at the HumiSeal website http://www.humiseal.com/.

** For SL240X Longwave: 600 LFM

# A.8 FPDP Connector Pin Assignments

The FPDP connector pin assignments are shown in Table A-1. These assignments are the normal (non-inverted) connector pin assignment for the FPDP interface described in Table 2 of the *Front Panel Data Port Specifications*, ANSI/VITA 17-1998. Cable conductor numbers are shown in parenthesis. Pin 1 is adjacent to the connector index mark.

**Table A-1 FPDP Connector Pin Assignments**

| Pin | Row A | Row B | Row C | Row D |
|---|---|---|---|---|
| 1 | GND (1) | STROBE (2) | GND (3) | GND (4) |
| 2 | GND (5) | GND (6) | /NRDY (7) | GND (8) |
| 3 | /DIR (9) | GND (10) | RESERVED (11) | GND (12) |
| 4 | /SUSPEND (13) | GND (14) | GND (15) | GND (16) |
| 5 | PIO2 (17) | GND (18) | PIO1 (19) | GND (20) |
| 6 | RESERVED (21) | GND (22) | RESERVED (23) | GND (24) |
| 7 | PSTROBE (25) | GND (26) | /PSTROBE (27) | GND (28) |
| 8 | /SYNC (29) | GND (30) | /DVALID (31) | GND (32) |
| 9 | D31 (33) | D30 (34) | GND (35) | D29 (36) |
| 10 | D28 (37) | GND (38) | D27 (39) | D26 (40) |
| 11 | GND (41) | D25 (42) | D24 (43) | GND (44) |
| 12 | D23 (45) | D22 (46) | GND (47) | D21 (48) |
| 13 | D20 (49) | GND (50) | D19 (51) | D18 (52) |
| 14 | GND (53) | D17 (54) | D16 (55) | GND (56) |
| 15 | D15 (57) | D14 (58) | GND (59) | D13 (60) |
| 16 | D12 (61) | GND (62) | D11 (63) | D10 (64) |
| 17 | GND (65) | D09 (66) | D08 (67) | GND (68) |
| 18 | D07 (69) | D06 (70) | GND (71) | D05 (72) |
| 19 | D04 (73) | GND (74) | D03 (75) | D02 (76) |
| 20 | GND (77) | D01 (78) | D00 (79) | GND (80) |

# A.9 RS-232 Pin-out for NGSL VME Carrier

Figure A-1 shows the pin-out of the RS-232 connector on the NGSL VME card.

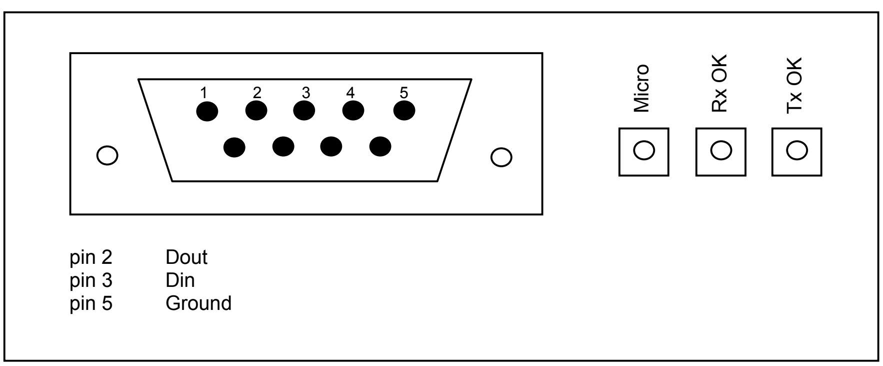


**Figure A-1 RS-232 Connector Pins for NGSL VME Carrier**

# A.10 RS-232 Pin-out on PCI FibreXtreme Carrier

The PCI FibreXtreme Carrier card's RS-232 port uses an RJ-45 connector. Pin assignments are shown in Table A-2.

**Table A-2 PCI FibreXtreme Carrier Card's RS-232 Pin Assignments**

| Pin | Signal | Direction |
|---|---|---|
| 1 | DCD | Not Connected |
| 2 | RTS | Not Connected |
| 3 | GND | |
| 4 | TxD | Out |
| 5 | RxD | In |
| 6 | GND | |
| 7 | CTS | Not Connected |
| 8 | DTR | Not Connected |

A 14-foot RJ-45 straight cable and RJ-45 Female to DB-9 Female Adapter are provided with each PCI FibreXtreme Carrier card. These items can be used to connect the PCI FibreXtreme Carrier card's RJ-45 connector to a personal computer's DB-9 serial port.

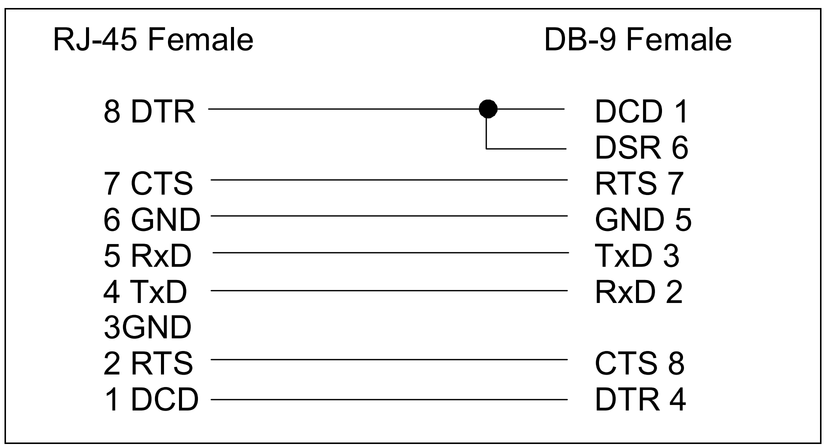


**Figure A-2 RJ-45 Female to DB-9 Female Adapter**

# A.11 Media Interface Specifications

## A.11.1 SL100X Fiber-Optic Media Interface Specifications

Connector:........................................................Duplex LC

**850 nm:**

Media:..........................................50 µm or 62.5 µm multi-mode fiber
Fibre Channel Formats: ................100-M5-SN-I (1 Gbps, 50 µm fiber)
100-M6-SN-I (1 Gbps, 62.5 µm fiber)
Maximum Fiber Length:...............500 meters with 50 µm fiber
300 meters with 62.5 µm fiber
Transmit Wavelength: ..................830 to 860 nm
Transmit Power: ...........................-10 to -4 dbm
Receive Wavelength:....................770 to 860 nm
Receive Sensitivity: ......................-16 to 0 dbm

**1300 nm:**

Media:..........................................9 µm single-mode fiber
Fibre Channel Formats: ................100-SM-LL-I (1 Gbps, single-mode fiber, intermediate distance)
100-SM-LC-L (1 Gbps, single-mode fiber, low cost long distance)
Maximum Fiber Length:...............10 km
Transmit Wavelength: ..................1285 to 1330 nm
Transmit Power: ...........................-9 to –3 dBm
Receive Wavelength:....................1100 to 1600 nm
Receive Sensitivity: ......................-20 to –3 dBm

**1550 nm:**

Media:..........................................8.3/125 µm single-mode fiber
Maximum Fiber Length:...............51 km
Transmit Wavelength: ..................1535 to 1565 nm
Transmit Power: ...........................2 to 5 dBm
Receive Wavelength:....................1535 to 1565 nm
Receive Sensitivity: ......................-26 to –3 dBm

## A.11.2 SL240X Fiber-Optic Media Interface Specifications

Connector: ..........................................Duplex LC

**850 nm:**

Media:..........................................50 µm or 62.5 µm multi-mode fiber
Maximum Fiber Length:...............250 m with 50 µm fiber
125 m with 62.5 µm fiber
Transmit Wavelength: ..................830 to 860 nm
Transmit Power: ...........................-8 to -4 dbm
Receive Wavelength:....................770 to 860 nm
Receive Sensitivity: ......................-12 to 0 dbm

**1300 nm:**

Media:........................................9 µm single-mode fiber
Maximum Fiber Length:...............2 km
Transmit Wavelength: ..................1285 to 1335 nm
Transmit Power: ...........................-7.5 to –3 dBm
Receive Wavelength:....................1270 to 1355 nm
Receive Sensitivity: ......................-18 to –3 dBm

**1550 nm:**

Media:........................................8.3/125 µm single-mode fiber
Maximum Fiber Length:...............26 km (max), 10 km (min)
Transmit Wavelength: ..................1500 to 1580 nm
Transmit Power: ...........................-2 to 3 dBm
Receive Wavelength:....................1500 to 1580 nm
Receive Sensitivity: ......................-30 to –6 dBm

## A.11.3 SL100X HSSDC2 Copper Media Interface

Cable:...............................................................150 Ohm shielded, Quad
Maximum Cable Length: .................................Up to 30 meters with equalized cable
Compatibility: ..................................................1 Gbps, shielded, balanced cable
Connector:........................................................HSSDC2 (Fibre Channel "Style-2")
Data Rate: ........................................................1.0625 Gbps

## A.11.4 SL240X HSSDC2 Copper Media Interface

Cable:...............................................................100 Ohm shielded, Quad
Maximum Cable Length: .................................Up to 10 meters with equalized cable
Compatibility: ..................................................2.5 Gbps, shielded, balanced cable
Connector:........................................................HSSDC2 (Infiniband)
Data Rate: ........................................................2.5 Gbps

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# APPENDIX B

# REGISTER SET

## TABLE OF CONTENTS

# B.1 Overview

The FibreXtreme NGSL VMER, PCI FibreXtreme Carrier and SL240X rehostable CMC FPDP cards are designed so configuring the cards is as simple as possible. With minimal configuration, an SL240X FPDP card can transfer data between the link interface and the FPDP interface. This section describes the register set bit definitions.

These definitions apply to the Access column shown in the following tables:

- R/W – Readable/Writable bit.
- R/WOC – Readable/Write One Clear bit.
- W – Write-only bit.
- R – Read-only bit.
- None – Do not read or write to this bit.

## B.1.1 Interrupt CSR (INT_CSR) – Offset 0x00

**NOTE:** Do not write a '1' to bit 20, Enable Link Error Interrupt, of the Interrupt CSR register. With the current revision of firmware, this resets the microcontroller on the NGSL VMER card and the PCI FibreXtreme Carrier card, and causes the active register configuration to be reloaded from the EEPROM. This may be fixed in a future firmware revision and these bits will work as described in this manual.

| Bit | Description | Access | Reset Value |
|---|---|---|---|
| 3 to 0 | Reserved | None | 0 |
| 4 | Link Error Interrupt – A '1' indicates active, a '0' indicates not active. Write '1' to clear. | R/WOC | 0 |
| 5 | FPDP Interrupt – A '1' indicates active, a '0' indicates not active. Write '1' to clear. | R/WOC | 0 |
| 6 | Threshold Interrupt – A '1' indicates active, a '0' indicates not active. Write '1' to clear. | R/WOC | 0 |
| 7 | Reserved | None | 0 |
| 19 to 8 | Reserved | None | 0 |
| 20 | Enable Link Error Interrupt – Set to '1' to enable interrupts, set to '0' to disable interrupts. | R/W | 0 |
| 21 | Enable FPDP Interrupt – Set to '1' to enable interrupts, set to '0' to disable interrupts | R/W | 0 |
| 22 | Enable Threshold Interrupt – Set to '1' to enable interrupts, set to '0' to disable interrupts | R/W | 0 |
| 23 | Reserved | None | 0 |
| 31 to 24 | Reserved | None | 0 |

## B.1.2 Board CSR (BRD_CSR) – Offset 0x04

| Bit | Description | Access | Reset Value |
|---|---|---|---|
| 0 | Reserved | None | 0 |
| 1 | Reset – Write ‘1’ to reset the card. Writing ‘0’ has no affect. | W | 0 |
| 2 | Reserved | None | 0 |
| 3 | JTAG TCK# – Controls the TCK# line on the JTAG port. | R/W | 0 |
| 4 | JTAG TMS# – Controls the TMS# line on the JTAG port. | R/W | 0 |
| 5 | JTAG TDO# – Controls the TDO# line on the JTAG port. | R/W | 0 |
| 6 | JTAG TDI# - TDI# line from the JTAG port. | R | 1 |
| 7 | JTAG Enable – Enable the JTAG port on the FPGA. | R/W | 0 |
| 14 to 8 | Revision ID – Revision level of the card controller. | R | See desc. |
| 15 | SL100X/SL240X – A ‘1’ indicates this is an SL240X card, a ‘0’ indicates this is an SL100X card. | R | See desc. |
| 23 to 16 | Extended Revision ID – These bits are used to identify intermediate or special firmware revisions. Bit 23 = ‘0’ indicates the Copy Master Mode bit in the Link Control register is ‘0’ after a card reset. Bit 23 = ‘1’ indicates the Copy Master Mode bit in the Link Control register is ‘1’ after a card reset. | R | See desc. |
| 31 to 24 | Reserved | None | 0 |

### B.1.3 Link Control (LINK_CTL) – Offset 0x08

| Bit | Description | Access | Reset Value |
|---|---|---|---|
| 0 | Allow Remote Transmitter – Set to ‘1’ to enable the remote transmitter to send link data. Set to ‘0’ to request the remote transmitter to stop sending link data. This flow control request will be ignored if the remote end is configured to ignore flow control. This signal is typically set to a '1' for most applications. It exists to provide a mechanism to disable the remote transmitter by forcing the transmitted flow control to a STOP state. | R/W | 0 |
| 1 | CRC Enable – Set to ‘1’ to enable the CRC checking/generation of link data. Set to ‘0’ to disable CRC checking/generation.<br><br>**NOTE**: CRC should be used in almost all applications. It offers excellent coverage of data errors and has very little impact on link throughput for maximum frame sizes. The option of disabling CRC is only retained for compatibility with older third-part devices. Both nodes on the link (or all nodes in a loop configuration) should be set to a common CRC mode or the resulting mismatch will cause data errors and/or link errors. | R/W | 0 |
| 2 | Ignore Flow Control – Set to ‘1’ to ignore flow control from the remote end and continue transmitting when the link is down. Set to ‘0’ to stop transmission when the link goes down or the remote end is sending a STOP ordered set back.<br><br>**NOTE:** In almost every application, flow control should be enabled. Even if the application must sustain maximum link throughput, it is better to drop the data at the sending source should the system experience a temporary overload condition. Some exotic conditions could apply where flow control is not desirable, but they require very careful system planning and should be confirmed with Systran prior to architectural finalization. One possible exception is for applications that cannot utilize a duplex fiber-optic link, which means status information (link up and state of flow control) is not available from the remote node. In this circumstance, flow control should be disabled to allow the transmitter to function without the receiver connected normally. | R/W | 0 |
| 3 | Convert SYNC – For all FPDP operations, set to ‘0’. When ‘1,’ a SYNC without DVALID is appended after every SYNC with DVALID from the link. | R/W | 0 |
| 5 to 4 | Reserved | None | 0 |
| 6 | SYNC as D0 – If ‘1’ then bit 0 of the data stream is used as /SYNC in the outgoing and incoming data stream. If ‘0’ then bit 0 is not used as /SYNC. | R/W | 0 |
| 7 | Reserved | None | 0 |

| Bit | Description | Access | Reset Value |
|---|---|---|---|
| 8 | Disable Receiver – A ‘1’ disables the link interface from placing data in the Receive FIFO. When set to ‘1,’ this signal also prevents the modification of the DIR, NRDY, and SUSPEND flags in the retransmitted data stream if Loop (Copy) Mode is enabled. Set to a '0' for normal operation, where received link data will be placed into the Receive FIFO. When the receiver is enabled and Loop (or Copy) Mode is enabled, the status of the SUSPEND request will be updated as appropriate in the retransmitted data stream. If Loop (or Copy) Mode is selected (LWRAP = ‘1’), the values of DIR and NRDY are used as follows: if the receive interface is enabled (Disable Receiver = ‘0’), the values transmitted are the received link values ORed with the host-interface values; otherwise, the values are retransmitted according to their received link values. | R/W | 0 |
| 9 | Disable Transmitter – A ‘1’ disables the link interface from removing data from the Transmit FIFO. A ‘0’ indicates normal transmit operation. Set this bit to ‘1’ when loop mode is enabled via the LWRAP bit. | R/W | 0 |
| 10 | EWRAP – This signal controls loopback operation of the user interface’s data stream. A ‘1’ indicates the outgoing data stream is electronically wrapped into the incoming data stream at the serializer/deserializer. A ‘0’ indicates non-wrapped data flow to and from the link interface. This is typically used for testing purposes. | R/W | 0 |
| 11 | LWRAP – This signal controls the loopback operation of the link interface’s data stream and implements the Copy Mode described in the ANSI/VITA 17.1 Serial FPDP specification. Set to a ‘1’ to enable loop mode, whereby the incoming data stream is electronic wrapped into the outgoing data stream internally to the FPGA. Set to a ‘0’ for normal operation utilizing a point-to-point topology. The configuration of the nodes is intended to be static.<br><br>**NOTE**: When changing loop topologies, the resulting change in the way link data is used may cause bad data or error conditions on the receiving nodes. It will be necessary to deploy a mechanism in the system to clean up these conditions after reconfiguration. | R/W | 0 |
| 12 | Copy Master Mode - Set to '1' on the loop initiator device in any topology with more than two cards (for example, loop or chained). The loop initiator will then place four IDLE ordered sets or three IDLE ordered sets plus a SWDV ordered set per fiber frame. When '0', the loop initiator will place one IDLE ordered set or one SWDV ordered set per fiber frame. All receivers in the loop or chain should have this bit set to '0.' Do not set this bit to '1' on any device in a point-to-point topology (that is, two cards) because throughput will decrease by a factor related to frame size. | R/W | 0 |

| Bit | Description | Access | Reset Value |
|---|---|---|---|
| 15 to 13 | Reserved | None | 0 |
| 16 | Reset SR – Write ‘1’ to clear any latched status information from the registers. Writing ‘0’ has no effect. | W | 0 |
| 17 | Clear SYNC without DVALID – Write ‘1’ to release a FIFO stopped on SYNC without DVALID. Writing ‘0’ has no effect. | W | 0 |
| 18 | Reserved | None | 0 |
| 19 | Erase TX FIFO – Set to a ‘1’ to reset the Transmit FIFO. This bit is included for testing and special scenarios and, as such, should not be used in the majority of applications. A hardware-level reset (e.g., the /RESET pin on the CMC connectors) performs a reset of the entire SL100X/SL240X FPGA logic, including the FIFOs and is the only reset that should normally be used. Resetting the Transmit FIFO or Receive FIFO independently from the SL100X/SL240X FPGA logic can cause undesirable effects because each 32-bit Serial FPDP data word occupies two entries in the respective FIFO and the link and host are independently filling and draining these FIFOs. Applying the FIFO resets without applying special precaution can result in a misalignment of data in these FIFOs. | W | 0 |
| 20 | Erase RX FIFO – Set to a ‘1’ to reset the Receive FIFO. This bit is included for testing and special scenarios and, as such, should not be used in the majority of applications. A hardware-level reset (e.g., the /RESET pin on the CMC connectors) performs a reset of the entire SL100X/SL240X FPGA logic, including the FIFOs and is the only reset that should normally be used. Resetting the Transmit FIFO or Receive FIFO independently from the SL100X/SL240X FPGA logic can cause undesirable effects because each 32-bit Serial FPDP data word occupies two entries in the respective FIFO and the link and host are independently filling and draining these FIFOs. Applying the FIFO resets without applying special precaution can result in a misalignment of data in these FIFOs. | W | 0 |
| 31 to 21 | Reserved | None | 0 |

## B.1.4 Link Status (LINK_STAT) – Offset 0x0C

| Bit | Description | Access | Reset Value |
|---|---|---|---|
| 7 to 0 | 8B/10B Errors – This is an 8-bit counter counting the current number of 8B/10B decoding errors discovered. These bits are cleared through 'Reset SR' in LINK_CTL. | R | 0 |
| 8 | Link Down – A '1' indicates the link has gone down at some point since the last 'Reset SR'. A '0' indicates the link has not gone down since the last 'Reset SR'. This bit is cleared through 'Reset SR' in LINK_CTL. | R | 0 |
| 9 | Link Up – This bit reflects the current status of the link. A '1' indicates the link is currently up. A '0' indicates the link is currently down. Note that this bit is not latched like the 'Link Down' bit. | R | 0 |
| 10 | Synchronization Error – A '1' indicates the card has corrected a synchronization error on the incoming data stream. A '0' indicates the card has not corrected a synchronization error on the incoming data stream. This bit is cleared through 'Reset SR' in LINK_CTL. | R | 0 |
| 11 | Checksum Error – A '1' indicates the card has detected a checksum error on the incoming data stream. A '0' indicates the card has not detected a checksum error on the incoming data stream. This bit is cleared through 'Reset SR' in LINK_CTL. | R | 0 |
| 12 | RX FIFO Overflow - A '1' indicates the Receive FIFO has overflowed. A '0' indicates the Receive FIFO has not overflowed. This bit is cleared through 'Reset SR' in LINK_CTL. | R | 0 |
| 13 | TX FIFO Overflow – A '1' indicates the Transmit FIFO has overflowed. A '0' indicates the Transmit FIFO has not overflowed. This bit is cleared through 'Reset SR' in LINK_CTL. | R | 0 |
| 31 to 14 | Reserved | None | 0 |

## B.1.5 FPDP Flags (FPDP_FLGS) – Offset 0x10

| Field | Description | Access | Reset Value |
|---|---|---|---|
| 0 | Send SYNC – Write ‘1’ to send SYNC without DVALID. Writing ‘0’ has no effect. | W | 0 |
| 1 | PIO1 Out – State of the PIO1 line sent across the link. | R/W | 0 |
| 2 | PIO2 Out – State of the PIO2 line sent across the link. | R/W | 0 |
| 3 | DIR Out – State of the DIR line sent across the link. | R/W | 0 |
| 4 | NRDY Out – State of the NRDY line sent across the link. | R/W | 0 |
| 7 to 5 | Reserved. | None | 0 |
| 8 | SYNC Received – A ‘1’ indicates a SYNC without DVALID has been received. Cleared through ‘Clear SYNC’ in the LINK_CTL register. A ‘0’ indicates no SYNC has been received. | R | 0 |
| 9 | PIO1 In – State of the PIO1 line received from the link. | R | 0 |
| 10 | PIO2 In - State of the PIO2 line received from the link. | R | 0 |
| 11 | DIR In – State of the DIR line received from the link. | R | 0 |
| 12 | NRDY In – State of the NRDY line received from the link. | R | 0 |
| 13 | Rcvd STOP – Indicates that a STOP flow control primitive was received from the remote receiver. This bit is read only and will be dynamically changing. | R | 0 |
| 14 | Sent STOP – Indicates that a STOP flow control primitive was sent to the remote transmitter. This bit is read only and will be dynamically changing. | R | 0 |
| 15 | FIFO Overflow – Indicates that the Remote Transmitter FIFO Overflow bit was set in the received Status End of Frame primitive (EOFa or EOFn Fibre Channel ordered sets). This indicates that the remote node detected an overflow condition in its transmit FIFO. This bit is read only and will be dynamically changing. | R | 0 |
| 16 | Latched version of status bit 13. This bit is cleared by writing a ‘0’ to it. It should be noted that this bit might not appear to be cleared immediately after writing a ‘0’ to it. This is because another STOP may have been received immediately after clearing it. | R/W | 0 |
| 17 | Latched version of status bit 14. This bit is cleared by writing a ‘0’ to it. It should be noted that this bit might not appear to be cleared immediately after writing a ‘0’ to it. This is because another STOP may have been sent immediately after clearing it. | R/W | 0 |
| 18 | Latched version of status bit 15. This bit is cleared by writing a ‘0’ to it. It should be noted that this bit might not appear to be cleared immediately after writing a ‘0’ to it. This is because another FIFO Overflow may have been received immediately after clearing it. | R/W | 0 |
| 31 to 19 | Reserved. | None | 0 |

## B.1.6 Receive FIFO Threshold– Offset 0x14

| Field | Description | Access | Reset Value |
|---|---|---|---|
| 19 to 0 | Number of 32-bit words in the Receive FIFO. | R | 0 |
| 20 | Rearm Threshold Interrupt – Write ‘1’ to rearm the threshold register. Writing ‘0’ has no effect. | W | 0 |
| 21 | Data present – A ‘1’ indicates data is present on the output. A ‘0’ indicates no data is present. | R | 0 |
| 29 to 22 | Reserved. | None | 0 |
| 31 to 30 | Interrupt Threshold – Selects one of the following levels of the Receive FIFO to interrupt on:<br><br>00 – Interrupt threshold set to Receive FIFO Not Empty<br>01 – Interrupt threshold set to Receive FIFO ¼ Full<br>10 – Interrupt threshold set to Receive FIFO ½ Full<br>11 – Interrupt threshold set to Receive FIFO ¾ Full | R/W | 0 |

## B.1.7 Laser Transmitter Control – Offset 0x18

| Field | Description | Access | Reset Value |
|---|---|---|---|
| 25 to 0 | Reserved. | None | 0 |
| 26 | Manual laser shutdown – Set to ‘1’ to shutdown the laser. Set to ‘0’ for normal operation. | R/W | 0 |
| 31 to 27 | Reserved. | None | 0 |

# APPENDIX C

# CARRIER/CMC CONFIGURATION

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# FIGURES



# TABLES

## C.1 Overview

The FibreXtreme carrier cards and SL240X rehostable CMC FPDP cards are easy to configure. With minimal configuration, an SL240X FPDP card can transfer data between the link interface and the FPDP interface. This appendix describes how to configure the VME and rehostable CMC cards.

The configuration signals are routed from the FibreXtreme FPDP card to the FPDP Configuration Interface connector (P3) on the SL240X rehostable CMC card. If a FibreXtreme FPDP card is not used, the custom carrier must send these configuration signals correctly to the FPDP Configuration Interface connector (P3) on the SL240X rehostable CMC card. See Appendix G, Rehostable CMC FPDP Interface, for details on the CMC card's interface connectors.

**NOTE**: An NGSL VMER or PCI FibreXtreme Carrier card is required to configure an SL240X CMC card's registers.

**NOTE**: No register configuration is required if an SL240X rehostable CMC card is installed on a FXSL VMER card or a Dual VMER card because these three VME cards are switch configurable. The SL240X CMC card's registers are not used in this case.

**NOTE**: CRC should be used in almost all applications. It offers excellent coverage of data errors and has very little impact on link throughput for maximum frame sizes. The option of disabling CRC is only retained for compatibility with older third-part devices. Both nodes on the link (or all nodes in a loop configuration) should be set to a common CRC mode or the resulting mismatch will cause data errors and/or link errors.

**NOTE**: In almost every application, flow control should be enabled. Even if the application must sustain maximum link throughput, it is better to drop the data at the sending source should the system experience a temporary overload condition. Some exotic conditions could apply where flow control is not desirable, but they require very careful system planning and should be confirmed with Systran prior to architectural finalization. One possible exception is for applications that cannot utilize a duplex fiber optic link, which means status information (link up and state of flow control) is not available from the remote node. In this circumstance, flow control should be disabled to allow the transmitter to function without the receiver connected normally.

# C.2 NGSL VMER and PCI FibreXtreme Carrier Card Configuration Setup

To configure the cards, set up the environment shown in Figure C-1 or Figure C-2. Connect an RS-232 cable from an RS-232-capable terminal to the DB-9 connector on the NGSL VMER card or to the RJ-45 connector on the PCI FibreXtreme Carrier card. Using a VT-100 terminal emulation program, configure the COM port with these settings: 9600 Baud, 8 data bits, 1 stop bit, no parity.

The fiber-optic loopback cable connected to the rehostable CMC card's laser transceiver is optional. However, it is nice because it allows the Link Up LED on the CMC card to turn on after the CMC card's configuration process. This is the only visible indicator that the CMC card is configured.

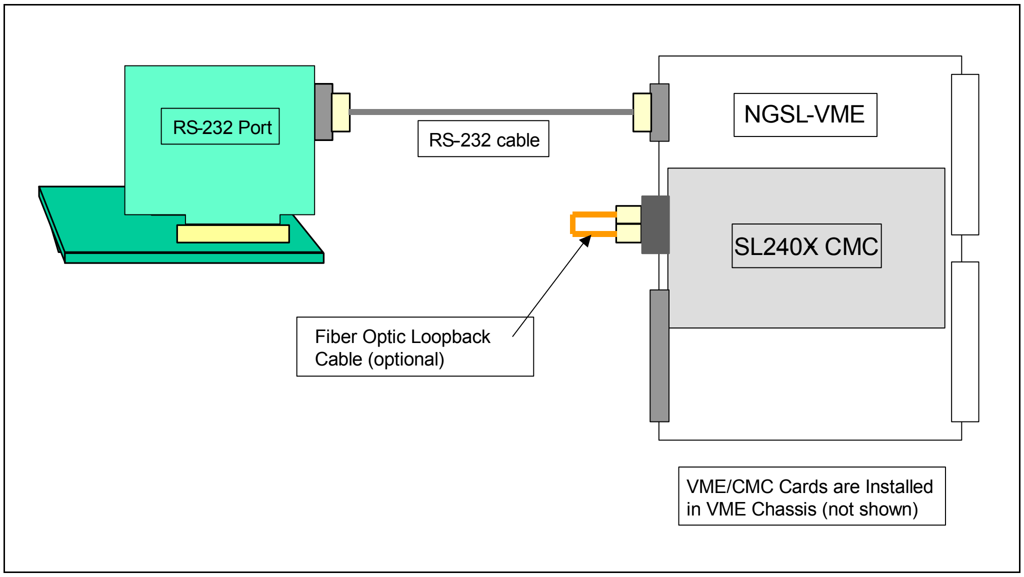


**Figure C-1 NGSL VME card Configuration Environment**

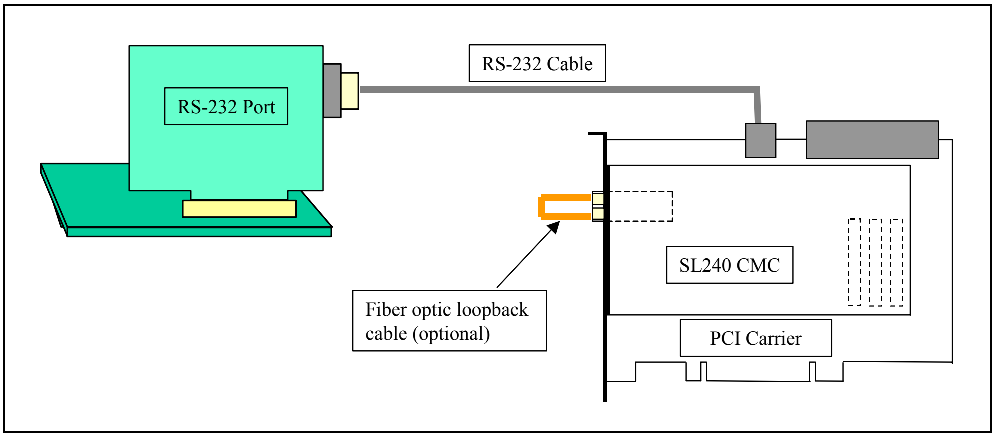


**Figure C-2 PCI FibreXtreme Carrier Card Configuration Environment**

# C.3 NGSL VMER and PCI FibreXtreme Carrier Card Register Offsets

The carrier card registers bits are defined below. All register bits shown are readable and writable. The carrier card registers occupy offsets 0x0 to 0x3 on the carrier card.

## C.3.1 PIO and Carrier Configuration – Offset 0x0

| Bit | Description | Reset Value |
|---|---|---|
| 0 | **RX Clock Select** – Set to ‘1’ to use the TTL FPDP strobe signal. Set to ‘0’ to use the PECL FPDP strobe signal. | 0 |
| 1 | Reserved. Always drive as ‘0’. | 0 |
| 2 | **Master** – Set to ‘1’ if this card is an FPDP-TM or an FPDP-RM. Set to ‘0’ if this card is an FPDP-R. | 0 |
| 3 | **Transmit** – Set to ‘1’ if this card is an FPDP-TM. Set to ‘0’ if this card is an FPDP-RM or an FPDP-R. | 0 |
| 4 | **PIO1 Reversed** – If ‘0’, PIO1 maps to PIO1_IN or PIO1_OUT, depending on ‘PIO1 Direction.’ If ‘1’, PIO1 maps to PIO2_IN or PIO2_OUT, depending on ‘PIO1 Direction.’ | 0 |
| 5 | **PIO2 Reversed** – If ‘0’, PIO2 maps to PIO2_IN or PIO2_OUT, depending on ‘PIO2 Direction.’ If ‘1’, PIO2 maps to PIO1_IN or PIO1_OUT, depending on ‘PIO2 Direction.’ | 0 |
| 6 | **PIO1 Direction** – This bit selects the direction of PIO1. Set to ‘1’ if PIO1 is an output. Set to ‘0’ if PIO1 is an input. | 0 |
| 7 | **PIO2 Direction** – This bit selects the direction of PIO2. Set to ‘1’ if PIO2 is an output. Set to ‘0’ if PIO2 is an input. | 0 |

## C.3.2 Reserved Register – Offset 0x1

| Bit | Description | Reset Value |
|---|---|---|
| 7 to 0 | Reserved | 0 |

## C.3.3 CMC Configuration – Offset 0x2

<table>
<tr><th>Bit</th><th>Description</th><th>Reset Value</th></tr>
<tr><td>0</td><td>CRC Enable – If ‘Microcontroller Present’ is ‘0’, this value is ignored and the CMC register value is used. Set to ‘1’ to enable CRC checking/generation of link data. Set to ‘0’ to disable CRC checking/generation.</td><td>0</td></tr>
<tr><td>1</td><td>Ignore Flow Control – If ‘Microcontroller Present’ is ‘0’, this value is ignored and the CMC register value is used. Set to ‘1’ to ignore flow control from the remote end and continue transmitting when the link is down. Set to ‘0’ to stop transmission when the link goes down or the remote end on the link interface is sending a STOP ordered set back.</td><td>0</td></tr>
<tr><td>2</td><td>Convert SYNC – If ‘Microcontroller Present’ is ‘0’, this value is ignored and the CMC register value is used. For all FPDP operations, set to ‘0’. When set to ‘1’, a SYNC without DVALID is appended after every SYNC with DVALID from the link.</td><td>0</td></tr>
<tr><td>4 to 3</td><td>FPDP-TM Clock Configuration. Controls the FPDP transmitter clock frequency. The FPDP transmitter clock is the reference clock (53.125 MHz or 125 MHz) divided by 2, 4, 3, or 6. The clock divisions available for standard cards are:
<table>
<tr><th>CLK_CFG0<br>Bit 4</th><th>CLK_CFG1<br>Bit 3</th><th>SL100X<br>(53.125 MHz)</th><th>SL240X<br>(125 MHz)</th></tr>
<tr><td>0</td><td>0</td><td>26.5625 MHz</td><td>62.5 MHz</td></tr>
<tr><td>0</td><td>1</td><td>13.2813 MHz</td><td>31.25 MHz</td></tr>
<tr><td>1</td><td>0</td><td>17.7083 MHz</td><td>41.6667 MHz</td></tr>
<tr><td>1</td><td>1</td><td>8.8542 MHz</td><td>20.8333 MHz</td></tr>
</table></td><td>0</td></tr>
<tr><td>5</td><td>Microcontroller Present – Set to ‘0’ to use the configuration signals from the microcontroller interface. Set to ‘1’ to use the configuration signals from the P3 connector. For the NGSL VMER and PCI FibreXtreme Carrier cards, the P3 connector signals are driven by this register when this bit is set to ‘1’.</td><td>0</td></tr>
<tr><td>6</td><td>Enable CMC – Set to ‘1’ to enable the CMC card. A ‘0’ holds the CMC card in reset.</td><td>0</td></tr>
<tr><td>7</td><td>Reserved</td><td>0</td></tr>
</table>

## C.3.4 Reserved Register – Offset 0x3

| Bit | Description | Reset Value |
|---|---|---|
| 7 to 0 | Reserved | 0 |

## C.4 CMC Register Offsets

The CMC registers are described in Appendix B, Register Set.

## C.5 NGSL VMER and PCI FibreXtreme Carrier Configuration Commands

The configuration software runs on the microcontroller on the carrier card. This software is accessed through a terminal emulation program. Eight configuration commands are available. These commands are listed below and are explained in the following sections.

- ac
- ec <configuration>
- gc <configuration>
- lc <configuration>
- sc <configuration>
- br <register set> <address>
- bw <register set> <address>
- help

Four unique CARRIER/CMC register configurations can be stored in the EEPROM on the NGSL VMER or PCI FibreXtreme Carrier FPDP card. The different configurations are identified as 0, 1, 2, or 3. The EEPROM is shipped without any default configurations.

**NOTE**: All numbers entered or displayed using this configuration software are hexadecimal.

**NOTE:** The configuration software is identical on both the NGSL VMER and PCI carrier cards.

### C.5.1 Active Configuration (ac)

This command displays the number of the current active configuration. The active configuration is the configuration loaded from the EEPROM every time the carrier card is powered on.

### C.5.2 Edit Configuration (ec <configuration>)

This command allows a configuration stored in the EEPROM to be edited. The current value of a register is shown before the colon. A new register value may be entered after the colon followed by pressing the ENTER key. If the current register value is already correct, press the ENTER key by itself. This will keep the existing value for that register. Go through all 11 registers in this manner.

**NOTE**: Each time a register value is changed, all bits in that register are rewritten. Ensure all new register values are correct before hitting the ENTER key.

The **ec** command has the following parameter:

| | |
|---|---|
| **configuration** | One of four possible register configurations identified as 0, 1, 2, or 3. |

An example output from this command is shown below.

```
SL100X/SL240X FPDP VME Monitor v1.0
% ec 0
VME
  0 = 0C : 4
  1 = 00 :
  2 = 40 :
  3 = 00 :
CMC
  00 = 00000000 :
  04 = 00000000 :
  08 = 00000001 : 5
  0C = 00000000 : _
```

## C.5.3 Get Configuration (gc <configuration>)

This command lists the register settings of the desired configuration stored in the EEPROM. The **gc** command has the following parameter:

| | |
|---|---|
| **configuration** | One of four possible register configurations identified as 0, 1, 2, or 3. |

An example output from this command is shown below.

```
SL100X/SL240X FPDP VME Monitor v1.0
% gc 0
VME
  0 = 0C
  1 = 00
  2 = 40
  3 = 00
CMC
  00 = 00000000
  04 = 00000000
  08 = 00000001
  0C = 00000000
  10 = 00000000
  14 = 00000000
  18 = 00000000
```

## C.5.4 Load Configuration (lc <configuration>)

This command immediately loads a stored configuration from the EEPROM. However, this command does not change the active configuration loaded at power up. The **sc** command must be used to change the active configuration. The **lc** command has the following parameter:

| | |
|---|---|
| **configuration** | One of four possible register configurations identified as 0, 1, 2, or 3. |

**WARNING**: It is sometimes necessary to power cycle the carrier card for the new configuration to load. If a power cycle is required, ensure sc<configuration> is set to the desired configuration before power cycling the carrier card.

## C.5.5 Set Configuration (sc <configuration>)

This command determines the configuration stored in the EEPROM that will be used the next time the carrier card is powered up. Once a configuration is set, that active configuration will be used every time the carrier card is powered up. The active configuration will not be loaded until the carrier card has its power cycled or the **lc** command is used. The **sc** command has the following parameter:

| | |
|---|---|
| **configuration** | One of four possible register configurations identified as 0, 1, 2, or 3. |

### C.5.6 Bus Read (br <register set> <address>)

This command reads directly from the carrier card's registers and the CMC registers. This command is typically used only for debugging. The **br** command has the following parameters:

| | |
|---|---|
| **register set** | '0' to access carrier card's registers.<br>'1' to access SL240X CMC registers. |
| **address** | Register offset. |

An example output from this command is shown below.

```
SL100X/SL240X FPDP VME Monitor v1.0
% br 1 4
08 = 00001340
```

### C.5.7 Bus Write (bw <register set> <address>)

This command writes directly to the carrier card's registers and the CMC registers. Any registers written using the **bw** command are lost when power is removed from the carrier/CMC cards. This command is typically used only for debugging.

The current value of a register is shown before the colon. A new register value may be entered after the colon followed by pressing the ENTER key. If the current register value is already correct, press the ENTER key by itself. This will keep the existing value for that register.

**NOTE**: Each time a register value is changed, all bits in that register are rewritten. Ensure all new register values are correct before hitting the ENTER key.

The **bw** command has the following parameters:

| | |
|---|---|
| **register set** | '0' to access carrier card's registers.<br>'1' to access SL240X CMC registers. |
| **address** | Register offset. |

An example output from this command is shown below.

```
SL100X/SL240X FPDP VME Monitor v1.0
% bw 1 8
08 = 00000001 : 5
```

### C.5.8 Help (h)

The **h** command displays on-line help for all available configuration commands.

## C.6 NGSL VME and PCI Carrier Card Default Configurations

Factory testing requires the configurations be set to some default values. These default configuration values are listed below.

## C.6.1 Configuration 0 – FPDP-TM with CRC Disabled

```
VME
  0 = 0C
  1 = 00
  2 = 40
  3 = 00
CMC
  00 = 00000000
  04 = 00000000
  08 = 00000001
  0C = 00000000
  10 = 00000000
  14 = 00000000
  18 = 00000000
  1C = 00000000
```

## C.6.2 Configuration 1 – FPDP-RM with CRC Disabled

```
VME
  0 = 04
  1 = 00
  2 = 40
  3 = 00
CMC
  00 = 00000000
  04 = 00000000
  08 = 00000000
  0C = 00000000
  10 = 00000000
  14 = 00000000
  18 = 00000000
  1C = 00000000
```

## C.6.3 Configuration 2 – FPDP-TM with CRC Enabled

```
VME
  0 = 0C
  1 = 00
  2 = 40
  3 = 00
CMC
  00 = 00000000
  04 = 00000000
  08 = 00000003
  0C = 00000000
  10 = 00000000
  14 = 00000000
  18 = 00000000
  1C = 00000000
```

## C.6.4 Configuration 3 - FPDP-RM with CRC Enabled

```
VME
  0 = 04
```

```
  1 = 00
  2 = 40
  3 = 00
CMC
  00 = 00000000
  04 = 00000000
  08 = 00000002
  0C = 00000000
  10 = 00000000
  14 = 00000000
  18 = 00000000
  1C = 00000000
```

# C.7 FXSL VMER Configuration

## C.7.1 Switch Configurations

> **CAUTION**: Never change any of the switches on the FibreXtreme FXSL VMER card while power is applied to the card.

There are twenty-eight switches (J1 to J28) on the card that must be configured before installing the cards. Figure C-2 shows the location, numbers, and default setting for each switch. Tables C-1 and C-2 give the description of the switch settings.

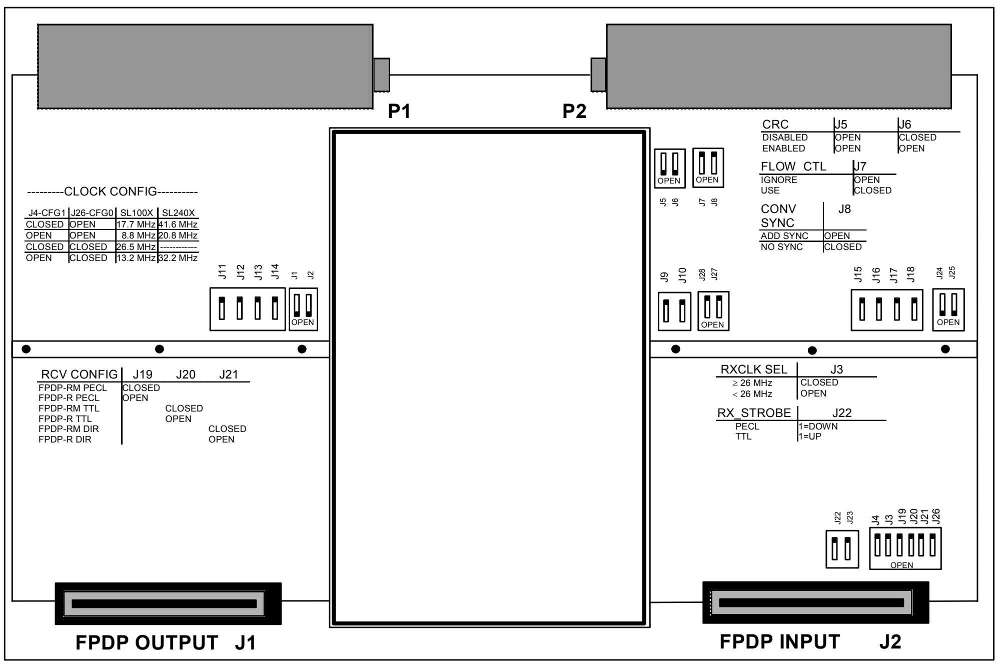


**Figure C-3 FibreXtreme FXSL VMER Configuration Switches**

(Default positions shown; ▯ indicates switch position DOWN)



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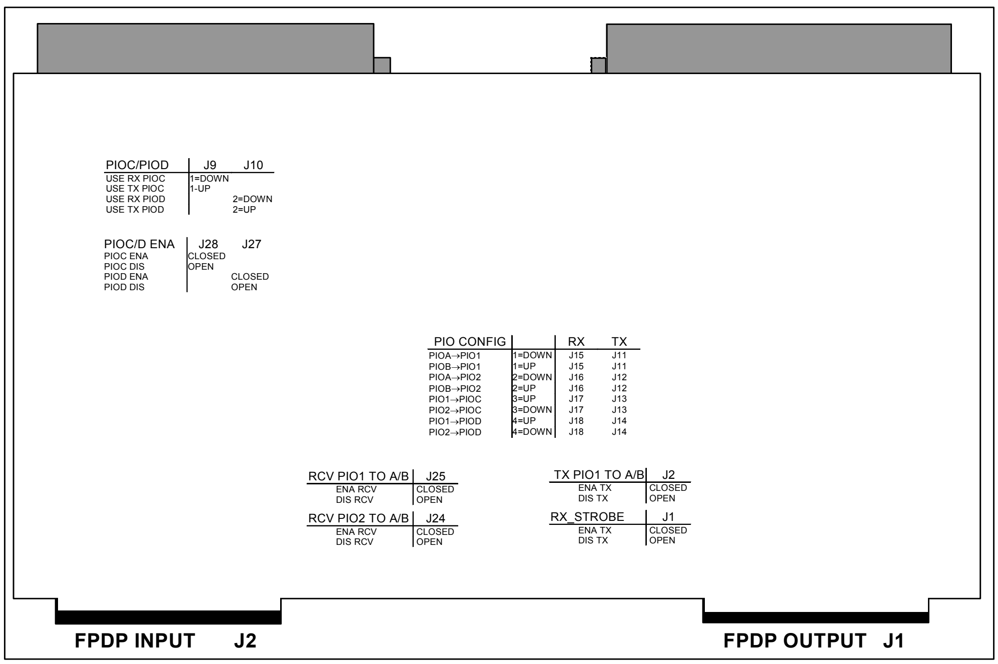


**Figure C-4 FibreXtreme FXSL VMER Solder Side**

**Table C-1 FXSL VMER Configuration Switch Descriptions**

| Switch | Location | Switch Position | Description |
|---|---|---|---|
| TX PIO2 TO A/B | J1 | CLOSED | TX PIO2 to A/B ENABLED |
| | | OPEN | TX PIO2 to A/B DISABLED |
| TX PIO1 TO A/B | J2 | CLOSED | TX PIO1 to A/B ENABLED |
| | | OPEN | TX PIO1 to A/B DISABLED |
| RXCLK_SEL | J3 | CLOSED | For a receiver STROBE ≥ 26.5625 MHz |
| | | OPEN | For a receiver STROBE < 26.5625 MHz |
| TXCLK_SEL | J4 | CLOSED | See Table C-2 |
| | | OPEN | |
| MODE0 | J5 | OPEN | Reserved for future expansion |
| MODE1 | J6 | CLOSED | CRC disabled |
| | | OPEN | CRC enabled |
| IGNORE_FC | J7 | CLOSED | To use flow control from the remote node |
| | | OPEN | To ignore flow control from the remote node |
| CONVERT_SYNC | J8 | CLOSED | A SYNC without DVALID will **NOT** be added after every SYNC with DVALID |
| | | OPEN | To add a SYNC without DVALID after every received SYNC with DVALID |
| PIO1_IN | J9 | 1 = UP | To use the TX PIOC |
| | | 1 = DOWN | To use the RX PIOC |
| PIO2_IN | J10 | 2 = UP | To use the TX PIOD |
| | | 2 = DOWN | To use the RX PIOD |
| TX_PIO1_CFG | J11 | 1 = UP | To use PIOB |
| | | 1 = DOWN | To use PIOA |
| TX_PIO2_CFG | J12 | 2 = UP | To use PIOB |
| | | 2 = DOWN | To use PIOA |
| TX_PIOC_CFG | J13 | 3 = UP | To use PIO2 |
| | | 3 = DOWN | To use PIO1 |
| TX_PIOD_CFG | J14 | 4 = UP | To use PIO2 |
| | | 4 = DOWN | To use PIO1 |
| RX_PIO1_CFG | J15 | 1 = UP | To use PIOB |
| | | 1 = DOWN | To use PIOA |
| RX_PIO2_CFG | J16 | 2 = UP | To use PIOB |
| | | 2 = DOWN | To use PIOA |
| RX_PIOC_CFG | J17 | 3 = UP | To use PIO2 |
| | | 3 = DOWN | To use PIO1 |
| RX_PIOD_CFG | J18 | 4 = UP | To use PIO2 |
| | | 4 = DOWN | To use PIO1 |
| PECL_TERM | J19 | CLOSED | To use the card as FPDP-RM |
| | | OPEN | To use the card as FPDP-R |
| TTL_TERM | J20 | CLOSED | To use the card as FPDP-RM |
| | | OPEN | To use the card as FPDP-R |
| DIR_TERM | J21 | CLOSED | To use the card as FPDP-RM |
| | | OPEN | To use card as FPDP-R |

| Switch | Location | Switch Position | Description |
|---|---|---|---|
| STROBE_SEL | J22 | 1 = DOWN | To use PECL STROBE on receive interface |
| | | 1 = UP | To use TTL STROBE on receive interface |
| Reserved | J23 | 2 = DOWN | Always leave in default position |
| RCV PIO2 TO A/B | J24 | CLOSED | RCV PIO2 to A/B ENABLED |
| | | OPEN | RCV PIO2 to A/B DISABLED |
| RCV PIO1 TO A/B | J25 | CLOSED | RCV PIO1 to A/B ENABLED |
| | | OPEN | RCV PIO1 to A/B DISABLED |
| CLF_DBL | J26 | 1 = UP | See Table C-2 |
| | | 1 = DOWN | |
| PIOD ENA | J27 | CLOSED | PIOD ENABLED |
| | | OPEN | PIOD DISABLED |
| PIOC ENA | J28 | CLOSED | PIOC ENABLED |
| | | OPEN | PIOC DISABLED |

**Table C-2 TXCLK_SEL Switch Settings for FXSL VMER Cards**

| J4- TXCLK_SEL | J26-CLK_DBL | SL100X | SL240X |
|---|---|---|---|
| CLOSED | CLOSED | 26.5625 MHz | 62.5000 MHz |
| CLOSED | OPEN | 17.7083 MHz | 41.6667 MHz |
| OPEN | CLOSED | 13.2813 MHz | 31.2500 MHz |
| OPEN | OPEN | 8.8542 MHz | 20.8333 MHz |

# C.8 Dual VMER FPDP Card Configuration

**CAUTION**: Never change any of the switches on the Dual VMER FPDP card while power is applied to the card.

There are thirty-two switches (J2 to J17 and J20 to J35) on the Dual VMER FPDP card that must be configured before installing the cards. Figure C-3 shows the location, and default setting for each switch. Tables C-3 and C-4 give a description of the switch settings.

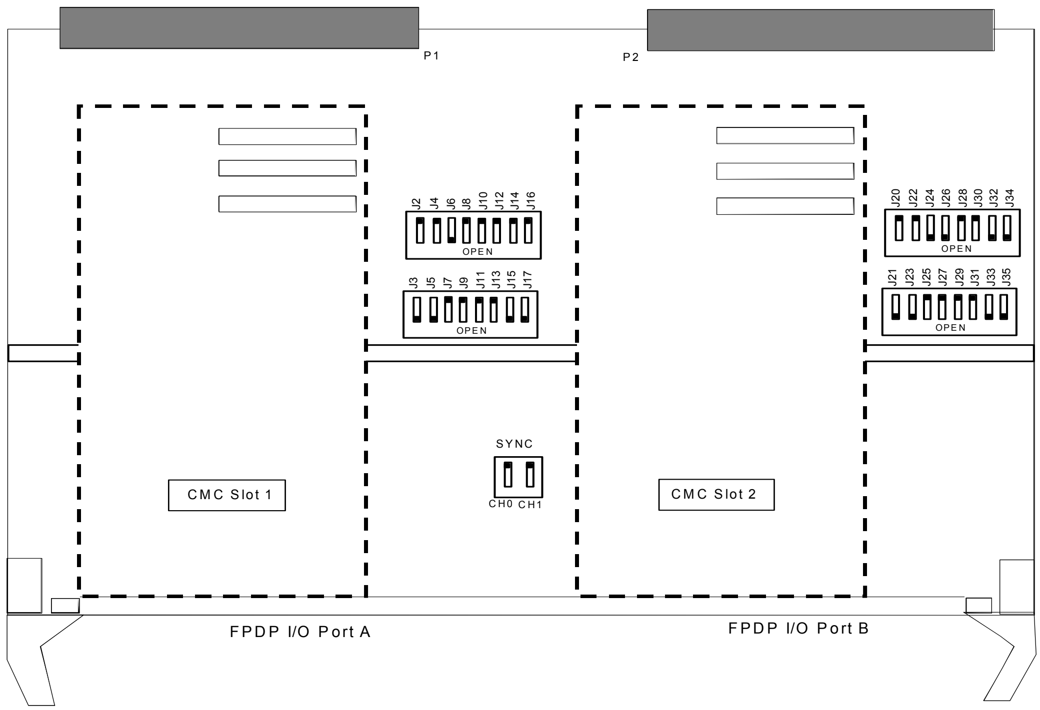


**Figure C-5 FibreXtreme Dual VMER FPDP Configuration Switches**

(Default positions shown; ▯ indicates switch position DOWN)

**NOTE:** The default switch settings shown in Figure C-3 and Table C-3 assume the FPDP ports are both configured as transmit master ports (FPDP-TM). The TRANSMIT switches (J8 and J26) control the direction of the FPDP ports A and B respectively. All other switches are application specific and must be configured on installation.

**Table C-3 Dual VMER FPDP Switch Configuration Descriptions**

| Switch | Port A Location | Port B Location | Switch Position | Description |
|---|---|---|---|---|
| RX CLK_SEL | J2 | J20 | CLOSED | Selects the PECL strobe on the receiver side |
| | | | OPEN (default) | Selects the TTL strobe on the receiver side |
| WRAP | J4 | J22 | CLOSED (default) | No Wrap |
| | | | OPEN | Wrap the CMC's Receive and Transmit port to one another – for debugging |
| MASTER | J6 | J24 | CLOSED | Selects the FPDP-R feature (termination disabled) |
| | | | OPEN (default) | Selects the FPDP-TM/FPDP-RM feature (termination enabled) |
| TRANSMIT | J8 | J26 | CLOSED (default) | FPDP port is an FPDP-R (M) Interface |
| | | | OPEN | FPDP port is an FPDP-TM Interface |
| PIO REV1 | J10 | J28 | CLOSED (default) | Selects PIO1<->CMC PIO1 |
| | | | OPEN | Selects PIO1<->CMC PIO2 |
| PIO REV2 | J12 | J30 | CLOSED (default) | Selects PIO2<->CMC PIO2 |
| | | | OPEN | Selects PIO2<->CMC PIO1 |
| PIO DIR1 | J14 | J32 | CLOSED | Direction of PIO1 line is output |
| | | | OPEN (default) | Direction of PIO1 line is input |
| PIO DIR2 | J16 | J34 | CLOSED | Direction of PIO2 line is output |
| | | | OPEN (default) | Direction of PIO2 line is input |
| MODE 0 | J3 | J21 | CLOSED | Reserved for future expansion |
| | | | OPEN (default) | |
| MODE 1 | J5 | J23 | CLOSED (default) | CRC disabled |
| | | | OPEN | CRC enabled |
| IGNORE FC | J7 | J25 | CLOSED (default) | Use Flow Control from the remote end |
| | | | OPEN | Ignore Flow Control from the remote end |
| CONVERT SYNC | J9 | J27 | CLOSED (default) | A SYNC without DVALID is **not added** after every received SYNC with DVALID |
| | | | OPEN | Adds a SYNC without DVALID after every received SYNC with DVALID |
| CLOCK SEL0 | J11 | J29 | CLOSED (default) | See Table C-4 |
| | | | OPEN | |
| CLOCK SEL1 | J13 | J31 | CLOSED | See Table C-4 |
| | | | OPEN (default) | |
| RESERVED | J15 | J33 | CLOSED | Reserved for future expansion |
| | | | OPEN (default) | |
| RESERVED | J17 | J35 | CLOSED | Reserved for future expansion |
| | | | OPEN (default) | |
| RESERVED | CH0 | - | 1 = DOWN (default) | Always leave in default position |
| RESERVED | - | CH1 | 2 = DOWN (default) | Always leave in default position |

**Table C-4 CLOCK SEL0 and CLOCK SEL1 Switch Settings for Dual VMER FPDP Cards**

| CLOCK SEL1 J13 (Port A) J31 (Port B) | CLOCK SEL0 J11 (Port A) J29 (Port B) | Dual VMER Card with SL100X CMC Card | Dual VMER Card with SL240X CMC Card |
|---|---|---|---|
| CLOSED | CLOSED | 26.5625 MHz | 62.5000 MHz |
| OPEN | CLOSED | 17.7083 MHz | 41.6667 MHz |
| CLOSED | OPEN | 13.2813 MHz | 31.2500 MHz |
| OPEN | OPEN | 8.8542 MHz | 20.8333 MHz |

# C.9 Programmed Input/Outputs (PIOs)

## C.9.1 FXSL VMER FPDP Cards

The PIO1 and PIO2 are generic input/output lines from the FPDP input and FPDP output ports. The PIOA and PIOB lines connect to PIO1 and PIO2 received from the FibreXtreme link interface. The PIO1 and PIO2 lines transmitted to the FibreXtreme link interface come from the PIOC and PIOD lines from the FPDP input and FPDP output ports. Switches J9 and J10 select which PIOC and PIOD line is transmitted across the link. See Figures C-4 and C-5.

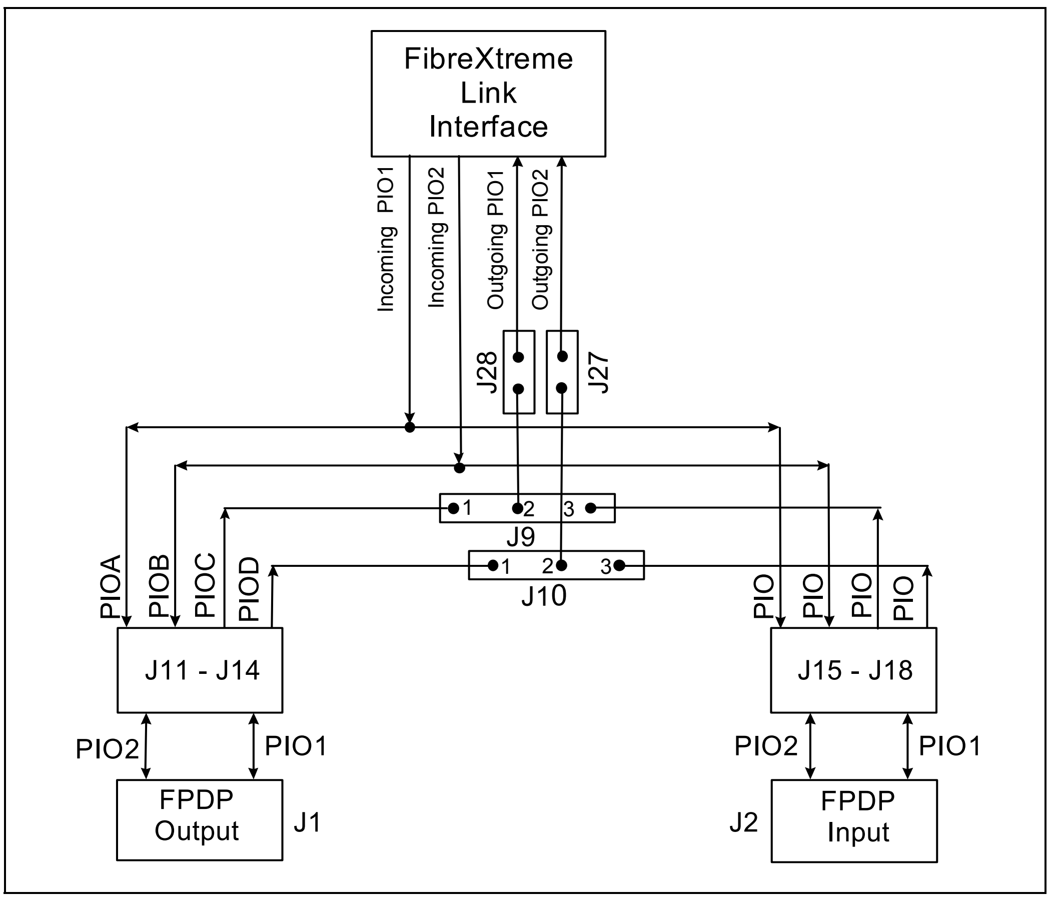


**Figure C-6 PIO Line Connections on FXSL VMER FPDP Cards**

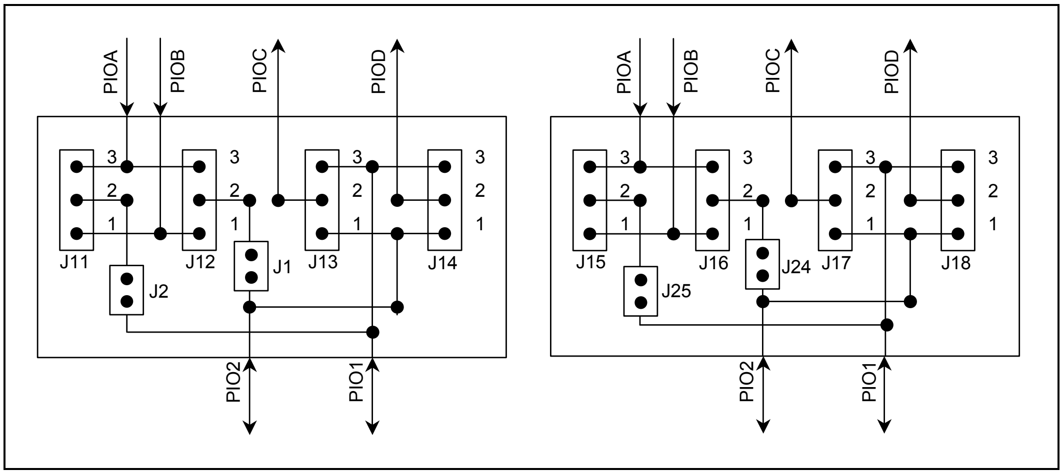


**Figure C-7 Interconnection Details of Switches J11 – J18 on FXSL VMER FPDP Cards**

### C.9.2 Dual VMER FPDP Card

The PIO lines are handled in a different manner on the FibreXtreme Dual VMER FPDP card. The PIO lines between the FPDP port and the SL240X CMC interface are controlled by programmable logic and switches J10, J12, J14, and J16 for Port A and J28, J30, J32, and J34 for Port B. Refer to Table C-3 for appropriate switch settings.

## C.10 FPDP-R vs. FPDP-RM

By default the FPDP receiver interface on the FibreXtreme FXSL VMER FPDP card is an FPDP-RM. This card can be configured as an FPDP-R instead of an FPDP-RM by setting switches J19, J20, and J21 to OPEN.

To configure the FibreXtreme Dual VMER FPDP card as an FPDP-R, set switch J6 for Port A or J24 for Port B to CLOSED.

For more information about FPDP standards, go to the VITA website at http://www.vita.com/vso/.

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# APPENDIX D

# SL100X/SL240X PROTOCOL

## TABLE OF CONTENTS



## FIGURES



## TABLES

# D.1 Overview

The SL100X/SL240X Serial FPDP protocol (also known as ANSI/VITA 17.1) is designed to provide near optimal throughput while maintaining low overhead. The link transfer rate for SL100X cards is 1.0625 Gbps, and the transfer rate for SL240X cards is 2.5 Gbps. Since an 8B/10B encoding scheme is used, this corresponds to a raw data rate of 106.25 MBps (1 MB = $10^6$ bytes) for SL100X and 250 MBps for SL240X. Based on the protocol presented here, the usable throughput of this link available to the user is 105 MBps for SL100X or 247 MBps for SL240X. All ordered sets used by this protocol are standard Fibre Channel ordered sets with the exception of positive IDLE, which is allowed for a more flexible receiver interface. Note that the protocol referred to throughout this document is the protocol used by the transmitter and accepted by the receiver. The receiver does not have to see the protocol defined here to receive data. Any generic Fibre Channel data stream with an IDLE at least every 4096 words can be used.

# D.2 Ordered Sets Used

Fibre Channel denotes a certain mapping of the transmission words in the 8B/10B protocol to be ordered sets, which denote special control information for Fibre Channel. These same ordered sets are used in ANSI/VITA 17.1, but are assigned different meaning.

There are eighteen ordered sets used by SL240X to denote different information. Twelve of these ordered sets are used to embed five bits of data—eight start-of-frame (SOF) sets are used to embed three bits at the start of a frame, and four status-end-of-frame (SEOF) sets are used to embed two bits at the end of the frame. The SOF ordered sets embed three FPDP signals—PIO1, PIO2, and DIR.

Note that although the direction signal on FPDP is active low (/DIR), the signal transmitted on the link is active high (DIR).

The four EOF ordered sets embed the FPDP signal NRDY (once again, the inverted version of the FPDP interface’s /NRDY) and Transmit FIFO Overflow flag.

There are two additional EOF ordered sets used by SL240X to denote the actual end of frame. The Mark EOF (MEOF) denotes a frame that has SYNC associated with it, and the Frame EOF (FEOF) denotes a normal data frame. The other four ordered sets are inter-frame padding used to denote flow control information and alternate frame interpretations. Table D-1 shows the mappings from the Fibre Channel ordered sets onto the ANSI/VITA 17.1 ordered sets, along with the meaning associated with each ordered set.

**Table D-1 Ordered Set Mapping**

| Fibre Channel Ordered Set | ANSI/VITA 17.1 Ordered Set | Description |
|---|---|---|
| SOFc1 | SOF | Start of Frame:<br>PIO1 = 0, PIO2 = 0, DIR = 0 |
| SOFi1 | SOF | Start of Frame:<br>PIO1 = 0, PIO2 = 0, DIR = 1 |
| SOFn1 | SOF | Start of Frame:<br>PIO1 = 0, PIO2 = 1, DIR = 0 |
| SOFi2 | SOF | Start of Frame:<br>PIO1 = 0, PIO2 = 1, DIR = 1 |
| SOFn2 | SOF | Start of Frame:<br>PIO1 = 1, PIO2 = 0, DIR = 0 |
| SOFi3 | SOF | Start of Frame:<br>PIO1 = 1, PIO2 = 0, DIR = 1 |
| SOFn3 | SOF | Start of Frame:<br>PIO1 = 1, PIO2 = 1, DIR = 0 |
| SOFf | SOF | Start of Frame:<br>PIO1 = 1, PIO2 = 1, DIR = 1 |
| EOFt | SEOF | Status EOF:<br>FIFO Overflow = 0, NRDY = 0 |
| EOFdt | SEOF | Status EOF:<br>FIFO Overflow = 0, NRDY = 1 |
| EOFa | SEOF | Status EOF:<br>FIFO Overflow = 1, NRDY = 0 |
| EOFn | SEOF | Status EOF:<br>FIFO Overflow = 1, NRDY = 1 |
| EOFni | MEOF | Mark EOF:<br>EOF for a SYNC frame |
| EOFdti | FEOF | Frame EOF:<br>EOF for a normal data frame |
| R_RDY | SWDV | SYNC with DATA Valid:<br>Says that the next frame will be a SYNC with DATA frame |
| NOS | STOP | Tells the remote transmitter to stop sending data |
| CLS | GO | Tells the remote transmitter it can continue to send data |
| IDLE | IDLE | IDLE character:<br>Used as a padding word to maintain receiver synchronization |

## D.3 Frames

There are four basic frame types defined in ANSI/VITA 17.1 - an IDLE frame, data frame, a SYNC without data frame, and a SYNC with data frame. The data is divided into frames so the FPDP signals are sampled at some minimum interval, and so the receiver is guaranteed to see IDLEs to maintain synchronization. SYNC is used to delimit data streams and maintain host program synchronization. This signal is under user control for PCI based products, and is the same as the FPDP /SYNC signal for CMC/FPDP based products. Whenever a SYNC appears on the output of the Transmit FIFO, the current frame is terminated and the proper SYNC frame (SYNC with data or SYNC without data) is sent. Figure D-1 shows the four types of frames and the ordered set placement within those frames.

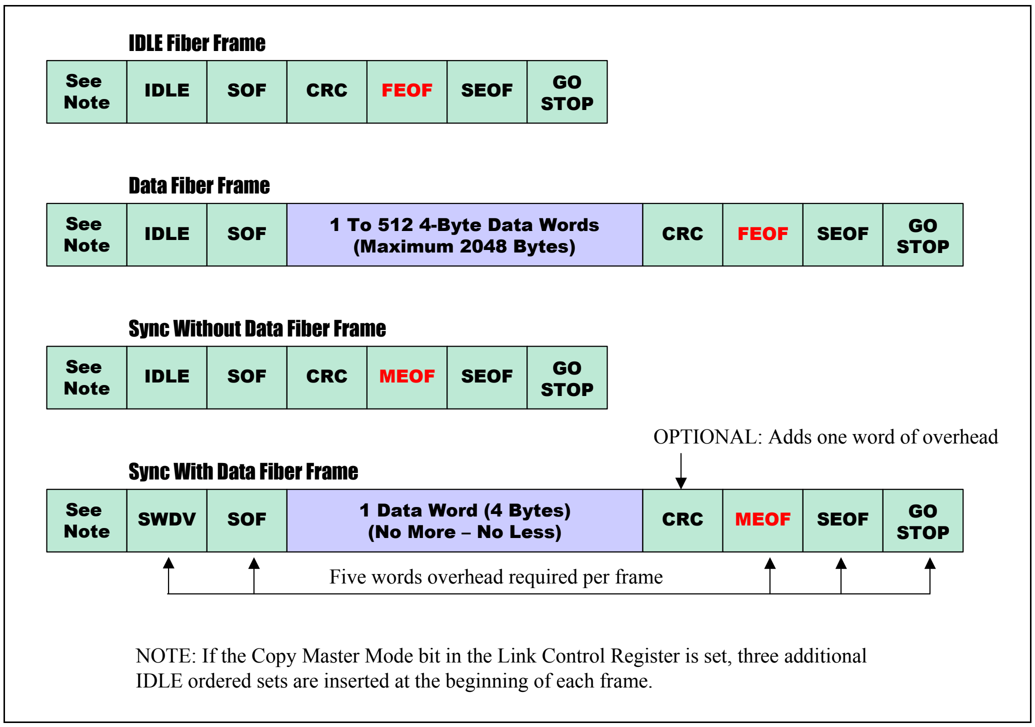


**Figure D-1 ANSI/VITA 17.1 Framing Protocol**

## D.3.1 Link Bandwidth

With CRC disabled and the Copy Mode Master bit clear (‘0’), there is a five-word overhead for every frame transmitted. Since frames can contain up to 512 words of data, this results in an efficiency of 99.03%. With CRC enabled and the Loop Master bit clear, there is a six-word overhead for every frame transmitted. This results in a maximum efficiency of 98.84%. With the Copy Mode Master bit set (‘1’), three additional ordered sets are added per frame. This results in an efficiency of 98.46 percent without CRC and 98.27 percent with CRC. Table D-2 gives the theoretical maximum sustained throughput based on these numbers.

**Table D-2 Maximum Sustained Throughput**

| Card | With CRC and Copy Mode Master bit = 0 | Without CRC and Copy Mode Master bit = 0 | With CRC and Copy Mode Master bit = 1 | Without CRC and Copy Mode Master bit = 1 |
|---|---|---|---|---|
| SL100X | 105.02 MBps | 105.22 MBps | 104.41 MBps | 104.61 MBps |
| SL240X | 247.10 MBps | 247.58 MBps | 245.68 MBps | 246.15 MBps |

**NOTE**: The Copy Master Mode is located in the Link Control register.

## D.3.2 FPDP Signal Sample Rate

The states of the FPDP signals (PIO1, PIO2, DIR, and NRDY) are transmitted across the link at varying rates. The worst-case rate at which these signals are sampled is for CRC checked filled data frames and the Copy Mode Master bit set . In this case, the signals are sampled every 521 words. For CRC checked filled data frames and the Copy Mode Master bit clear, these signals are sampled every 518 words. Table D-3 summarizes the worst-case sampling frequencies for the different link transmission speeds (SL100X and SL240X).

**Table D-3 Sampling Frequencies**

| Card | With CRC and Copy Mode Master bit = 0 | Without CRC and Copy Mode Master bit = 0 | With CRC and Copy Mode Master bit = 1 | Without CRC and Copy Mode Master bit = 1 |
|---|---|---|---|---|
| SL100X | 51.28 KHz | 51.38 KHz | 50.98 KHz | 51.08 KHz |
| SL240X | 120.65 KHz | 120.89 KHz | 119.96 KHz | 120.19 KHz |

**NOTE**: The Copy Master Mode is located in the Link Control register.

## D.4 Data Transmission and Flow Control

As SL100X/SL240X is seen as a point-to-point link from the transmitter, there is no need to log into the receiver node to begin sending data. SL100X/SL240X cards can begin transmission as soon as they are started and data is available in the Transmit FIFO. Using the frames described above, the transmitter sets up a constant stream of frames, into which it inserts data as it becomes available. Data is only inserted if the flow control signal from the remote end is GO—if it is STOP, then the data waits in the Transmit FIFO until the signal changes. Curtiss-Wright Controls' SL100X/SL240X cards use the same protocol when transmitting from either end to allow the link to operate bi-directionally. Since these data streams are independent, the maximum throughput on the link would be 210 MBps (105 MBps/direction) for SL100X or 494 MBps for SL240X.

The receiver should transmit the STOP signal when it has space for the data contained in 20 km of fiber or less left. Assuming 5 µs/km for the speed of light, this gives us 100 µs of data. For SL100X, each 32-bit word (40 bits on the link) takes 37.64 ns, there are 2657 words stored in 20 km of cable. For SL240X, each 32-bit word (40 bits on the link) takes 16 ns, so there are 6250 words stored in 20 km of cable. The first 10 km is reserved for sending the STOP signal to the transmitter, and the second 10 km is for the data already contained in the receive fiber.

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# APPENDIX E

# ORDERING INFORMATION

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## TABLES

# E.1 Overview

This appendix contains the order number for all Curtiss-Wright Controls, Inc. products mentioned in this manual. For an up to date list, or for inquiries about these products, contact Curtiss-Wright Controls, Inc. Sales.

# E.2 Ordering Information

## E.2.1 SL100X FPDP

Refer to section 2.3 for detailed descriptions of the various SL100X FPDP ordering configurations.

**Table E-1 SL100X CMC Standard**

| Order Number | Description |
|---|---|
| FHE4-FM4MWB04-00 | SL100X CMC, 850 nm laser |
| FHE4-FM4SWB04-00 | SL100X CMC, 1300 nm laser |
| FHE4-FM4LRB04-00 | SL100X CMC, 1550 nm laser |
| FHE4-FM4H2B04-00 | SL100X CMC, HSSDC2 |
| | |
| FHE4-FC4MWB04-00 | PCI FibreXtreme Carrier with one FPDP port, SL100X CMC, 850 nm laser |
| FHE4-FC4SWB04-00 | PCI FibreXtreme Carrier with one FPDP port, SL100X CMC, 1300 nm laser |
| | |
| FHE4-FP4MWB04-00 | NGSL VMER with one FPDP port, SL100X CMC, 850 nm laser |
| FHE4-FP4SWB04-00 | NGSL VMER with one FPDP port, SL100X CMC, 1300 nm laser |
| FHE4-FP4LRB04-00 | NGSL VMER with one FPDP port, SL100X CMC, 1550 nm laser |
| FHE4-FP4H2B04-00 | NGSL VMER with one FPDP port, SL100X, HSSDC2 |
| | |
| FHE2-FR4MWB04-00 | FXSL VMER with two FPDP ports, SL100X CMC, 850 nm laser |
| FHE2-FR4SWB04-00 | FXSL VMER with two FPDP ports, SL100X CMC, 1300 nm laser |
| FHE2-FP4LRB04-00 | NGSL VMER with two FPDP ports, SL100X CMC, 1550 nm laser |
| FHE2-FR4H2B04-00 | FXSL VMER with two FPDP ports, SL100X, HSSDC2 |
| | |
| FHE4-FSMWBMWB-00 | Dual VMER with two SL100X CMC cards, one FPDP port per CMC card, 850 nm laser |
| FHE4-FSSWBSWB-00 | Dual VMER with two SL100X CMC cards, one FPDP port per CMC card, 1300 nm laser |
| FHE4-FSLRBSWB-00 | Dual VMER with two SL100X CMC cards, one FPDP port per CMC card, 1550 nm laser |
| FHE4-FSH2BH2B-00 | Dual FXSL VMER with two SL100X CMC cards, one FPDP port per CMC card, HSSDC2 |

**Table E-2 SL100X CMC Ruggedized Level 1**

| Order Number | Description |
|---|---|
| FHE4-FM4MWB04-R1 | Ruggedized Level 1 SL100X CMC, 850 nm laser |
| FHE4-FM4SWB04-R1 | Ruggedized Level 1 SL100X CMC, 1300 nm laser |
| | |
| FHE4-FP4MWB04-R1 | Ruggedized Level 1 NGSL VMER with one FPDP port, SL100X CMC, 850 nm laser |
| FHE4-FP4SWB04-R1 | Ruggedized Level 1 NGSL VMER with one FPDP port, SL100X CMC, 1300 nm laser |
| | |
| FHE4-FSMWBMWB-R1 | Ruggedized Level 1 Dual VMER with two SL100X CMC cards, one FPDP port per CMC card, 850 nm laser |
| FHE4-FSSWBSWB-R1 | Ruggedized Level 1 Dual VMER with two SL100X CMC cards, one FPDP port per CMC card, 1300 nm laser |
| | |
| FHE2-FR4MWB04-R1 | Ruggedized Level 1 FXSL VMER with two FPDP ports, SL100X CMC, 850 nm laser |
| FHE2-FR4SWB04-R1 | Ruggedized Level 1 FXSL VMER with two FPDP ports, SL100X CMC, 1300 nm laser |

**Table E-3 SL100X CMC Ruggedized Level 2**

| Order Number | Description |
|---|---|
| FHE4-FM4MWB04-R2 | Ruggedized Level 2 SL100X CMC, 850 nm laser |
| FHE4-FM4SWB04-R2 | Ruggedized Level 2 SL100X CMC, 1300 nm laser |
| | |
| FHE4-FP4MWB04-R2 | Ruggedized Level 2 NGSL VMER with one FPDP port, SL100X CMC, 850 nm laser |
| FHE4-FP4SWB04-R2 | Ruggedized Level 2 NGSL VMER with one FPDP port, SL100X CMC, 1300 nm laser |

## E.2.2 SL240X FPDP

Refer to section 2.3 for detailed descriptions of the various SL240X FPDP ordering configurations.

**Table E-4 SL240X CMC Standard**

| Order Number | Description |
|---|---|
| FHE6-FM6MWB04-00 | SL240X CMC, 850 nm laser |
| FHE6-FM6SWB04-00 | SL240X CMC, 1300 nm laser |
| FHE6-FM6LRB04-00 | SL240X CMC, 1550 nm laser |
| FHE6-FM6H2B04-00 | SL240X CMC, HSSDC2 |
| | |
| FHE6-FC6MWB04-00 | PCI FibreXtreme Carrier with one FPDP port, SL240X CMC, 850 nm laser |
| FHE6-FC6SWB04-00 | PCI FibreXtreme Carrier with one FPDP port, SL240X CMC, 1300 nm laser |
| | |
| FHE6-FP6MWB04-00 | NGSL VMER with one FPDP port, SL240X CMC, 850 nm laser |
| FHE6-FP6SWB04-00 | NGSL VMER with one FPDP port, SL240X CMC, 1300 nm laser |
| FHE6-FP6LRB04-00 | NGSL VMER with one FPDP port, SL240X CMC, 1550 nm laser |
| FHE6-FP6H2B04-00 | NGSL VMER with one FPDP port, SL240X, HSSDC2 |
| | |
| FHE2-FR6MWB04-00 | FXSL VMER with two FPDP ports, SL240X CMC, 850 nm laser |
| FHE2-FR6SWB04-00 | FXSL VMER with two FPDP ports, SL240X CMC, 1300 nm laser |
| FHE2-FR6LRB04-00 | FXSL VMER with two FPDP ports, SL240X CMC, 1550 nm laser |
| FHE2-FR6H2B04-00 | FXSL VMER with two FPDP ports, SL240X, HSSDC2 |
| | |
| FHE6-FSMWBMWB-00 | Dual VMER with two SL240X CMC cards, one FPDP port per CMC card, 850 nm laser |
| FHE6-FSSWBSWB-00 | Dual VMER with two SL240X CMC cards, one FPDP port per CMC card, 1300 nm laser |
| FHE6-FSLRBSWB-00 | Dual VMER with two SL240X CMC cards, one FPDP port per CMC card, 1550 nm laser |
| FHE6-FSH2BH2B-00 | Dual VMER with two SL240X CMC cards, one FPDP port per CMC card, HSSDC2. |

**Table E-5 SL240X CMC Ruggedized Level 1**

| Order Number | Description |
|---|---|
| FHE6-FM6MWB04-R1 | Ruggedized Level 1 SL240X CMC, 850 nm laser |
| FHE6-FM6SWB04-R1 | Ruggedized Level 1 SL240X CMC, 1300 nm laser |
| | |
| FHE6-FP6MWB04-R1 | Ruggedized Level 1 NGSL VMER with one FPDP port, SL240X CMC, 850 nm laser |
| FHE6-FP6SWB04-R1 | Ruggedized Level 1 NGSL VMER with one FPDP port, SL240X CMC, 1300 nm laser |
| | |
| FHE2-FR6MWB04-R1 | Ruggedized Level 1 FXSL VMER with two FPDP ports, SL240X CMC, 850 nm laser |
| FHE2-FR6SWB04-R1 | Ruggedized Level 1 FXSL VMER with two FPDP ports, SL240X CMC, 1300 nm laser |

**Table E-6 SL240X CMC Ruggedized Level 2**

| Order Number | Description |
|---|---|
| FHE6-FM6MWB04-R2 | Ruggedized Level 2 SL240X CMC, 850 nm laser |
| FHE6-FM6SWB04-R2 | Ruggedized Level 2 SL240X CMC, 1300 nm laser |
| | |
| FHE6-FP6MWB04-R2 | Ruggedized Level 2 NGSL VMER with one FPDP port, SL240X CMC, 850 nm laser |
| FHE6-FP6SWB04-R2 | Ruggedized Level 2 NGSL VMER with one FPDP port, SL240X CMC, 1300 nm laser |

## E.2.3 Carrier Card (without CMC)

**Table E-7 Carrier Card (Without CMC)**

| Order Number | Description |
|---|---|
| FHE4-FP000000-00 | NGSL VMER Carrier with one FPDP port (w/o CMC card) |
| FHG4-FC000000-00 | PCI FibreXtreme Carrier with one FPDP port (w/o CMC card) |
| FHE2-FR000000-00 | FXSL VMER Carrier with two FPDP Ports (w/o CMC card) |
| FHE4-FS000000-00 | Dual VMER Carrier with one FPDP Port per CMC card (w/o CMC cards) |

# E.3 Media Interface

## E.3.1 Short Wavelength: Multimode Fiber-Optic Cable

The following table lists the order numbers for the simplex and duplex, 50/125 µm multimode fiber-optic cables, for use with the short wavelength laser media interface.

**Table E-8 Multimode Fiber-Optic Cable (LC – LC)**

| Simplex Part Number | Duplex Part Number | Length | Cable End 1 | Cable End 2 |
|---|---|---|---|---|
| FHAC-M1LC3000-00 | FHAC-M2LC3000-00 | 3 m | LC | LC |
| FHAC-M1LC5000-00 | FHAC-M2LC5000-00 | 5 m | LC | LC |
| FHAC-M1LC1001-00 | FHAC-M2LC1001-00 | 10 m | LC | LC |
| FHAC-M1LC2001-00 | FHAC-M2LC2001-00 | 20 m | LC | LC |
| FHAC-M1LC3001-00 | FHAC-M2LC3001-00 | 30 m | LC | LC |
| FHAC-M1LCxxxx-00 | FHAC-M2LCxxxx-00 | Custom | LC | LC |

**Table E-9 Multimode Fiber-Optic Cable (LC – ST)**

| Simplex Part Number | Duplex Part Number | Length | Cable End 1 | Cable End 2 |
|---|---|---|---|---|
| FHAC-M1LCST03-00 | FHAC-M2LCST03-00 | 3 m | LC | ST |
| FHAC-M1LCST05-00 | FHAC-M2LCST05-00 | 5 m | LC | ST |
| FHAC-M1LCST10-00 | FHAC-M2LCST10-00 | 10 m | LC | ST |
| FHAC-M1LCST20-00 | FHAC-M2LCST20-00 | 20 m | LC | ST |
| FHAC-M1LCST30-00 | FHAC-M2LCST30-00 | 30 m | LC | ST |
| FHAC-M1LCSTxx-00 | FHAC-M2LCSTxx-00 | Custom | LC | ST |

**Table E-10 Multimode Fiber-Optic Cable (SC – LC)**

| Simplex Part Number | Duplex Part Number | Length | Cable End 1 | Cable End 2 |
|---|---|---|---|---|
| FHAC-M1SCLC01-00 | FHAC-M2SCLC01-00 | 1 m | SC | LC |
| FHAC-M1SCLC03-00 | FHAC-M2SCLC03-00 | 3 m | SC | LC |
| FHAC-M1SCLC05-00 | FHAC-M2SCLC05-00 | 5 m | SC | LC |
| FHAC-M1SCLC10-00 | FHAC-M2SCLC10-00 | 10 m | SC | LC |
| FHAC-M1SCLC20-00 | FHAC-M2SCLC20-00 | 20 m | SC | LC |
| FHAC-M1SCLC30-00 | FHAC-M2SCLC30-00 | 30 m | SC | LC |
| FHAC-M1SCLCxx-00 | FHAC-M2SCLCxx-00 | Custom | SC | LC |

## E.3.2 Long Wavelength: Singlemode Fiber-Optic Cable

The following table lists the order numbers for the simplex and duplex, 9/125 µm singlemode fiber-optic cables, for use with the long wavelength laser media interface.

**Table E-11 Singlemode Fiber-Optic Cable (LC –LC)**

| Simplex Part Number | Duplex Part Number | Length | Cable End 1 | Cable End 2 |
|---|---|---|---|---|
| FHAC-S1LC3000-00 | FHAC-S2LC3000-00 | 3 m | LC | LC |
| FHAC-S1LC5000-00 | FHAC-S2LC5000-00 | 5 m | LC | LC |
| FHAC-S1LC1001-00 | FHAC-S2LC1001-00 | 10 m | LC | LC |
| FHAC-S1LC2001-00 | FHAC-S2LC2001-00 | 20 m | LC | LC |
| FHAC-S1LC3001-00 | FHAC-S2LC3001-00 | 30 m | LC | LC |
| FHAC-S1LCxxxx-00 | FHAC-S2LCxxxx-00 | Custom | LC | LC |

**Table E-12 Singlemode Fiber-Optic Cable (SC –LC)**

| Simplex Part Number | Duplex Part Number | Length | Cable End 1 | Cable End 2 |
|---|---|---|---|---|
| FHAC-S1SCLC01-00 | FHAC-S2SCLC01-00 | 1 m | SC | LC |
| FHAC-S1SCLC03-00 | FHAC-S2SCLC03-00 | 3 m | SC | LC |
| FHAC-S1SCLC05-00 | FHAC-S2SCLC05-00 | 5 m | SC | LC |
| FHAC-S1SCLC10-00 | FHAC-S2SCLC10-00 | 10 m | SC | LC |
| FHAC-S1SCLC20-00 | FHAC-S2SCLC20-00 | 20 m | SC | LC |
| FHAC-S1SCLC30-00 | FHAC-S2SCLC30-00 | 30 m | SC | LC |
| FHAC-S1SCLCxx-00 | FHAC-S2SCLCxx-00 | Custom | SC | LC |

## E.3.3 HSSDC2 Copper Media Interface: 1.0625 Gbps

Shielded 150-Ohm Shielded Quad copper cable with HSSDC2 (Fibre Channel) connectors, for use with the HSSDC2 copper media interface.

**Table E-13 Shielded 150-Ohm Quad Copper Cable with HSSDC2 (Fibre Channel) Connectors**

| Order Number | Description |
|---|---|
| FHAC-Q2H11000-00 | 1 m HSSDC2 cable, equalized |
| FHAC-Q2H13000-00 | 3 m HSSDC2 cable, equalized |
| FHAC-Q2H15000-00 | 5 m HSSDC2 cable, equalized |
| FHAC-Q2H11001-00 | 10 m HSSDC2 cable, equalized |
| FHAC-Q2H12001-00 | 20 m HSSDC2 cable, equalized |
| FHAC-Q2H12501-00 | 25 m HSSDC2 cable, equalized |
| FHAC-Q2H13001-00 | 30 m HSSDC2 cable, equalized |

## E.3.4 HSSDC2 Copper Media Interface: 2.5 Gbps

Shielded 100-Ohm Shielded Quad copper cable with HSSDC2 (InfiniBand) connectors, for use with the HSSDC2 copper media interface.

**Table E-14 Shielded 100-Ohm Quad Copper Cable with HSSDC2 (InfiniBand) Connectors**

| Order Number | Description |
|---|---|
| FHAC-Q2H31000-00 | 1 m HSSDC2 cable, equalized |
| FHAC-Q2H33000-00 | 3 m HSSDC2 cable, equalized |
| FHAC-Q2H35000-00 | 5 m HSSDC2 cable, equalized |
| FHAC-Q2H31001-00 | 10 m HSSDC2 cable, equalized |

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# APPENDIX F

# FPDP PRIMER

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## FIGURES



## TABLES

# F.1 FPDP Overview

This appendix provides a brief discussion of Front Panel Data Port (FPDP). For more information about FPDP, refer to *Front Panel Data Port Specifications, ANSI/VITA 17-1998* or go to the VITA website at: www.vita.com/vso/. The SL100X/SL240X cards implement a serial version of FPDP on their link interface, which is standard ANSI/VITA 17.1. Most of the concepts from the parallel FPDP specification are applicable to the Serial FPDP world, so they are described here.

Many real-time systems require high-speed, low-latency data transfers on a sustained basis. However, the primary bus (for example, VME bus) cannot provide the required bandwidth and latency at all times because of bus contention. The primary bus must also handle other tasks such as system control. The FPDP bus provides a solution to this problem. Using FPDP, two or more cards are connected by a simple, parallel, synchronous interface using 80-conductor ribbon cable running across the cards' front panels or through a 1.0625 Gbps or 2.5 Gbps serial interface. For parallel FPDP, devices on the FPDP bus must consist of one FPDP Transmit Master (FPDP-TM) and one FPDP Receive Master (FPDP-RM). Multiple FPDP Receiver (FPDP-R) devices may also exist on the bus. For Serial FPDP, there is one master for the bus (which acts as FPDP-TM and FPDP-RM), and one or more receiver nodes. Since only one FPDP-TM can exist on the bus, no bus contention between devices is possible. Figure F-1 shows an example VME FPDP card interconnection using parallel FPDP.

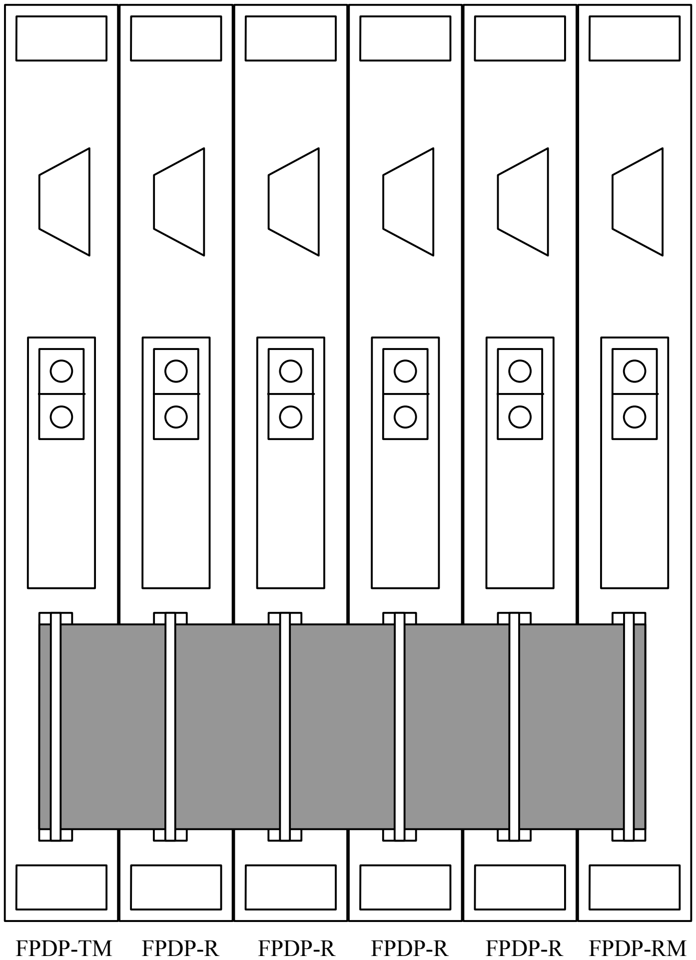


**Figure F-1 Example Configuration With Multiple VME FPDP Cards Connected**

Several advantages of an FPDP interface include:

- Simple hardware is required to interface to FPDP.
- FPDP does not interfere with the normal bus operations – VME or PCI traffic can continue without data transfers wasting bus bandwidth.
- No bus contention is possible because there is only one transmitter.
- No special backplane is required.
- FPDP allows connections from VME chassis to VME chassis.
- Systems may have multiple FPDP buses and thus provides scaleable bandwidth.
- Multiple FPDP busses may coexist in one chassis.
- Throughput can be accurately computed in the design stage.
- Little software development is required to move data between cards.
- Framed or unframed data may be transmitted across the FPDP link.
- Low latency.

Some additional advantages of parallel FPDP are:

- Low cost, 32-bit parallel interface provided through a ribbon cable.
- 160 MBps sustained data rate.

Some additional advantages of Serial FPDP are:

- Noise immune fiber-optic interface.
- Significantly increased transmission distance (10 km).
- Standard cards for parallel FPDP, custom backplanes.

# F.2 Terminology

Some FPDP specific terms are defined below.

## F.2.1 FPDP Transmit Master (FPDP-TM)

An FPDP-TM is a device that transmits data and timing signals onto the FPDP bus. This device also terminates the bus signals at one end of the ribbon cable bus for parallel FPDP. Only one FPDP-TM may exist on an FPDP bus.

## F.2.2 FPDP Receive Master (FPDP-RM)

An FPDP-RM is a device that receives data from the FPDP bus synchronously with the timing signals provided by the FPDP-TM. This device also terminates the bus signals at one end of the ribbon cable bus for parallel FPDP. Only one FPDP-RM may exist on an FPDP bus.

## F.2.3 FPDP Receiver (FPDP-R)

An FPDP-R is a device that receives data from the FPDP bus synchronously with the timing signals provided by the FPDP-TM. As opposed to the FPDP-RM, this device does not terminate any bus signals on parallel FPDP. Multiple FPDP-R devices may exist on an FPDP bus.

# F.3 Parallel FPDP Theory of Operation

## F.3.1 Clock Signals

A single FPDP-TM generates a free-running clock. This clock frequency determines the maximum transfer rate on the bus. FPDP provides both a PECL (Positive Emitter Coupled Logic) and TTL strobe on the bus, with the PECL clock used for higher frequency ( > 20 MHz) transfers. If designing to the CMC card, only an LVTTL clock is generated by the card's FPDP transmitter port, since it is driving to a PCB instead of a long ribbon cable.

An FPDP receiver card (FPDP-R or FPDP-RM) accepts the PECL or TTL clock generated by the transmitter and uses it as the word clock for the data transfers. This clock is generally in the range of 0 to 40 MHz on standard FPDP busses, though the FPDP specification does not state a hard maximum frequency at which the bus may be run. The CMC card has a LVTTL clock input that it uses for the word clock.

## F.3.2 Data Framing

The FPDP specification does not allow for the transmission of address information. However, many systems have data coming from several cards or channels. The way to identify data from each channel is through framing. A synchronization pulse signal, /SYNC, was defined for framing purposes. The frame size is defined as the number of data items in the frame. Unframed data may also be transmitted onto the FPDP bus. The four data frame types defined by the FPDP specification are listed and described below.

- Unframed data
- Single frame data
- Fixed size repeating frame data
- Dynamic size repeating frame data

## UNFRAMED DATA

- Used when the source and the organization of the data is not important.
- Used when the FPDP receivers do not need to be synchronized to the data stream.
- /SYNC is not required.

When unframed data is transmitted onto the FPDP bus, no synchronization is required. Thus, the FPDP-TM must not generate /SYNC, and the FPDP-RM and FPDP-R devices must not require a /SYNC pulse in order to correctly receive data.

## SINGLE FRAME DATA

- Synchronization must occur prior to data to which it applies.
- Synchronization occurs between data blocks.
- /SYNC must be asserted before /DVALID is asserted.
- Synchronization occurs infrequently, perhaps only once.

When single frame data is transmitted onto the FPDP bus, the FPDP-TM must assert a /SYNC pulse before valid data starts being transmitted. Valid data is transmitted when the data valid signal /DVALID is asserted. Thus, a /SYNC pulse must be asserted before /DVALID is asserted when transmitting single frame data. After a /SYNC pulse is asserted, the FPDP-RM and FPDP-R devices should not accept data until the first STROBE period after /DVALID is asserted. The /SYNC pulse does not have to be asserted again until before the start of the next data transmission.

## FIXED SIZE REPEATING FRAME DATA

- Synchronization must occur prior to data to which it applies.
- Synchronization occurs at the same time the last data word in the block before is transferred.
- /SYNC must be asserted at the end of the data block while /DVALID is still asserted.
- Because synchronization occurs at the end of the data block, the first data block will not be synchronized.
- Synchronization occurs frequently.
- All data frames are the same size.

When fixed or dynamic size repeating frame data is transmitted onto the FPDP bus, the FPDP-TM must assert a /SYNC pulse while /DVALID is already asserted. The /SYNC pulse must be asserted at the same time as the last data item of every frame. The FPDP-RM and FPDP-R devices must recognize that the current data is the last data item in current frame when both /SYNC and /DVALID are asserted. Since /SYNC is asserted at the end of a frame, the first data frame transmitted will not be synchronized. As a result, the system designer may wish to discard this first unsynchronized data frame. All data frames are the same size when fixed size repeating frame data is transmitted.

### DYNAMIC SIZE REPEATING FRAME DATA

- Synchronization must occur prior to data to which it applies.
- Synchronization occurs at the same time the last data word in the block before is transferred.
- /SYNC must be asserted at the end of the data block while /DVALID is still asserted.
- Because synchronization occurs at the end of the data block, the first data block will not be synchronized.
- Synchronization occurs frequently.
- Data frames may vary in size.

For dynamic size repeating frame data, the behavior of the /SYNC pulse is the same as for fixed size repeating frame data, with the exception of varying sized frames.

## F.4 Serial FPDP Theory of Operation

The protocol and framing for Serial FPDP are listed in Appendix D. Serial FPDP operates similar to parallel FPDP with respect to maintaining data framing with the SYNC signal, but the SYNC signal does not correlate with data frames on the fiber. Any form of data framing listed in section F.3.2 can be mapped to Serial FPDP, since the data stream and SYNCs are maintained. However, the timing may not be exactly the same as the parallel FPDP version due to link framing overhead and the fact that the link operates asynchronously to the parallel FPDP frequencies.

## F.5 Parallel FPDP Signal Timing

Figure F-2 shows the timing for several FPDP interface signals. This figure is accurate for all four data framing types. See section F.3.2 for a discussion of framing. The Data Valid signal, /DVALID, is asserted by the FPDP-TM when valid data is transmitted onto the FPDP bus but not before at least 16 STROBE periods have occurred. The FPDP-TM must de-assert /DVALID when no more data remains in its buffer until valid data is again available. To avoid losing data when the receiver's FIFO is almost full, the receiver (FPDP-RM or FPDP-R) must assert the /SUSPEND signal to hold off the transmitter. The FPDP-TM must de-assert /DVALID within 16 STROBE periods and keep it de-asserted until /SUSPEND is de-asserted. Per the FPDP specification, after /SUSPEND is de-asserted, the FPDP-TM must wait for at least one STROBE period before re-asserting /DVALID. With the FibreXtreme SL240X card, after /SUSPEND is de-asserted, the FPDP-TM must wait for at least two STROBE periods before re-asserting /DVALID. The /SUSPEND signal is asynchronous to the STROBE clock and should be double synchronized by the FPDP-TM before being used in order to avoid metastability problems.

The FPDP-TM must not transmit data onto the FPDP bus until the Not Ready signal, /NRDY, is de-asserted by the FPDP-RM and FPDP-R devices. The FPDP-RM and FPDP-R devices must assert /NRDY when they are not ready to accept data and must de-assert /NRDY otherwise. The /NRDY signal is asynchronous to the STROBE clock and should be double synchronized by the FPDP-TM before being used in order to avoid metastability problems.

According to the *Front Panel Data Port Specifications, ANSI/VITA 17-1998,* the FPDP-TM transmits the Data Direction signal /DIR. FPDP-RM and FPDP-R devices may receive /DIR. The /DIR signal is not given a firm definition of use. Possible uses of this signal include providing a status indication available to be read by software or to allow operation to be inhibited until /DIR is asserted. The /DIR signal may be asynchronous with other FPDP signals. An SL240 FPDP-TM inverts and passes this signal from the link interface to the FPDP interface. An SL240 FPDP-R or FPDP-RM inverts and passes this signal from the FPDP interface to the link interface. DIR is an active-high signal on the link interface. /DIR is an active-low signal on the FPDP interface

Two user-defined Programmable I/O (PIO) signals, PIO1 and PIO2, are reserved in the *Front Panel Data Port Specifications*. These are auxiliary signals that are not required for core FPDP functions. However, these signals can be user-defined to allow the FPDP-TM, FPDP-RM, and FPDP-R devices to transfer information that is not part of the FPDP specifications. The FPDP-TM, FPDP-RM, and FPDP-R devices must not drive either of the PIO lines immediately at power up of the system. This is to avoid the possibility of two devices driving the same PIO line simultaneously and causing damage to the driver device.

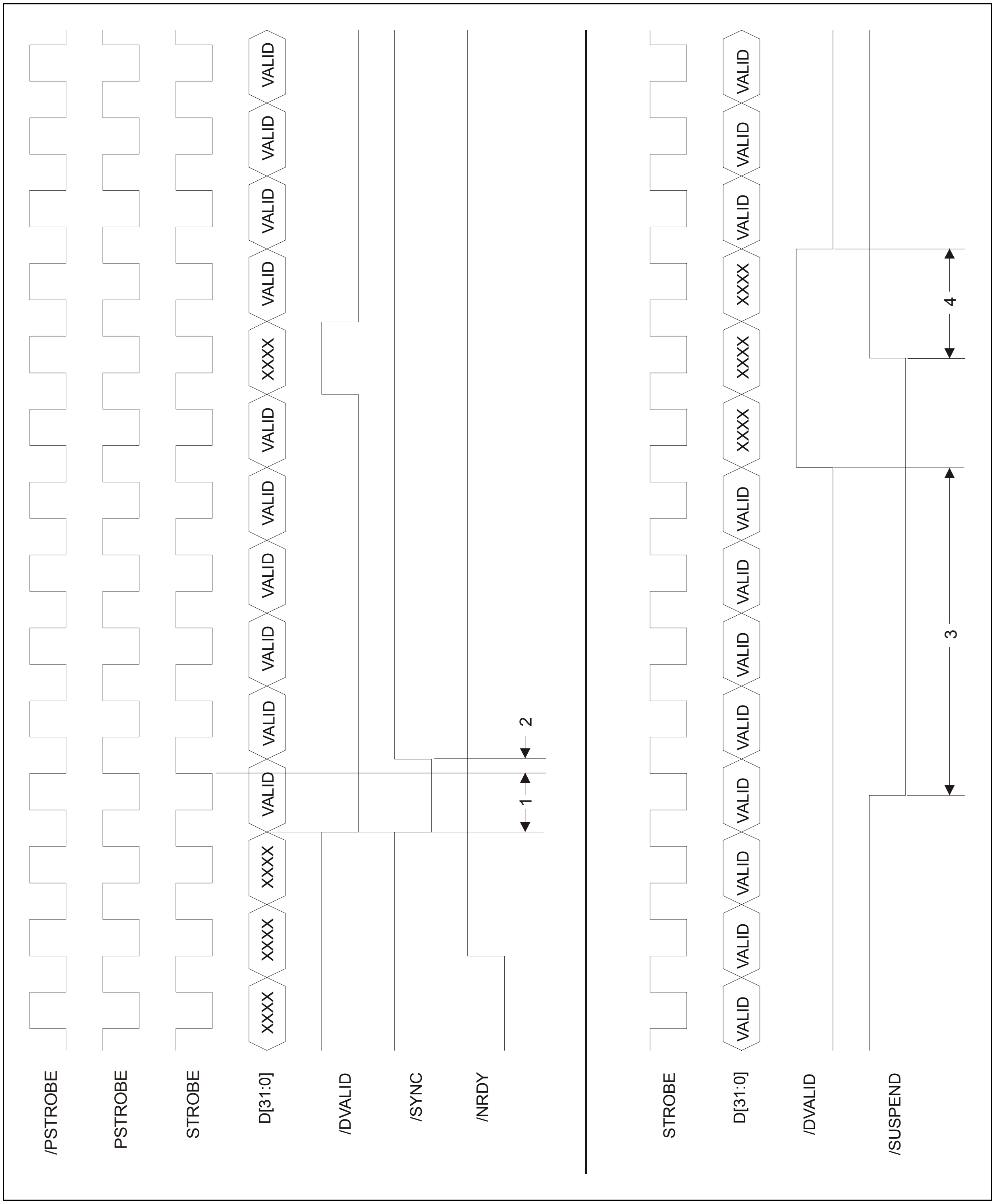


**Figure F-2 Parallel FPDP Interface Timing Diagram**

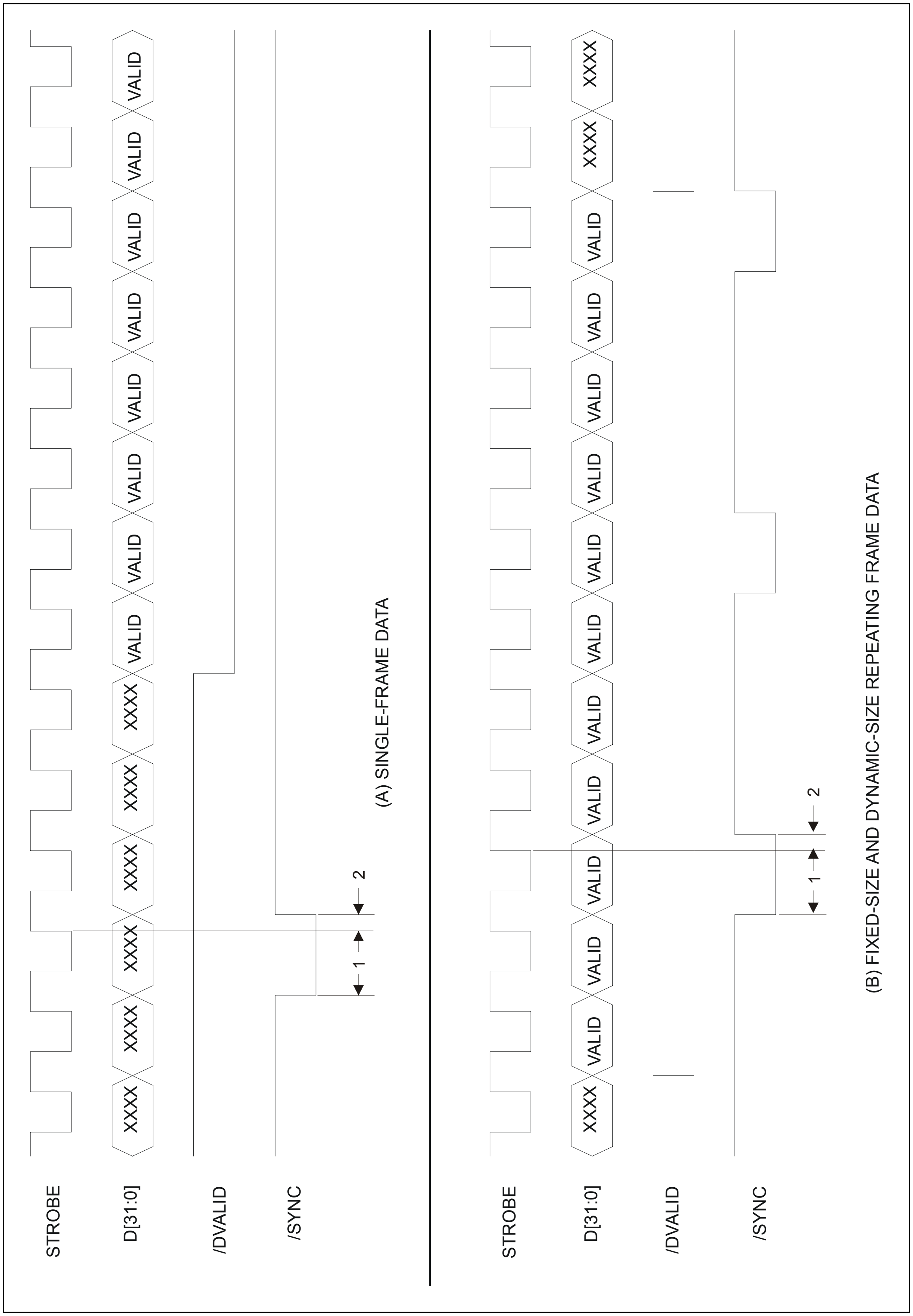


**Figure F-3 FPDP Timing Diagrams Showing the Use of Framing**

The timing parameters from Figures F-2 and F-3 are detailed in Tables F-1 and F-2. These timing specifications are taken from Front Panel Data Port Specifications, ANSI/VITA 17.

**Table F-1 Parallel FPDP Timing Specifications**

| Parameter | Description | At Transmitter End of Cable | At Receiver End of Cable | FPDP Clock Used |
|---|---|---|---|---|
| 1 | Data, /DVALID, /SYNC setup time | 6.0 ns min. | 5.0 ns min. | TTL |
| 1 | Data, /DVALID, /SYNC setup time | 5.5 ns min. | 4.5 ns min. | +/- PECL |
| | | | | |
| 2 | Data, /DVALID, /SYNC hold time | 12.8 ns min. | 11.8 ns min. | TTL |
| 2 | Data, /DVALID, /SYNC hold time | 12.0 ns min. | 11.0 ns min. | +/- PECL |

**Table F-2 FPDP Transmitter Interface Timing Specifications**

| Parameter | Description | Min | Max |
|---|---|---|---|
| 3 | **/SUSPEND** asserted to data stop | --- | 16 clocks |
| 4 | **/SUSPEND** de-asserted to data started | 1 clock | --- |

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# APPENDIX G

# REHOSTABLE CMC FPDP INTERFACE

## TABLE OF CONTENTS

# FIGURES



# TABLES

# G.1 Overview

The SL240X rehostable CMC FPDP card is easily integrated into custom sensor and DSP hardware. This section details the electrical, mechanical, and thermal requirements for the CMC card.

# G.2 Mechanical Details

The SL240X rehostable CMC FPDP card is a single CMC as defined in IEEE P1386. There is one deviation from this standard on the card—it includes a P6 connector not listed in the specification. This card complies with the height requirements defined in IEEE P1386. Figure G-1 shows the connector placement as well as other dimensions.

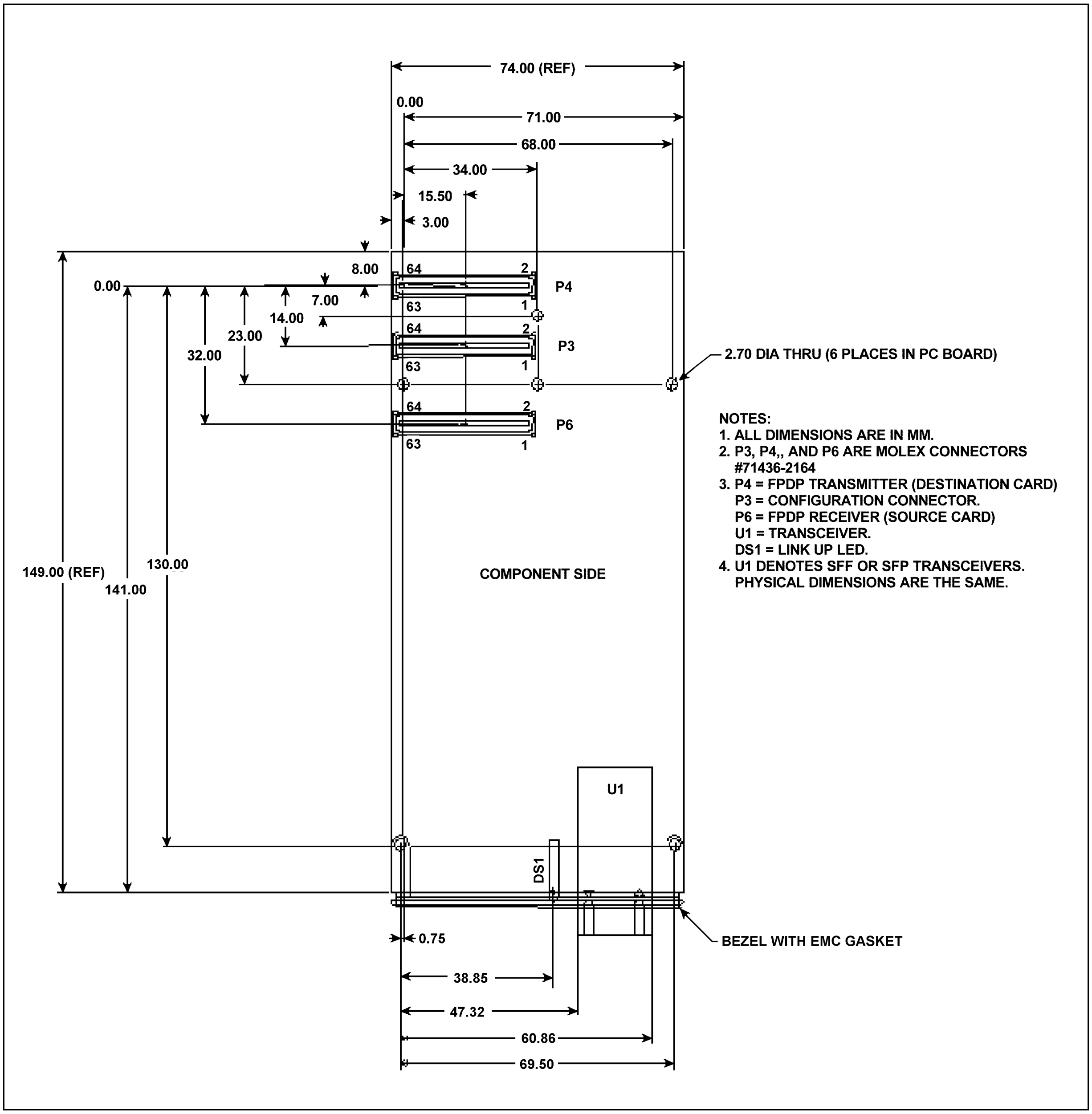


**Figure G-1 SL240X Rehostable CMC FPDP Card Dimensions**

# G.3 Terminology

The carrier cards and rehostable CMC FPDP cards are both bi-directional. However, the discussion below gives a point of reference for transmit and receive operations. As shown in Figure G-2 on a card acting as the data source, the FPDP interface acts as a receiver while the link interface acts as a transmitter. Conversely, for a card acting as a data destination, the FPDP interface acts as a transmitter while the link interface acts as a receiver. Therefore, throughout this manual, the term “FPDP receiver” is synonymous with “source card” and “FPDP transmitter” is synonymous with “destination card.”

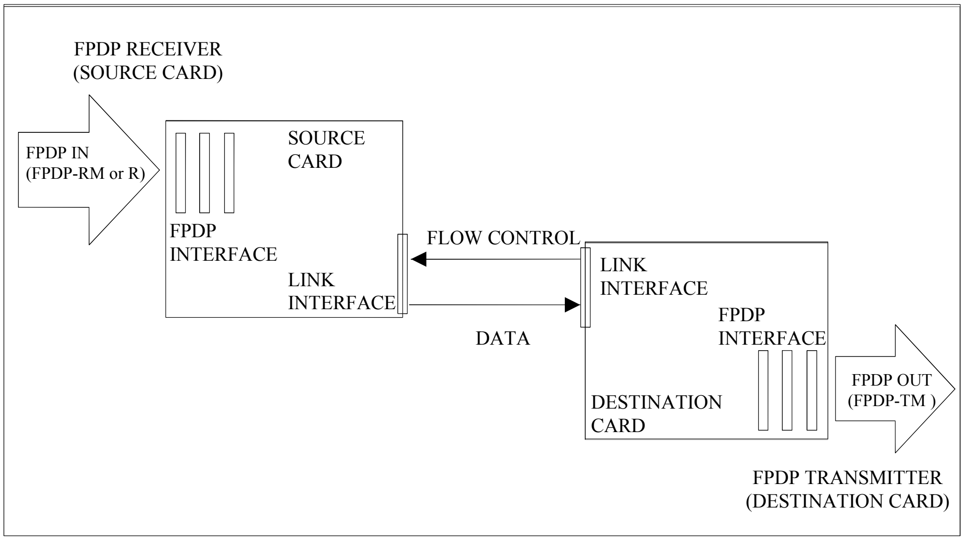


**Figure G-2 FPDP and SL240X Terminology**

# G.4 CMC Mating Connectors

The SL240X rehostable CMC card uses the 10 mm stacking height defined in IEEE P1386. There are several vendors for mating connectors for the CMC cards. Table G-1 lists the connectors verified by Curtiss-Wright Controls to work correctly.

**Table G-1 Connectors to Interface the SL240X Rehostable CMC Card**

| Manufacturer | Part number |
|---|---|
| Molex | 71439-0164 |
| AMP | 120521-1 |

## G.4.1 Configuration Signal Interconnects

SL240X rehostable CMC cards, whether used as source or destination cards, need to have the configuration connector wired. The configuration connector is in position P3. Table G-2 lists the signal assignments on that connector. Tie all RESERVED pins to a 10 kΩ resistor tied to ground. Table G-3 gives descriptions of these signals.

SL240X rehostable CMC cards may be installed on a custom carrier card instead of on a Curtiss-Wright Controls 6U VME or PCI carrier card. This custom carrier card may use a microcontroller to access the SL240X CMC card's register set. If a microcontroller is used, all pins listed in Table G-2 must be used. However, access to the register set is not mandatory to transmit and receive data through the SL240X CMC card. The SL240X rehostable CMC card will also work without a microcontroller on the carrier card. If no microcontroller is used, many of the pins listed in Table G-2 are not used and can be ignored or tied to a constant voltage level. The microcontroller-specific signals from Table G-2 are listed below.

- MCU_PRESENT_L
- ADS_L
- WEN_L
- REN_L
- INT_L
- SEL_L
- AD[15:0]
- MCLK
- CFG[1:0]

If a microcontroller is not used, the microcontroller-specific signals should be handled as shown below.

| | |
|---|---|
| MCU_PRESENT_L | Tie to +3.3 V through a 10k resistor |
| ADS_L | Tie to +3.3 V through a 10k resistor |
| WEN_L | Tie to +3.3 V through a 10k resistor |
| REN_L | Tie to +3.3 V through a 10k resistor |
| INT_L | Ignore. This is an output. |
| SEL_L | Tie to +3.3 V through a 10k resistor |
| AD[15:0] | Ignore. |
| MCLK | Tie to ground through a 10k resistor |
| CFG[1:0] | Tie to ground through a 10k resistor |

Even if the microcontroller interface is used, the ADS_L pin should still have an external pullup resistor. This external pullup resistor is a precaution to try to avoid the potential of simultaneous register reads and writes to the SL240X CMC card's FPGA if the other FPGA deploying the microcontroller interface is powered up at the same time. It is recommended to have the FPGA deploying the microcontroller interface initialize all of the SL240X CMC card's registers after all FPGAs are powered up to ensure all registers are set to the right values.

The configuration signals affected by MCU_PRESENT_L are CRC_EN, CLK_CFG[1:0], IGNORE_FC, and CONVERT_SYNC. If MCU_PRESENT_L is set to '0,' the configuration signals from the SL240X CMC card's register set are used. If MCU_PRESENT_L is set to '1,' the configuration signals from the P3 connector's pins are used.

**Table G-2 FPDP Configuration Interface (P3)**

| Pin | Input Lines | Output Lines | Pin | Input Lines | Output Lines |
|---|---|---|---|---|---|
| A1 | AD0 | AD0 | B2 | GND | |
| A3 | GND | | B4 | AD1 | AD1 |
| A5 | AD2 | AD2 | B6 | AD3 | AD3 |
| A7 | AD4 | AD4 | B8 | GND | |
| A9 | +3.3 V | | B10 | AD5 | AD5 |
| A11 | AD6 | AD6 | B12 | AD7 | AD7 |
| A13 | AD8 | | B14 | GND | |
| A15 | GND | | B16 | AD9 | |
| A17 | AD10 | | B18 | AD11 | |
| A19 | AD12 | | B20 | GND | |
| A21 | +3.3 V | | B22 | AD13 | |
| A23 | AD14 | | B24 | AD15 | |
| A25 | N.C. | N.C. | B26 | GND | |
| A27 | GND | | B28 | N.C | N.C. |
| A29 | PECL_IN | | B30 | N.C | N.C. |
| A31 | /PECL_IN | | B32 | GND | |
| A33 | GND | | B34 | N.C | N.C. |
| A35 | N.C. | N.C. | B36 | N.C. | N.C. |
| A37 | N.C. | N.C. | B38 | GND | |
| A39 | +3.3 V | | B40 | N.C. | N.C. |
| A41 | /SEL | | B42 | | /INT |
| A43 | /MCU_PRESENT | | B44 | GND | |
| A45 | GND | | B46 | /REN | |
| A47 | RESERVED | | B48 | /WEN | |
| A49 | CRC_EN | | B50 | GND | |
| A51 | GND | | B52 | /ADS | |
| A53 | CLK_CFG0 | | B54 | MCLK | |
| A55 | CLK_CFG1 | | B56 | GND | |
| A57 | +3.3 V | | B58 | CFG0 | |
| A59 | IGNORE_FC | | B60 | CFG1 | |
| A61 | CONVERT_SYNC | | B62 | GND | |
| A63 | GND | | B64 | RESERVED | |

Certain signals are important for the transmitter interface, while others are important only for the receive interface. In the following signal descriptions, a ‘1’ refers to a logic high level (above 2.0 V), while a ‘0’ refers to a logic low level (less than 0.8 V). All signals use the LVTTL Input/Output standard.

**Table G-3 Signal Descriptions for FPDP Configuration Interface (P3)**

| Signal Name | Signal Direction | Signal Description |
|---|---|---|
| AD[15:0] | AD[15:8] are input<br>AD[7:0] are Bi-directional | **Register Address/Data Bus**. This bus contains the address of the desired register and one byte of this register's data. The bit definitions for reads/writes are:<br>AD[15:13] = don't cares<br>AD[12:10] = register select<br>AD[9:8] = byte select<br>AD[7:0] = data<br>where<br>AD[12:10] CMC Register Accessed<br>000 0x00<br>001 0x04<br>010 0x08<br>011 0x0C<br>100 0x10<br>101 0x14<br>110 0x18<br>111 0x1C (not defined for SL100X/SL240X CMC register set)<br>AD[9:8] CMC Register Bits Accessed<br>00 7:0<br>01 15:8<br>10 23:16<br>11 31:24<br>When a register read is performed, AD[15:8] = "00000000" is read back. For register reads/writes, the register bits are shown in AD[7:0] in the following bit order: 31:24, 23:26, 15:8, 7:0. This does not mean the most significant byte must be accessed first and the least significant byte must be accessed last. The byte accessed is determined solely by AD[9:8]. See section G-9, microcontroller Interface, for details. |
| /ADS | Input | **Address Strobe**. Set to '0' to enable register access. Set to '1' to disable register access. See section G-9, microcontroller Interface, for details. |
| CFG[1:0] | Input | **Configuration Bus**. These are the configuration signals for the microcontroller interface. These are reserved for future expansion, and should be driven as "00". |

<table>
<tr><th>Signal Name</th><th>Signal Direction</th><th>Signal Description</th></tr>
<tr><td>CLK_CFG0<br>CLK_CFG1</td><td>Input</td><td>FPDP-TM Clock Configuration. Controls the FPDP transmitter clock frequency. The FPDP transmitter clock is the reference clock (53.125 MHz or 125 MHz) divided by 2, 3, 4, or 6. The clock divisions available for standard cards are:
<table>
<tr><th>CLK_CFG0</th><th>CLK_CFG1</th><th>SL100X (53.125 MHz)</th><th>SL240X (125 MHz)</th></tr>
<tr><td>0</td><td>0</td><td>26.5625 MHz</td><td>62.5 MHz</td></tr>
<tr><td>0</td><td>1</td><td>13.2813 MHz</td><td>31.25 MHz</td></tr>
<tr><td>1</td><td>0</td><td>17.7083 MHz</td><td>41.6667 MHz</td></tr>
<tr><td>1</td><td>1</td><td>8.8542 MHz</td><td>20.8333 MHz</td></tr>
</table></td></tr>
<tr><td>CONVERT_SYNC</td><td>Input</td><td>Convert Sync. If /MCU_PRESENT is asserted, this value is ignored and the internal register value is used. Set to ‘0’ for all FPDP operations. When set to ‘1,’ a SYNC without DVALID is appended after every SYNC with DVALID from the link.</td></tr>
<tr><td>CRC_EN</td><td>Input</td><td>CRC Enable. If /MCU_PRESENT is asserted, this value is ignored and the internal register value is used. Set to ‘1’ to enable CRC checking/generation of link data. Set to ‘0’ to disable CRC checking/generation.<br>NOTE: CRC should be used in almost all applications. It offers excellent coverage of data errors and has very little impact on link throughput for maximum frame sizes. The option of disabling CRC is only retained for compatibility with older third-part devices. Both nodes on the link (or all nodes in a loop configuration) should be set to a common CRC mode or the resulting mismatch will cause data errors and/or link errors.</td></tr>
<tr><td>IGNORE_FC</td><td>Input</td><td>Ignore Flow Control. If /MCU_PRESENT is asserted, this value is ignored and the internal register value is used. Set to ‘1’ to ignore flow control from the remote end and continue transmitting when the link is down. Set to ‘0’ to stop transmission when the link goes down or when the remote end is sending a STOP ordered set back.<br>NOTE: In almost every application, flow control should be enabled. Even if the application must sustain maximum link throughput, it is better to drop the data at the sending source should the system experience a temporary overload condition. Some exotic conditions could apply where flow control is not desirable, but they require very careful system planning and should be confirmed with Curtiss-Wright Controls prior to architectural finalization. One possible exception is for applications that cannot utilize a duplex fiber-optic link, which means status information (link up and state of flow control) is not available from the remote node. In this circumstance, flow control should be disabled to allow the transmitter to function without the receiver connected normally.</td></tr>
<tr><td>/INT</td><td>Output</td><td>Interrupt. A ‘0’ indicates an interrupt occurred. A ‘1’ indicates no interrupt has occurred.</td></tr>
</table>

| Signal Name | Signal Direction | Signal Description |
|---|---|---|
| MCLK | Input | **microcontroller Clock**. This is the clock for the microcontroller interface. Its frequency should be less than 30 MHz and should never be disabled if the microcontroller interface is being used. See section G-9, microcontroller Interface, for details. |
| /MCU_PRESENT | Input | **microcontroller Present**. Set to ‘0’ to use configuration signals from the microcontroller interface. Set to ‘1’ to use configuration signals from the P3 connector. |
| /REN | Input | **Read Enable**. microcontroller read enable. See section G-9, microcontroller Interface, for details. |
| /WEN | Input | **Write Enable**. microcontroller write enable. See section G-9, microcontroller Interface, for details. |
| /SEL | Input | **microcontroller Select**. microcontroller select. See section G-9, microcontroller Interface, for details. |
| PECL_IN | Input | **Reference Clock Input**. Reference clock for custom applications. This clock is not used on standard cards. |
| /PECL_IN | Input | **Reference Clock Input**. Reference clock for custom applications. This clock is not used on standard cards. |

## G.4.2 Source Card Signal Interconnects

A source card for the system has to have the P3 interface and the P6 interface wired for operation. The P6 connector is the FPDP receiver interface.

Table G-4 lists the signal connections for the P6 connector. An asterisk “*” is used to designate signals that are common on the P4 and P6 connectors. All RESERVED pins should be tied to a 10 kΩ resistor tied to ground. Table G-5 gives descriptions of these signals. Figure G-3 provides a visual description of notes 1 and 2.

**WARNING**: PIO1_IN and PIO2_IN are shared between the transmit and receive FPDP connectors on the rehostable CMC FPDP card. Do not drive PIO1_IN and PIO2_IN on the transmit and receive connectors with different voltage levels. Doing so may damage the circuit or the CMC FPDP card.

**NOTE 1**: /RDIR, PIO1_IN, PIO2_IN, and /TNRDY are encoded into the Serial FPDP data stream by the encoder logic at the appropriate time during the framing sequence. To guarantee a pulse on these signals is propagated to the remote Serial FPDP receiver, the pulse width must be equal to or greater than the maximum time between the respective ordered sets, which is 521 reference clock periods (up to 512 words of data in each frame with an overhead of up to nine ordered sets). The reference clock is typically driven by an on-board oscillator. The standard reference clock frequency for SL100X is 53.125 MHz, while the standard reference clock frequency for SL240X is 125 MHz. These signals do not propagate through the Transmit FIFO within the SL100X/SL240X CMC card and thus cannot be directly associated with the corresponding data. Their use is not affected by the state of the Disable Transmitter bit in the Link Control register. Thus, /RDIR, PIO1_IN, PIO2_IN, and /TNRDY are transmitted onto the link regardless of if the transmission of link data is enabled.

In non-loop operation (LWRAP = ‘0’ in the Link Control register), /RDIR, PIO1_IN, PIO2_IN, and /TNRDY are directly inserted into the Serial FPDP data stream based on the values of the signals from the FPDP interface. If Loop (or Copy) mode is selected (LWRAP = ‘1’), the values of PIO1_IN and PIO2_IN are retransmitted according to their received link values and the values of /RDIR and /TNRDY are used as follows: if the receive interface is enabled (Disable Receiver = ‘0’ in the Link Control register), the values transmitted are the received link values logically ORed with the FPDP-interface values; otherwise, the values are retransmitted according to their received link values. The use of /RDIR and /TNRDY is consistent with the use of flow control (retransmission of a STOP request) for loop operations. See the ANSI/VITA 17.1 Serial FPDP specification for additional details.

**NOTE 2**: /TDIR, PIO1_OUT, PI02_OUT, and /RNRDY are decoded from the Serial FPDP data stream by the decoder logic and are latched based on the last value received by the data stream. These signals do not propagate through the Receive FIFO within the SL100X/SL240X CMC card and thus cannot be directly associated with the corresponding data. Their use is not affected by the state of the Disable Receiver bit in the Link Control register. Thus, /TDIR, PIO1_OUT, PIO2_OUT, and /RNRDY are received from the link regardless of if the reception of link data is enabled.

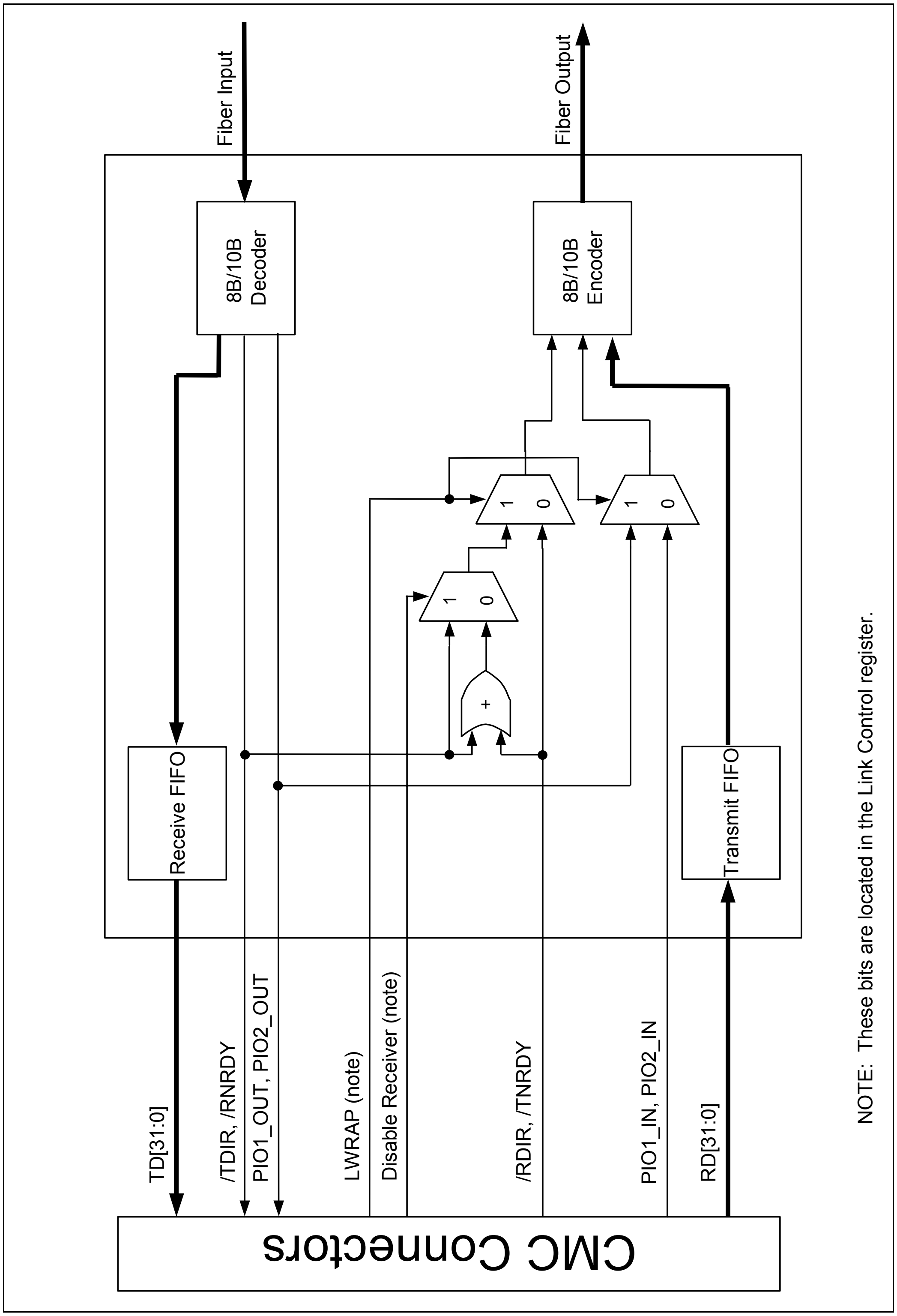


**Figure G-3 Signal Flow of PIO1, PIO2, DIR, and NRDY Through an SL100X/SL240X CMC Card**

**Table G-4 FPDP Receiver Interface (P6)**

| Pin | Input Lines | Output Lines | Pin | Input Lines | Output Lines |
|---|---|---|---|---|---|
| A1 | PIO2_IN* | | B2 | | PIO2_OUT* |
| A3 | +5 V** | | B4 | PIO1_IN* | |
| A5 | | RERROR | B6 | | PIO1_OUT* |
| A7 | | /RNRDY | B8 | GND | |
| A9 | GND | | B10 | | /RSUSPEND |
| A11 | RSTROBE | | B12 | GND | |
| A13 | GND | | B14 | /RDVALID | |
| A15 | /RESET* | | B16 | GND | |
| A17 | | RESERVED | B18 | /RDIR | |
| A19 | /RSYNC | | B20 | | RESERVED |
| A21 | RD31 | | B22 | +5 V** | |
| A23 | GND | | B24 | RD30 | |
| A25 | RD29 | | B26 | RD28 | |
| A27 | RD27 | | B28 | GND | |
| A29 | RD26 | | B30 | RD25 | |
| A31 | GND | | B32 | RD24 | |
| A33 | RD23 | | B34 | RD22 | |
| A35 | RD21 | | B36 | GND | |
| A37 | RD20 | | B38 | RD19 | |
| A39 | +5 V** | | B40 | RD18 | |
| A41 | RD17 | | B42 | RD16 | |
| A43 | RD15 | | B44 | GND | |
| A45 | RD14 | | B46 | RD13 | |
| A47 | GND | | B48 | RD12 | |
| A49 | RD11 | | B50 | RD10 | |
| A51 | RD9 | | B52 | +5 V** | |
| A53 | RD8 | | B54 | RD7 | |
| A55 | GND | | B56 | RD6 | |
| A57 | RD5 | | B58 | RD4 | |
| A59 | RD3 | | B60 | GND | |
| A61 | RD2 | | B62 | RD1 | |
| A63 | +5 V** | | B64 | RD0 | |

* These signals are common on the P4 and P6 connectors.

** SL100X/SL240X CMC cards do not require 5 VDC. However, Curtiss-Wright Controls recommends supplying 5 VDC to P4 and P6 connectors.

Certain signals are important for the transmitter interface, while others are important only for the receive interface. In the following signal descriptions, a ‘1’ refers to a logic high level (above 2.0 V), while a ‘0’ refers to a logic low level (less than 0.8 V). All signals use the LVTTL Input/Output standard.

**Table G-5 Signal Descriptions for FPDP Receiver Interface (P6)**

| Signal Name | Signal Direction | Signal Description |
|---|---|---|
| RD[31:0] | Input | **Receive Data Bus**. This is data from the FPDP interface to the Transmit FIFO of the SL240X card. It is placed in the Transmit FIFO on a rising edge of RSTROBE with /RDVALID asserted. |
| /RDIR | Input | **Receive Data Direction**. This is the data direction signal from the FPDP interface. It has no affect on SL240X card operation. See note 1 for additional information on its operation. |
| /RDVALID | Input | **Receive Data Valid**. Set to ‘0’ to place the data on the RD[31:0] bus in the Transmit FIFO of the SL240X card on this clock. Set to ‘1’ to not place the data on the RD[31:0] bus in the Transmit FIFO. |
| RERROR | Output | **Receive Error**. A ‘1’ indicates the link interface is down and flow control is not ignored (IGNORE_FC = ‘0’); A ‘0’ indicates the error has not occurred. RERROR is asserted for at least four RSTROBE periods. |
| /RNRDY | Output | **Receive Not Ready**. A ‘0’ indicates the FPDP receiver is not ready to accept data. A ‘1’ indicates the FPDP receiver is ready to accept data. /RDVALID or /RSYNC should not be asserted while /RNRDY is asserted. See note 2 for additional information on its operation. |
| PIO1_IN | Input | **Programmable I/O 1**. This is a user-defined input that is passed straight to the encoder interface and embedded in the data stream. This input line is shared with the FPDP transmitter interface (P4). See note 1 for additional information on its operation. |
| PIO2_IN | Input | **Programmable I/O 2**. This is a user-defined input that is passed straight to the encoder interface and embedded in the data stream. This input line is shared with the FPDP transmitter interface (P4). See note 1 for additional information on its operation. |
| PIO1_OUT | Output | **Programmable I/O 1**. This is a user-defined output that is removed from the data stream at the decoder interface. This output line is shared with the FPDP transmitter interface (P4). See note 2 for additional information on its operation. |
| PIO2_OUT | Output | **Programmable I/O 2**. This is a user-defined output that is removed from the data stream at the decoder interface. This output line is shared with the FPDP transmitter interface (P4). See note 2 for additional information on its operation. |
| /RESET | Input | **Global Reset**. Set to ‘0’ to perform a global reset of the SL240X card including state machines, FIFOs, and output signals. Set to ‘1’ for normal operation. For a power-on reset, /RESET must be asserted for at least 10 ms after the power has reached 4.5 V. Any time /RESET is asserted after a valid power level has been achieved, the reset is asynchronous and /RESET must be asserted for at least 150 ns. This signal is common with the FPDP transmitter interface (P4). |
| RSTROBE | Input | **FPDP Receiver Clock**. This is the clock input for the receiver interface. All receiver signals are timed off the rising edge of this clock. RSTROBE should be a free-running clock. Allowable frequencies are 0-90 MHz. RSTROBE is terminated on the CMC card as shown in Figure G-4. |
| /RSUSPEND | Output | **Receive Suspend**. This signal asserts flow control from the SL240X card. A ‘0’ indicates the SL240X card’s Transmit FIFO has room for not more than 16 data words. A ‘1’ indicates there is room for more than 16 data words in the Transmit FIFO. |
| /RSYNC | Input | **Receive Synchronization**. Set to ‘0’ to assert /RSYNC. This signal is used for framing data or synchronizing source and destination nodes. It will remain synchronized with the data stream. The default value of /RSYNC is ‘0.’ Do not leave this signal float or tie it to ‘0.’ If it is continually ‘0,’ link throughput is dramatically decreased since every Serial FPDP frame will be a SYNC with DATA frame, which contains only one data word. |

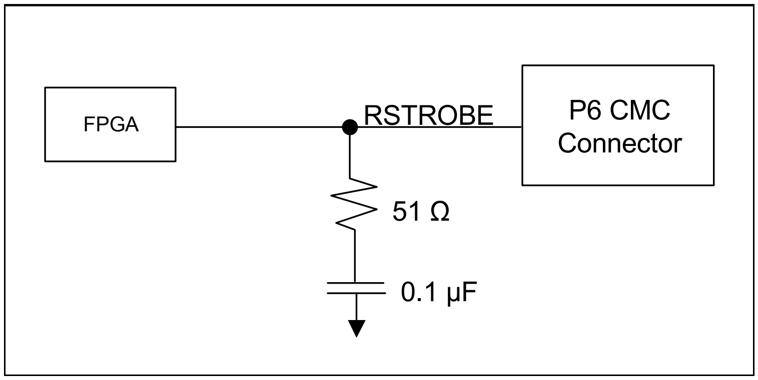


**Figure G-4 RSTROBE Termination on the CMC Card**

## G.4.3 Destination Card Signal Interconnects

A destination card for the system must have the P3 interface and the P4 interface wired for operation. The P4 connector is the FPDP transmitter interface.

Table G-6 lists the signal connections for the P4 connector. An asterisk "*" is used to designate signals that are common on the P4 and P6 connectors. Table G-7 gives descriptions of these signals. Figure G-5 provides a visual description of notes 1 and 2.

**WARNING**: PIO1_IN and PIO2_IN are shared on the transmit and receive FPDP connectors on the rehostable CMC FPDP card. Do not drive PIO1_IN and PIO2_IN on the transmit and receive connectors with different voltage levels. Doing so may damage the circuit or the CMC FPDP card.

**NOTE 1**: /RDIR, PIO1_IN, PIO2_IN, and /TNRDY are encoded into the Serial FPDP data stream by the encoder logic at the appropriate time during the framing sequence. To guarantee a pulse on these signals is propagated to the remote Serial FPDP receiver, the pulse width must be equal to or greater than the maximum time between the respective ordered sets, which is 521 reference clock periods (up to 512 words of data in each frame with an overhead of up to nine ordered sets). The reference clock is typically driven by an on-board oscillator. The standard reference clock frequency for SL100X is 53.125 MHz, while the standard reference clock frequency for SL240X is 125 MHz. These signals do not propagate through the Transmit FIFO within the SL100X/SL240X CMC card and thus cannot be directly associated with the corresponding data. Their use is not affected by the state of the Disable Transmitter bit in the Link Control register. Thus, /RDIR, PIO1_IN, PIO2_IN, and /TNRDY are transmitted onto the link regardless of if the transmission of link data is enabled.

In non-loop operation (LWRAP = '0' in the Link Control register), /RDIR, PIO1_IN, PIO2_IN, and /TNRDY are directly inserted into the Serial FPDP data stream based on the values of the signals from the FPDP interface. If Loop (or Copy) mode is selected (LWRAP = '1'), the values of PIO1_IN and PIO2_IN are retransmitted according to their received link values and the values of /RDIR and /TNRDY are used as follows: if the receive interface is enabled (Disable Receiver = '0' in the Link Control register), the values transmitted are the received link values logically ORed with the FPDP-interface values; otherwise, the values are retransmitted according to their received link values. The use of /RDIR and /TNRDY is consistent with the use of flow control (retransmission of a STOP request) for loop operations. See the ANSI/VITA 17.1 Serial FPDP specification for additional details.

**NOTE 2**: /TDIR, PIO1_OUT, PI02_OUT, and /RNRDY are decoded from the Serial FPDP data stream by the decoder logic and are latched based on the last value received by the data stream. These signals do not propagate through the Receive FIFO within the SL100X/SL240X CMC card and thus cannot be directly associated with the corresponding data. Their use is not affected by the state of the Disable Receiver bit in the Link Control register. Thus, /TDIR, PIO1_OUT, PIO2_OUT, and /RNRDY are received from the link regardless of if the reception of link data is enabled.

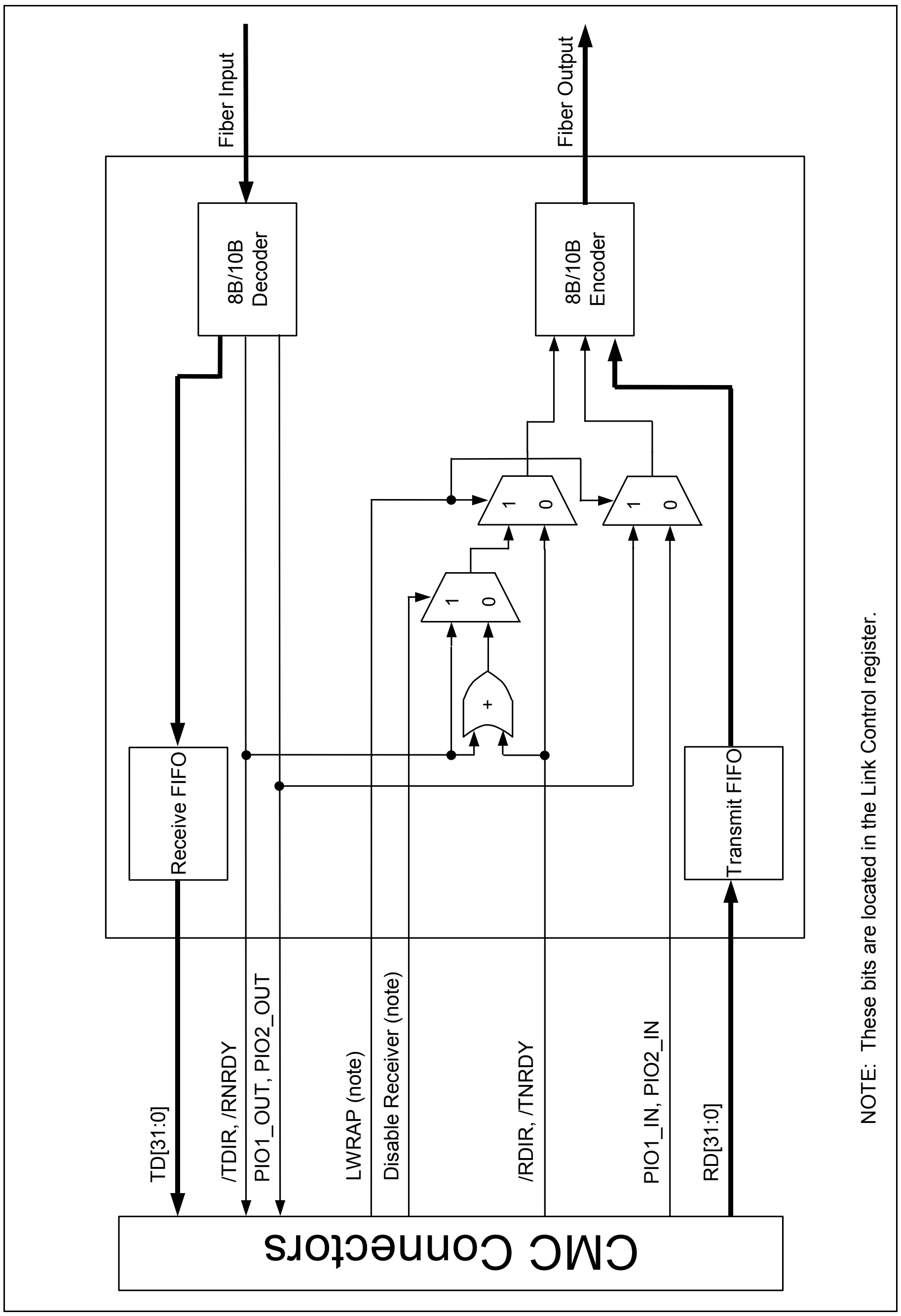


**Figure G-5 Signal Flow of PIO1, PIO2, DIR, and NRDY Through an SL100X/SL240X CMC Card**

**Table G-6 FPDP Transmitter Interface (P4)**

| Pin | Input Lines | Output Lines | Pin | Input Lines | Output Lines |
|---|---|---|---|---|---|
| A1 | | TD0 | B2 | N.C. | N.C. |
| A3 | | TD1 | B4 | GND | |
| A5 | +5 V** | | B6 | +5 V** | |
| A7 | | TD2 | B8 | | TD3 |
| A9 | | TD4 | B10 | | TD5 |
| A11 | | TD6 | B12 | | TD7 |
| A13 | | TD8 | B14 | | TD9 |
| A15 | GND | | B16 | | TD10 |
| A17 | GND | | B18 | GND | |
| A19 | | TD11 | B20 | | TD12 |
| A21 | | TD13 | B22 | | TD14 |
| A23 | | TD15 | B24 | | TD16 |
| A25 | | TD17 | B26 | | TD18 |
| A27 | | TD19 | B28 | GND | |
| A29 | +5 V** | | B30 | +5 V** | |
| A31 | | TD20 | B32 | | TD21 |
| A33 | | TD22 | B34 | | TD23 |
| A35 | GND | | B36 | | TD24 |
| A37 | GND | | B38 | | TD25 |
| A39 | | TD26 | B40 | | TD27 |
| A41 | | TD28 | B42 | GND | |
| A43 | GND | | B44 | | TD29 |
| A45 | | TERROR | B46 | | TD30 |
| A47 | /RESET* | | B48 | | TD31 |
| A49 | +5 V** | | B50 | | PIO2_OUT* |
| A51 | | /TSYNC | B52 | GND | |
| A53 | | /TDIR | B54 | +5 V** | |
| A55 | | /TDVALID | B56 | PIO2_IN* | |
| A57 | /TSUSPEND | | B58 | | PIO1_OUT* |
| A59 | GND | | B60 | GND | |
| A61 | /TNRDY | | B62 | GND | |
| A63 | | TSTROBE | B64 | PIO1_IN* | |

* These signals are common on the P4 and P6 connectors.

** SL100X/SL240X CMC cards do not require 5 VDC. However, Curtiss-Wright Controls recommends supplying 5 VDC to P4 and P6 connectors.

Certain signals are important for the transmitter interface, while others are important only for the receive interface. In the following signal descriptions, a '1' refers to a logic high level (above 2.0 V), while a '0' refers to a logic low level (less than 0.8 V). All signals use the LVTTL Input/Output standard.

**Table G-7 Signal Descriptions for FPDP Transmitter Interface (P4)**

<table>
<tr><th>Signal Name</th><th>Signal Direction</th><th>Signal Description</th></tr>
<tr><td>TD[31:0]</td><td>Output</td><td>Transmit Data Bus. This is data from the Receive FIFO of the SL240X card to the FPDP interface. It is clocked out of the Receive FIFO synchronously to TSTROBE with /TDVALID asserted.</td></tr>
<tr><td>/TDIR</td><td>Output</td><td>Transmit Data Direction. This is the data direction signal to the FPDP interface. See note 2 for additional information on its operation.</td></tr>
<tr><td>/TDVALID</td><td>Output</td><td>Transmit Data Valid. A '0' indicates data on the TD[31:0] bus is valid. A '1' indicates data on the TD[31:0] bus is not valid.</td></tr>
<tr><td>TERROR</td><td>Output</td><td>Transmit Error. A '1' indicates any of the following items has occurred:<ul><li>Receive FIFO overflow;</li><li>The link interface is down;</li><li>CRC Error;</li><li>8B/10B decoding error;</li></ul>TERROR is asserted for at least four TSTROBE periods. These four error conditions are logically ORed together. They are given unique bits in the Link Status register if the register set is being used. A '0' indicates none of the above errors have occurred.<br>NOTE: There is no guaranteed timing between TERROR with respect to /TDVALID and /TSYNC. Also, there is no guarantee that TERROR will occur no later than 'x' clock ticks after a /TSYNC pulse. In this case, 'x' cannot be quantified and guaranteed. Data is still placed into the Receive FIFO if an error is detected. There is no real indication where the error occurred.</td></tr>
<tr><td>/TNRDY</td><td>Input</td><td>Transmit Not Ready. Set to '0' to tell the FPDP interface that the FPDP receiver is not ready to accept data yet. This signal is encoded and sent over the link interface. Set to '1' to tell the FPDP interface that the FPDP receiver is ready to accept data. See note 1 for additional information on its operation.</td></tr>
<tr><td>PIO1_IN</td><td>Input</td><td>Programmable I/O 1. This is a user-defined input that is passed straight to the encoder interface and embedded in the data stream. This input line is shared with the FPDP receiver interface (P6). See note 1 for additional information on its operation.</td></tr>
<tr><td>PIO2_IN</td><td>Input</td><td>Programmable I/O 2. This is a user-defined input that is passed straight to the encoder interface and embedded in the data stream. This input line is shared with the FPDP receiver interface (P6). See note 1 for additional information on its operation.</td></tr>
<tr><td>PIO1_OUT</td><td>Output</td><td>Programmable I/O 1. This is a user-defined output that is removed from the data stream at the decoder interface. This output line is shared with the FPDP receiver interface (P6). See note 2 for additional information on its operation.</td></tr>
<tr><td>PIO2_OUT</td><td>Output</td><td>Programmable I/O 2. This is a user-defined output that is removed from the data stream at the decoder interface. This output line is shared with the FPDP receiver interface (P6). See note 2 for additional information on its operation.</td></tr>
<tr><td>/RESET</td><td>Input</td><td>Global Reset. Set to '0' to perform a global reset of the SL240X card including state machines, FIFOs, and output signals. Set to '1' for normal operation. For a power-on reset, /RESET must be asserted for at least 10 ms after the power has reached 4.5 V. Any time /RESET is asserted after a valid power level has been achieved, the reset is asynchronous and /RESET must be asserted for at least 150 ns. This signal is common with the FPDP receiver interface (P6).</td></tr>
</table>

| Signal Name | Signal Direction | Signal Description |
|---|---|---|
| TSTROBE | Output | **FPDP Transmitter Clock Output.** This is a clock-divided version of the reference clock (53.125 MHz or 125 MHz). This clock's frequency is determined by CLK_CFG[1:0]. All signals sent to the FPDP interface are synchronized to this clock. |
| /TSUSPEND | Input | **Transmit Suspend.** This signal asserts flow control to the FPDP interface. It should be set to '0' when the FPDP receiver has less than two words of space left in its receive FIFO. Otherwise, set to '1'. Data will not start transmitting if /TSUSPEND is set to '0'. |
| /TSYNC | Output | **Transmit Synchronization.** This signal is a '0' when a /TSYNC is clocked out of the Receive FIFO. Otherwise, it is a '1'. The transmitter at the remote end determines if /TSYNC with /TDVALID or /TSYNC without /TDVALID is sent. |

# G.5 Programmed Inputs/Outputs (PIOs)

The PIO1_IN, PIO2_IN and /RESET inputs to the rehostable CMC FPDP card are shared between the transmit (P4) and receive (P6) interfaces. These signals should always be driven from the same source to avoid logic contention and possible damage to the hardware. The PIO1_OUT and PIO2_OUT signals are also shared between the P4 and P6 connectors. Figure G-6 shows the connection of these signals on the CMC card.

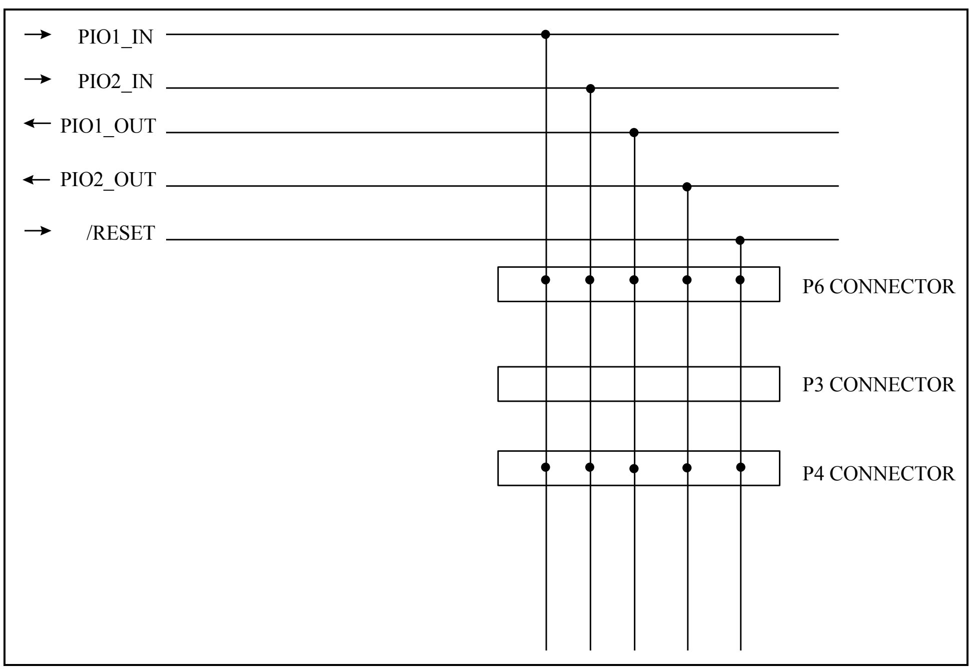


**Figure G-6 PIO Line Interconnectivity**

The state of the PIO lines is transmitted across the link interface, embedded in the Start Of Frame (SOF) ordered set. Refer to Appendix D, SL100X/SL240X Protocol, for more information.

# G.6 Thermal Specifications

The SL240X rehostable CMC card stays within the thermal specifications of IEEE P1386. Airflow is recommended for the card, though operation at 0 to 50°C ambient is feasible without airflow. Components on this card may become very warm during operation. Care should be taken to ensure this does not disturb other cards in the system.

# G.7 Electrical Specifications

## G.7.1 DC Characteristics

The signaling interface on the SL240X rehostable CMC card is a 5 V tolerant, 3.3 V signaling interface. Table G-8 lists some of the electrical parameters for this interface.

**Table G-8 DC Characteristics**

| Parameter | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 2.0 | 5.5 | V |
| $V_{IL}$ | Input Low Voltage | -0.5 | 0.8 | V |
| $I_I$ | Input Leakage Current | -10 | 10 | µA |
| $V_{OH}$ | Output High Voltage | 2.4 | 3.3 | V |
| $V_{OL}$ | Output Low Voltage | --- | 0.4 | V |
| $I_{OH}$ | Output High Current | --- | -24 | mA |
| $I_{OL}$ | Output Low Current | --- | 24 | mA |

The power on sequence for the card should guarantee /RESET is asserted for a minimum of 10 ms after the power has reached 4.5 V. This allows the local oscillators sufficient time to begin operation, as well as reset overhead for the card. Any time /RESET is asserted after a valid power level has been achieved, the reset is asynchronous and /RESET must be asserted for at least 150 ns.

## G.7.2 AC Characteristics

Table G-9 and Table G-10 contain the major timing components involved with interfacing the SL240X rehostable CMC card. Table G-9 provides timing parameters for the source side. Table G-10 provides timing parameters for the destination side. Bi-directional cards must meet the timing parameters in both Table G-9 and Table G-10.

**Table G-9 Source Card AC Characteristics**

| Signal | Min. | Max. | Units |
|---|---|---|---|
| Receiver STROBE | --- | 70 | MHz |
| Data D[31:0] setup | 5 | --- | ns |
| /DVALID setup | 5 | --- | ns |
| /SYNC setup | 5 | --- | ns |

**Table G-10 Destination Card AC Characteristics**

| Signal | Min. | Max. | Units |
|---|---|---|---|
| Data D[31:0] clock-to-out | --- | 9 | ns |
| /DVALID clock-to-out | --- | 9 | ns |
| /SYNC clock-to-out | --- | 9 | ns |

**NOTE**: The delay listed in the destination card characteristics is the clock-to-out delay of the signals. The setup time on buffers receiving this signal should be:

$$\text{time}_{setup} < \left( \frac{1}{\text{Transmitter Strobe}} \right) - \text{Delay}$$

For example, if the strobe is 40 MHz, the clock period is 25 ns. Therefore, the setup time should be less than 25 ns – 9 ns = 16 ns.

# G.8 Transmitting Data

Data is transmitted through the FPDP interface. Figure G-4 shows the timing for a few of these transactions. In addition to this appendix, see Appendix F, FPDP Primer, for details about these signals.

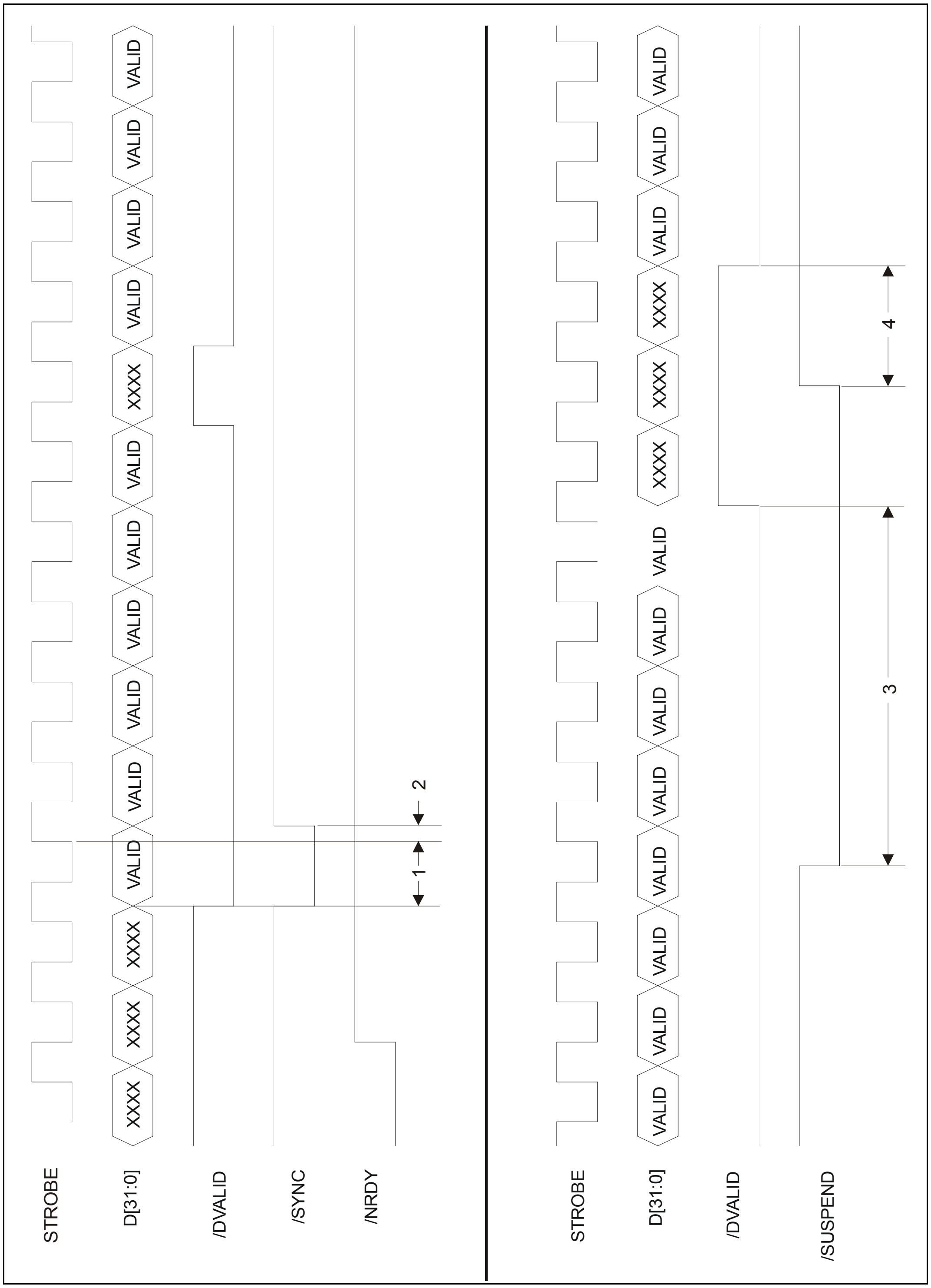


**Figure G-7 Parallel FPDP Interface Timing Diagram**

**Table G-11 FPDP Transmitter Interface Timing Parameters**

| Parameter | Description | Min | Max |
|---|---|---|---|
| 1 | Data, **/DVALID**, **/SYNC** setup time | 5 ns | --- |
| 2 | Data, **/DVALID**, **/SYNC** hold time | 0 ns | --- |
| 3 | **/SUSPEND** asserted to data stop | --- | 16 clocks |
| 4 | **/SUSPEND** de-asserted to data started | 1 clock | --- |

## G.9 Microcontroller Interface

The microcontroller interface on the SL240X CMC card is used to access the internal control and status registers. This provides the same flexibility as the PCI based cards, but without actually requiring a full PCI bus. This bus only has one valid configuration defined, which is designed for 8-bit microcontrollers and PLDs. The register map in Appendix B contains the contents and offsets of these registers. Burst operations are not permitted on this interface.

To read from the registers, three clock cycles are needed. The first clock cycle is used to transfer the address to the CMC card. The second clock cycle is used as a turn-around cycle for the bus, since it can be driven from bi-directional bus interfaces. On the third clock cycle, the data is actually transferred back to the initiator. Figure G-8 shows a single read from the registers.

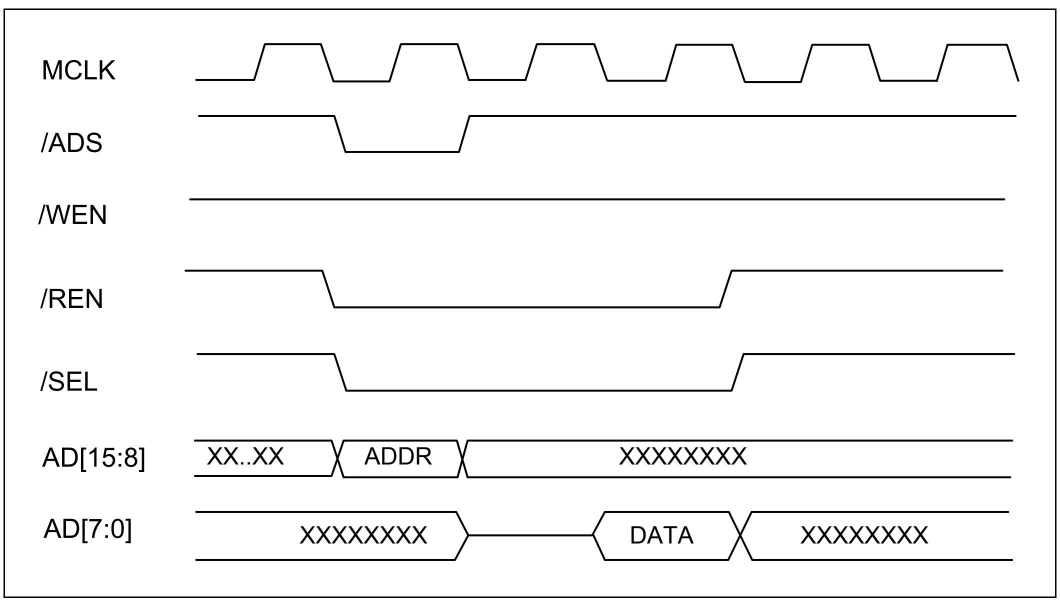


**Figure G-8 Microcontroller Single Read**

To write to the registers, three clock cycles are needed. The first clock cycle is used to transfer the address to the CMC card. The second clock cycle has no operation assigned to it, and is left unused to remain consistent with the read operation. On the third clock, the data is actually written to the register. Note that all of the registers in the interface are 32-bit registers, and the other 24 bits written to the register on a write operation are the current read values for those bits. Figure G-9 shows a single write to the registers.

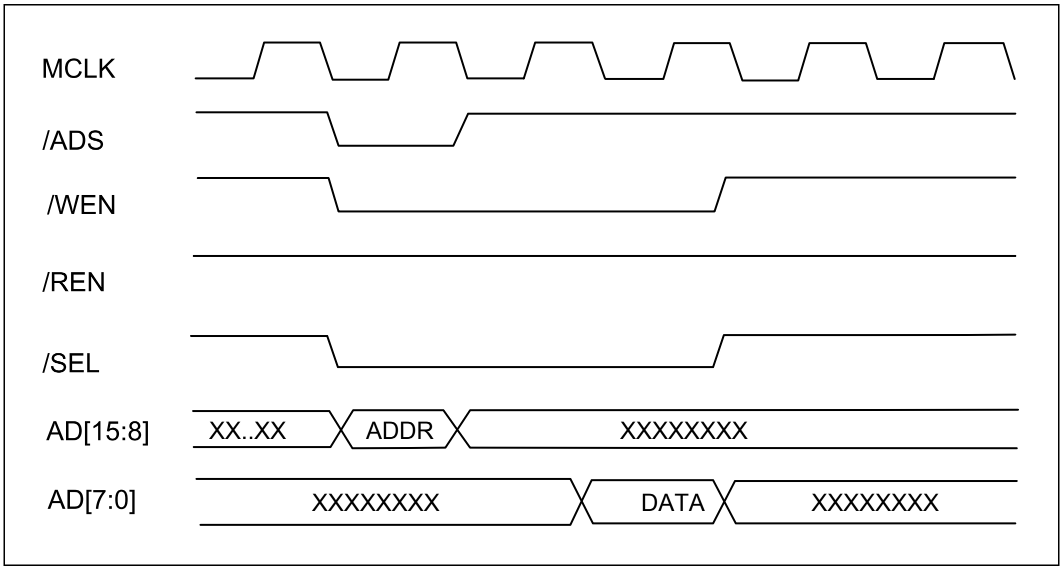


**Figure G-9 Microcontroller Single Write**

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# GLOSSARY

**1x3** ----------------------------------A 3-pin connector for use with copper media.

**8B/10B** -----------------------------A data-encoding scheme developed by IBM for translating byte-wide data to an encoded 10-bit format.

**AAL5** --------------------------------ATM Adaptation Layer for computer data.

**active** -------------------------------A term used to denote a port that is receiving a signal.

**AL**-----------------------------------See Arbitrated Loop.

**ALPA**--------------------------------Arbitrated Loop Physical Address.

**ANSI**---------------------------------American National Standards Institute.

**AP** -----------------------------------Access Point.

**API**----------------------------------Applications Program Interface.

**APID** -------------------------------Access Point Identification Number. A number ranging between 0 and 65535 that is assigned by the user to identify a process. All APID's attached to a single FX board must be unique.

**arbitrated loop** -------------------The simplest form of a Fabric topology. Has shared bandwidth, distributed topology. Interconnects NL_ports/FL_ports at the nodes/Fabric using unidirectional links. It has only one active L_port-L_port connection, so blocking is possible. A fairness algorithm ensures that no L_port is blocked from accessing the loop. Should any link in the loop fail, communication between all L_ports is terminated (see cross-point, point-to-point).

**ASIC**--------------------------------Application Specific Integrated Circuit. An integrated circuit designed to perform a specific function. ASICs are typically made up of several interconnected building blocks and can be quite large and complex.

**ATM** --------------------------------Asynchronous Transfer Mode. A network technology that transfers data in small 53-byte packets, and permits transmission over long distances. Proposed speeds range from 25 Mbps to 622 Mbps.

**Auto-Speed Negotiation** --------This feature enables FibreXpress FX200 cards to interoperate with existing FC devices at 1.0625 Gbps, and provides seamless transition to higher performance 2.125 Gbps devices.

**bandwidth** -------------------------The amount of data that can be transmitted over a channel.

**baud** --------------------------------A unit of speed in data transmission, usually equal to one bit per second.

**Bi-Directional card** --------------A FibreXtreme Simplex Link card with both source and destination capabilities.

**BIOS**--------------------------------Basic Input/Output System.

**bps** ----------------------------------bits per second.

**broadcast** --------------------------Sending a transmission to all nodes on a network.

**BSP** ---------------------------------Board Support Package. A set of software routines written by the OS vendor or SBC vendor that provides support for a particular SBC.

**burst transfers**--------------------Messages are transmitted in a format that includes the initial address followed by all the data. Burst transfers eliminate the need for repeated addresses for each data block, permitting higher throughput.

**channel** ----------------------------A point-to-point link that transports data from one point to another at the highest speed with the least delay, performing simple error correction in hardware. Channels are hardware intensive and have lower overhead than networks. Channels do not have the burden of station management.

**channel network** -----------------Combines the best attributes of both channel and network, giving high bandwidth, low latency I/O for client server. Performance is measured in transactions per second instead of packets per second.

**circuit** ------------------------------Bi-directional path allowing communications between two L_Ports.

**circuit-switched mode**-----------Data transfer through a dedicated connection (Class 1).

**CMC**--------------------------------Common Mezzanine Card.

**communications protocol** ------A special sequence of control characters that are exchanged between a computer and a remote terminal in order to establish synchronous communication.

**CRC** --------------------------------Cyclic Redundancy Check. A code used to check for errors in Fibre Channel.

**crossbar switch** -------------------Multipurpose, non-blocking 32-port cross-point switch for digital speeds up to 2.5 Gbps (See cross-point).

**cross-point**-------------------------Provides a bi-directional connection between a node (N_port) and the Fabric (F_port). Can be configured to be non-blocking by providing multiple paths between any two F_ports. Adding stations to a Fabric does not reduce the point-to-point channel bandwidth (see point-to-point).

**datagram** --------------------------Type of data transfer for Class 3 service. Transfer has no confirmation of receipt and rapid data transmission.

**dBm**---------------------------------decibels relative to one milliwatt.

**destination only card**------------A FibreXtreme Simplex Link card that is only capable of receiving data.

**direct connect links**--------------An actual physical, dedicated connection between two devices with the entire bandwidth available to serve each direct link. Direct links provide a fast and reliable medium for sending large volumes of data.

**DMA**--------------------------------Direct Memory Access.

**DMA write** ------------------------The DMA engine on the bus controller writes the data from the host computer to the SRAM buffer, freeing the host CPU for other tasks. (FibreXpress board becomes a master for the bus.)

**E_Port**------------------------------Element Port. Used to connect fabric elements together.

**ECL**---------------------------------Emitter Coupled Logic.

**ethernet** ----------------------------A widely used shared networking technology.

**exchange** ---------------------------One or more sequences for a single operation that are not concurrent, but are grouped together.

**F_Port**------------------------------Fabric Port. The access point of the fabric for physically connecting the user's N_Port.

**fabric** -------------------------------A self-managed, active, intelligent switching mechanism that handles routing in Fibre Channel Networks.

**fabric elements** -------------------Another name for ports.

**FC** -----------------------------------Fibre Channel.

**FC-AL**------------------------------Fibre Channel Arbitrated Loop. Provides a low-cost way to attach multiple ports in a loop without hubs and switches.

**FCP** ---------------------------------Fibre Channel Protocol. The mapping of the SCSI communication protocol over Fibre Channel.

**FC-PH**------------------------------Fibre Channel Physical interface. Fibre Channel Physical standard, consisting of the three lower levels, FC-0, FC-1, and FC-2.

**FCSI** --------------------------------Fibre Channel Systems Initiative is made up of IBM, Hewlett-Packard and Sun Microsystems. This group strives to advance Fibre Channel as an affordable, high-speed interconnection standard.

**FC-SW** -----------------------------Fibre Channel Switch Fabric standard. Formerly known as FC-XS: Fibre Channel Xpoint Switch. The crosspoint-switched fabric topology is the highest-performance Fibre Channel fabric, providing a choice of multiple path routings between pairs of F_ports.

**Fibre Channel** --------------------Fibre Channel (FC) is a serial data transfer interface technology operating at speeds up to 1 Gbps. It is defined as an open standard by ANSI. It operates over copper and fiber optic cabling at distances of up to 10 kilometers. Supported topologies include point-to-point, arbitrated-loop, and fabric switches.

**FibreXpress** -----------------------A Curtiss-Wright Controls, Inc. trademark name for a family of networking products that maximize the superior communication and interconnect capabilities of ANSI standard Fibre Channel. The FX200 series of 64-bit adapters support up to 200 MB per second (400 MB per second duplex) throughput. The FX100 series supports 100 MB per second throughput.

**FibreXtreme** ----------------------A Curtiss-Wright Controls, Inc. trademark name for a family of networking products based on the original Simplex Link technology, Curtiss-Wright Controls' FibreXtreme Serial FPDP Data Link moves data at a sustained 247 MB per second with microsecond latency. Supports up to 2.5 Gbps serial data link using a highly specialized communications protocol optimized for maximum data throughput.

**FibreXtreme Simplex Link** ----A high-speed, point-to-point, communication network capable of transfers in excess of 100 MB/s.

**FIFO**--------------------------------first in first out

**Firmware** --------------------------Microprocessor executable code, typically for embedded type processors.

**Flash** --------------------------------A type of Electrical Erasable Programmable Read Only Memory (EEPROM). Erased and written to in blocks vs. bytes.

**FL_Port** ----------------------------Fabric Loop Port. Joins an arbitrated loop to the fabric.

**FPDP** -------------------------------Front Panel Data Port.

**frame** -------------------------------A linear set of transmitted bits that define a basic transport element. A frame is the smallest indivisible packet of data that is sent on the FC.

**frame-switched mode** -----------Data transfer is connectionless (Classes 2 and 3) and data transmission is in frames. The bandwidth is allocated on a link-by-link basis. Frames from same port are independently switched and may take different paths.

**FTP application** ------------------A test application for transferring files from one computer to another.

**FX** ------------------------------------FibreXpress.

**G_Port** ------------------------------A port which can function as either an F_Port or an E_Port. Its function is defined at login.

**Gbps** ---------------------------------Gigabits per second.

**gigabit** -------------------------------One billion bits, or one thousand megabits.

**GLM**---------------------------------Gigabit per second Link Module. A Link Module that can be used for optical or copper media.

**HANDLE** --------------------------Abstraction for the *Handle* in Windows and *file descriptor* in Unix.

**HBA** ---------------------------------Host Bus Adapter.

**heartbeat** --------------------------A visual indicator that flashes periodically to indicate the embedded controller is functioning properly.

**HIPPI** ------------------------------High Performance Parallel Interface. An 800 Mbps interface to supercomputer networks (previously called high-speed channel) developed by ANSI.

**HSSDC**------------------------------High Speed Serial Data Connectors and Cable Assemblies. A type of high-speed interconnect system which allows for transmission of data rates greater than 2 Gbps and up to 30 meters.

**hunt group** ------------------------A group of lines that are linked so that one call to the group will find the line that is free. This provides the ability for more than one port to respond to the same alias address.

**I/O** ----------------------------------Input/Output.

**IOCB** --------------------------------I/O Control Block. A block of information stored in system memory, usually of fixed length, which contains control codes and data. The IOCB is created by a host computer and sent to some other computer. The IOCB contains command/instructions, data, and memory pointers intended to direct the other computer to perform some function.

**inactive** ------------------------------A term used to denote a port that is not receiving a signal.

**intermix** -----------------------------A Fibre-Channel-defined mode of service that reserves the full Fibre Channel bandwidth for a dedicated (Class 1) connection, but also allows connectionless (Class 2) traffic to share the link if the bandwidth is available.

**IP** -------------------------------------Internet Protocol is a data communications protocol.

**IPI**------------------------------------Intelligent Peripheral Interface.

**insertion delay** --------------------The amount of time the data is delayed for the insertion of FXSL framing protocol. It is measured from when the data becomes available at the FIFO to when the data is actually transmitted on the link. The actual values are either 188 ns in Mode-0 or Mode-1 (with no CRC), or 226 ns in Mode-2 or Mode-3 (with CRC).

**KB** ----------------------------------Kilobytes. IEEE convention: A capital K is used for binary (1024) kilo, and a lowercase k is used for decimal (1000) kilo.

**Kb** ------------------------------------Kilobits.

**Kbps** ---------------------------------Kilobits per second.

**L_Port**------------------------------Loop Port. Either an FL_Port or an NL_Port that supports the arbitrated loop topology.

**LAN** --------------------------------Local Area Network, typically less than 5 kilometers. Transmissions within a LAN are mostly digital, carrying data at rates above 1 Mbps.

**latency**------------------------------The delay between the initiation of data transmission and the receipt of data at its destination.

**LCF** ---------------------------------Link_Control Facility. Provides logical interface between nodes and the rest of Fibre Channel.

**Link Module** ----------------------A mezzanine board mounted on the board to interface between the board and the network.

**longword**---------------------------32-bit or 4-byte word.

**LP** -----------------------------------Lightweight Protocol.

**LX1500**------------------------------LinkXchange LX1500 Crossbar Switch.

**LX2500**------------------------------LinkXchange LX2500 Crossbar Switch.

**Mbps**--------------------------------Megabits per second.

**MBps** -------------------------------Megabytes per second.

**MB** ----------------------------------Megabytes.

**media** -------------------------------Means of connecting nodes; either fibre optics, coaxial cable or unshielded twisted pair.

**ms** -----------------------------------Milliseconds

**mW** ---------------------------------Milliwatt.

**µs** -----------------------------------Microseconds

**monitor** ----------------------------An application program used to display the status and change the configuration of the driver.

**multicast** ---------------------------A single transmission is sent to multiple destination N_ports, a one-to-many transmission. Multicasting provides a way for one host to send packets to a selective group of hosts.

**N_Port**------------------------------Node Port. A Fibre-Channel-defined entity at the node end of a link that connects to the fabric via an F-Port.

**network** ----------------------------Connects a group of nodes, providing the protocol that supports interaction among these nodes. Networks are software intensive, and have high overhead. Networks also operate in an environment of unanticipated connections. Networks have a limited ability to provide the I/O bandwidth required by today's applications and client/server architectures.

**NL_Port**----------------------------Node Loop Port. Joins nodes on an arbitrated loop.

**node**---------------------------------A host computer and interface board. Each processor, disk array, workstation or any computing device is called a node. Connects to FC through a node port (N_Port).

**normal write** ----------------------A host CPU writes data to the SRAM buffer through the bus and bus controller (FibreXpress board operates as a slave of the bus).

**ns** ----------------------------------nanoseconds.

**NVRAM** ---------------------------Non-Volatile Random Access Memory. Generic term for memory that retains its contents when power is turned off.

**OFC**---------------------------------Open Fibre Control. A safety interlock system used on some FC shortwave links.

**one-to-many**-----------------------One node transmits to multiple nodes. See broadcast, multicast.

**operation**---------------------------One of Fibre Channel's building blocks composed of one or more exchanges.

**out-of-band control**--------------On the LinkXchange products, a method of issuing switch commands that does not use any bandwidth of the 32 switch ports.

**PCB** ---------------------------------Printed Circuit Board.

**PCI** ----------------------------------Peripheral Component Interface.

**PECL** -------------------------------Positive Emitter Coupled Logic.

**PIO**----------------------------------Programmed Input/Output.

**PMC** --------------------------------PCI Mezzanine Card. Everything that is true for PCI cards is true for PMC except there is a footprint or card format change.

**point-to-point** --------------------Bi-directional links that interconnect the N_ports of a pair of nodes. Non-blocking.

**port** --------------------------------A physical element through which information passes. It is an electrical or optical interface with a pair of wires or fibers—one each for incoming and outgoing data.

**profiles** -----------------------------Subsets of Fibre Channel standards that improve interoperability and simplify implementation. It is like a cross-section of FC, providing guidelines for implementing a particular application.

**protocols** ---------------------------Data transmission conventions encompassing timing, control, formatting, and data representation. This set of hardware and software interfaces in a terminal or computer allow it to transmit over a communication network, and these conventions collectively form a communications language.

**retimed**----------------------------"Retimed" port cards use a phase-locked loop to recover the clock from a serial data stream. They then use the recovered clock to strobe the data through a one-bit latch to minimize the accumulation of edge jitter. This process is sometimes called "reclocked." (Retimed port cards do *not* synchronize the data to a local crystal-controlled reference clock.) Non-retimed port cards do not clock the serial data stream at all. From a timing standpoint, they function as gate delays as the data passes asynchronously through them.

**RISC**--------------------------------Reduced Instruction Set Computer. A type of microprocessor that executes a limited number of instructions that typically allows it to run faster than a Complex Instruction Set Computer (CISC).

**RJ-45** ------------------------------Short for Registered Jack-45. An eight-wire connector commonly used to connect computers onto a local-area network (LAN), especially Ethernet. RJ-45 connectors look similar to the RJ-11 connectors used for connecting telephone equipment, but they are somewhat wider.

**SAP** --------------------------------Service Access Point.

**SBC** ----------------------------------Single Board Computer.

**SCSI** ---------------------------------Small Computer System Interface.

**sequence** ----------------------------The unit of transfer, made up of one or more related frames for a single operation.

**SFF**-----------------------------------Small Form Factor. Based on SFF MSA.

**SFF MSA** --------------------------Small Form Factor Transceiver Multisource Agreement (SFF MSA), July 5, 2000.

**shared connect links**-------------The ability to send and receive data without establishing a dedicated physical connection so that other devices can also use the medium. This shared link is more efficient for smaller data transmissions because the overhead of direct connect link is avoided.

**SRAM** -------------------------------Static Random Access Memory.

**SRAM Transfer** ------------------Process in which the data is transferred from the host computer to the SRAM buffer by normal or by DMA write.

**SFP**-----------------------------------Small Form Factor Pluggable based on MultiSource Agreement (MSA), September 14, 2000, FO Transceiver Industry.

**STP**-----------------------------------Shielded Twisted Pair. A type of cable media.

**striping** ------------------------------To multiply bandwidth by using multiple ports in parallel.

**switched fabric** -------------------(see the definition for “fabric”).

**SYNC**--------------------------------FibreXtreme Simplex Link primitive used to synchronize the source and destination cards.

**SYNC with DVALID**------------A special case of the SYNC primitive occurring in the middle of a buffer of data.

**source only card**------------------A FibreXtreme Simplex Link card that is only capable of sending data.

**TCP** ----------------------------------Transmission Control Protocol.

**terminal application**-------------A test application that sends characters received from the keyboard and displays received characters.

**throughput application** ---------An application that tests the throughput for the given system.

**time-out** -----------------------------The time allotted for a native message to travel the network ring and return. If this time is exceeded, an automatic retransmission of the native message occurs.

**topology** -----------------------------Refers to the order of information flow due to logical and physical arrangement of stations on a network.

**TTL** ----------------------------------Transistor-Transistor Logic.

**ULP** ----------------------------------Upper Level Protocol.

**VHDL** ------------------------------Very high-speed integrated circuit Hardware Description Language.

**VME** --------------------------------Acronym for VERSA-module Europe: bus architecture used in some computers.

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