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PMC Module

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SCRAMNet® GT

Hardware Reference
for PCI and PMC Cards

Document No. G-T-MR-G1PCPMCP-A-0-A1

CURTISS WRIGHT Controls, Inc.
Embedded Computing

FOREWORD

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FCC

This product is intended for use in industrial, laboratory or military environments. This product uses and emits electromagnetic radiation, which may interfere with other radio and communication devices. The user may be in violation of FCC regulations if this device is used in other than the intended market environments.

CE

As a component part of another system, this product has no intrinsic function and is therefore not subject to the European Union CE EMC directive 89/336/EEC.

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1. INTRODUCTION

1.1 How To Use This Manual

1.1.1 Purpose

This document is a reference manual for the SCRAMNet-GT PCI and PMC card host interface. It provides a physical and functional description of the SCRAMNet GT network interface card (NIC). The manual describes how to unpack, set up, install and operate the hardware.

1.1.2 Scope

This information is intended for systems designers, engineers and network installation personnel. You need at least a systems level understanding of general computer processing, of memory and hardware operation, and of the specific host processor to effectively use this manual.

1.1.3 Style Conventions

- Hexadecimal values are written with a "0x" prefix. For example, 0x03FF
- Code and monitor screen displays of input and output are boxed and indented on a separate line. Text that represents user input is bolded. Text that the computer displays on the screen is not bolded. For example:

```
C:\ls
file1          file2              file3
```

- Large samples of code are Courier font, at least one size less than context, and are usually on a separate page or in an appendix.

1.2 Related Information

- PCI Local Bus Specification, Revision 2.2, 18 DEC 1998, PCI SIG
- CMC Specification (IEEE P1386/Draft 2.4a), Revision 21 MAR 2001, IEEE
- PMC Specification (IEEE P1386.1/Draft 2.4a), Revision 21 JAN 2001, IEEE
- *SCRAMNet GT API Guide*, Curtiss-Wright Controls, Inc. (Document No. G-T-ML-G1AP1)
- Curtiss-Wright Controls, Inc web address: www.cwcembedded.com

1.3 Quality Assurance

Curtiss-Wright Controls' Corporate policy is to provide our customers with the highest quality products and services. In addition to the physical product, the company provides documentation, sales and marketing support, hardware and software technical support, and timely product delivery. Our quality commitment begins with product concept, and continues after receipt of the purchased product.

Curtiss-Wright Controls' Quality System conforms to the ISO 9001 international standard for quality systems. ISO 9001 is the model for quality assurance in design, development, production, installation and servicing. The ISO 9001 standard addresses all 20 clauses of the ISO quality system, and is the most comprehensive of the conformance standards.

Our Quality System addresses the following basic objectives:

- Achieve, maintain and continually improve the quality of our products through established design, test, and production procedures.
- Improve the quality of our operations to meet the needs of our customers, suppliers, and other stakeholders.
- Provide our employees with the tools and overall work environment to fulfill, maintain, and improve product and service quality.
- Ensure our customer and other stakeholders that only the highest quality product or service will be delivered.

The British Standards Institution (BSI), the world's largest and most respected standardization authority, assessed Curtiss-Wright Controls' Quality System. BSI's Quality Assurance division certified we meet or exceed all applicable international standards, and issued Certificate of Registration, number FM 31468, on May 16, 1995. The scope of Curtiss-Wright Controls' registration is: "Design, manufacture and service of high technology hardware and software computer communications products." The registration is maintained under BSI QA's bi-annual quality audit program.

Customer feedback is integral to our quality and reliability program. We encourage customers to contact us with questions, suggestions, or comments regarding any of our products or services. We guarantee professional and quick responses to your questions, comments, or problems.

1.4 Technical Support

Technical documentation is provided with all of our products. This documentation describes the technology, its performance characteristics, and includes some typical applications. It also includes comprehensive support information, designed to answer any technical questions that might arise concerning the use of this product. We also publish and distribute technical briefs and application notes that cover a wide assortment of topics. Although we try to tailor the applications to real scenarios, not all possible circumstances are covered.

Although we have attempted to make this document comprehensive, you may have specific problems or issues this document does not satisfactorily cover. Our goal is to offer a combination of products and services that provide complete, easy-to-use solutions for your application.

If you have any technical or non-technical questions or comments, contact us. Hours of operation are from 8:00 a.m. to 5:00 p.m. Eastern Standard/Daylight Time.

- Phone: (937) 252-5601 or (800) 252-5601
- E-mail: support@systran.com
- Fax: (937) 252-1465
- World Wide Web address: www.cwcembedded.com

1.5 Ordering Process

To learn more about Curtiss-Wright Controls' products or to place an order, please use the following contact information. Hours of operation are from 8:00 a.m. to 5:00 p.m. Eastern Standard/Daylight Time.

- Phone: (937) 252-5601 or (800) 252-5601
- E-mail: info@systran.com
- World Wide Web address: www.cwcembedded.com

2. PRODUCT OVERVIEW

2.1 Overview

This chapter describes the SCRAMNet GT cards, their features and network environments.

2.2 Network Features

The SCRAMNet GT Network has the following features:

- A ring topology with a maximum network throughput of approximately 1.0 Gigabytes (GB/s) to 205 Megabytes (MB/s) (base10).
- All writes to SCRAMNet GT memory generate network traffic (no filtering occurs based on current values present in memory.
- Protocol-supported network addressing for 512 MB shared memory for each node processor.
- Variable-length message packet with a maximum pay load of 128 bytes.
- 255-node capacity on each ring.
- No operating or system software is required to support network protocol.
- No network-dependent application software is required.

CAUTION: Check with the host computer manufacturer to find out which slots are available for third party PCI memory cards before installing the SCRAMNet+ Network board into any system. Installing any type of PCI card in a non-standard PCI slot may result in serious damage to the host machine.

2.3 Card Features

Curtiss-Wright Controls' SCRAMNet GT family of products includes PCI and PCI Mezzanine (PMC) form factor cards.

The PCI and PMC versions provide this link via the PCI bus. The PCI bus is used in most standard PCs, and the PMC format is used in most popular single-board computers. Both of these variations interoperate completely on the link interface, providing seamless integration between diverse platforms.

2.3.1 SCRAMNet GT PCI

Figure 2-1 SCRAMNet GT PCI Card

2.3.2 SCRAMNet GT PCI Features

The major SCRAMNet GT PCI card features are listed below:

- PCI Short form factor requiring one single slot in the computer chassis
- Bus support for 33 MHz/66 MHz PCI operation for 32/64 bit buses
- Supports +3.3.V PCI signaling voltage only (not 5 volt tolerant)
- Physical interface of 2.5 GB per second for short wavelength laser (850 nm), long wavelength laser (1300 nm)
- Supports “concurrent” network and host accesses with no loss of network data or need to implement network flow control
- Status LED that report link status
- Selectable local host interrupts for error and status conditions
- Two Small Form Factor Pluggable (SFP) media options available— short wavelength laser (850 nm) and long wavelength laser (1300 nm)
- 2.5 GB/s fiber-optic interface with redundant transceiver option for network topology redundancy
- Operates with the LinkXchange family of switches (2.5 GB or faster).

2.3.3 SCRAMNet GT PMC

Figure 2-2 SCRAMNet GT PMC Card

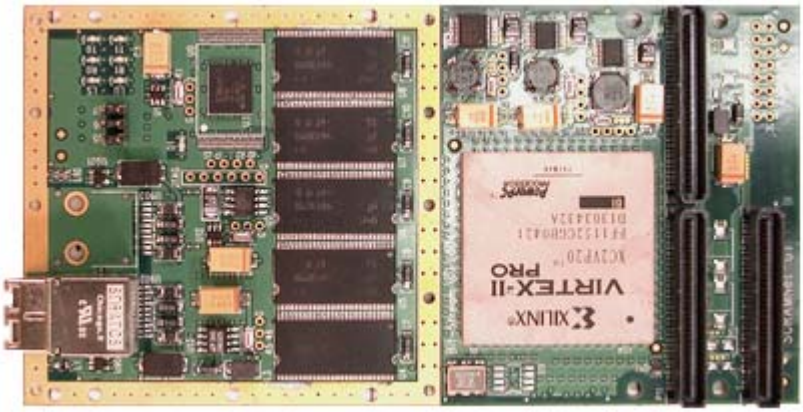


Figure 2-3 SCRAMNet GT Conduction Cooled

2.3.4 SCRAMNET-GT PMC Features

The major SCRAMNet GT PMC card features are listed below:

- Single-width PMC requiring one single slot on the single board computer
- Bus support for 33 MHz/66 MHz PCI operation for 32/64 bit buses
- Supports +3.3.V PCI signaling voltage only (not 5 volt tolerant)
- Physical interface of 2.5 GB/s for short wavelength laser (850 nm), long wavelength laser (1300 nm)
- Supports “concurrent” network and host accesses with no loss of network data or need to implement network flow control
- Status LED that report link status
- Selectable local host interrupts for error and status conditions
- Two Small Form Factor Pluggable (SFP) media options available— short wavelength laser (850 nm) and long wavelength laser (1300 nm)
- 2.5 GB/s fiber-optic interface with redundant transceiver option for network topology redundancy
- Operates with the LinkXchange LX2500 family of switches (2.5 GB or faster)
- Operating temperature –40°C to + 85°C (Conduction cooled model)

2.3.5 SFP Media Options

The physical media interface of the SCRAMNet GT design uses SFP transceiver modules. These modules are hot swappable, providing an efficient way to modify the media interface configuration as needed.

Two basic SFP media options are available for the SCRAMNET-GT. These media options are a long wavelength laser (1300 nm) and short wavelength laser (850 nm). All cards use a Duplex LC style connector available from most major cable manufacturers.

Figure 2-4 SFP Transceiver Module

Long wavelength laser interconnections are recommended for distances longer than 300 meters, as loss in multimode fiber degrades connections with short wavelength lasers past this distance.

The short wavelength version is useful for intrasystem connections, where you are connecting between cards on the same backplane. It is also suited for short reach intersystem connections (< 300 m).

The SFP transceivers comply with the Small Form-factor Pluggable transceiver MultiSource Agreement (SFP MSA) to ensure compatibility between the different transceiver manufacturers.

2.3.6 Firmware Dependencies

The specifications and features described in this manual are based on firmware revisions at the time of publication. Performance may vary between firmware revisions. Please contact Technical Support for more information.

2.3.7 LED Descriptions

Three sets of status LEDs are visible from the front panel of the SCRAMNet GT board. The position of the LEDs is shown in Figure 2-5 for PCI and Figure 2-6 for PMC.

Link Select (LS)

The Link Select LED indicates which channel of the SCRAMNet GT board is selected. When the LED is off, channel 0 is selected. When the LED is on, channel 1 is selected.

Link Up (LU)

The Link Up LED turns on when the selected channel is receiving a valid SCRAMNet GT signal.

Signal Detect (R0, R1)

The Signal Detect LEDs indicate a signal is being received by the corresponding transceiver.

Laser Enable (T0, T1)

The Laser Enable LEDs indicate the corresponding transceiver is turned on.

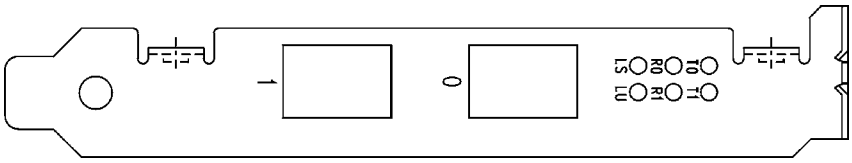


Figure 2-5 SCRAMNet GT PCI Faceplate

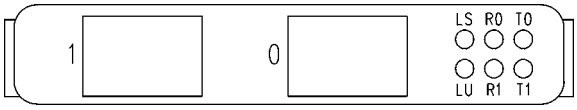


Figure 2-6 SCRAMNet GT PMC Faceplate

2.4 Applications

SCRAMNet GT cards are used in a variety of topologies for a variety of applications. The following sections detail typical topologies used and some applications. Many other applications are possible in these configurations.

2.4.1 LinkXchange LX 2500 Crossbar Switch

Curtiss-Wright Controls' LX 2500 Crossbar Switch provides the following features:

- Up to 32 non-blocking media-specific I/O ports.
- Up to 2.5 GB/s/port baud rate (port-card dependent).
- Support for multiple point-to-point, loop, and broadcast communication links simultaneously.
- Automatic I/O Port fault isolation.
- Multiple media options.
- Out-of-band control through an RS-232 port.
- Can be connected to a modem and controlled from a remote location.

For more detailed information regarding LX2500 features and operation, contact Curtiss-Wright Controls, Inc. and request a copy of the *LinkXchange LX2500 Crossbar Switch Hardware Reference Manual* or visit our web site.

2.4.2 LXVME 2500 Crossbar Switch

Curtiss-Wright Controls' LXVME 2500 Crossbar Switch provides the following features:

- 16 non-blocking SFP transceiver ports (with optional 8-port expansion card)
- 3.2 GB/s/port baud rate

- 25.6 GB/s total bandwidth (51.2 GB/s with optional 8-port expansion card)
- Supports Arbitrated Loop, Point-to-Point, One-to-Many communication links
- Optional bypass of retiming circuitry for each port
- Retimed ports support short wavelength (850 nm), long wavelength (1300 nm), and HSSDC2 physical media options
- SFP transceiver MultiSource Agreement (SFP MSA) compatibility for each port to ensure functional support for transceivers from other manufacturers
- Flexible automatic I/O port fault isolation
- Multiple media options
- Hot-swappable SFP modules
- Cross-point configuration controlled across VME Bus or RS-232 port
- Front panel “Signal Detect” status indicators for each port provided
- Front panel “Power On” status indicator
- Front panel “Transmitter On” status indicator for each port
- Front panel “Heartbeat” status indicator
- Provides unique VME card base addressing
- Card Reset switch
- Password Reset switch
- Watchdog timer
- 32 KB Non-volatile SRAM (NVSRAM)

For more detailed information regarding LX2500 features and operation, contact Curtiss-Wright Controls, Inc. and request a copy of the *LinkXchange LXVME 2500 Crossbar Switch Hardware Reference Manual* or visit our web site.

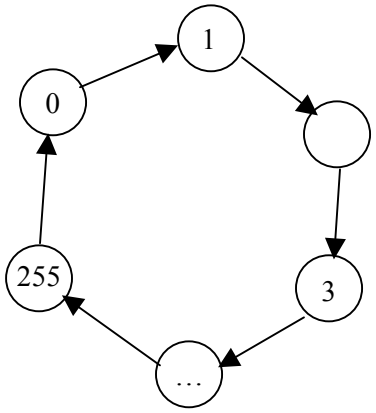
2.5 Topologies

There are six typical topologies for the SCRAMNet GT card. These topologies should cover most customer applications, though if another topology is desired contact Curtiss-Wright Controls, Inc. Technical Support to see if it is possible. The topologies are:

- Non-redundant ring
- Redundant ring
- Point-to-Point
- Daisy Chain
- DSP Pipeline
- Monitoring
- Switch ring
- Redundant switch ring

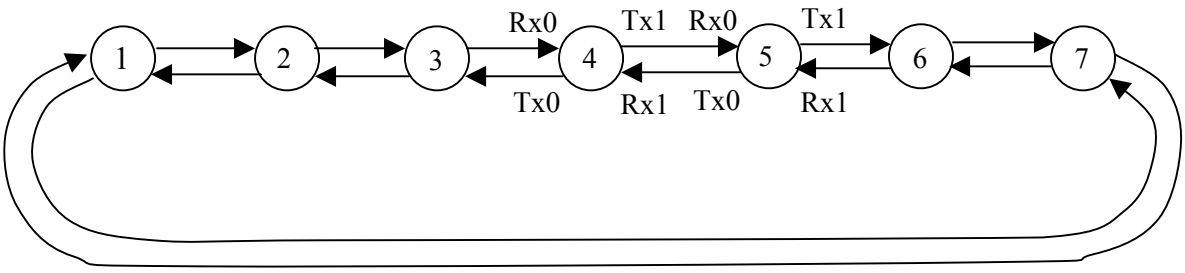
2.5.1 Non-Redundant Ring

A ring with a single transmit/receive connection per node.



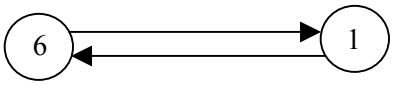
2.5.2 Redundant Ring

A ring with two transmit/receive connections per node.



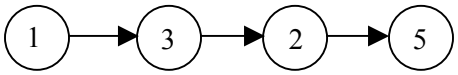
2.5.3 Point-to-Point

A network topology in which one node connects directly to another node.



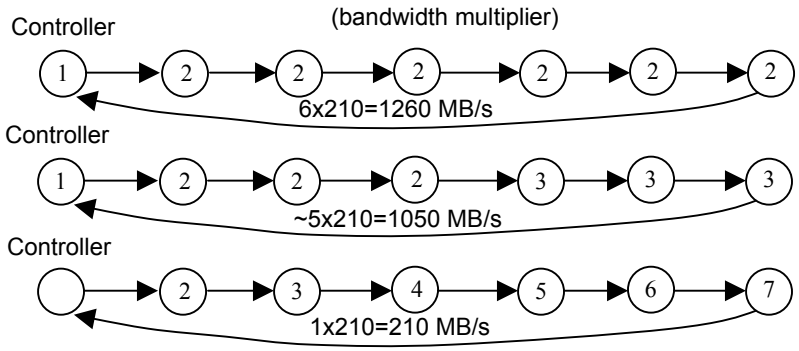
2.5.4 Daisy Chain

A configuration in which devices are connected to each other in sequence.



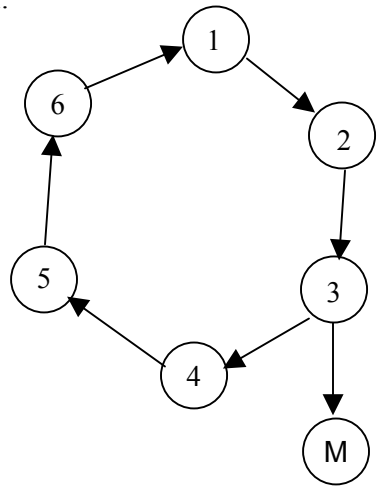
2.5.5 DSP Pipeline

A series of processing nodes where each successive node takes the results from the previous node and performs an additional layer of processing.



2.5.6 Monitoring

A ring with a monitor.



2.5.7 Switch Ring

The LinkXchange LX-2500 switch can extend a ring or connect multiple rings.

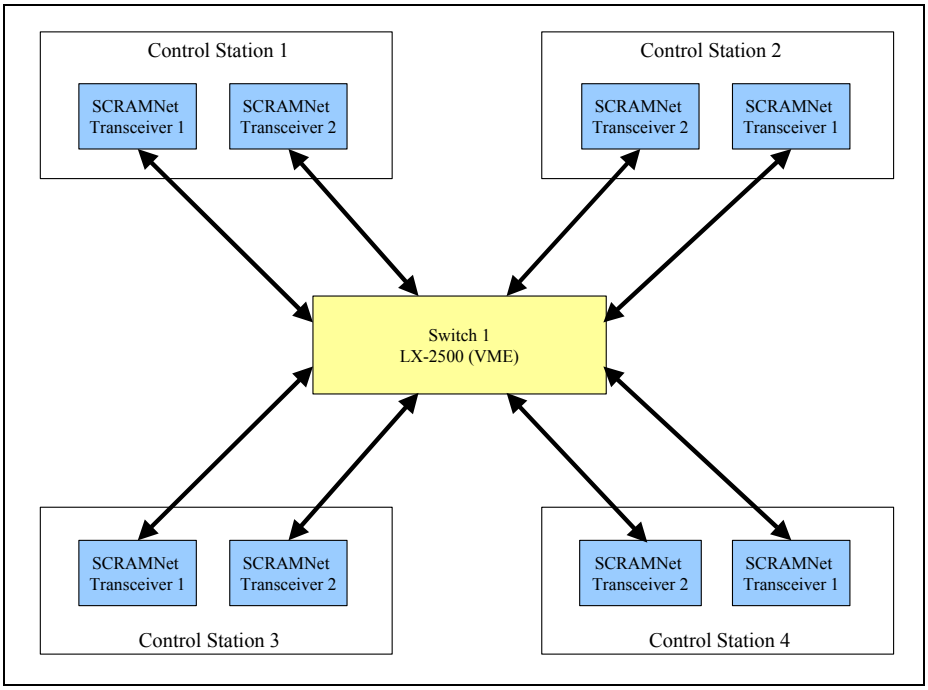


Figure 2-7 Switch Ring

Any node can be the initiating node. Any data write by the host to the SCRAMNet GT NIC memory triggers a message to all nodes to replicate the new data.

2.5.8 Redundant Switch Ring

Multiple LX-2500 switches provide redundancy to protect network integrity.

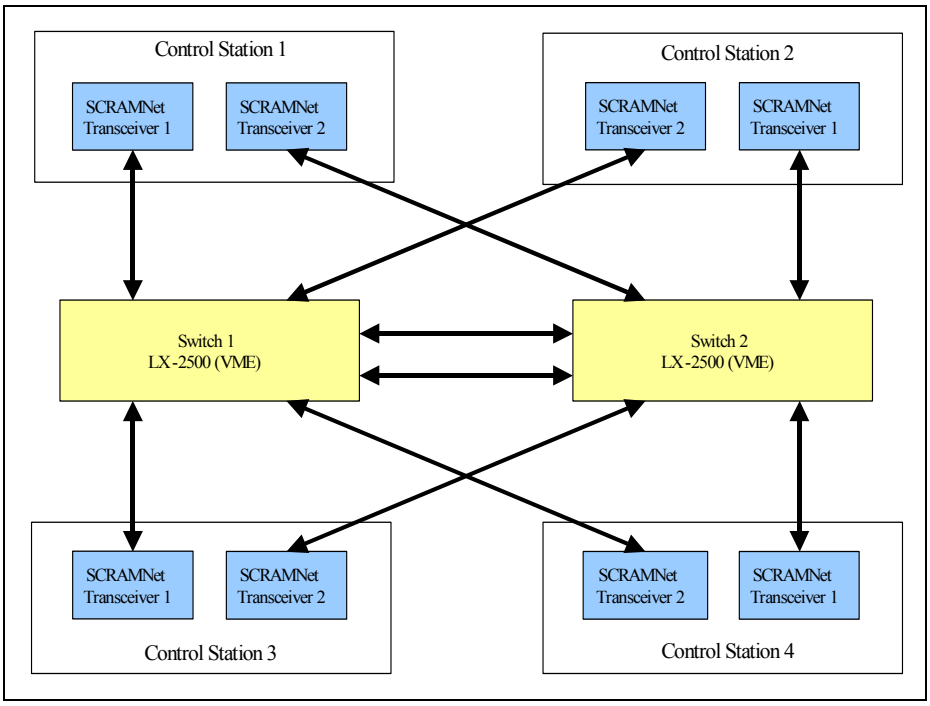


Figure 2-8 Redundant Switch Ring

3. INSTALLATION

3.1 Overview

SCRAMNet GT cards require only one slot on the host computer backplane and interface directly to a fiber-optic cable

To install a SCRAMNet GT card, follow the steps below:

1. Unpack the card.
2. Inspect the card.
3. Install the card.
4. Connect the cables.

3.2 Unpack the Card

CAUTION: Exercise care regarding the static environment. Use an anti-static mat connected to a wristband when handling or installing the SCRAMNet GT card. Failure to do this may cause permanent damage to the components on the card.

Follow the steps below to unpack the card:

1. Put on the wristband attached to an anti-static mat.
2. Remove the card and anti-static bag from the carton.
3. Place the bag on the anti-static mat.
4. Open the anti-static bag and remove the card.
5. In the unlikely event that you should need to return your SCRAMNet GT card, please keep the original shipping materials for this purpose.

Any optional equipment is shipped in separate cartons.

3.3 Inspect the Card

The SCRAMNet GT card consists of a single card with a built-in network interface. If the card was damaged in shipping, notify Curtiss-Wright Controls, Inc. or your supplier immediately.

3.4 Configure the SCRAMNet GT PCI Card

3.4.1 Installing SFP Modules

The physical media interface of the SCRAMNet GT PCI design uses SFP transceiver modules. These modules are hot swappable, providing an efficient way to modify the media interface configuration as needed. Always take the usual precautions against electrostatic discharge when handling SFP modules.

The SFP module contains a printed circuit board (PCB) that mates to an SFP electrical connector, located within the metal SFP receptacle cage on the SCRAMNet GT PCI card. The SFP PCB is exposed through a cutout on the back end of the SFP module. The orientation of the SFP must be correct to insert it successfully into the receptacle cage.

To insert an SFP module, hold the module with the PCB cutout facing downward toward the SCRAMNet GT PCI card and slide it into the receptacle cage on the card. There will be a small click as the module latches into place. The SFP module is designed to only fit into the receptacle cage a certain way. If the SFP module is inserted wrong, it will not fully slide into the receptacle cage. If this happens, remove the module and reinsert it correctly.

To remove an SFP module, press or slide the latch release on the module. This is usually a button or tab on the bottom side of the module that moves toward the rear of the card. The module will pop out slightly as the latch releases. Pull the module out of the receptacle cage.

The SCRAMNet GT PCI cards are shipped with a Dust/EMI plug for each SFP transceiver receptacle. Install these in empty receptacles to prevent contamination of internal components and to optimize EMI performance.

3.5 Install the Cards

WARNING: Turn off all power to your operating system before attempting to install the SCRAMNet GT Cards.

WARNING: SCRAMNet GT cards support +3.3 V PCI signaling only. Installing this card in any host system with +5 V PCI signaling slots can cause irreparable damage.

3.5.1 SCRAMNet GT PCI Card

To install the SCRAMNet GT PCI card, push the card into the motherboard, as shown in Figure 3-1, steps 1 and 2, until it is firmly seated. Install the mounting screw as shown in step 3.

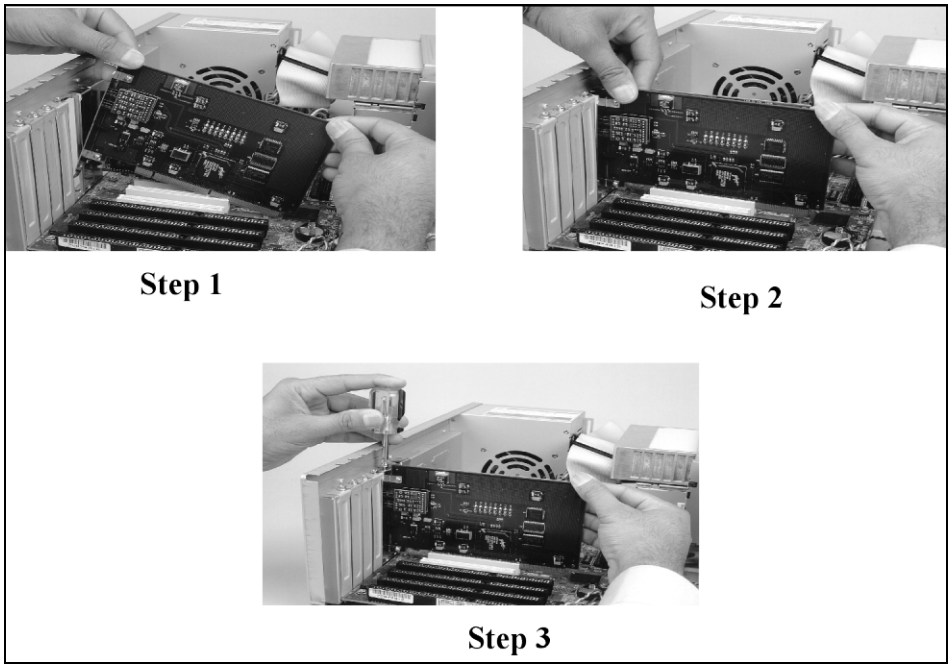


Figure 3-1 SCRAMNet GT PCI Card Installation

3.5.2 SCRAMNet GT PMC Card

To install the SCRAMNet GT PMC card, insert the card into an available slot by pushing the faceplate into the cutout on the carrier until it butts up against the mating connector as shown in Figure 3-2, steps 1 and 2. Then firmly push the connectors together. Install the four mounting screws through the PCB of the host SBC to fasten it in place, as shown in step 3.

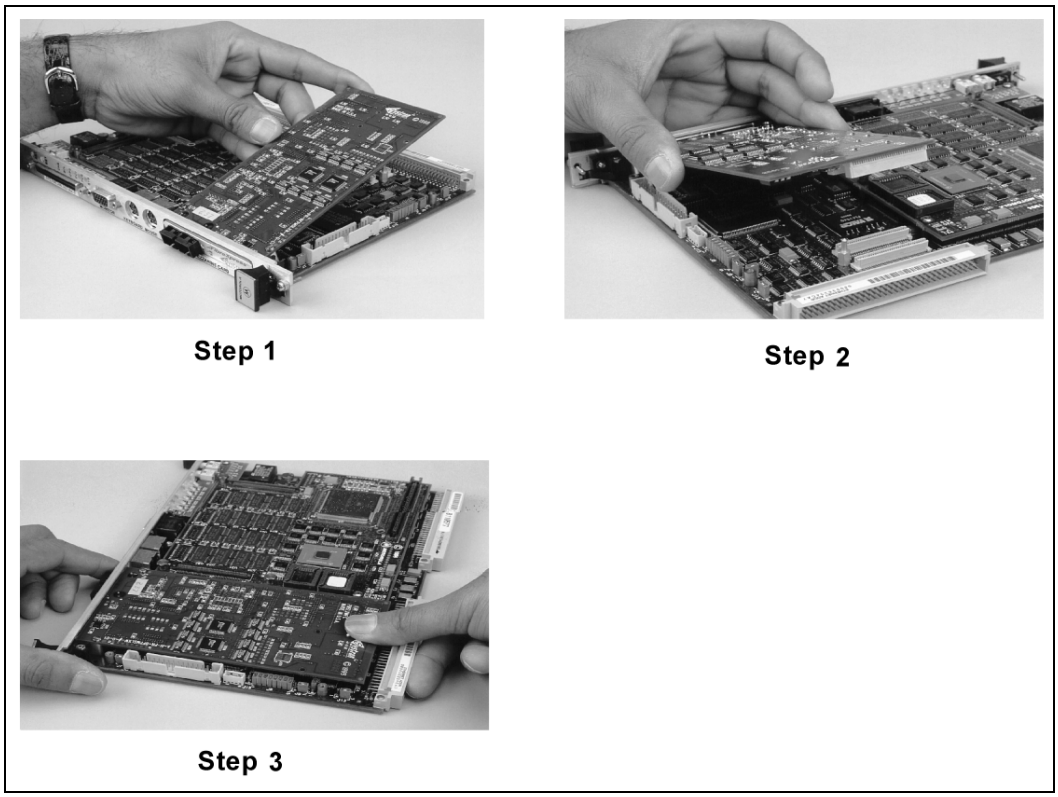


Figure 3-2 SCRAMNet GT PMC Card Installation

3.6 Connect the Fiber Optic Cables

The two factors to consider when connecting the cables are the topology and the transmission media used. The cards can be connected in several different topologies depending on your application. See section 2.5, Topologies, for more detailed examples.

Fiber-optic Cable Precautions

CAUTION: Fiber-optic cables are made of glass and may break if crushed or bent in a loop with less than a 2-inch radius.

Look at the cable ends closely before inserting them into the connector. If debris is inserted into the transmitter/receiver connector, it may not be possible to clean the connector out and could result in damage to the transmitter or receiver lens. Hair, dirt, and dust can interfere with the light signal transmission.

Use an alcohol-base wipe to clean the cable ends.

For short wavelength laser modules, either a 50 µm or 62.5 µm core diameter cable should be used. For distances up to 300 meters 62.5 µm can be used. Distances up to 500 meters 50 µm cable. For distances greater than 500 meters (up to 10 kilometers), long wavelength laser modules with 9 µm core cable should be used.

The optional fiber-optic cables may be shipped in a separate carton. Remove the rubber boots on the fiber-optic transmitters and receivers as well as the ones on the fiber-optic cables. Replace these rubber boots when cables are not in use or if the node must be returned to the factory. Attach the fiber-optic cables to the connectors on the SL240 card.

Figure 3-3 and Figure 3-4 depict the types of fiber-optic connectors needed for the SL240 card.

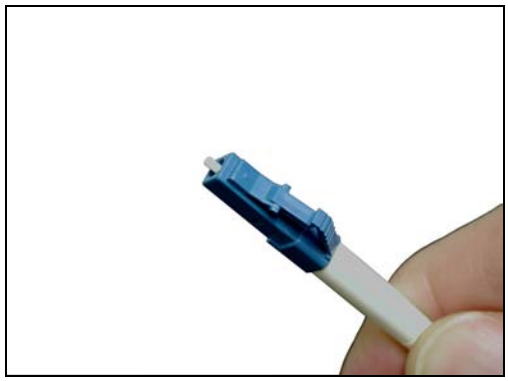


Figure 3-3 Fiber-optic Simplex LC Connector

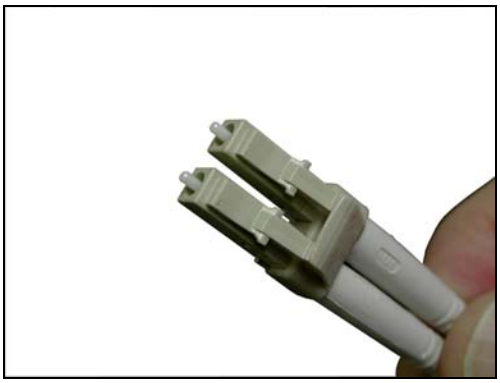


Figure 3-4 Fiber-optic Duplex LC Connector

3.7 Troubleshooting

If the system does not boot correctly, power down the machine, reseat the card, double-check cable connections, and turn the system back on. If problems persist, contact Curtiss-Wright Controls, Inc. Technical Support at **(800) 252-5601** or **support@systran.com** for assistance.

Please be prepared to supply the following information:

Machine: _____
OS Name: _____
OS Version: _____
Card Type: _____
Card Serial No.: _____
Firmware Revision*: _____
Driver Revision*: _____
API Revision*: _____
Problem Reproducibility: _____
Problem Description: _____

* This information is available as output from the **gtmon -V** command.

4. OPERATION

4.1 Overview

The SCRAMNet GT Network is a shared-memory system. Every computer on the network has a constantly updated local copy of all global data, which is passed to all the network computers. The network protocol is implemented in the SCRAMNet GT hardware and therefore no software overhead is required to retrieve this information from the network.

The protocol is transparent to the computer. This frees computer processor time for application algorithm execution and other real-time tasks. Since any computer on the network has access to data in the shared memory, any computer can read or modify the shared data and thereby communicate with the other computers on the network.

The SCRAMNet GT software is designed to help facilitate application software development. The software consists of a device driver, an API library, and a set of utility applications. See the *SCRAMNet GT API Guide* for more information.

4.2 Network Hardware

4.2.1 Network Paradigm

The SCRAMNet GT Network is a connectionless-broadcast shared-memory network. Each host processor on the network has access to its own local copy of shared memory that is updated over a high-speed, serial-ring network. The network is optimized for the high-speed transfer of data among multiple, real-time computers that are all solving portions of the same real-time problem

4.2.2 Ring Topology

The SCRAMNet GT Network is a ring topology network. The ring topology supports circuit-switch operation for topology reconfiguration and fault isolation. Ring protocol is register insertion with source message removal.

Data is transmitted at a maximum of 2.5 GB/s over fiber-optic cables. There is an approximate 1µs (minimum) latency at each node as the message packet works its way around the ring. Delay can be imposed when a node must complete the transmission of a native message packet before retransmitting a foreign message packet. A SCRAMNet GT Network can accommodate up to 255 nodes per network ring.

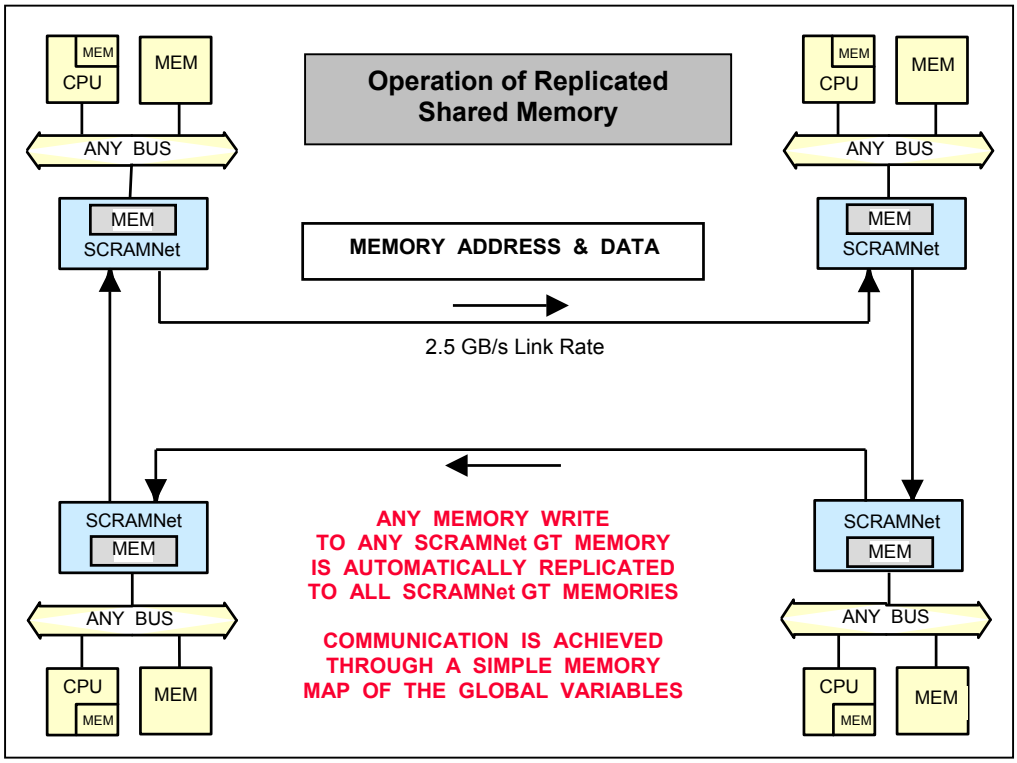


Figure 4-1 Replicated Shared Memory

4.2.3 Physical Interface

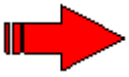
Fiber Optic Short Wavelength (850 nm)—2.5 GB/s
Fiber Optic Long Wavelength (1300 nm)—2.5 GB/s

4.2.4 Network Size

The network supports up to 255 nodes. Each node on the GT network has an associated node ID. When a node transmits a native packet, it sends its node ID as part of the packet header. When a node receives a data packet, it compares its own node ID with the node ID in the received packet header. If the node IDs match, the packet is identified as a native packet and is not retransmitted. If they do not match, the packet is identified as a foreign packet and is retransmitted without modification. This packet removal mechanism prevents traffic from circulating around the ring more than once.

It follows from above, that if two nodes on a ring share the same node ID, they will remove non-native packets from the ring.

Valid node IDs range from 0 to 255. However, node ID 0 is used by default when boards are first powered on and is not recommended for use. The node ID is software programmable.



NOTE: It is possible the architecture will treat network traffic originating from node ID 0x00 differently to reduce effects from improperly initialized nodes. Consequently, the number of nodes supported is 255.

The maximum fiber length supported is 10 km based on the ring size, media used, and status messaging.

4.2.5 Interface Standards

The SCRAMNet GT interface is a proprietary interface running at 2.5GB/s. The interface uses both 8B/10B decoding and CRC32 error checking.

4.2.6 Network Framing

Frame types include:

- Variable length data frame
- Sub-length data frame (for transactions less than 32-bits)
- Interrupt frames.

Message packets are variable-length message with support for payload sizes as integer multiples of four bytes. Payload size can range from a 4-byte minimum to a 128-byte maximum. Network logic transparently handles appropriate generation of framing, including length selection. Framing overhead includes delimiters, source node ID, age, address, and other control functions.

Sub-length data frames include 32-bits of data with four independent byte enables to support transfer sizes less than 32 bits, preserving the concept of memory transparency.

4.2.7 Link Interface

- Laser Enable (one per link)
- Link Select-Link Up
- Laser Signal Detect (one per link)

4.2.8 Network Throughput

The maximum network throughput is approximately 2.5 GB/s to 205 MB/s (base10).

4.2.9 Error Detection

All network frames include a Cyclical Redundancy Check (CRC) to facilitate error detection in the network receiver interface.

The CRC is automatically verified by network hardware without user intervention. In addition, the end of frame delimiter incorporates flags for CRC errors such that a detected CRC error on one node is detectable on other downstream nodes, even though the frame may have been modified (corrected) in the retransmission process. The network also includes other error detection mechanisms, such as an invalid transmission word encountered during the decoding process. Network errors include CRC error, encoding error, framing error, and expired message.

4.2.10 Latency

Node insertion latency and node retransmit latency are approximitly 1µs each.

4.2.11 Throughput

Sustained throughputs of 2.5 GB/s are possible using DMA or high performance 64 bit/66 Mhz platforms.

4.2.12 Message Ordering

The host writes to the network progress in-order; multiple priorities cannot be used. Once on the network, messages are not reordered.

4.2.13 Memory

In its simplest form, the SCRAMNet GT Network system appears as general-purpose memory. The use of this memory depends only on the conventions and limitations imposed by the specific host computer system and operating system. On most processors, this means that the application program can use this memory in the same way as any other data-storage area of memory. The memory cannot be used as instruction space.

The major difference between SCRAMNet GT memory and system memory is that any data written into SCRAMNet GT memory is automatically sent to the same SCRAMNet GT memory location in all nodes on the network. This is why it is also referred to as replicated shared memory.

When a host computer writes to the shared memory, the SCRAMNet GT node host adapter supplies the proper handshaking logic. The shared memory behaves somewhat like resident or local memory.

A device driver is required for specified operating systems. The device driver performs the following functions: device configuration, mapping memory, interrupt handling, hardware accessing, performing transfer of user buffers to/from network memory, and memory allocation. When performing a transfer of the user-specified buffer to/from network memory, the driver works in conjunction with the operating system and the SCRAMNet GT, breaking the user buffer into multiple DMA transfers. This is a result of paging, physical memory requirements, and the need to have a contiguous memory region for the DMA descriptors.

4.2.13.1 Memory Management

When the populated memory size is less than the size supported by network addressing, the SCRAMNet GT's shared memory is mapped into the lowest area of network address space.

4.2.14 FIFO Buffers

The SCRAMNet GT card contains various FIFO buffers used for temporarily storing information during normal send and receive operation of the node.

4.2.14.1 Retransmit FIFO

This buffer is used to receive foreign messages from the network, and send them on, or to hold received foreign messages while inserting a native message from the host onto the network.

Each node is responsible for receiving foreign messages, writing them to its copy of shared memory, and re-transmitting the message to the next node.

4.2.14.2 Receive FIFO

The Receive FIFO is designed as a temporary holding place for incoming foreign messages while the shared memory is busy servicing a host request. This FIFO is designed so it can never be overrun.

4.2.15 Network Status Messaging

The network logic in each node deploys a timer in the transmission logic that identifies when a local network status-messaging interval has expired. This interval of approximately 1µs is chosen based on maximum media transmission delays, fidelity of status updates, and impacts to network throughput. When the status message interval expires, the node generates a network status message automatically (with no software overhead).

Priority for transmitted traffic is first given to retransmitted traffic (from the insertion buffer), then to network status messages, and finally to locally generated traffic (from the transmit buffer). When the network status message is generated, it includes the local node ID and applicable status/control information (local age determined by the local receive logic, information regarding the local node such as RX_EN, TX_EN, RT_EN, link up, signal detects and enables for applicable link interfaces, etc.).

4.2.15.1 Look-Up Table

Each node that receives these status messages decodes the appropriate information from the status message and stores this in a look-up table based on the age of the packet when it was received. This indicates when updates to each table entry have been made. By examining the entries in the lookup table, the topology of the network from each node's perspective can be determined. It is also possible to detect duplicate network node IDs because the reported "age" field, which is shared between nodes automatically, will vary. Based on this variance, it is also possible to determine where ring integrity is broken. The automatic nature of this messaging ensures updates that react to network topology changes with no user intervention.

4.2.15.2 Shared Information

- Node ID
- Upstream Node ID
- Laser Enable (one per link)
- Link Select
- Redundant Link Capable
- Transmit Enable
- Receive Enable
- Retransmit Enable
- Write Me Last
- Link Up
- Laser Signal Detect (one per link)
- Data valid

4.2.16 Interrupts

Selectable local host interrupts are available for error and status conditions.

In addition, broadcast and unicast network interrupts are available for user-level signaling and synchronization between nodes. These interrupts are initiated by the sender and are optionally received by the other nodes. A 32-bit user-defined vector identifies conditions associated with this notification event. These network interrupts propagate from host to host through the network medium.

The receiving nodes can individually enable up to 32 general-purpose broadcast network interrupts. The sender at origination specifies the user-defined interrupt number and vector. These broadcast network interrupts are named HBI (Host Broadcast Interrupt) events.

Up to 256 (per node) general-purpose unicast network interrupts can be used for point-to-point signaling between nodes. While each node can enable receipt of the unicast interrupts, they are not individually selectable on a node-by-node basis based on the source node ID. Rather, enabling unicast interrupts allows an interrupt on reception of a unicast network interrupt from any node on the network. The sender specifies the destination node ID and user-defined interrupt vector at origination. These unicast network interrupts are named HUI (Host Unicast Interrupt) events.

In normal operation, network interrupts will not be processed on receipt by the originating node (e.g., interrupt self function). However, when Interrupt Self is enabled, network interrupts can be processed (subject to interrupt enables) on the originating node.

Network interrupts (HBI and HUI) may be initiated via PIO accesses (via the appropriate SW function) or via an interrupt flag (separate chain entry) on DMA operations. Separate target locations for each HBI and HUI interrupt eliminate the necessity of a semaphore for network interrupt initiation.

The HBI and HUI events are stored in the Network to Host Interrupt Queue (NHI_Q), located on the SCRAMNet GT card. HBI and HUI events are stored in the NHI_Q in the order of reception. The receiving node has access in the interrupt queue to the source node ID, interrupt vector, and interrupt type (broadcast with interrupt level or unicast). A counter indicates the number of interrupts that have been written to the NHI_Q. A subset of this counter value (as a function of queue size) indicates the value of the write pointer. The queue provides numerous advantages over a FIFO including: performance, parallel accesses by multiple threads, elimination of access mechanism to protect critical region, and the ability to skip queue entries.

4.2.17 Modes of Operation

The Figure 4-2 shows the configuration switches for each mode of operation.

4.2.17.1 Write-Me-Last Mode

The Write-Me-Last mode of operation allows the originating node to be the last node in the ring to have the data deposited to its memory. This can be useful for synchronization. This means that when the host performs a write to the SCRAMNet GT shared memory, this data is not immediately written to the host node's memory, but is first sent to the other nodes on the network. When the message returns to the originating node it is written to shared memory, and is then removed from the network ring.

Therefore, host-originated data written to shared memory travels the ring updating the SCRAMNet GT node memories on the ring and, upon returning to the originating node, that node writes the data to its own shared memory as the last node on the ring. This guarantees that the data is available on all other nodes.

WARNING: This mode is not recommended for applications that use duplicate node IDs or for open-ring topologies.

4.2.17.2 TX Enable

Transmit enable mode allows data to be transmitted to the network. The default condition is on.

4.2.17.3 RX Enable

Receive enable mode allows data to be received from the network. The default condition is on.

4.2.17.4 RT Enable

Retransmit mode allows received data to be retransmitted to the network. The default condition is on.

4.2.17.5 Interrupt Self

Interrupt self allows network interrupts generated by the node to interrupt the generating node upon receipt from the network. The default condition is OFF.

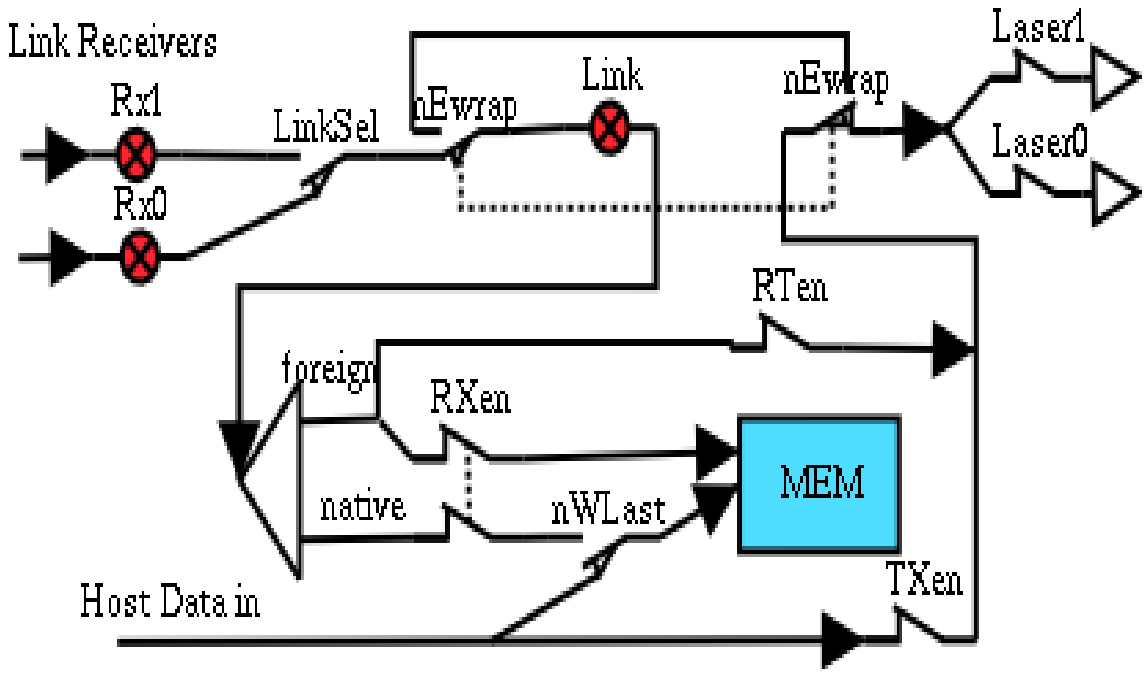


Figure 4-2 Configuration Switch Diagram

4.3 SCRAMNet GT Block Diagram

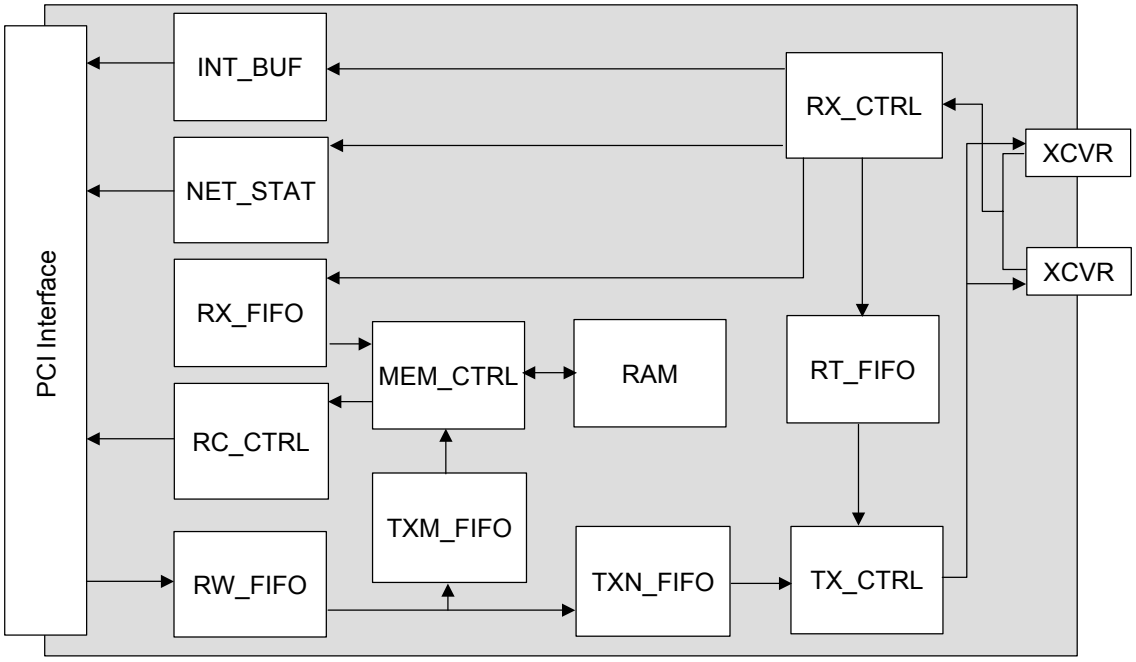


Figure 4-3 SCRAMNet GT Block Diagram

4.3.1 Network Logic

XVCR ..... SFP 2.5 GB/s fiber optic transceiver.

RX_CTRL..... Receive control logic. Decodes receive framing protocol

RT_FIFO..... Retransmit FIFO. Buffers retransmitted link data

TXN_FIFO..... Transmit to Network FIFO. Buffers network transmit data

TX_CTRL..... Transmit control logic. Handles transmit framing protocol

4.3.2 Host Logic

INT_BUF ..... Network to Host Interrupt Queue. Buffers received network interrupts

NET_STAT..... Network Status Look Up Table

RX_FIFO ..... Receive FIFO. Buffers received data

MEM_CTRL..... Memory Controller

RAM ..... Memory. 125 MHz 32-bit DDR SDRAM

TXM_FIFO..... Transmit to Memory FIFO. Buffers transmit data

RW_FIFO ..... Read/Write FIFO

RC_CTRL..... Read Cache Controller

4.4 Host Hardware

4.4.1 Target Interface

4.4.1.1 Control plane

The control plane supports control and status of both host and link interfaces via Control and Status Registers.

4.4.1.2 Data plane.

The data plane can also be used to access shared memory and initiate network traffic. The target interface may be accessed by the host microprocessor (via PIO operations) or by another PCI card (via peer-to-peer DMA initiated by the other board's DMA controller).

4.4.2 Initiator Interface

4.4.2.1 Data Plane.

The initiator interface may be used to access shaired memory for DMA to other boards' target interface.

4.4.3 Bus Support

The hardware supports 33 MHz/66 MHz PCI operation for both 32-bit and 64-bit buses.

The hardware supports a +3.3.V PCI signaling voltage.

4.4.4 Byte Swapping

The hardware contains steering logic supporting both Little Endian and Big Endian accesses for the target and initiator interfaces. The byte-swapping logic also includes the ability to swap 32-bit words within a 64-bit access. The target and initiator logic contain independent settings for the byte and word (32-bit) swapping.

- CSRs – Network Management Status (8 byte) – driver controlled (BAR0 & BAR1)
- Target Shared Memory/Network (8, 32 byte) – user controlled (BAR2)
- Initiator Shared Memory/Network (8, 32 byte) – planned

4.4.5 Interrupt Support

The hardware supports both network and applicable host interrupts.

No interrupts are generated by the hardware until explicitly enabled by the software (driver and/or user).

Network interrupts (HBI and HUI) may be initiated via PIO accesses (via the appropriate SW function) or via an interrupt flag (separate chain entry) on DMA operations (planned.)

Separate target locations for each HBI and HUI interrupt avoid the necessity of a semaphore for network interrupt initiation.

4.4.6 Counter/Timers

The host logic provides 16 counter/timers for monitoring network performance. While associated with network functionality, this logic resides within the host interface. Each counter/timer has its own dedicated mode of operation to allow simultaneous monitoring of three critical parameters (see Appendix B for definitions).

- Network timer
- Host timer
- Latency timer
- Shared Memory Traffic counter
- Interrupt Traffic counter
- Hunt Traffic counter
- Network Interrupt counter
- Host Interrupt counter
- Link Error counter
- Link Down counter
- Decoder Error counter
- Synchronization Error counter
- CRC Error counter
- EOF Error counter
- Protocol Error counter
- RX FIFO Error counter

4.4.7 Reconfiguration

You can install firmware updates without returning the card to the factory.

LEDs on the subassembly provide a visual status of important product functions, such as network status (see Chapter **3**).

See Section 2.3.7 for descriptions of these LEDs

APPENDIX A

SPECIFICATIONS

TABLE OF CONTENTS

A.1 Hardware Specific

A.1.1 PCI Specifications

Hardware Compatibility:..... PCI specification version 2.1
Physical Dimensions:
PCI Card..... 174.6 x 106.7 mm, one slot
Weight:
PCI Card..... 144.57 g
Electrical Requirements: ..... 10 watts per PCI Spec. version 2.1
Temperature Range
Storage: ..... -40° TO +85° C
Operation:..... 0° to +50° C Humidity Range:
Storage..... 0% to 95% (noncondensing)
Operating..... 10% to 90% (noncondensing)
Network Line Transmission Rate: ..... 2.5 GB/s
Message Length: ..... Variable
Bit Error Rate:..... TBD
Maximum Nodes on Network Ring: 255
Maximum Node Separation:
Standard Fiber: ..... 300 meters
Long Link Fiber: ..... 10 kilometers
Shared Memory:
On-board Memory..... 128 MB
Effective Per-Node Bandwidth:
4 bytes/packet: ..... **TBD**
128 bytes/packet: ..... 200 MB/s
Node Latency:
4 bytes/packet: ..... 1 µs
128 bytes/packet: ..... 1 µs
Mean Time Between Failures (MTBF)..... TBD

A.1.2 PMC Specifications

Physical Dimensions:
PMC Card..... 74.0 x 149.0 mm, one slot
Weight:
PMC Card..... 124 g (Conduction cooled board, 90.71 g)
Electrical Requirements: ..... 10 watts
Temperature Range
Storage: ..... -40° TO +85° C
Operation:..... 0° TO +50° C (-40° TO +85° C, conduction cooled)
Humidity Range:
Storage..... 0% to 95% (noncondensing)
Operating..... 10% to 90% (noncondensing)
Network Line Transmission Rate: ..... 2.5 GB/s
Message Length: ..... Variable

Bit Error Rate: ..... TBD
Maximum Nodes on Network Ring: 255
Maximum Node Separation:
    Standard Fiber: ..... 300 meters
    Long Link Fiber: ..... 10 kilometers
Shared Memory:
    On-board Memory ..... 128 MB
Effective Per-Node Bandwidth:
    4 bytes/packet: ..... TBD
    128 bytes/packet: ..... 200 MB/s
Node Latency:
    4 bytes/packet: ..... 1 µs
    128 bytes/packet: ..... 1 µs
Mean Time Between Failures (MTBF) ..... 12,395 hours at 80°C Airborne Inhabited Cargo (Conduction cooled board)

A.2 Media Interface Specifications

A.2.1 Fiber-Optic Media Interface Specifications

Connector:..... Duplex LC

850 nm:

Media..... 50 µm or 62.5 µm multimode fiber
Fibre Channel Formats:..... 100-M5-SN-I (1 Gbps, 50 µm fiber)
100-M6-SN-I (1 Gbps, 62.5 µm fiber)
Maximum Fiber Length: ..... 500 meters with 50 µm fiber
300 meters with 62.5 µm fiber
Transmit Wavelength:..... 830 to 860 nm
Transmit Power: ..... -10 to-5 dbm
Receive Wavelength:..... 770 to 860 nm
Receive Sensitivity:..... -16 to 0 dbm

1300 nm:

Media..... 9 µm single-mode fiber*
Fibre Channel Formats:..... 100-SM-LL-I (1 Gbps, single-mode fiber, intermediate distance)
100-SM-LC-L (1 Gbps, single-mode fiber, low cost long distance)
Maximum Fiber Length: ..... 10 km
Transmit Wavelength:..... 1285 to 1330 nm
Transmit Power: ..... -9.5 to -3 dBm
Receive Wavelength:..... 1100 to 1600 nm
Receive Sensitivity: -19 to -3 dBm

A.3 PCI Configuration Space

Vendor ID: 0x1387 (Curtiss-Wright Controls, Inc.)
Device ID: 0x5310 (SCRAMNet-GT)
SubVendor ID: 0x1387 (Curtiss-Wright Controls, Inc.)
Subsystem Device ID: 0x5310 (SCRAMNet-GT)
Base Class Code: 0x02 (Network Controller)
Sub-Class Code: 0x80 (Other network Controller)
Register-level Programmable Interface: 0x00 (non-defined for this base class)

BAR0 (Control/Status registers):
Enabled
Size=256B (0x100 bytes)
Prefetching Disabled
Memory Space
A32
BAR1 (Network Management registers):
Enabled
Size=8kB (0x2000 bytes)
Prefetching Disabled
Memory Space

A32
BAR2 (Shared Memory):
Enabled
Size= Host Bus Requested Target Memory Size
Typically same as Populated Memory Size
128MB (0x8000000 bytes)
512MB (0x20000000 bytes)
Prefetching Enabled
Memory Space
A32

A.4 Part Number Ordering Information

A.4.1 66 MHZ SC-GT PMC Ordering Information

Order Number	Description
H- AS-GPM128SC-00	SCRAMNet GT, Unpopulated
H- AS-GPM128SC-20	SCRAMNet GT, 850 Nm Short Wave Pluggable Transceiver
H- AS-GPM128SC-22	SCRAMNet GT , 850 Nm Short Wave Pluggable Transceiver (x2)
H- AS-GPM128SC-23	SCRAMNet GT, (x1) & 1300nm (x1) Pluggable Transceivers
H- AS-GPM128SC-30	SCRAMNet GT, 1300nm Long Wave Pluggable Transceiver
H- AS-GPM128SC-33	SCRAMNet GT, 1300nm Long Wave Pluggable Transceiver (x2)

A.4.2 66 MHz SC-GT PCI Ordering Information

Order Number	Description
H- AS-GPC128SC-00	SCRAMNet GT, Unpopulated
H- AS-GPC128SC-20	SCRAMNet GT, 850 Nm Short Wave Pluggable Transceiver
H- AS-GPC128SC-22	SCRAMNet GT , 850 Nm Short Wave Pluggable Transceiver (x2)
H- AS-GPC128SC-23	SCRAMNet GT, (x1) & 1300nm (x1) Pluggable Transceivers
H- AS-GPC128SC-30	SCRAMNet GT, 1300nm Long Wave Pluggable Transceiver
H- AS-GPC128SC-33	SCRAMNet GT, 1300nm Long Wave Pluggable Transceiver (x2)

APPENDIX B

COUNTER/TIMER DEFINITIONS

B.1 Counter/Timer Definitions

Counter/Timer	Definition
NET_TMR	Network timer. This timer is incremented on every network transmit clock period. For 2.5 Gbps product configurations, the network transmit clock period is 8 ns and rolls over approximately every 34.4 s.
HST_TMR	Host timer. This timer is incremented on every host bus clock period. For 66 MHz PCI product configurations, the host bus clock period is approximately 15.2 ns and rolls over approximately every 65.2 s.
LAT_TMR	Latency timer: This timer measures transit latency. The timer begins counting on transmission of the auto-message and stops counting on receipt of a native auto-message. The latency is incremented on every network transmit clock period that the native auto-message is in transit. For 2.5 Gbps product configurations, the network transmit clock period is 8ns and rolls over approximately every 34.4 s.
SM_TRFC_CNTR	Shared Memory Traffic counter. This counter is incremented on every reception of 32-bit network shared memory data phase (native or foreign). Note that network memory traffic representing network traffic of less than 32-bits are treated like 32-bits for purposes of counting network traffic.
INT_TRFC_CNTR	Interrupt Traffic counter. This counter is incremented on every reception of network interrupt traffic (native or foreign).
HNT_TRFC_CNTR	Hunt Traffic counter. This counter is incremented on every reception of 32-bit network shared memory data phase from the node ID specified by the HNT_ID field to the LNK_CTL register. Note that network memory traffic representing network traffic of less than 32-bits are treated like 32-bits for purposes of counting network traffic. Note also that this counter only counts shared memory traffic from the specified node and not network interrupt traffic.
NHIQ_INT_CNTR	Network Interrupt counter. This counter is incremented on every network interrupt that has been placed into the NHIQ. This value gives a total number of interrupt received and the lowest bits (8 for a queue of 256) give the effective address of the next interrupt location within the queue, allowing the current position of the last interrupt data to be determined by subtracting 1.
HST_INT_CNTR	Host Interrupt counter. This counter is incremented on every new assertion of a host interrupt request.
LNK_ERR_CNTR	Link Error counter. This counter is incremented on every network error (including decoder error, synchronization error, CRC error, EOF error, protocol error, RXF error, and transition of link down).
LNK_DOWN_CNTR	Link Down counter. This counter is incremented on transition of a link down.
DEC_ERR_CNTR	Decoder Error counter. This counter is incremented on every 8b/10b decoding error.

Counter/Timer	Definition
SYNC_ERR_CNTR	Synchronization Error counter. This counter is incremented on every ordered set synchronization error.
CRC_ERR_CNTR	CRC Error counter. This counter is incremented on every CRC error.
EOF_ERR_CNTR	EOF Error counter. This counter is incremented on every end-of-frame error.
PRTCL_ERR_CNTR	Protocol Error counter. This counter is incremented on every protocol error.
RXF_ERR_CNTR	RX FIFO Error counter. This counter is incremented on every RX FIFO error.

GLOSSARY

address-only cycle ---------- A DTB cycle that consists of an address broadcast, but no data transfer. The slave does not acknowledge address-only cycles and the master terminates the cycle without waiting for an acknowledgment.

alarm ---------- Manually resetable latched error condition.

bad message---------- A message error condition reported by a node's receiver circuitry. This condition is automatically corrected by SCRAMNet+ hardware.

block read cycle ---------- A DTB cycle used to transfer a block of 1 to 256 bytes from a slave to a master. This transfer is done using a string of 1-, 2-, or 4-byte data transfers. Once the block transfer is started, the master does not release the DTB until all of the bytes have been transferred. It differs from a string of read cycles in that the master broadcasts only one address and address modifier (at the beginning of the cycle.) The slave increments this address on each transfer so that the data for the next cycle is retrieved from the next higher location.

block write cycle ---------- A DTB cycle used to transfer a block of 1 to 256 bytes from a master to a slave. The block write cycle is very similar to the block read cycle. It uses a string of 1-, 2-, or 4-byte data transfers and the master does not release the DTB until all of the bytes have been transferred. It differs from a string of write cycles in that the master broadcasts only one address and address modifier (at the beginning of the cycle). Then the slave increments this address on each transfer so that the next transfer is stored in the next higher location.

board ---------- See PCB.

BURST ---------- A protocol where messages are transmitted without error correction to gain higher throughput.

BURST+ ---------- Also BURST PLUS. A variable-length message packet size enhancement for the burst protocol. Maximum packet size may be set to 256 bytes or 1024 bytes, plus a 46-bit header.

bus timer---------- A functional module that measures the time each data transfer takes on the DTB and terminates the DTB cycle if a transfer takes too long. Without this module, it could wait forever for a slave to respond if the master tries to transfer data to or from a nonexistent slave location. The bus timer prevents this by terminating the cycle.

card---------- See PCB.

carrier loss---------- A hardware failure reported when the incoming light link has failed because it is too weak or nonexistent in one or both fibers from the preceding node.

CSR ---------- Control/status register. These registers are used for configuration and control and provide status values that can be interrogated. These registers are located in the computer's address space. Power-up register values are contained in the EEPROM.

daisy chain topology---------- A configuration in which devices are connected to each other in sequence

deterministic ---------- Completely predictable message transit time from application to application.

DTB---------- Data transfer bus. One of the four buses provided by the backplane. The data transfer bus allows masters to direct the transfer of binary data

	between themselves and slaves.
data-transfer-bus cycle	A sequence of level transitions on the signal lines of the DTB that result in the transfer of an address or an address and data between a master and a slave. There are 34 types of data transfer bus cycles.
DMA	Direct memory access transfer. An I/O transfer conducted by a device controller which accesses memory directly and, as a result, can transfer a large volume of data without requesting a processor interrupt after each unit amount. Contrast with programmed I/O (PIO) transfer.
device interrupt	An interrupt received on interrupt priority levels 20-23. Device interrupts can be requested only by devices, controllers, and memories.
DSP pipeline	A series of processing nodes where each successive node takes the results from the previous node and performs an additional layer of processing.
edges	Transitions that appear on a signal line.
EEPROM	The EEPROM stores the initial power-up register values. The EEPROM can be programmed either over the backplane or by most PROM programmers. An EEPROM Initialization (EPI) Program is included in the Systran software utilities.
falling edge	The time during which a signal makes its transition from high to low.
FIFO	A data storage method; First In First Out. Also refers to the specific storage area; Transmit FIFO, Interrupt FIFO, etc.
foreign message	A message that is in (passing through) a node other than the one of origin.
functional module	A collection of electronic circuitry that resides on one board and works together to accomplish a task.
halfword	Any double byte on even 16 bit boundaries.
insert a node	The act of placing a node on a network for the purpose of transmitting and receiving messages.
interrupt	An event that changes the normal flow of instruction execution other than an exception or a branch, jump, case or call instruction.
interrupt acknowledge cycle	A DTB cycle, initiated by an interrupt handler, that reads a status/ID from an interrupter. An interrupt handler generates this cycle when it detects an interrupt request from an interrupter and it has control of the DTB.
interrupter	A functional module that generates an interrupt request on the priority interrupt bus and then provides states/ID information when the interrupt handler requests it.
interrupt handler	A functional module that detects interrupt requests generated by interrupters and responds to those requests by asking for status/ID information.
ISR	Interrupt service routine. A routine executed when a device interrupt occurs.
I/O space	The regions of host processor physical address space that contain the configuration registers, device control, states registers and data registers. These regions are physically noncontiguous.

latched ---------- Data is electrically stored in a circuit until it is needed. A method of coordinating two synchronous events.

locking a page in memory ------ Making a page ineligible for either paging or swapping. A page stays locked in physical memory until the operating system specifically unlocks it.

longword ---------- Four bytes (32 bits) of data.

loopback ---------- A method of transmitting to the same node's receivers for testing purposes. Applies to both fiber optic and wire media. Also, a test that loops the outgoing signal back to its source.

master ---------- A functional module that initiates DTB cycles to transfer data between itself and a slave module.

message packet ---------- See packet.

native message ---------- A message that is received by the node of origin.

node latency ---------- The time delay at a node before a foreign message can be retransmitted.

packet ---------- A message that travels on the network. The minimum packet consists of 81 bits and 1 start bit. The packet includes five fields: Source ID (8 bits), Age (8 bits), Control (3 bits), Data Address (21 bits), Data (32 bits), and 9 parity bits; one for every 8 bits.

PCB ---------- A printed circuit board, its collection of electronic components, and the connectors that can be plugged into the backplane.

physical address ---------- The address used by hardware to identify a location in physical memory or on directly-addressable secondary storage devices (such as disks). A physical memory address consists of a page-frame number and the number of a byte within the page.

PLATINUM ---------- A protocol where messages are transmitted as fast as the system will allow with error correction enabled.

PLATINUM+ ---------- Also platinum plus. A variable-length message packet size enhancement for the platinum protocol. Maximum packet size may be set to 256 bytes or 1024 bytes, plus a 46-bit header.

point-to-point topology ---------- A network topology in which one node connects directly to another node.

priority interrupt bus ---------- One of the four buses provided by the backplane. The priority interrupt bus allows interrupter modules to send interrupt requests to interrupt handler modules, and interrupt handler modules to acknowledge these interrupt requests.

PIO ---------- Programmed I/O transfer. An I/O transfer, primarily conducted by a driver program, that requires processor intervention after each byte or word is transferred. Contrast with Direct Memory Access (DMA) transfer.

protocol violation ---------- A signal error at the physical layer (fiber or coax) resulting from noise on the transmission lines or a result of hardware failure. This violation can be any one of the following:

Missing transition for two clock periods on either line

Parity error

Framing error

read cycle ---------- A DTB cycle used to transfer 1-, 2-, 3-, or 4-bytes from a slave to a

	master. The cycle begins when the master broadcasts an address and an address modifier. Each slave captures this address and address modifier, and checks to see if it is to respond to the cycle. If so, it retrieves the data from its internal storage, places it on the data bus, and acknowledges the transfer. Then the master terminates the cycle.
read-modify-write cycle	A DTB cycle that is used to both read from, and write to, a slave's byte location(s) without permitting any other master to access that location during that cycle. This cycle is most useful in multi-processing systems where certain memory locations are used to control access to certain systems resources, for example, semaphore locations.
requester	A functional module that resides on the same board as a master or interrupt handler and requests use of the CTB whenever its master or interrupt handler needs it.
retry	A hardware failure condition reported when the first attempt to send a message around the network has resulted in some type of bit error. The message will be retransmitted indefinitely by the originating node until it is received correctly by the originating node. Valid only in error correction mode (PLATINUM.)
retry time-out	A hardware failure condition reported when the first attempt to send a message around the network is not received by the originating node within the time out period specified in CSR5. The message will be retransmitted indefinitely by the originating node until it is received correctly by the originating node. Valid only in error correction mode (PLATINUM.)
ring topology	A network topology in which every node has exactly two branches connected to it.
rising edge	The time during which a signal makes its transition from low to high.
Rx	Abbreviation for receive or receiver.
SCSI	Refers to the American National Standard for Information Systems Small Computer System Interface - 1 (X3.131-1986) or the ANSI Small Computer System Interface - 2 (X3.131-1989). This standard defines mechanical, electrical and functional requirements for attaching small computers to each other and to intelligent peripheral devices.
SFP	Small form factor pluggable transceiver.
shared memory (SM)	SCRAMNet memory physically located on the network board. This dual-ported memory is accessible by the host and the network. A host write to shared memory results in a transmitted write to all SCRAMNet nodes at the same relative location.
shortword	16 bits. Also referred to as halfword.
signal mnemonics	Terms used to identify signal line events. (1) An asterisk following the name of signals that are level-significant denotes the signal is true/valid when the signal is low. (2) A asterisk following the name of signals that are edge-significant denotes the actions initiated by that signal occur on the falling edge.
slave	A functional module that detects DTB cycles initiated by a master and, when those cycles specify its participation, transfers data between itself and the master.

slot ---------- A position where a board can be inserted into a backplane. If the system has both a J1 and a J2 backplane (or a combination J1/J2 backplane) each slot provides a pair of 96-pin connectors. If the system has only a J1 backplane, then each slot provides a single 96-pin connector. Also, another name for message packet.

system clock driver ---------- A functional module that provides a 16 MHz timing signal on the utility bus.

time-out---------- Also network time-out. The time written to CSR5 that must elapse before a native message will be retransmitted. The time-out must be a non-zero value.

Tx ---------- Abbreviation for transmit or transmitter.

UAT---------- A master that sends or receives data in an unaligned fashion.

utility bus---------- One of the four buses provided by the backplane. This bus includes signals that provide periodic timing and coordinate the power-up and power-down of sequence of the system.

write cycle---------- A DTB cycle used to transfer 1-, 2-, 3-, or 4-bytes from a master to a slave. The cycle begins when the master broadcasts an address and address modifier and places data on the DTB. Each slave captures this address and address modifier, and checks to see if it is to respond to the cycle. If so, it stores the data and then acknowledges the transfer. The master then terminates the cycle.

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