Datel DVME-630A2

High-Speed Analog Input Board

In Stock

New From Surplus Stock

Open Web Page

https://www.artisantg.com/73220-1

DATEL®
INNOVATION AND EXCELLENCE

DVME-630

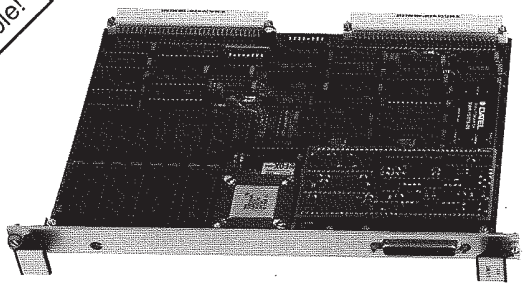
Very High Speed VME bus A/D-DSP Coprocessor Board

PRODUCT DATA

FEATURES

- **Up to 4MHz A/D sample rate**
- **Up to 16S/8D analog input channels**
- **Choice of 12- or 14-bit A/D resolution**
- **4-Channel simultaneous sample/hold's are optional**
- **On-board 320C30 32MHz digital signal processor**
- **512 kilobyte dual-ported RAM**
- **Two 1k x 32 internal DSP RAM**
- **8k x 32 Expansion RAM**
- **On-board DSP library - FFT's, filters, matrix math, floating point, etc.**
- **Fast, simple, powerful command Executive**
- **No local programming required.**
- **Vectored interrupt to VME bus host**

1.5Mb fast SRAM available!



DESCRIPTION

Advanced performance from the DVME-630's on-board Digital Signal Processor (DSP) offers a broad range of high speed waveform analysis and recording applications. The DVME-630 will acquire up to sixteen analog input channels, digitize them and store them in local memory while DSP math processing and data transfer is done concurrently. The system is intended for preprocessing "seamless" A/D data streams to the host system.

The DVME-630 is ideal for non-stop, continuous Fast Fourier Transform (FFT) processing, communications receiver signal collection to disk or simultaneous graphics display of spectral data. Application areas include signal recovery from noisy channels, harmonic distortion analyzers and vibration/resonance filtering systems. For use with ultrasonic, sonar or acoustic signals, the interrupt-driven, simultaneous block transfers of data insure no information loss. Other uses include high speed mapping and imaging, satellite channels, astrophysics, seismology, biomedical signals, array processing, control systems, simulators, engine analyzers, aerodynamics and vehicle systems.

The board consists of a pluggable analog input subsection, timer-counters, DSP central processing unit (CPU), dual port RAM, local RAM, bus interface, registers and DC power supply. Input signals pass through a very high speed channel multiplexer (except model DVME-630D,F) to a sampling analog-to-digital (A/D) converter. On model DVME-630A or F, two or four channels are acquired simultaneously. A choice of channels, input ranges, speeds and resolution is offered in the analog section.

A/D triggering for spectral and FFT applications must be precisely controlled. This is handled by a programmable timer-counter section which can control the interval between A/D conversions and the interval between multi-sample A/D

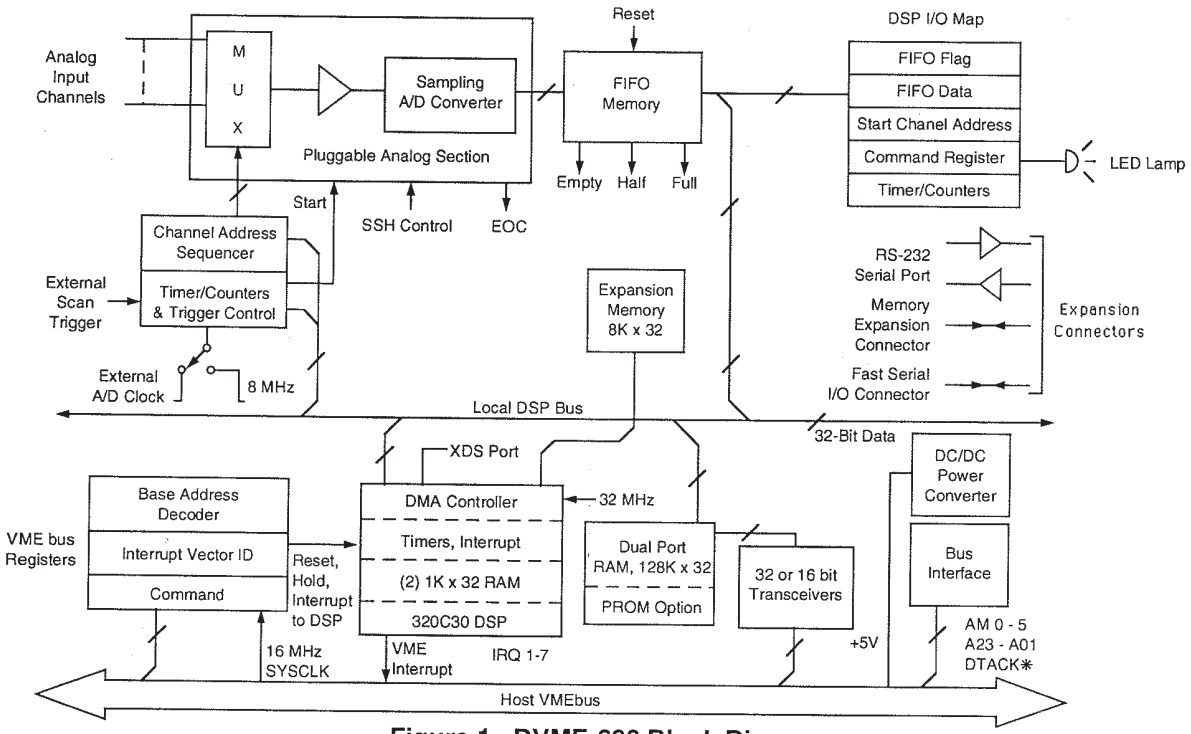


Figure 1. DVME-630 Block Diagram

scans. The number of samples may also be counted for repeating array sampling. The timer-counter may use an on-board crystal oscillator or an external timebase for precision phase-tracking.

The digital output of the A/D passes directly to a first-in, first-out (FIFO) memory. The FIFO acts to decouple the precision timing of the A/D section with the block transfers governed by the DSP internal direct memory access (DMA) controller. Additional timers internal to the DSP are also used.

A/D FIFO data may be sent to dual port random access memory (DPR) shared with the host VME bus. The DPR is organized as 128k by 32 bits of fast static RAM. The user may also set up the DPR as 256k by 16 bits, allowing all access using only the P1 connector if needed. Local A/D-FIFO block transfers may be controlled by the DMA controller in the DSP. The DMA may run in background while math processing continues. Local FIFO and DMA TC interrupts to the DSP arbitrate these activities. Typically, a swapped dual buffer method is used so that samples are not lost during other processing. Local hardware registers control all A/D, FIFO and trigger activity.

Single cycle fetch and execution, parallel instructions, zero-overhead of looping instructions, software variable wait-states, block repeat and a 64-word internal instruction cache memory are some of the advanced high speed features of the Texas Instruments 320C30 DSP. The DSP uses 32-bit local data paths for very high speed. Simultaneous access attempts to the DPR by both the VME bus host and the DSP are resolved by high speed arbitration logic. The DSP also has a separate 8k by 32-bit local expansion memory for the stack or temporary data. The architecture of the DSP allows simultaneous processing of two tables from two sections of memory. This provides optimum processing of FFT's and other array functions.

The DVME-630 DPR appears as both read/write memory addresses and as two hardware control registers mapped into the top of the DPR. The registers include a command register and a software programmable interrupt vector ID register. The DVME-630 will operate with all 680X0, 880X0, 80X86, RISC and SPARC CPU's. The DPR base address may be located anywhere up to 16 megabytes on 512 kilobyte boundaries. The board will also operate with all popular operating systems including SUN, UNIX, OS-9, PDOS, pSOS, VxWorks, MS-DOS, VRTX and others.

Executive Software

Access to the on-board DSP library and all A/D-timer functions is provided in the Executive software package. After loading in the Executive from host disk to the DPR, the DSP is transitioned from reset to run using a command register control bit. The board may be reset at any time using this technique. The comprehensive Executive software package offers fast A/D sample collection and DSP math without writing any local programs. A simple, powerful, high speed command list is used to access the local DSP library. On the VME bus side, the Exec driver controls very fast buffer transfers to disk or memory using VME bus interrupts generated from the DVME-630. Either host DMA transfers or CPU program transfers may be used. Host interrupt levels are also jumper programmable. Software is available in professionally-written, heavily-commented "C" source format on popular disk media. The software is highly portable to most VME platforms.

FUNCTIONAL SPECIFICATIONS

(Typical at +25°C, dynamic conditions, Gain = 1, unless noted)

ANALOG INPUTS			
Number of Channels	4 channels (models A,B,C) 1 channel (model D) 16S/8D channels (model E) 2 simultaneous channels (model F)		
Input Configuration	single-ended, non-isolated (except DVME-630D,E = diff.)		
Full Scale Input Ranges (user-selectable)	0 to +10V ±10V	±5V	±1V
DVME-630A	yes	no	2 chans. gain = 10
DVME-630B	yes	yes	no
DVME-630C	yes	yes	no
DVME-630D	no	no	±5V
DVME-630E	yes	yes	note 8
DVME-630F	0 to +10V	yes	no
Programmable gain	models A and E, see note 8		
Input Impedance [Note 5]	10 MΩ, min. power on (2kΩ, -630D, –1kΩ, -630F) 1.5kilohms power off		
Input Bias Current	±1nA		
Input Capacitance	10pF per channel		
Input Overvoltage	±15V (no damage)		
Overvoltage Recovery Time	2 microseconds maximum		
Common Mode Voltage Range	±10V maximum referred to analog common (-630E). ±1V (-630D)		
Common Mode Reject.	–80dB (g = 100) -630E only [DC to 60Hz]		
Addressing Modes	1. Single channel 2. Simultaneous sampling (DVME-630A and -630F only) 3. Sequential with autosequenced addressing 4. Random addressing by internal software		

SAMPLE/HOLD	
Acq. Time (FSR step) to 0.01% of FSR	900 ns max. (DVME-630A) 750ns max. (DVME-630B,E) 200ns max. (DVME-630C) 50ns max. (DVME-630D) 165ns max. (DVME-630F)
Aperture Delay	15ns (DVME-630A) 20ns (DVME-630B,C,E,F) 10ns (DVME-630D)
Aperture Delay Uncertainty	±8ns (DVME-630A,D) ±40ns (DVME-630B,C,E,F)
Droop Rate	1µV/µs all models except 1.5µs/µs (DVME-630A)
SSH Chanel-to-Channel Linearity Tracking (DVME-630A only)	± 0.03%

A/D CONVERTER	
Resolution	12 bits (DVME-630A,C,D,E) 14 bits (DVME-630B)
Conversion Period	1.6µs (DVME-630B) 500 nanoseconds (DVME-630A,C,E) 200 nanoseconds (DVME-630D) 400 nanoseconds (DVME-630F)
Output Coding	Positive-true right-justified straight binary (unipolar) or right-justified two's complement (bipolar) with sign extension through bit 15.
A/D Trigger Sources (Software selectable)	1. Local Pacer sample clock 2. External TTL sample clock

TOTAL SYSTEM DC CHARACTERISTICS G = 1 [Note 6]	
Integral Non-linearity at +25°C	±1 LSB of FSR (630A,C,E,F) ±1.5 LSB of FSR (630B,D)
Diff. Non-linearity at +25°C	± 0.75 LSB of FSR (630A,C,E) ± 1 LSB of FSR (630B,D,F)
Full Scale Temperature Coefficient	±0.1 LSB per °C (630A,C,E,F) ±0.3 LSB per °C max (630B,D)
Zero or Offset Temp. Coefficient	±0.1 LSB per °C max (630A,C,E,F) ±0.3 LSB per °C max (630B,D)
Power Supply Reject.	±0.004% per % of bus +5V

A/D MEMORY	
Architecture	First-In, First-Out (FIFO)
Memory Capacity	1024 or 4096 samples. No DSP waits.

TOTAL SYSTEM DYNAMIC PERFORMANCE [Note 1]	
System Bandwidth (single channel, half-scale input)	1MHz (630A,C,F) 200kHz (630B,E) 2.5MHz (630D)
Total Throughput to FIFO (single channel, gain=1)	700 nanoseconds (630A) 2 microseconds (630B,E) 625 nanoseconds (630C) 200 nanoseconds (630D) 500 nanoseconds (630F)
Throughput to FIFO per A/D sample (sequential channels, gain = 1) [Note 3]	1 microsecond (630A) 3 microseconds (630B) 2 microseconds (630C) 4 microseconds (630E) 500 nanoseconds (630F)
Total Harmonic Distortion (Note 2)	-72dB (630A,C,E) -75dB (630B) -68dB (630D) -70dB (630F)

TRIGGER CONTROL	
Programmable Timer/Counter Type	82C54 (DSP waits required)
Functions	1. A/D sample counter. 2. A/D start rate (16 bit divisor) 3. SSH sample counter (630A)
Pacer Sample Counter	3 to 65,536 samples. Drives the Acquire flag gate for A/D start pulses. Larger sample blocks may be programmed.
Timer Clock Source (User-selectable)	1. Internal 8MHz crystal clock 2. External TTL input, 10MHz maximum
Trigger	Starts a frame programmable from DSP CLK

LOCAL MICROCOMPUTER	
CPU Type	Texas Instruments TMS 320C30 Digital Signal Processor
Local Data Bus	32 bits
CPU Clock Speed	32MHz
Local DMA Controller	Internal to 320C30 CPU
Primary Memory (Dual access to VME bus)	128k x 32 static RAM, expandable to 384k x 32 total using MEM-30.
PROM Option	32k x 32 of primary memory may be replaced by user-programmed Read Only Memory. Additional wait states may be needed during PROM access.
Expansion Memory (No VME bus access)	8k x 32 static RAM
Internal DSP Memory	Two 1k x 32
Dual Port Access from VME bus	Hold mode by control bit or dynamic hold per each access.
CPU Test Port	Supports TI XDS1000 Extended Development System.
Local Interrupts to DSP	Int 0-3 from VME host request, A/D FIFO or sample count acquire flags or optional external interrupt.
Wait States	May be software programmed via CPU register up to 7 waits. Defaults to 7 waits at reset.

VMEbus INTERFACE	
Standards Compliance	IEEE P1014/D1.0
Data Bus Width	16 bits using P1 connector or 32 bits using P1 and P2. Changed by alternate transceiver sockets on board.
Address Bus	24 address lines (A23-A1) plus 6 Address Modifiers.
Address Modifier Codes	39 hex or 3D hex, selectable.
VME bus Interrupt	1 line, selectable IRQ 1-7*. Asserts maskable programmable 8-bit vector ID code.
VME bus Interrupt Source	via DSP I/O bit (software programmable).
Architecture	SAD24:SD16 or SAD24:SD32 memory-mapped slave consisting of 128k x 32-bit longwords of dual access RAM. The DVME-630 is not a bus master. A small register area overlays the top of the DPR. DSP location 0 is mapped at the bottom of DPR.
Control/Status Functions	DSP halt request, DSP reset/run, VME interrupt enable/disable, vector ID R/W, force local maskable interrupt to DSP.
Data Transfer	Uses 16MHz VME bus SYSCLK signal (required) to generate DTACK* with PAL programmed delay in 67ns steps. Will accept host DMA controller access.

CONNECTORS	
VME bus, P1 and P2	Two 96-pin male DIN connectors.
Analog Input Connect	DB-25S and trigger input
Memory Expansion (32-bit data)	72-pin header, unbuffered. Uses 0.025" square pins, 0.100" spacing, see MEM-30.
XDS CPU Port	12-pin header, 0.1" pinning.
Fast CPU Serial I/O [Incl. trigger, clock, etc.]	20-pin header, unbuffered, 0.1" pinning.
RS-232-C Asynch. Serial Port [uses software UART]	3-pin header (Xmt, Rcv, Gnd), 0.1" pinning.
MISCELLANEOUS	
LED Lamp	Front panel green LED lamp may be controlled by internal register bit for alarms, etc.
Analog Section Modularity	The MUX-S/H-A/D module is socketed for function interchange.
Analog Section Adjustments	Offset and gain per channel for SSH on DVME-630A and 630F. A single offset and gain pot is provided on DVME-630B,C,D,E. Recommended recalibration interval is 90 days in stable conditions.
Power Required	+5V dc ±5% at 4 Amps max. from VME bus.
Operating Temp Range	0 to +60°C. Forced cooling is recommended.
Storage Temp Range	-20 to +85°C
Relative Humidity	10% to 90%, non-condensing.
Altitude	0 to 10,000 feet.
Outline Dimensions	Double height VME, 6U outline. 9.19"W x 6.3"D x 0.6"H (233,5 x 160 x 15,24 mm).
Weight	22 ounces

NOTES

1. Total throughput includes MUX settling time after changing the channel address, S/H acquisition time to rated specifications, A/D conversion and FIFO transfer. Total throughput is not delayed by host software whenever the FIFO is not full.

2. THD test conditions are:
   a. Input frequency 500kHz (DVME-630A,F)
      200kHz (DVME-630B,E)
      300kHz (DVME-630C)
      1MHz (DVME-630D)
   b. Generator/filter THD is -90dB min.
   c. THD computed by FFT to 5th harmonic.

$$THD = 20 * \log 10 \frac{(V2^2 + V3^2 + V4^2 + V5^2)^{0.5}}{V_{IN}}$$

   d. Inputs are 1/2 full scale. No channel advance.
   e. A/D trigger rate = 1.5MHz (DVME-630A), 500kHz (DVME-630B,C,E), 4MHz (DVME-630D)

3. The rates shown for sequential sampling are the maximum A/D converter start rates and include required MUX sequencing and settling delays. For example, if four channels of the DVME-630C were scanned, the maximum sample rate on any one channel would be 2 microseconds X 4 channels = 8 microseconds (125kHz per channel).

4. To avoid overload recovery delays, do not let the analog input exceed ±10 Volts.

5. The input impedance of 10 Megohms minimum avoids attenuation errors from external input source resistance. For many applications, an inline coaxial 50-ohm shunt, inserted adjacent to the front connectors, is recommended to reduce line reflections and standing wave errors.

6. Allow 20 minutes warmup time to rated specifications for model DVME-630B.

7. The DVME-630 must be mapped in the physical memory of the host VME computer. On some operating systems (notably UNIX), a physical-to-logical addressing function supplied with the OS is used to access the board. The OS may need to know about this absolute physical memory reservation at boot-up time using a device driver. See the example programs available with the DVME-630.

8. Programmable Gain

Gains from x1 to x100 are available on the DVME-630E by installing a precision resistor. Additional settling delay will be needed at higher gains. Fixed gains of x1 and x10 on two channels are selectable on the DVME-630A. They offer 1 Volt input ranges.

Simultaneous Sample/Hold

As shown in Figure 2, four input signals are sampled at the same time using the DVME-630A's Simultaneous Sample/Hold (SSH) option. Once the signals are acquired they are rapidly digitized sequentially by the A/D converter. For correlation of phase-related signals, SSH removes skew delay errors from conventional multiplexer scanning. The DVME-630F employs a similar technique using two simultaneous A/D's.

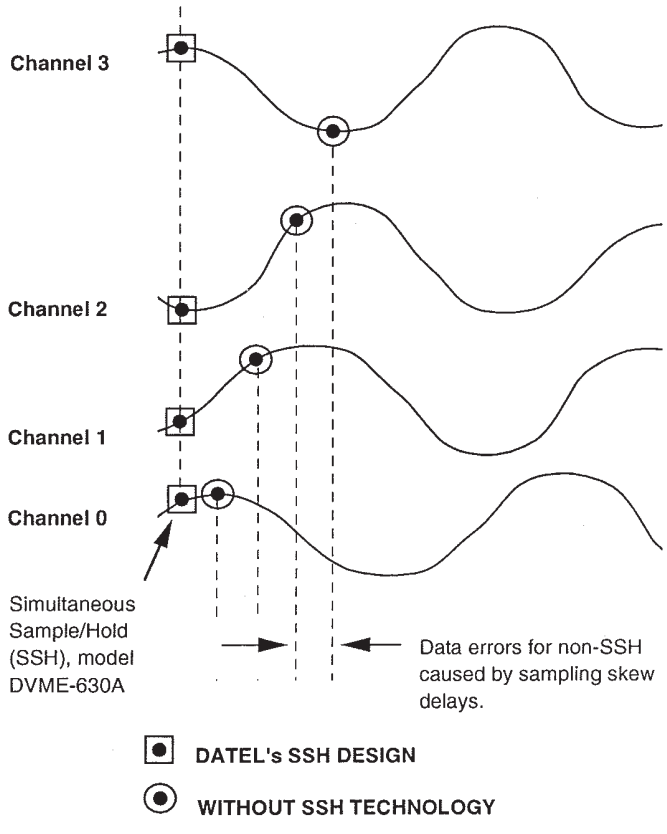


Figure 2. DVME-630A Simultaneous Sample/Hold

DVME-630 Software

The DVME-630 system has been designed to optimize three competing objectives:

Easy to Use (no local programming)
Fast
Powerful (access to full DSP library)

To achieve these mutually exclusive goals, a high speed command list form of control is used. The Application Function Block (AFB) is a short list calling local library functions. No local programming is needed. The user writes the AFB file with any text editor and it is then converted on the VME bus side to an internal binary form. The converted AFB is then downloaded to DVME-630 Dual Port RAM (DPR) and executed. The AFB is powerful because of full access to the local DSP library and because repeating functions may be looped. These loops in turn may be nested. Loops can run with a loop count or "forever" until stopped.

Unlike a slow ASCII interpreter, the AFB runs at the full speed of the 320C30 DSP with minimal overhead. And to accept fast A/D's without sample loss, only a fully integrated hardware/software system will handle the bandwidth. This hardware system consists of local FIFO A/D memory, local FIFO interrupts and a local Direct Memory Access (DMA) controller inside the DSP which runs in background. FIFO interrupts may cause DMA data block transfers while the DSP continues foreground processing.

Executive Package

The complete Executive software package is an integrated environment for full control of the DVME-630. It includes programs which run on both the host VME bus and the DVME-630. The Executive package consists of:

The AFB ASCII to binary file converter (PARSE).
A small menu shell.
The VME bus Host package (DVME-630SET.C).
The Executive scheduler, DSP library, boot code, vectors and full local DVME-630 system (SKED.OUT).

To use this environment, the user simply converts the AFB text file to a binary file, downloads this to the DVME-630 scheduler and retrieves data files. Once the configuration is saved, an application can be executed from one command line or from a batch file.

DVME-630 Host System Architecture

(See Figure 4)

When the DVME-630 is fully installed, the host VME memory map contains the device driver, the Interrupt Service Routine, a small menu program and the DVME-630's dual port RAM. These systems all work together to provide fast disk or buffer transfers of DSP'd A/D data. The entire system is controlled by simple user-written command files.

The primary function of the EXEC is a high speed disk data recorder. Data may be all sent to memory first (high speed) then saved to disk. Or data may be sent directly to disk (large capacity).

Software Hierarchy

The relationship between software in the VME bus host and in the DVME-630 is illustrated in this diagram. Control flows downward from the user's AFB and A/D data flows upward.

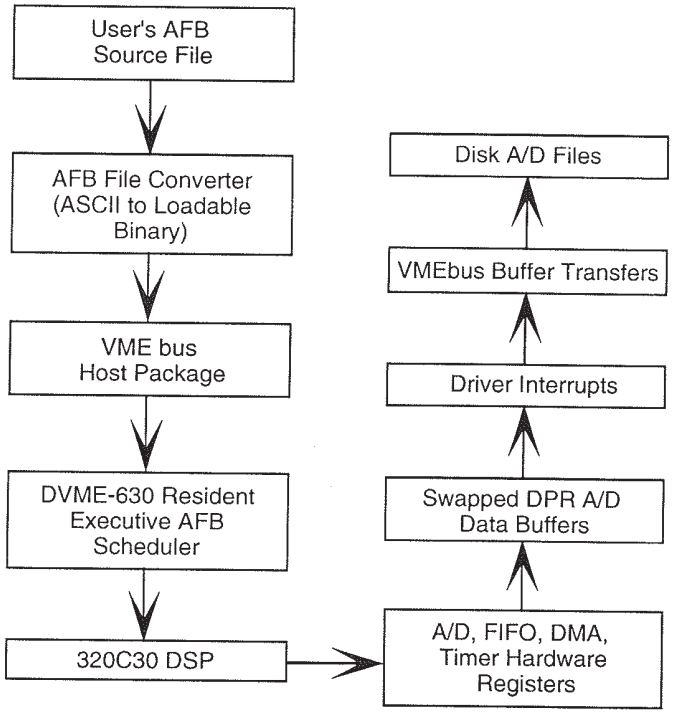


Figure 3. Software Hierarchy Flow Chart

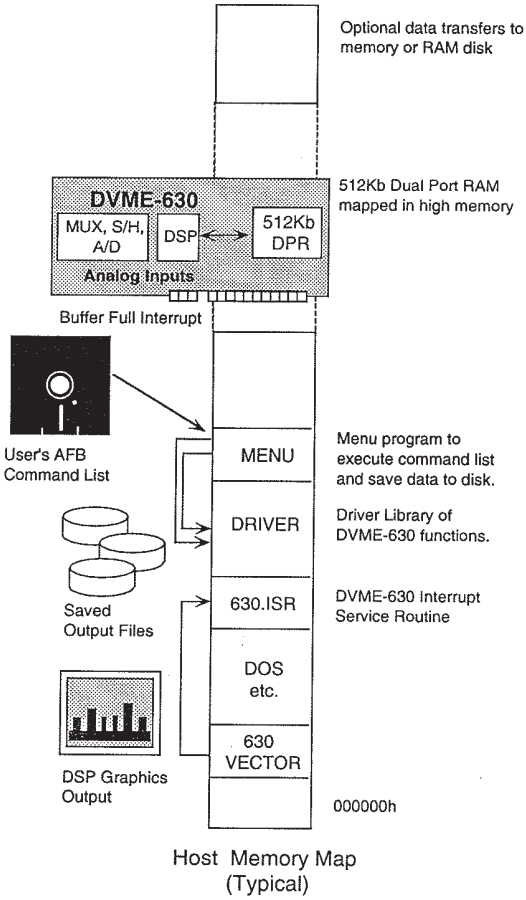


Figure 4. DVME-630 Host System Architecture

Library Functions

The following functions are downloaded at power up by the host to the DVME-630 DPR and form the resident on-board DSP library. They may be called from the DPR by including them in the user's downloaded AFB.

A/D Scan Routines

initad	Initialize the start channel address.
inittim1, inittim2, inittim3	Initialize timers 1, 2, or 3.
sadtsc	Select internal or external A/D trigger source.
sadcr	Select the A/D internal conversion rate.
sstr	Select the internal scan trigger rate.
sadspc	Select the number of A/D samples per frame.
stads	Set the total number of A/D samples under 65K. (For 65k or greater, refer to the special techniques).
sfifoi	Enable or disable local FIFO interrupts.
sadr	Enable or disable A/D conversions.
rfifo	Reset FIFO.
calad	Calibrate A/D single samples.
dma_intrpt	Enable or disable FIFO DMA interrupts.
fifoisr	FIFO local Interrupt Service Routine.
scommreg	Set A/D command register.

DSP Array Routines

fir	Do FIR filter on streaming non-stop array with user-supplied coefficients.
iir	Do IIR filter on in-place array with user-supplied coefficients.
linfir	Convolution on in-place linear array.
cirfir	Convolution on in-place circular array.
windham, windhan	Multiply a Hamming or Hanning window with signal data array.
windrec	Multiply a rectangular window with signal data array.
windblh	Multiply a Blackman-Harris window with signal data array.
windrco	Multiply a Raised Cosine window with signal data array.
cfftc	Do complex Fast Fourier Transform (FFT) on array.
fft	Do real FFT on array.
twiddle_c	Generate complex array of bit-reversed twiddle factors.
twiddle_r	Generate array of twiddles for real FFT.
dct	Do Discrete Cosine Transform on array (for signal compression).
magfft	Calculate magnitude of real FFT array.
dbfft	Performs log10 on FFT array to prepare data for graphic display.
call_sine, call_cos	Generate sine or cosine arrays.
call_const	Fill array with constant.
bitrev	Shuffle array with bit reverse addressing.

Array Conversion Routines

(The 320C30 DSP uses an internal 32-bit floating point format which is optimized for hardware speed)

ieeedsp	Convert IEEE-754 floating point array to 320 format.
dspieee	Convert 320 array to IEEE-754 floating point format.
matadd	Doubleword matrix addition on array.
matmul	Doubleword matrix multiplication on array.
hstgrm	Histogram of doubleword array.
int2float	Convert doubleword integer array to 320 floating point.
float2int	Convert 320 floating point array to doubleword integers.
sign_extend	Convert an array of 12, 14 or 16-bit A/D data to 32-bit signed integer format.
float_transfer	Sign extend A/D data, convert to floating point and block transfer between buffers.

Single Variable Transcendentals

sine, cosine, tangent
hyperbolic sine, cosine, tangent
inverse sine, cosine, tangent
square root, powers, exponential
natural logarithm, Base10 logarithm

(These functions are available in the TI "C" compiler library with user-written code)

Buffer Management

defsbuf, defdbuf defnbuf	Define single, double, or N buffers.
set_ibuf, set_obuf	Setup input and output double buffers. Post current buffer addresses in Exec status area. Interrupt the VME host that data is ready. Flag overflow errors. Used for non-stop A/D filling without sample loss.
ibuf_ready, ibuf_release	Used to sequence each swapped buffer FIFO DMA transfer.
switch_buffers	Swaps buffer pointers under AFB control.
unrav2, unrav4 unravx	Separate one array of sequential multi-channel data into two, four, or N single channel arrays.
concat	Compress an array of one A/D sample per 32-bit longword into an array of contiguous 16-bit A/D words. Concat forms a single 32-bit longword from the 16-bit LSB's of two longwords. MSB's are discarded.
dprxfer	Do swapped double buffer block transfers within DVME-630 local memory using buffer numbers.
addxfer	Do block transfers within DVME-630 local memory between absolute addresses. Overlapped transfers will preserve data.
int2pc	Select buffer ready or local timer interrupt to VME bus.
pause	Momentarily stop AFB execution to allow VME host access for table upload/ download.
expendable	Declare size of MEM-30 expansion RAM.
expxfer	Incremental copy from MEM-30 huge buffer to DPR window buffer.

VME Host Driver

The final portion of the full Executive package is the Driver containing a library of functions to control the DVME-630. This offers a simple menu to control the DVME-630. No programming is required. Because of the modular design of the driver, its functions may be used through the menu shell or may be controlled by a user's program after rewriting the menu shell.

The Driver functions are:

- Install VME bus Interrupt Service Routine (ISR) to respond to DVME-630 buffer full flags. A small UNIX device driver is included.
- Initialize the VME bus interrupt system.
- Set the DVME-630 memory base address and test memory.
- Download the Exec, library and full local system to the DVME-630 DPR from a system binary file.
- Boot the local DVME-630 system and confirm.
- Allocate a VME bus Host buffer to receive DVME-630 data.
- Download a converted AFB file and start execution.
- Collect data to buffer or disk using swapped double buffer interrupts.
- Stop the AFB and save the DVME-630 data buffer to a file.
- Load and run a user COFF object file.
- Calibrate the A/D. Halt and reset the DSP. Quit to the OS.
- Auto run in batch mode (no menues).

VMEbus Memory Map

	Byte Address
Interrupt Vector ID (Read/Write)	Base+7FFFFh
Command Register (Write Only)	Base+7FFFCh
Not Used	Base+7FFF8-Bh
Dual Port Random Access Memory	Base+7FFF7h (512kB) Base (DSP location 0)

Command Register (Write Base+7FFFCh)

Bits 0 - 3: Not used
Bit 4: VME interrupt enable
Bit 5: DSP interrupt request
Bit 6: DSP hold request
Bit 7: DSP reset/run

AFB Source File Format

The AFB source format uses symbolic names for internal DVME-630 library functions. The ASCII file may be written in free form with the user's choice of loop nesting indentation, skipped lines, etc. Comments after the function name delimiter are ignored. After the user writes the AFB, the PARSE file converter prepares a binary output file which is subsequently downloaded through the Driver for execution. Here is an AFB example which defines buffers, generates a sine wave, then prepares an FFT array for floating point output:

```
DEFDBUF,            ;function to define double buffer
0x0L,               ;starting buffer number
0x400L,             ;buffer length
0x200L,             ;alignment

DEFSBUF,            ;define single buffer for twiddles
0x2L,               ;buffer number
0x100L,             ;buffer length
0x100L,             ;alignment

TWIDDLE_R,          ;generate twiddle factors
0x2L,               ;buffer number 2

BEGIN,              ;begin flag
FOREVER,            ; -1 = loop forever flag

CALL_SINE,          ;fill buffer with sine array
0x00000000L,        ;buffer number 0
0x00000020L,        ;period of the sine wave

FFT,                ;do FFT on buffer
0x0L,               ;buffer number 0
0x200L,             ;number of points
0x9L,               ;Log 2 of number of points
0x2L,               ;buffer for twiddle factors

MAGFFT,             ;take magnitude of FFT data
0x0L,               ;buffer number 0
0x200L,             ;FFT size

DSPIEEE,            ;convert to IEEE format
0x0L,               ;buffer number 0
0x100L,             ;buffer length

SET_OBUF,           ;interrupt to VMEbus that buffer is
                    ready
0x0L,               ;buffer 0
0x100L,             ;buffer length
SWITCH_BUFFERS      ;swap double buffers

END                 ;end flag for this loop

END                 ;end of whole AFB
```

Extensions

The resident downloaded library and the host driver may be modified or extended by adding functions to the "C" source code. Data may be directed to screen or other peripherals. Multiple tasks may be interleaved between buffer uploads.

ORDERING INFORMATION

Model	A/D Bits	FIFO Size (Samples)	Chans.	Sample rate single chan.	Simul.S/H	PGA
DVME-630A1	12	1024	4s	1.5MHz	4 chans.	x1,x10 (two chans.)
DVME-630A2		4096				
DVME-630B1	14	1024	4s	500kHz	none	none
DVME-630B2		4096				
DVME-630C1	12	1024	4s	1MHz	none	none
DVME-630C2		4096				
DVME-630D1	12	1024	1d	4MHz	none	none
DVME-630D2		4096				
DVME-630E1	12	1024	16s/8d	500kHz	none	X1 to X100
DVME-630E2		4096		(1 chan.)		resistor select
DVME-630F1	12	1024	2 simul	2MHz	2 chans.	none
DVME-630F2		4096				

MEM-30

High speed 1 megabyte memory expansion module. Adds 256k x 32 of static RAM, located at 20000h to 5FFFFh. Total installed capacity is 1.5 megabytes. See MEM-30 data sheet.

Contact DATEL for MEM-30A (4 megabytes)

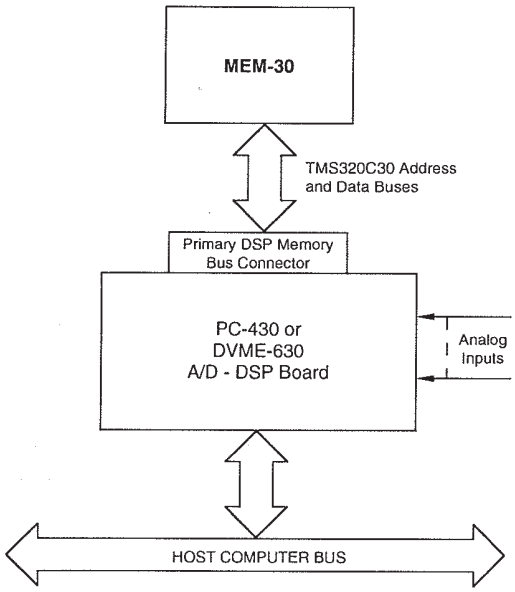
DVME-630EXEC

Executive software package in "C" source format on IBM-PC/AT high density 5.25" and 3.5" disks. Includes all local functions in downloadable binary format. Uses VT-100 terminal interface on host.

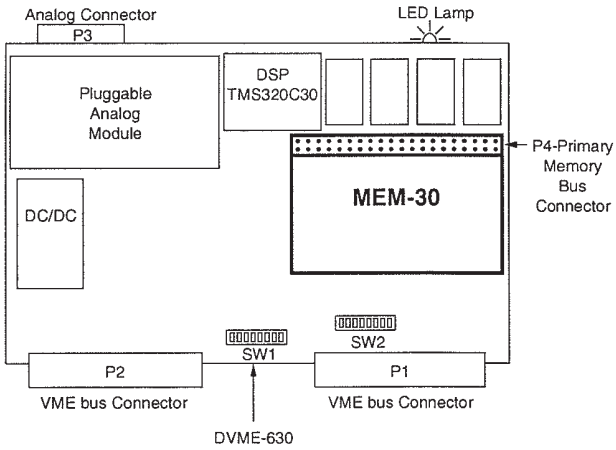
DVME-630SRC (Source code to 630EXEC)

"C" source code for all host and DSP local functions, boot code, vectors, scheduler, DSP math library, A/D, FIFO/DMA, buffer management and timer/counter function library. Supplied in "C" and Texas Instruments 320C30 Assembly language. IBM-PC/AT HD 3.5" and 5.25" disks. Includes UNIX device driver.

Each board is power-cycle burned-in, tested and calibrated. All models include a user's manual. The warranty period is one year.



MEM-30 Configuration



MEM-30 Installation

DATEL, Inc. 11 CABOT BOULEVARD, MANSFIELD, MA 02048-1194 TEL. (508) 339-3000 / FAX (508) 339-6356
INTERNATIONAL: DATEL (UNITED KINGDOM) Basingstoke Tel. (256) 880-444 • DATEL (FRANCE) Tel. (1) 3460.0101
DATEL (GERMANY) Tel. (89) 53-0741 • DATEL (JAPAN) Tokyo Tel. (3) 3779-1031 • Osaka Tel. (6) 354-2025