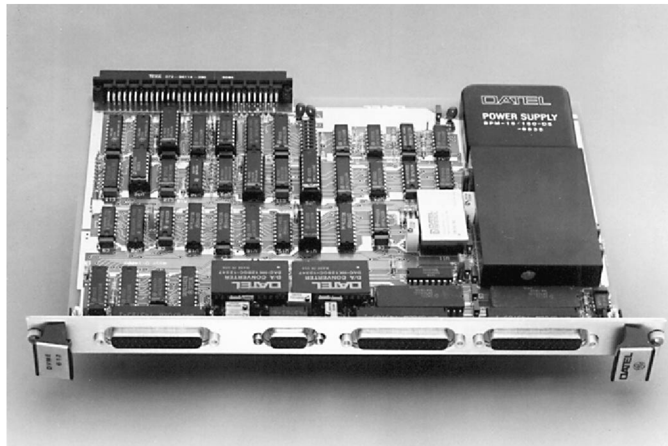
DVME-611/612
32SE/16D-Channel VME A/D-D/A Boards

INNOVATION and EXCELLENCE

FEATURES



- **Two models of VMEbus-based boards**
  DVME-611: 32 single-ended/16 differential A/D channels
  DVME-612: 32 single-ended/16 differential A/D channels and 2 D/A channels
- **Choice of A/D bits/speed**
  12 bits/2, 4, or 20 μSec.
  14 bits/4 μSec.
  16 bits/35 μSec.
- **Four input voltage ranges available: ±10V, ±5V, 0 to +5V, and 0 to +10V dc**
- **Three types of output coding:**
  Bipolar 2's complement
  Bipolar offset binary
  Unipolar straight binary
- **Up to 400 KHz throughput with a *fast throughput mode* for high-speed data transfers (single channel)**
- **On-board interrupt vector register for host system's service routines**
- **80 dB CMRR at gain of 128**
- **Two TTL digital outputs**
- **Eight-stage programmable gain amplifier (PGA)**
- **±0.05% full-scale range accuracy for D/A channels**
- **Channel expansion boards for up to 256 channels**
  DVME-641: Non-isolated, high-level inputs
  DVME-643: Isolated, thermocouple, RTD, high-level, 4-to-20 mA inputs
  DVME-645: Simultaneous sample/hold inputs

GENERAL DESCRIPTION

The DVME-611/612 are DATEL's VMEbus based high-end A/D conversion boards. The A/D boards provide up to 16-bit binary data from up to 32 single-ended or 16 differential analog input channels. DATEL also offers optional expansion boards for up to 256 single-ended or differential analog input channels. The DVME-612 is also equipped with two D/A channels, operable in four output voltage ranges.

The on-board hardware essentially consists of multiplexers, a PGA, an A/D converter, and registers. The PGA is programmable for gains from 1 to 128 in binary increments. Both the DVME-611 and the DVME-612 are available in several models depending upon the A/D converter module used. The A/D converter modules are easily field-replaceable. All models except the DVME-611D and the DVME-612D contain a sample/hold amplifier.

The host-programmable command register controls the A/D conversion process. Depending upon the contents of the command register, an external trigger may also initiate the A/D conversion process. The host system may obtain information pertaining to the A/D conversion and control selections by reading the status register.

The channel and control information from the channel select logic section is brought out to the J4 expansion connector. The control lines include End of Conversion (EOC), End of Scan (EOS), settling time delay, and external trigger signals. These control signals on the expansion connector are also usable with externally multiplexed input channels. The host system selects the start and final channels for the A/D scanning process.

The analog output section on the DVME-612 offers ±1/2 LSB differential non-linearity and operates at ±0.05% of full-scale range accuracy.

Functionally, the analog signal from the input channel is amplified and converted into binary data. The resolution depends on the A/D converter module used. Figure 1 is a functional block diagram of the DVME-611/612 A/D boards. Data from the A/D converter module is coded via jumpers into straight binary, offset binary, or 2's complement coding. The binary A/D data is transferred to the host system through the VMEbus transceivers.

The DVME-611/612 A/D boards can operate in a *fast throughput mode* for applications requiring fast data transfers. This mode is selectable using the command register. The *fast throughput mode* guarantees transfer of A/D data on to the VMEbus without having to test the conversion status. When A/D data is read, this mode delays the host CPU DTACK✱ while EOC = 0.

The DVME-611/612 A/D boards come with a user's manual. The user's manual describes the installation and calibration procedures for different applications and explains the theory of operation of the A/D boards. The user's manual also contains information on troubleshooting the boards

The boards are shipped with a 5.25 inch MS-DOS disk containing an example source program. Consult the factory regarding the availability of the diagnostic program's source code in other disk formats.

VME Interface

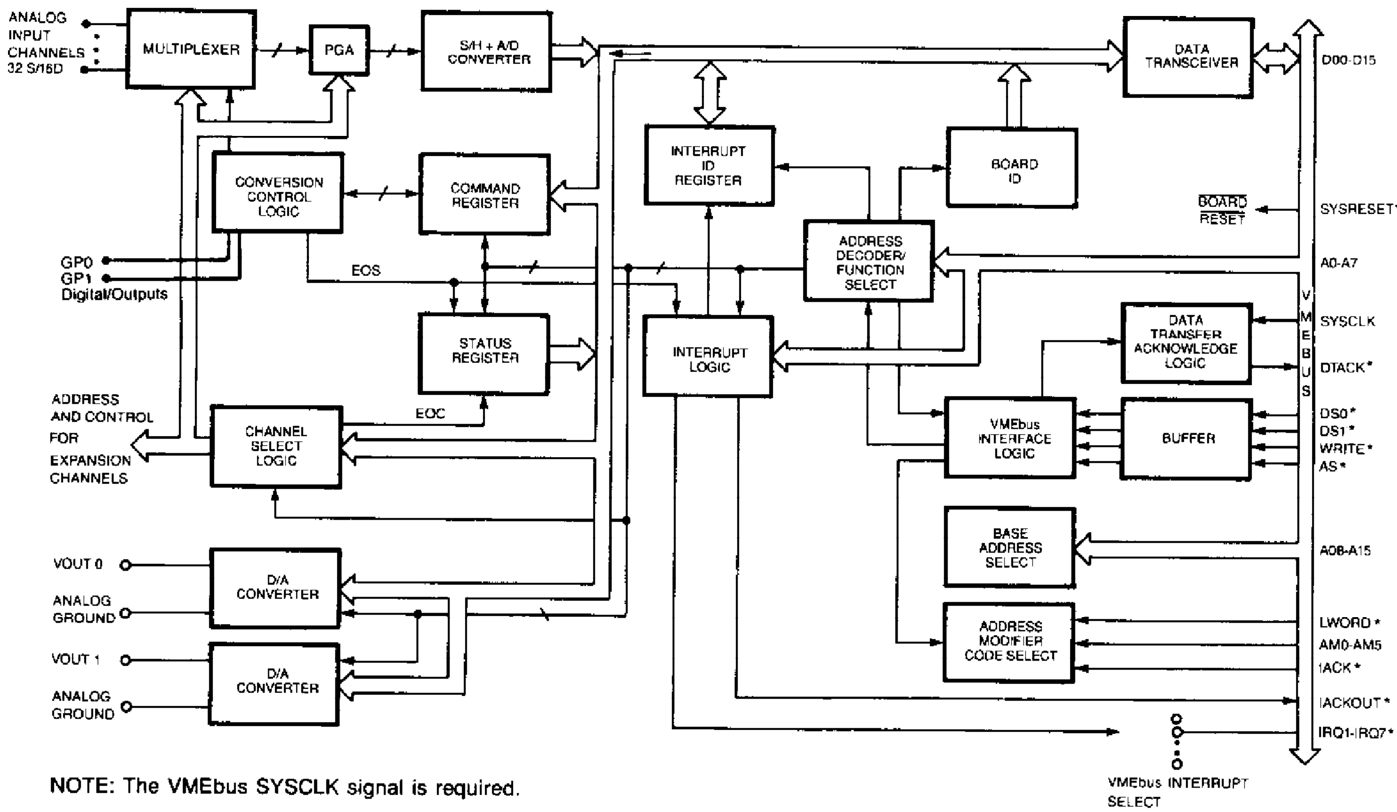
The DVME-611/612 interfaces to the host system using the P1 connector. The board uses short I/O space address lines and 16 data lines. On-board switches select the base address of the board. The board responds to address modifier codes 29H, 2DH, 39H, and 3DH for data output purposes.

The DVME-611/612 generates the data acknowledge (DTACK✱) signal to notify acceptance of data from the VME data lines, D00 through D15. The DTACK✱ signal is jumper-selectable for delay times from 125 nanoseconds to 1000 nanoseconds, accommodating different host systems.

The interface logic decodes VMEbus control lines (WRITE✱, DS0✱, DS1✱, and AS✱) to provide the interface control signals. These signals control the board select and the VMEbus transfer functions. The DVME-611/612 uses programmable array logic (PAL) devices for interface and control, guaranteeing true asynchronous operation.

VMEbus Interrupt Logic

The interrupt logic section senses an EOC or EOS condition and generates an interrupt request on one of the VMEbus interrupt lines (IRQ1✱ through IRQ7✱). The interrupt lines are jumper-selectable. The interrupt logic accepts IACK✱ and IACKIN✱ signals from the host system as interrupt acknowledge and daisy chain input signals. Depending upon the interrupt level, the on-board logic loads the interrupt ID number on to the VMEbus or generates the daisy chain IACKOUT✱ signal.



NOTE: The VMEbus SYSCLK signal is required.

Figure 1. DVME-611/612 Functional Block Diagram

FUNCTIONAL SPECIFICATIONS

(Typical at 25 °C, unless otherwise noted)

VMEbus INTERFACE

Data Bus .... 16 Bits. (A16:D16 slave)
Address Bus.................... Short I/O Space 16 address lines
Address Modifier Codes.. Codes used 29H, 2DH, 39H, and 3DH
Interrupts .... 1 line, jumper-selectable
2 interrupt ID's for EOC and EOS
Software programmable
Memory Mapping .... Short I/O space, user or supervisor 256 words allocated per board
Data Transfer.................... DTACK✱ signal line
Acknowledges the VMEbus host that data has been placed or accepted from the VMEbus data lines

ANALOG INPUT

Number of Channels........ 32 single-ended or 16 differential
Channel Expansion.......... 256 single-ended or differential; requires external multiplexing. Use DATEL's DVME-641, DVME-643, or DVME-645 mux boards.
Input Configuration.......... Single-ended or differential
Input Ranges .... ±10V, ±5V, 0 to +5V, or 0 to +10V, jumper-selectable. See Table 2.
Digital Outputs
Standard....................... Offset binary
Jumperable .... Straight binary or 2's complement
External Start Trigger ...... TTL compatible, negative going edge.
Minimum pulse width = 100 nS
Maximum pulse width = 2 µS
Common Mode Voltage... ±10V dc, maximum, non-isolated
Input Bias Current........... 8 nA, maximum
Over Voltage Protection.. ±35V dc, maximum
Input Impedance
Differential to ground ...... 10 megohms, minimum

PERFORMANCE

Programmable Gain......... Uses an AM-543MC for gains of X1, X2, X4, X8, X16, X32, X64, X128
Common Mode Rejection for ±10V input signal at 60 Hz, minimum .... 75 dB at a gain of 2
80 dB at a gain of 128
Full-Scale Range Accuracy, minimum
DVME-611A/612A.......... 0.025% at a gain of 1
DVME-611E/612E.......... 0.20% at a gain of 128
DVME-611B/612B.......... 0.05% at a gain of 1
0.20% at a gain of 128
DVME-611C/612C.......... 0.010% at a gain of 1
0.20% at a gain of 128
DVME-611D/612D.......... 0.0063% at a gain of 1
0.20% at a gain of 128
DVME-611F/612F .... 0.01% at a gain of 1
PGA plus MUX Settling Time, maximum................ 8 µS at a gain of 1
12 µS at a gain of 16
40 µS at a gain of 64
100 µS at a gain of 128

Min. conversion time
DVME-611A/612A.......... 20 µS at a gain of 1
110 µS at a gain of 128
DVME-611B,E/612B,E... 8 µS at a gain of 1
102 µS at a gain of 128
DVME-611C/612C.......... 35 µS at a gain of 1
110 µS at a gain of 128
DVME-611D/612D.......... 400 mS at a gain of 1
400 mS at a gain of 128
DVME-611F/612F .... 4 µS at gain = 1

Note: Allow 20 minutes warm-up for DVME-611F/612F

Resolution and Throughput

(Scan Mode)	Resolution in bits	Conversion time	Throughput conversions /sec.*
DVME-611A/612A	12	20 µS	40,320
DVME-611B/612B	12	4 µS	160,000
DVME-611C/612C	16	35 µS	18,667
DVME-611D/612D	16	400 mS	2.5
DVME-611E/612E	12	2 µS	see notes
DVME-611F/612F	14	4 µS	100,000

*Typical sample rate per channel in scan mode.

Temperature Drift and Linearity

Model	Gain Temperature Coefficient (ppm/ °C)	Zero Temperature Drift, (ppm/ °C)	Linearity Error
DVME-611A/612A	±20	20	1/2 LSB
DVME-611B/612B	±20	20	1/2 LSB
DVME-611C/612C	±20	20	2 LSB
DVME-611D/612D	±10	10	2 LSB
DVME-611E/612E	±20	±20	1/2 LSB
DVME-611F/612F	±15	±15	2 LSB

Optional Multiplexer Expansion Boards

Model	Number of expansion channels Single-ended	Differential	Input type
DVME-641	32	16	High-level, non-isolated
DVME-643T	–	8	Thermocouple Isolated
DVME-643H	–	8	High-level isolated
DVME-645	16	8	Simultaneous Sample/Hold high-level non-isolated

ANALOG OUTPUT (For DVME-612 models only)

Number of Channels 2
Output Range....................±10V, ±5V, 0 to +5V, or 0 to +10V
Digital Input Coding ....Bipolar 2's complement, bipolar offset binary or unipolar straight binary
Resolution.........................12 Bits, bits D0 through D3 not used
Reset ....Minus, full-scale, -10V for 2's complement and offset binary 0V for Unipolar
Full-Scale Range Accuracy ....05%, minimum
Diff. Non-Linearity ....0.5 LSB, minimum
Zero Temperature Drift.....5 ppm/ °C, maximum
Offset Temperature Drift..20 ppm/ °C, maximum
Gain Temperature Drift ....20 ppm/ °C, maximum
Settling Time.....................10 µS, maximum
Output Current..................5 milliamps, maximum
Output Impedance...........50 milliohms, typical

POWER SUPPLY REQUIREMENTS

+5V dc ±5% at 2.5 Amperes
Note: On-board dc-to-dc converter generates ±15V dc for the DVME-611/612 logic circuits

CONNECTORS

VMEbus P1 connector......96-pin male DIN connector
J1 and J2 Analog Input Connectors........................25-pin D-type female connectors
J3 Analog Output Connector..........................9-pin D-type female connector
J4 Analog Expansion Connector..........................25-pin D-type female connector

PHYSICAL-ENVIRONMENTAL

Outline Dimensions..........9.19"W x 6.3"D x 0.6"H (233.5 x 160 x 15.24 mm)
Weight................................1 lb. 0.5 oz. (467.8 grams)
Operating Temp. Range...0 to +60 °C
Storage Temp. Range.......-20 to +80 °C
Relative Humidity ....0 to 90%, non-condensing

DVME-611/612 Programming Information

The DVME-611/612 A/D boards use ten registers for data acquisition and control purposes. Table 1 lists the DVME-611/612 registers and their base address offsets. These registers are addressable locations in the host system's address space.

Address	Function	Contents
Base + 0 through Base + 63	Read	Manufacturer's/Board's identification
Base + 128	Write	Command register (80h)
Base + 128	Read	Status register (80h)
Base + 130	Write	Interrupt ID register (82h)
Base + 132	Write	EOC/EOS F/F Reset (84h)
Base + 134	Write	Gain register (86h)
Base + 136	Write	Start channel register (88h)
Base + 136	Read	Current channel register
Base + 138	Write	Final channel register (8Ah)
Base + 140	Write	Start conversion register (8Ch)
Base + 140	Read	A/D data register
Base + 142	Read	Status register (8Eh)
Base + 160	Write	D/A channel 0 (A0h)
Base + 162	Write	D/A channel 1 (A2h)

Table 1. DVME-611/612 Hardware Register Functions

Command Register

The DVME-611/612 boards scan their selected channels under control of the 16-bit command register. Programming the command register selects the modes for starting conversion, calibration, and fast throughput. This register also enables the interrupt, channel address auto-increment, and channel re-scan capabilities. Figure 2 shows the command register format.

Status Register

The DVME-611/612 status register indicates conditions relating to conversion status, channel scanning information, and modes selected. Figure 3 shows the status register format.

Total System Throughput

Total sample-to-sample throughput rate depends on the A/D-S/H settling and conversion period and the user's software period. During the software interval, data is transferred to the host and the next A/D conversion is started. By combining fast throughput mode (DTACK✱ EOC holdoff) with convert-on-read-data, throughput over 400 KHz may be achieved for gain = 1 in single channel mode for model DVME-611E. Data transfer and host memory pointer management may partially overlap A/D Conversion by using the convert-on-read mode.

Fast Throughput Mode

This mode holds off response of the DTACK✱ VMEbus signal with the simultaneous ANDing of three conditions: command register bit 5 = 1, EOC = 0, and a host read of the A/D data register. While DTACK✱ is held off, the host CPU executes wait states. When A/D conversion finishes, EOC = 1 and DTACK✱ is released. Normally the attempted A/D data read now completes, and data is transferred without any EOC polling. Fast throughput should be used with caution since the host must be completely dedicated to A/D data acquisition.

Table 2. A/D Full Scale Input Ranges (PGA gain = 1)

Input Range	Model 611/612A	611/612B,E	611/612C	611/612D	611/612F
0 to +5V	X	NA	NA	NA	NA
0 to +10V	X	X	NA	NA	S
±5V	X	NA	X	NA	S
±10V	X	X	X	X	X

X = supplied, NA = not available, S = solderable on module

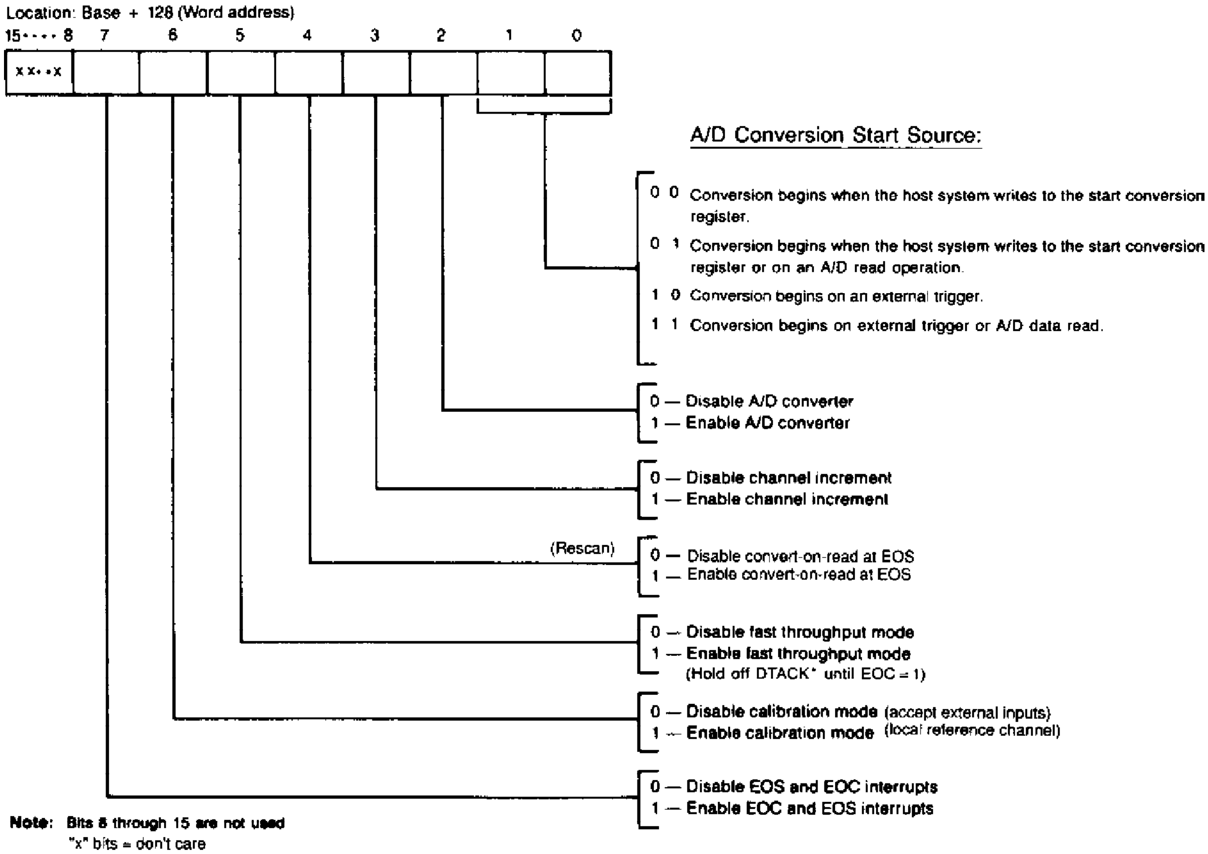


Figure 2: DVME-611/612 Command Register Format (WRITE)

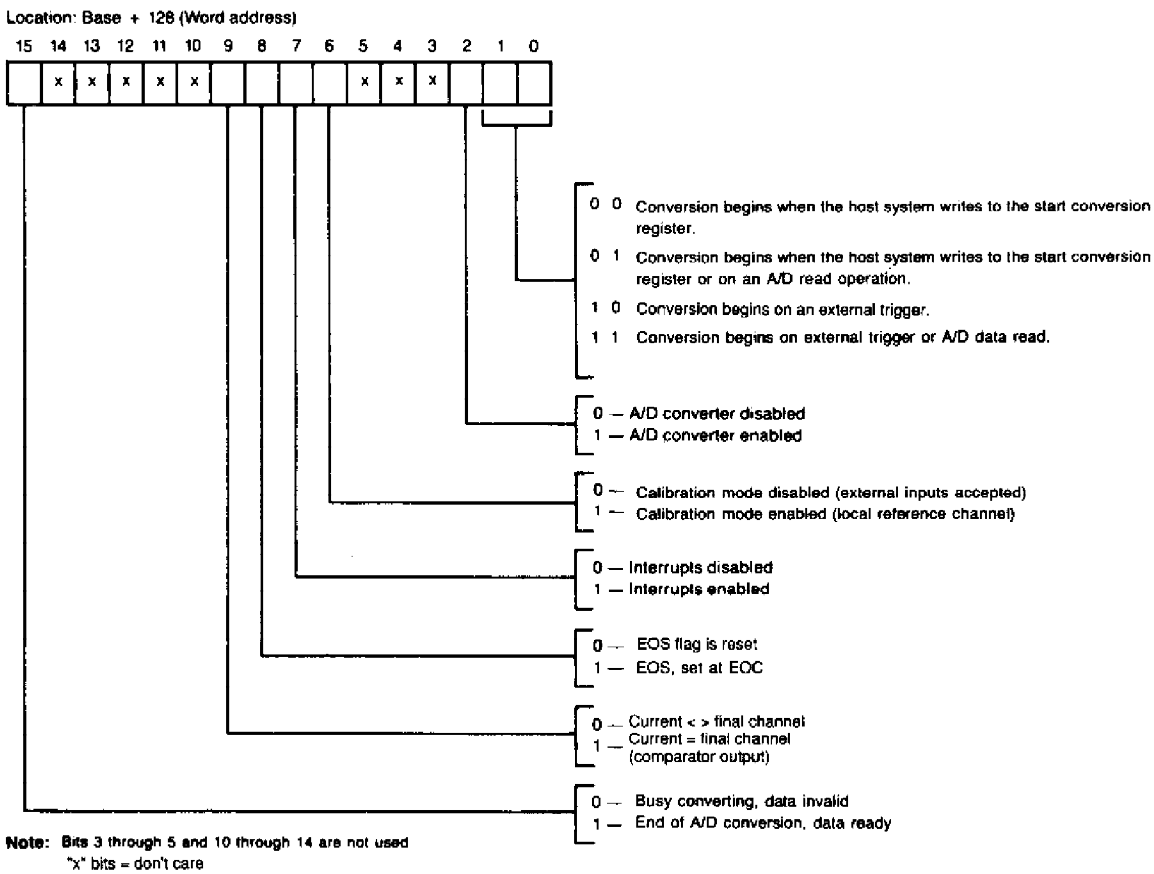


Figure 3: DVME-611/612 Status Register Format (READ)

Interrupt ID Register

This register contains the user-loaded interrupt ID number. On receiving the interrupt request, the host system tests the interrupt level using address lines A01 through A03. The host system must then acknowledge using the IACK* and the daisy chain IACKIN* signal lines. If the DVME-611/612 interrupt level matches the level code on the address lines, the interrupt logic loads the interrupt ID number on to the VMEbus (low byte). If the EOC/EOS interrupts and the multiple channel scan option are enabled, the board loads the ID number plus one on to the VMEbus data lines. The host system may use these ID's to differentiate the EOC and EOS interrupts. Figure 4 shows the register format of the interrupt ID register.

Word address: Base + 130 (Write) X = Don't Care

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	ID7	ID6	ID5	ID4	ID3	ID2	ID1	0

Figure 4: Interrupt ID Register Format

Gain Register and Digital Outputs

The least three significant bits of this register, when programmed, assign the gain to the differential amplifier in the PGA section. This register is programmable for gains from 1 to 128 in binary increments. Bits 6 and 7 of this register provide a general purpose digital output. The output signal lines from these two bits are available on pins 18 and 6 of the J4 connector. Figure 5 shows the gain register format.

Word address: Base + 134 (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	GP1	GP0	x	x	x	G2	G1	G0

Figure 5: Gain Register Format

Start Channel/Current Channel Register

User must load this register with the starting channel address when scanning a group of channels. This register contains the address of the channel being scanned. Figure 6 shows the format of this register.

Word address: Base + 136 (Read/Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

Figure 6: Start Channel/Current Channel Register

Final Channel Register

User must load this register with the final channel address when scanning a group of channels. The on-board comparator compares this register contents with the current channel register and generates the end of scan (EOS) signal. Figure 7 shows the format of this register.

Word address: Base + 138 (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0

Figure 7: Final Channel Register Format

Start Conversion Register

Writing any value to this register starts an A/D conversions on the channel indicated by the current channel register. Figure 8 shows the format of this register.

Word address: Base + 140 (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Figure 8: Start Conversion Register Format

A/D Data Register

The 16 bits of the A/D data register are connected to 16 VMEbus data lines. The host system may read this register to obtain the binary data of the analog input from the channel selected. Models DVME-611/612 A, E, and B do not use the four least significant data bits. The value of these bits defaults to zero for these models. Figure 9 shows the format of this register.

Word address: Base + 140 (Read)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AD1	AD2	AD3	AD4	AD5	AD6	AD7	AD8	AD9	AD10	AD11	AD12	AD13	AD14	AD15	AD16

MSB (Data is left-justified) LSB

Figure 9: A/D Register Format

D/A Channel Registers

The DVME-612 boards have two D/A channel registers. These registers form the input to the 12-bit hybrid D/A converters. These registers are programmable by the most significant 12 bits from the VMEbus data lines. Figure 10 shows the format of these registers.

Word address: Base + 160 (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DA1	DA2	DA3	DA4	DA5	DA6	DA7	DA8	DA9	DA10	DA11	DA12	x	x	x	x

MSB LSB

Figure 10a: D/A Channel 0 Register Format

Word address: Base + 162 (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DA1	DA2	DA3	DA4	DA5	DA6	DA7	DA8	DA9	DA10	DA11	DA12	x	x	x	x

MSB LSB

Figure 10b: D/A Channel 1 Register Format

EOC/EOS F/F Register

Writing any value to this register resets the EOC/EOS flip-flops. Figure 11 shows the format of this register.

Word address: Base + 132 (Write)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Figure 11: EOC/EOS F/F Register Format

(These F/F's are also reset by the next start of conversion or by reading A/D data.)

I/O Connections

The DVME-611/612 A/D boards use the J1 and J2 connectors for analog input connections and the J4 connector for channel expansion. The DVME-612 uses the J3 connector for analog output connections. Tables 2, 3, 4, and 5 list the I/O signals of the J1, J2, J3, and J4 connector respectively.

Table 3. DVME-611/612 Analog Input Connector - J1

PIN #	CONFIGURATION	
	SINGLE-ENDED	DIFFERENTIAL
24	CHANNEL 0 IN	CHANNEL 0 HIGH
12	CHANNEL 16 IN	CHANNEL 0 LOW
25	ANALOG RETURN	ANALOG RETURN
10	CHANNEL 1 IN	CHANNEL 1 HIGH
23	CHANNEL 17 IN	CHANNEL 1 LOW
11	ANALOG RETURN	ANALOG RETURN
21	CHANNEL 2 IN	CHANNEL 2 HIGH
9	CHANNEL 18 IN	CHANNEL 2 LOW
22	ANALOG RETURN	ANALOG RETURN
7	CHANNEL 3 IN	CHANNEL 3 HIGH
20	CHANNEL 19 IN	CHANNEL 3 LOW
8	ANALOG RETURN	ANALOG RETURN
18	CHANNEL 4 IN	CHANNEL 4 HIGH
6	CHANNEL 20 IN	CHANNEL 4 LOW
19	ANALOG RETURN	ANALOG RETURN
4	CHANNEL 5 IN	CHANNEL 5 HIGH
17	CHANNEL 21 IN	CHANNEL 5 LOW
5	ANALOG RETURN	ANALOG RETURN
15	CHANNEL 6 IN	CHANNEL 6 HIGH
3	CHANNEL 22 IN	CHANNEL 6 LOW
16	ANALOG RETURN	ANALOG RETURN
1	CHANNEL 7 IN	CHANNEL 7 HIGH
14	CHANNEL 23 IN	CHANNEL 7 LOW
2	ANALOG RETURN	ANALOG RETURN

Table 4. DVME-612 Analog Output Connector - J3

PIN #	SIGNAL LINE
1	CHANNEL 0 VOUT
6	ANALOG RETURN
4	CHANNEL 1 VOUT
9	ANALOG RETURN

Table 5. DVME-611/612 Analog Input Connector - J2

PIN #	CONFIGURATION	
	SINGLE-ENDED	DIFFERENTIAL
24	CHANNEL 8	CHANNEL 8 HIGH
12	CHANNEL 24	CHANNEL 8 LOW
25	ANALOG RETURN	ANALOG RETURN
10	CHANNEL 9	CHANNEL 9 HIGH
23	CHANNEL 25	CHANNEL 9 LOW
11	ANALOG RETURN	ANALOG RETURN
21	CHANNEL 10	CHANNEL 10 HIGH
9	CHANNEL 26	CHANNEL 10 LOW
22	ANALOG RETURN	ANALOG RETURN
7	CHANNEL 11	CHANNEL 11 HIGH
20	CHANNEL 27	CHANNEL 11 LOW
8	ANALOG RETURN	ANALOG RETURN
18	CHANNEL 12	CHANNEL 12 HIGH
6	CHANNEL 28	CHANNEL 12 LOW
19	ANALOG RETURN	ANALOG RETURN
4	CHANNEL 13	CHANNEL 13 HIGH
17	CHANNEL 29	CHANNEL 13 LOW
5	ANALOG RETURN	ANALOG RETURN
15	CHANNEL 14	CHANNEL 14 HIGH
3	CHANNEL 30	CHANNEL 14 LOW
16	ANALOG RETURN	ANALOG RETURN
1	CHANNEL 15	CHANNEL 15 HIGH
14	CHANNEL 31	CHANNEL 15 LOW
2	ANALOG RETURN	ANALOG RETURN

Table 6. DVME-611/612 Expansion Connector - J4

PIN #	SIGNAL LINE
13	EXTERNAL CHANNEL ADDRESS 0 OUT
25	EXTERNAL CHANNEL ADDRESS 1 OUT
12	EXTERNAL CHANNEL ADDRESS 2 OUT
24	EXTERNAL CHANNEL ADDRESS 3 OUT
11	EXTERNAL CHANNEL ADDRESS 4 OUT
23	EXTERNAL CHANNEL ADDRESS 5 OUT
10	EXTERNAL CHANNEL ADDRESS 6 OUT
22	EXTERNAL CHANNEL ADDRESS 7 OUT
16	DIGITAL GROUND
9	EXTERNAL CHANNEL ADDRESS VALID OUT
8	START CONVERSION STROBE OUT
20	SETTLING DELAY★ IN
7	END OF CONVERSION OUT
19	END OF SCAN OUT
17	EXTERNAL TRIGGER IN*
18	GENERAL PURPOSE OUTPUT 0
6	GENERAL PURPOSE OUTPUT 1
4	DIGITAL GROUND
21	RESERVED
5	RESERVED
1	EXTERNAL ANALOG LOW IN
14	EXTERNAL ANALOG HIGH IN
2, 15	ANALOG COMMON
3	+5V dc REFERENCE OUT (5mA)

DVME-611/612 Board Indentification Code

Byte Address	ASCII Code	Function
Base + 1	V	Identifier
+3	M	This ASCII code is present
+5	E	for all DATEL VMEbus boards
+7	I	
+9	D	
+0B	D	Manufacturer ID
+0D	A	DAT is the ID for DATEL
+0F	T	
+11	d	Board model number
+13	V	
+15	M	
+17	E	
+19	–	
+1B	6	
+1D	1	
+1F	1 or 2	

ORDERING INFORMATION

DVME-611 (A/D only)
DVME-612 (A/D + D/A)

- A - 12-bit/20 µS ADC
- B - 12-bit/4 µS ADC
- C - 16-bit/35 µS ADC
- D - DISCONTINUED*
- E - 12-bit/2 µS ADC
- F - 14-bit/4 µS

Optional Multiplexer Expansion Boards

DVME-641 - 32S/16D Channel high-level non-isolated inputs.
DVME-643 - 8D Channel isolated inputs.
DVME-645 - 16S/8D Channel simultaneous sample/hold high-level non-isolated inputs.

***DVME-611D and -612D are discontinued. Use DVME-611C and -612C instead.**

Each board includes a disk and manual.

DATEL VMEbus Short I/O Memory Organization

Base Address	Board Model Number	Function
Base + 0 through Base + 63	All DATEL VMEbus boards	Manufacturer's and Board's identification code
Base +64 through Base + 77	DVME-660	48 line digital I/O board
Base + 78 through Base + 127	Not used	
Base + 128 through Base + 143	DVME-611 DVME-612	DVME-611: 32 single-ended/ 16 differential channel A/D board DVME-612: 32 single-ended; 16 differential channel A/D board with 2 D/A channels
Base + 144 through Base + 151	DVME-602	DVME-602: 4-channel isolated board for measuring thermocouples, RTD's, strain gages, high-level, low-level, and 4-to-20 mA current loop inputs
Base + 152 through Base + 159	Not used	
Base + 160 through Base + 175	DVME-612 DVME-624 DVME-628	DVME-612: 32 single-ended/ 16 differential channel A/D board with 2 D/A channels DVME-624: 4-channel isolated D/A board
Base + 176 through Base + 191	Not used	
Base + 192 through Base + 255	Not used	

DATEL
INNOVATION and EXCELLENCE

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